# FDD2582

# MOSFET, N-Channel, POWERTRENCH®

## 150 V, 21 A, 66 mΩ

### Features

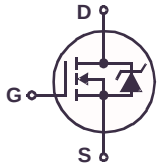
- $r_{DS(ON)}$ = 58 mΩ (Typ.), $V_{GS}$ = 10 V, $I_D$ = 7 A
- $Q_g$(tot) = 19 nC (Typ.), $V_{GS}$ = 10 V
- Low Miller Charge
- Low $Q_{RR}$ Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- These Devices are Pb−Free, Halide Free and are RoHS Compliant

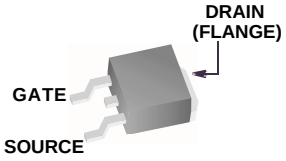
### Applications

- DC/DC Converters and Off−Line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24 V and 48 V Systems
- High Voltage Synchronous Rectifier
- Direct Injection / Diesel Injection Systems
- 42 V Automotive Load Control
- Electronic Valve Train System

**ON Semiconductor®**

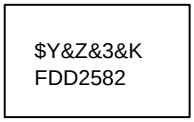
www.onsemi.com




**DPAk3 (TO−252 3 LD)**
**CASE 369AS**

### MARKING DIAGRAM




| | |
|---|---|
| $Y | = ON Semiconductor Logo |
| &Z | = Assembly Plant Code |
| &3 | = Numeric Date Code |
| &K | = Lot Code |
| FDD2582 | = Specific Device Code |

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

**MOSFET MAXIMUM RATINGS** ($T_C$ = 25°C, Unless otherwise noted)

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain to Source Voltage | | 150 | V |
| $V_{GS}$ | Gate to Source Voltage | | ±20 | V |
| $I_D$ | Drain Current | −Continuous ($T_C$ = 25°C, $V_{GS}$ = 10 V) | 21 | A |
| | | −Continuous ($T_C$ = 100°C, $V_{GS}$ = 10 V) | 15 | |
| | | −Continuous ($T_{amb}$ = 25°C, $V_{GS}$ = 10 V, $R_{\theta JA}$ = 52°C/W) | 3.7 | |
| | | −Pulsed | See Figure 4 | |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 1) | | 59 | mJ |
| $P_D$ | Power Dissipation | | 95 | W |
| | Derate above 25°C | | 0.63 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature | | −55 to 175 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting $T_J$ = 25°C, L = 1.17 mH, $I_{AS}$ = 10 A.

**THERMAL CHARACTERISTICS**

| Symbol | Parameter | Ratings | Units |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case TO−252 | 1.58 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient TO−252 | 100 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient TO−252, 1 $in^2$ copper pad area | 52 | |

**PACKAGE MARKING AND ORDERING INFORMATION**

| Device Marking | Device | Package | Shipping† |
|---|---|---|---|
| FDD2582 | FDD2582 | DPAK3 (TO−252 3 LD)<br>(Pb−Free, Halide Free) | 2500 units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 150 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 120 V, $V_{GS}$ = 0 V<br>$V_{DS}$ = 120 V, $V_{GS}$ = 0 V, $T_C$ = 150°C | | | 1<br>250 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V | | | ±100 | nA |
| **ON CHARACTERISTICS** | | | | | | |
| $V_{GS(TH)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 2 | | 4 | V |
| $r_{DS(on)}$ | Drain to Source On Resistance | $I_D$ = 7 A, $V_{GS}$ = 10 V<br>$I_D$ = 4 A, $V_{GS}$ = 6 V<br>$I_D$ = 7 A, $V_{GS}$ = 10 V, $T_C$ = 150°C | | 0.058<br>0.066<br>0.151 | 0.066<br>0.099<br>0.172 | Ω |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{ISS}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1 MHz | | 1295 | | pF |
| $C_{OSS}$ | Output Capacitance | | | 145 | | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | | | 30 | | pF |
| $Q_{g(TOT)}$ | Total Gate Charge at 10 V | $V_{GS}$ = 0 V to 10 V; $V_{DD}$ = 75 V, $I_D$ = 7 A, $I_g$ = 1.0 mA | | 19 | 25 | nC |
| $Q_{g(TH)}$ | Threshold Gate Charge | $V_{GS}$ = 0 V to 4.5 V; $V_{DD}$ = 75 V, $I_D$ = 7 A, $I_g$ = 1.0 mA | | 2.4 | 3.2 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | | 6.2 | | nC |
| $Q_{gs2}$ | Gate Charge Threshold to Plateau | | | 3.8 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | | 4.2 | | nC |
| **RESISTIVE SWITCHING CHARACTERISTICS** ($V_{GS}$ = 10 V) | | | | | | |
| $t_{ON}$ | Turn−On Time | $V_{DD}$ = 75 V, $I_D$ = 7 A<br>$V_{GS}$ = 10 V, $R_{GS}$ = 16 Ω | | | 41 | ns |
| $t_{d(ON)}$ | Turn−On Delay Time | | | 8 | | ns |
| $t_r$ | Rise Time | | | 19 | | ns |
| $t_{d(OFF)}$ | Turn−Off Delay Time | | | 32 | | ns |
| $t_f$ | Fall Time | | | 19 | | ns |
| $t_{OFF}$ | Turn−Off Time | | | | 77 | ns |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Voltage | $I_{SD}$ = 7 A<br>$I_{SD}$ = 4 A | | | 1.25<br>1.0 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_{SD}$ = 7 A, $\Delta I_{SD}/\Delta t$ = 100 A/μs | | | 67 | ns |
| $Q_{RR}$ | Reverse Recovery Charge | $I_{SD}$ = 7 A, $\Delta I_{SD}/\Delta t$ = 100 A/μs | | | 134 | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## TYPICAL CHARACTERISTICS $T_C$ = 25°C unless otherwise noted.

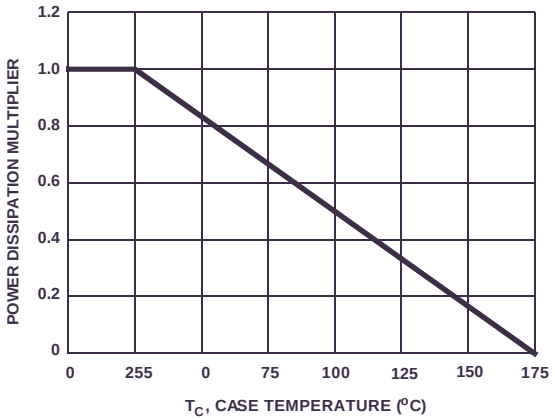



**Figure 1. Normalized Power Dissipation vs. Ambient Temperature**

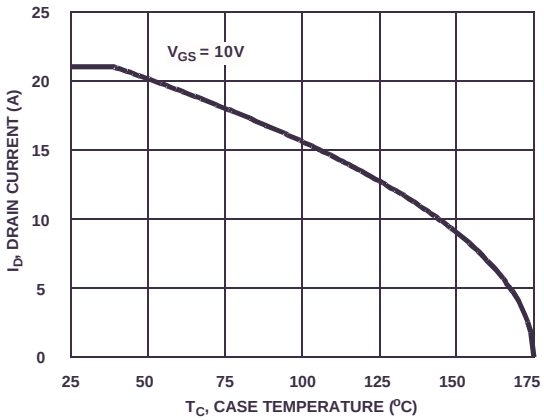



**Figure 2. Maximum Continuous Drain Current vs. Case Temperature**

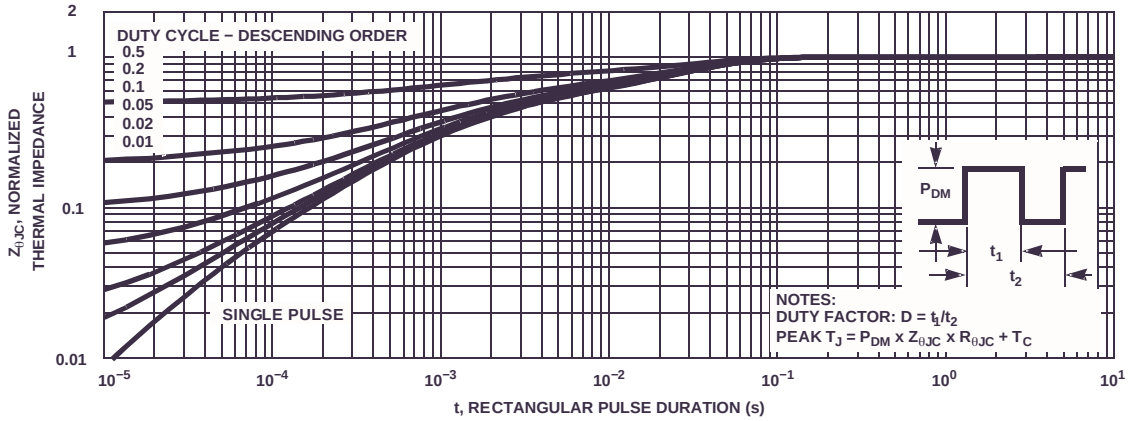



**Figure 3. Normalized Maximum Transient Thermal Impedance**

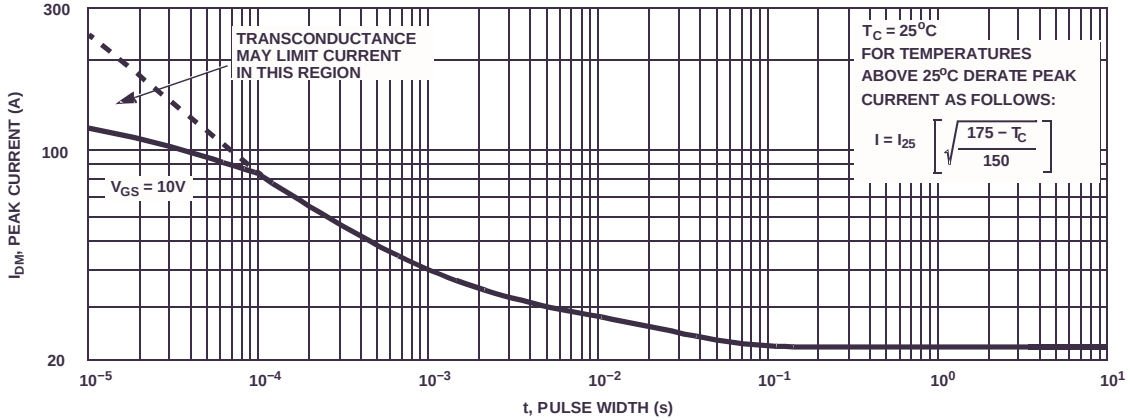



**Figure 4. Peak Current Capability**

## TYPICAL CHARACTERISTICS $T_C$ = 25°C unless otherwise noted.

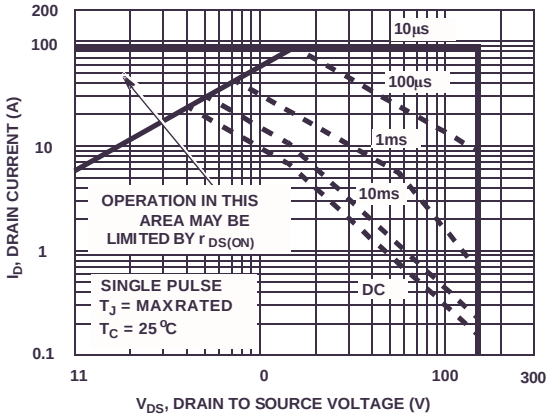
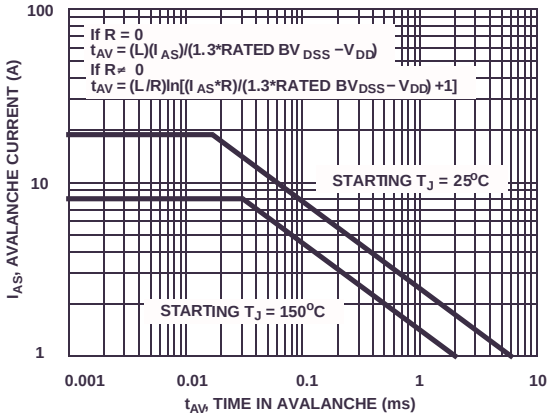



**Figure 5. Forward Bias Safe Operating Area**




Note: Refer to Application Notes AN7514 and AN7515

**Figure 6. Unclamped Inductive Switching Capability**

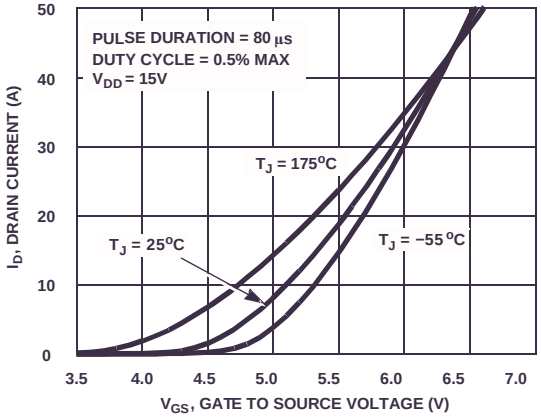



**Figure 7. Transfer Characteristics**

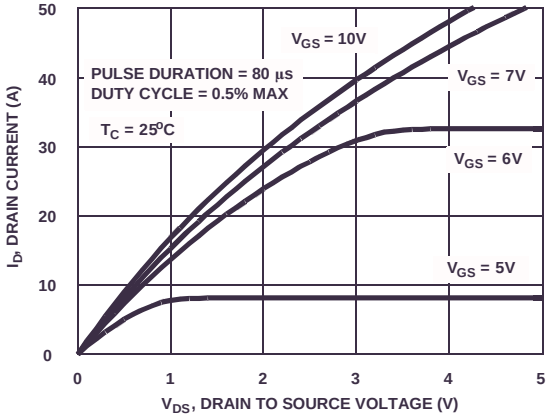



**Figure 8. Saturation Characteristics**

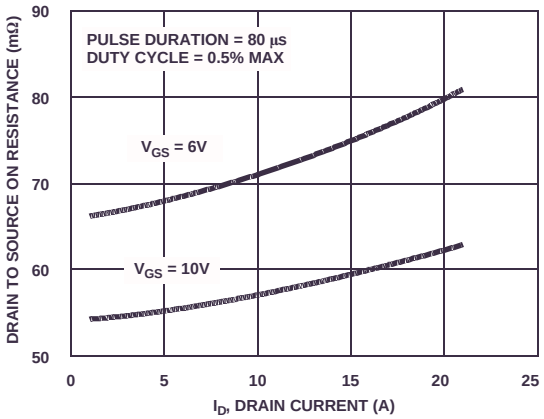



**Figure 9. Drain to Source On Resistance vs. Drain Current**

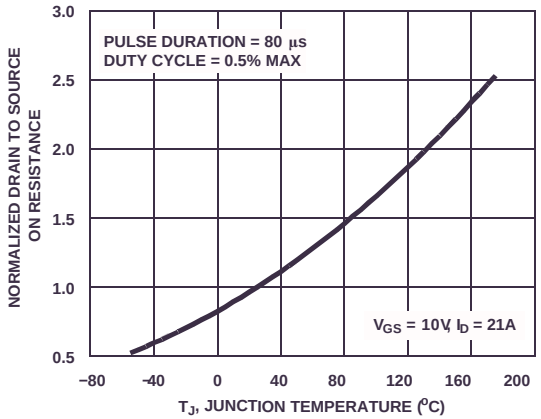



**Figure 10. Normalized Drain to Source On Resistance vs. Junction Temperature**

## TYPICAL CHARACTERISTICS $T_C$ = 25°C unless otherwise noted.

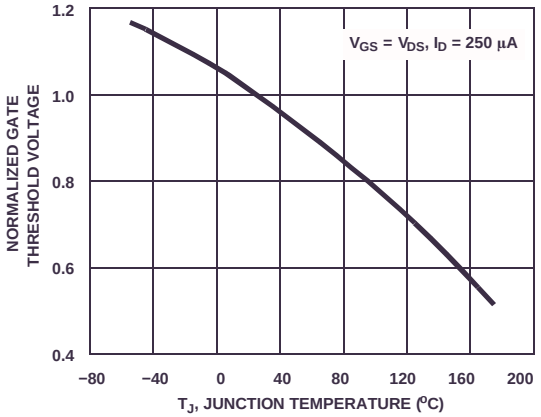



**Figure 11. Normalized Gate Threshold vs. Junction Temperature**

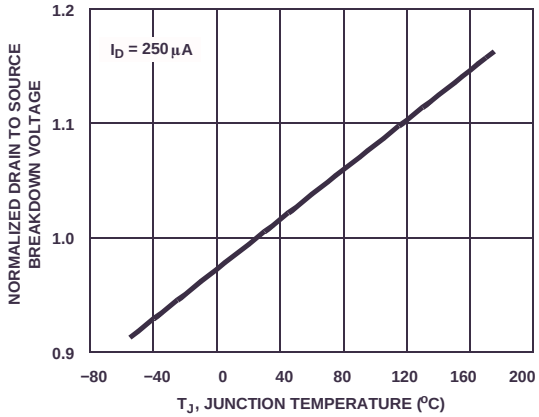



**Figure 12. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature**

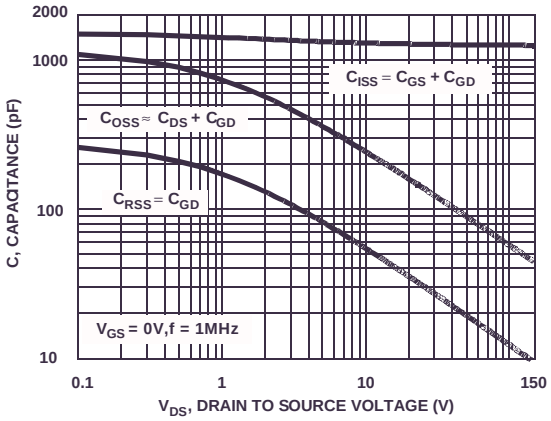



**Figure 13. Capacitance vs. Drain to Source Voltage**

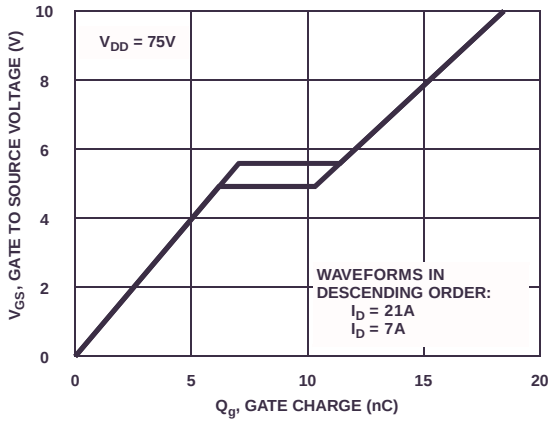



**Figure 14. Cate Charge Waveforms for Constant Gate Currents**

## TEST CIRCUITS AND WAVEFORMS

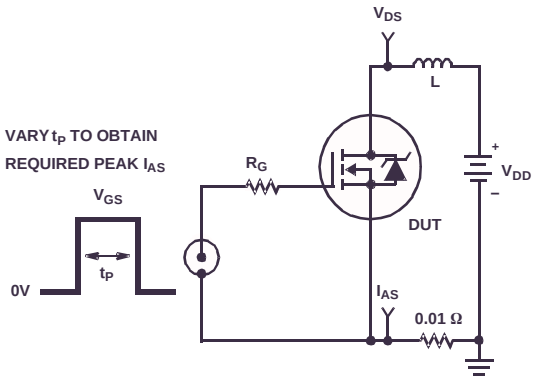



Figure 15. Unclamped Energy Test Circuit

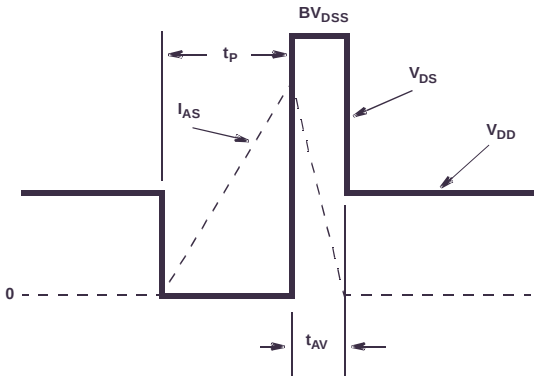



Figure 16. Unclamped Energy Waveforms

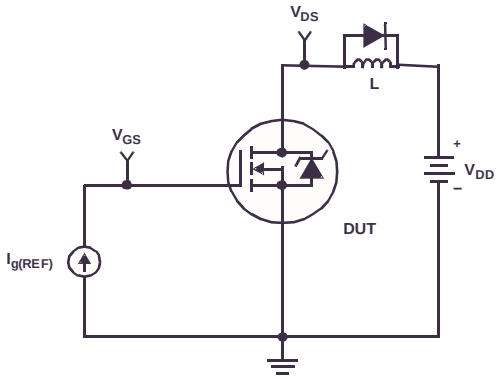



Figure 17. Gate Charge Test Circuit

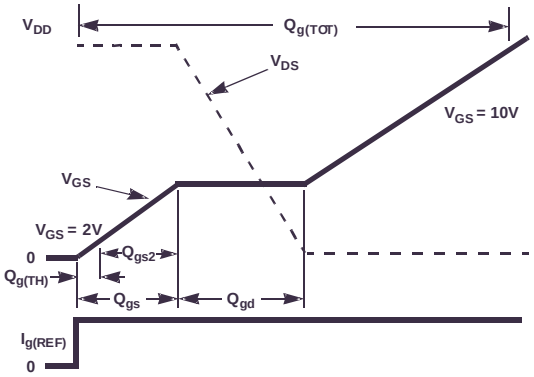



Figure 18. Gate Charge Waveforms

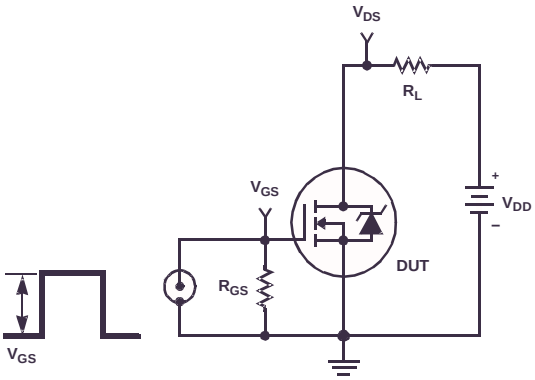



Figure 19. Switching Time Test Circuit

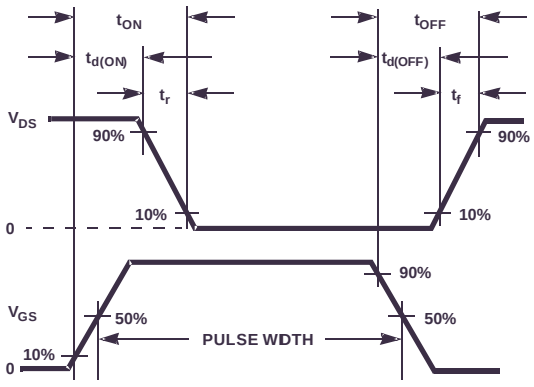



Figure 20. Switching Time Waveforms

### Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, $T_{JM}$, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, $P_{DM}$, in an application. Therefore, the application's ambient temperature, $T_A$ (°C), and thermal resistance $R_{\theta JA}$ (°C/W) must be reviewed to ensure that $T_{JM}$ is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad \text{(eq. 1)}$$

In using surface mount devices such as the TO−252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of $P_{DM}$ is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

ON Semiconductor provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR−4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the ON Semiconductor device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + \text{Area})} \quad \text{Area in } [\text{in}^2] \quad \text{(eq. 2)}$$

$$R_{\theta JA} = 33.32 + \frac{154}{(1.73 + \text{Area})} \quad \text{Area in } [\text{cm}^2] \quad \text{(eq. 3)}$$

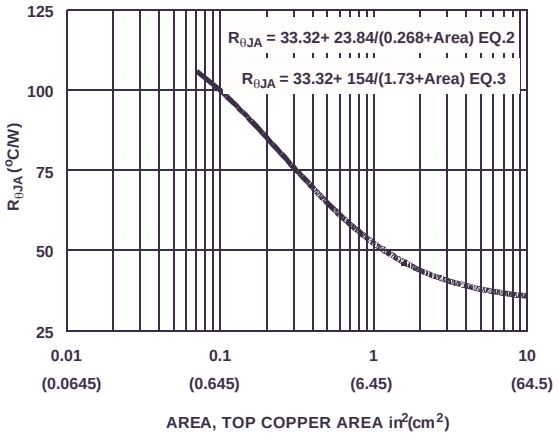



**Figure 21. Thermal Resistance vs. Mounting Pad Area**

## PSPICE Electrical Model

```
.SUBCKT FDD2582  2 1 3 ;       rev July 2002
Ca  12  8 4e-10
Cb  15  14 4.6e-10
Cin  6  8 1.24e−9

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 160.4
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 4.88e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 2.24e-9

RLgate 1 9 48.8
RLdrain 2 5 10
RLsource 3 7 22.4

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 37e-3
Rgate 9 20 1.8
RSLC1 5 51 RSLCMOD 1.0e-6
RSLC2 5 50 1.0e3
Rsource 8 7 RsourceMOD 11.9e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*42),2.5))}

.MODEL DbodyMOD D (IS=2.3E-12 RS=5.3e-3 TRS1=2.2e-3 TRS2=4.5e-7
+ CJO=8.8e-10 M=0.64 TT=3.8e-8 XTI=4.2)
.MODEL DbreakMOD D (RS=0.4 TRS1=1.4e-3 TRS2=-5e-5)
.MODEL DplcapMOD D (CJO=2.75e−10 IS=1.0e−30 N=10 M=0.67)

.MODEL MmedMOD NMOS (VTO=3.76 KP=2.7 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.64)
.MODEL MstroMOD NMOS (VTO=4.25 KP=30 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MweakMOD NMOS (VTO=3.2 KP=0.068 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=16.4 RS=0.1)

.MODEL RbreakMOD RES (TC1=1.1e-3 TC2=-1.1e-8)
.MODEL RdrainMOD RES (TC1=1.0e-2 TC2=2.6e-5)
.MODEL RSLCMOD RES (TC1=2.7e-3 TC2=2.0e-6)
.MODEL RsourceMOD RES (TC1=1.0e-3 TC2=1.0e-6)
.MODEL RvthresMOD RES (TC1=-3.9e-3 TC2=-1.7e-5)
.MODEL RvtempMOD RES (TC1=-3.7e-3 TC2=1.9e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5.0 VOFF=-2.0)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.0 VOFF=-5.0)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.4 VOFF=0.3)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.3 VOFF=-0.4)

.ENDS
```

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub−Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

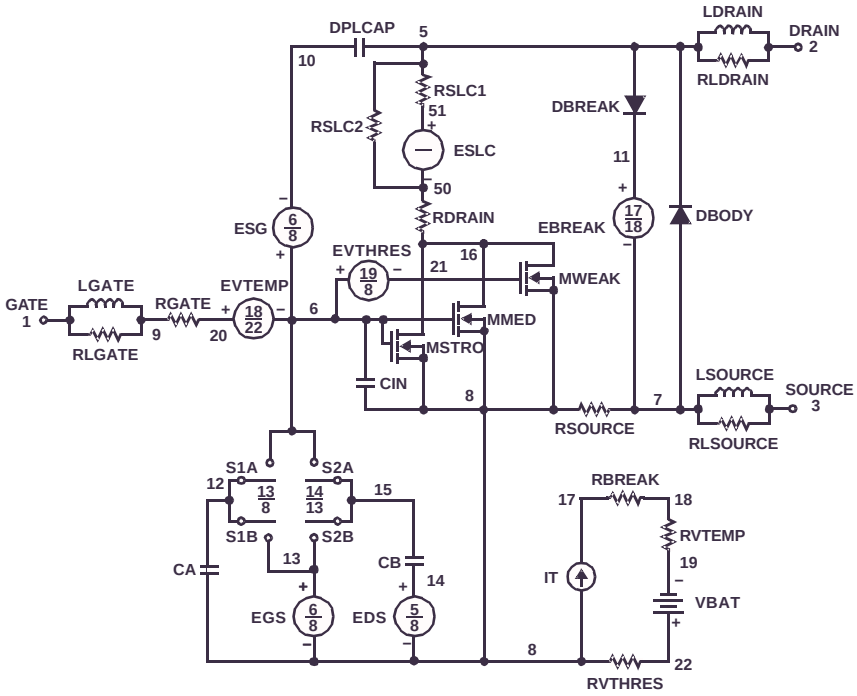



**Figure 22. PSPICE Electrical Model**

## SABER Electrical Model

```
REV July 2002
ttemplate FDD2582 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod =  (isl=2.3e-12,rs=5.3e-3,trs1=2.2e-3,trs2=4.5e-7,cjo=8.8e-10,m=0.64,tt=3.8e-8,xti=4.2)
dp..model dbreakmod = (rs=0.4,trs1=1.4e-3,trs2=-5.0e-5)
dp..model dplcapmod =  (cjo=2.75e-10,isl=10.0e-30,nl=10,m=0.67)
m..model mmedmod = (type=_n,vto=3.76,kp=2.7,is=1e-30, tox=1)
m..model mstrongmod = (type=_n,vto=4.25,kp=30,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=3.2,kp=0.068,is=1e-30, tox=1,rs=0.1)
sw_vcsp..model s1amod =  (ron=1e-5,roff=0.1,von=-5.0,voff=-2.0)
sw_vcsp..model s1bmod =  (ron=1e-5,roff=0.1,von=-2.0,voff=-5.0)
sw_vcsp..model s2amod =  (ron=1e-5,roff=0.1,von=-0.4,voff=0.3)
sw_vcsp..model s2bmod =  (ron=1e-5,roff=0.1,von=0.3,voff=-0.4)
c.ca n12 n8 = 4e-10
c.cb n15 n14 = 4.6e-10
c.cin n6 n8 = 1.24e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 160.4
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evthres n6 n21 n19 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 4.88e-9
l.ldrain n2 n5 = 1.0e-9
l.lsource n3 n7 = 2.24e−9

res.rlgate n1 n9 = 48.8
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 22.4

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1=1.1e-3,tc2=-1.1e-8
res.rdrain n50 n16  = 37e-3, tc1=1.0e-2,tc2=2.6e-5
res.rgate n9 n20 = 1.8
res.rslc1 n5 n51  = 1.0e-6, tc1=2.7e-3,tc2=2.0e-6
res.rslc2 n5 n50 = 1.0e3
res.rsource n8 n7  = 11.9e-3, tc1=1.0e-3,tc2=1.0e-6
res.rvthres n22 n8  = 1, tc1=-3.9e-3,tc2=-1.7e-5
res.rvtemp n18 n19  = 1, tc1=-3.7e-3,tc2=1.9e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/42))** 2.5))
}
}
```

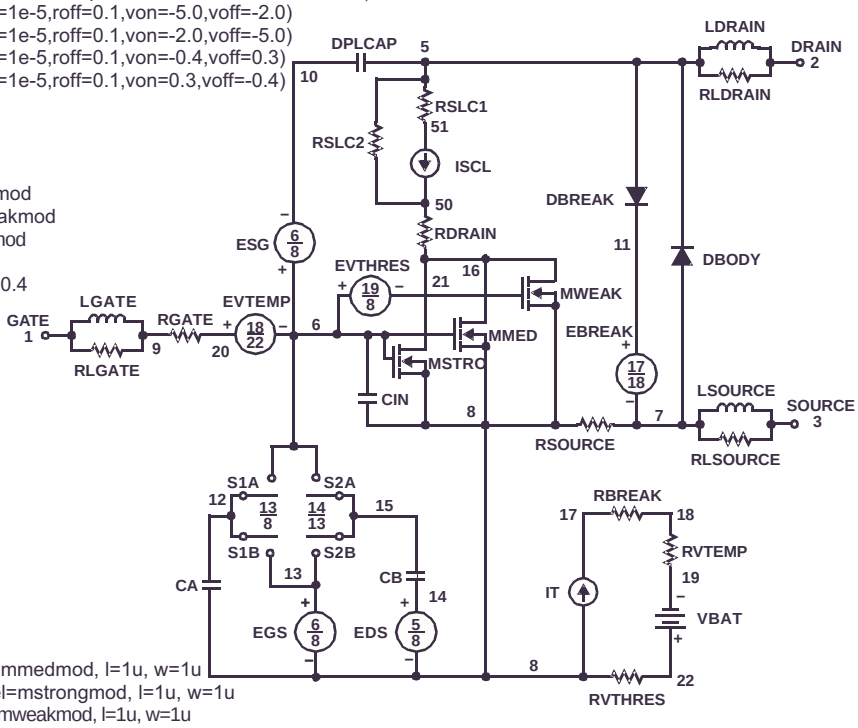



**Figure 23. SABER Electrical Model**

## SPICE / SABER Thermal Model

### *SPICE Thermal Model*

REV 19 July 2002

FDD2582

CTHERM1 TH 6 1.6e-3
CTHERM2 6 5 4.5e-3
CTHERM3 5 4 5.0e-3
CTHERM4 4 3 8.0e-3
CTHERM5 3 2 8.2e-3
CTHERM6 2 TL 4.7e-2

RTHERM1 TH 6 3.3e-2
RTHERM2 6 5 7.9e-2
RTHERM3 5 4 9.5e-2
RTHERM4 4 3 1.4e-1
RTHERM5 3 2 2.9e-1
RTHERM6 2 TL 6.7e-1

### *SABER Thermal Model*

SAB

thermal_c th, tl
{
ctherm.ctherm1 th 6 =1.6e-3
ctherm.ctherm2 6 5 =4.5e-3
ctherm.ctherm3 5 4 =5.0e-3
ctherm.ctherm4 4 3 =8.0e-3
ctherm.ctherm5 3 2 =8.2e-3
ctherm.ctherm6 2 tl =4.7e-2

rrtherm.rtherm1 th 6 =3.3e-2
rtherm.rtherm2 6 5 =7.9e-2
rtherm.rtherm3 5 4 =9.5e-2
rtherm.rtherm4 4 3 =1.4e-1
rtherm.rtherm5 3 2 =2.9e-1
rtherm.rtherm6 2 tl =6.7e-1
}

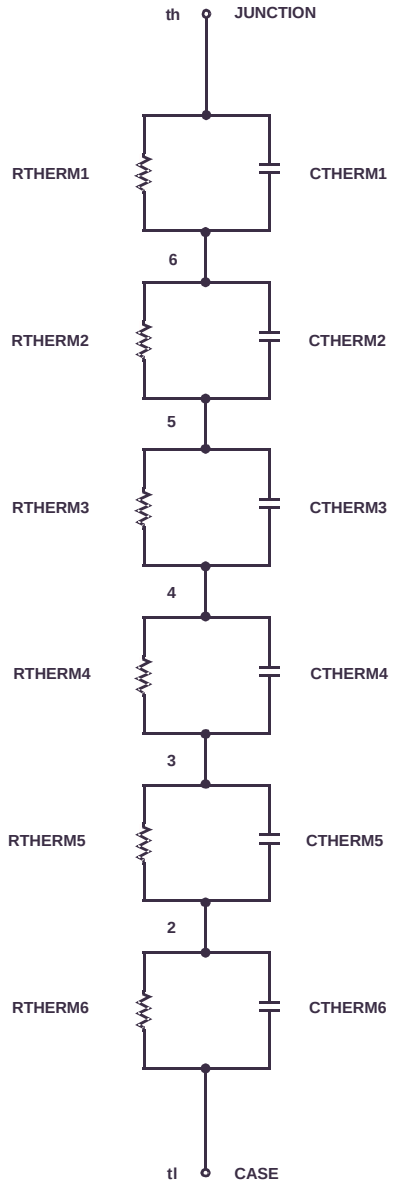
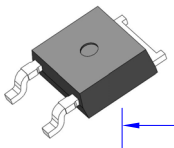


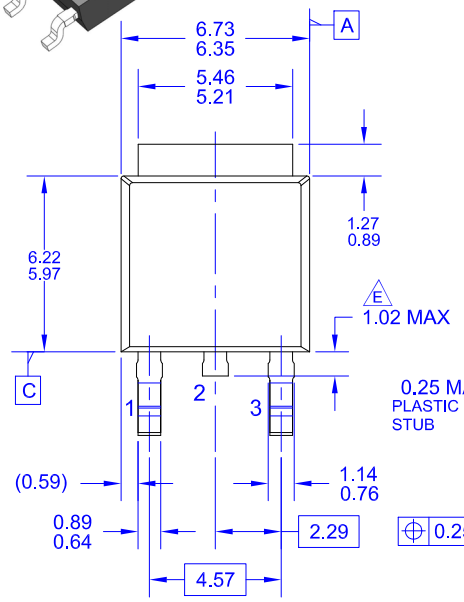

**Figure 24. SPICE / SABER Thermal Model**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

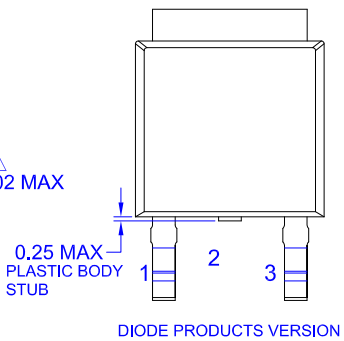
**DPAK3 (TO−252 3 LD)**
CASE 369AS
ISSUE O

DATE 30 SEP 2016



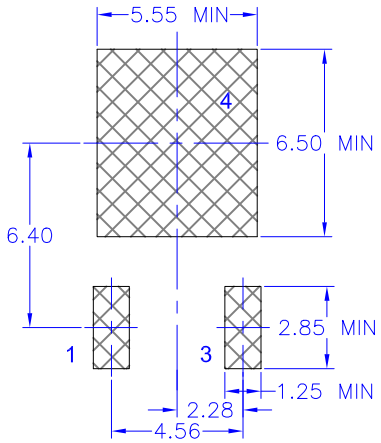



NON-DIODE PRODUCTS VERSION

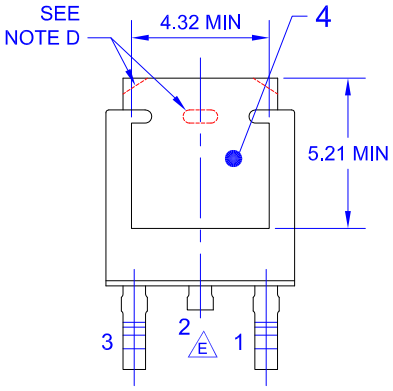



DIODE PRODUCTS VERSION

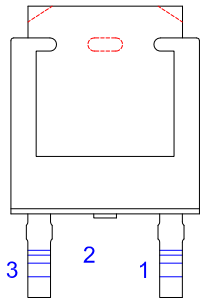
0.25 M A M C




LAND PATTERN RECOMMENDATION




NON-DIODE PRODUCTS VERSION

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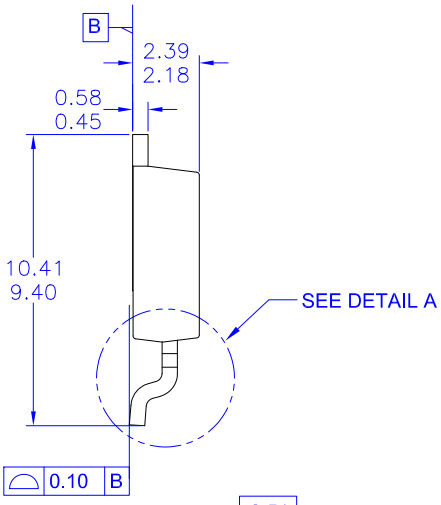
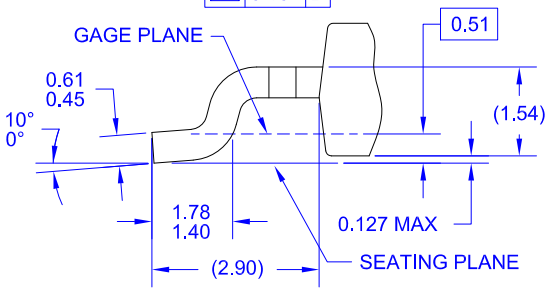



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.




DETAIL A
(ROTATED -90°)
SCALE: 12X

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