Preliminary Data Sheet

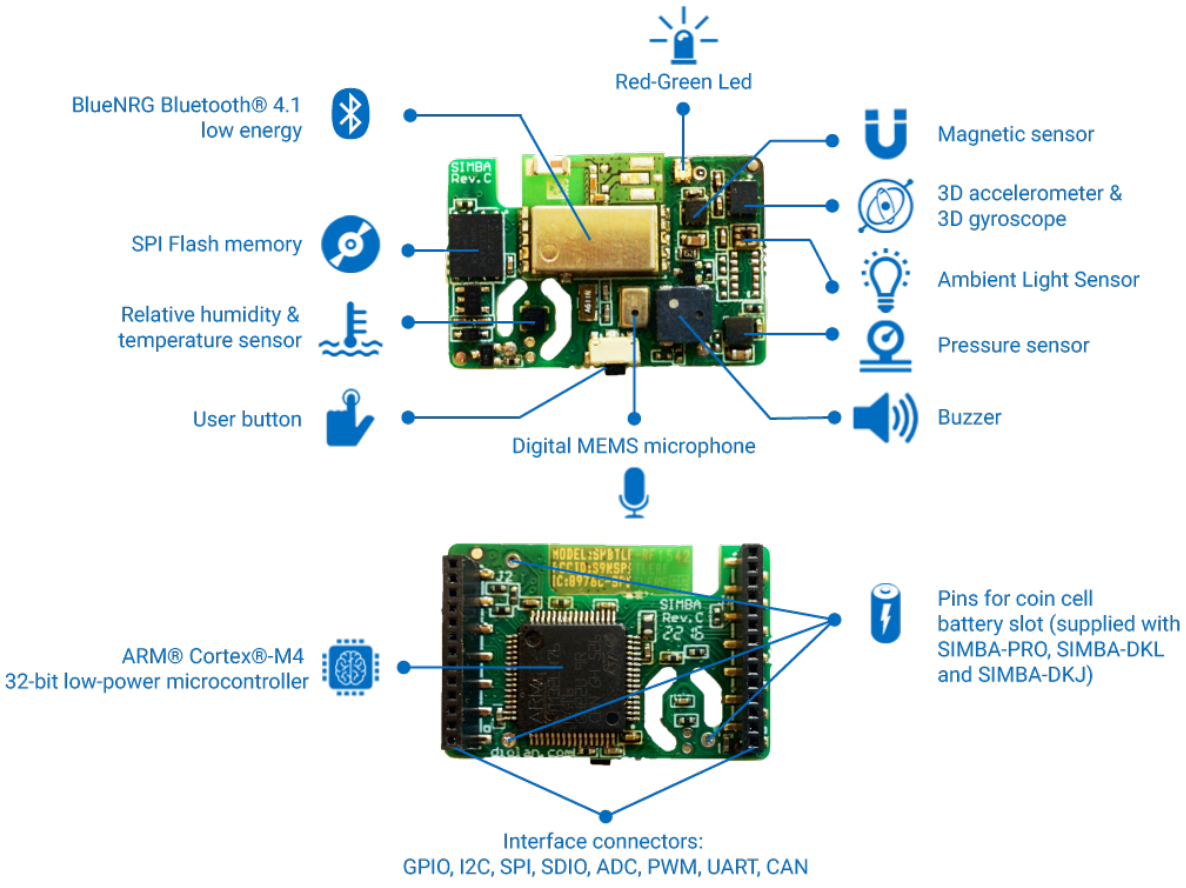
---

*Sensi*BLE

SIMBA-xxx

Version 1.1.3

*Sensi*BLE – Certified Product combining MCU, Sensors and Bluetooth.



List of Content

List of Figures

List of Tables

1 Overview

1.1 General Information

The *Sensi*BLE is a high performance System on Module. *Sensi*BLE integrates Micro Controller, variety of Sensors and BLE connectivity. It provides an ideal building block that easily integrates with a wide range of target markets requiring rich functionality. *Sensi*BLE Compact, cost effective and with low power consumption.
*Sensi*BLE IoT Module is a World's smallest system-on-board (SoB), self-contained, low-power, outperform Micro-Controller, multiple MEMS sensors and wireless Bluetooth Low Energy connectivity.

The *Sensi*BLE enables wireless connectivity, not requiring any RF experience or expertise. It provides a complete RF platform in a tiny form factor and being a certified solution optimizes the time to market of the final applications.

*Sensi*BLE IoT Module is a Bridging-the-Gap solutions to any embedded design. Fit to the vast array of battery-powered applications requiring the integration of Multiple Sensors with BLE connectivity without compromising on cost and power consumption.

*Sensi*BLE Capable to work down to 2v.

Supported products:

1. Base Part numbers

SIMBA : SensiBLE Module (Base part number)
SIMBA-BAT-CR2032 : Battery Holder (Coin Battery) + CR2032 battery
SIM-DB1-JC : Development Board with JTAG Connector (w/o SensiBLE Module)
SIM-DB1-SL : Development Board with ST-LInk (w/o SensiBLE Module)

2. SensiBLE Module Versions

SIMBA-BASE : module with MCU + BLE + SIMBA-BAT-CR2032
SIMBA-STD : module with most of sensors (*) + BLE + SIMBA-BAT-CR2032
SIMBA-PRO : Full configuration sensors + BLE + SIMBA-BAT-CR2032
(*)Not include microphone and Buzzer.

3. Eval Kit part Number

SIMBA-DKL - Development Kit (SIMBA-DB-21 + SIMBA-PRO + CR2032 battery)
SIMBA-DKJ - Development Board with JTAG Connector (SIMBA-DB-11 + SIMBA-PRO + CR2032 battery)

Schematics:
SIMBA-DB-11 - Development Board with JTAG Connector (w/o *Sensi*BLE Module)
SIMBA-DB-21 - Development Board with ST-LInk (w/o *Sensi*BLE Module)

Software:
BLUEMicrosystem1
MOTENV1

Contact SensiEDGE support services for further information:
mailto:Support@SensiEDGE.com.

1.2 Feature's Summary

Product Type	Module
Dimension	30 x 20 x 10 mm
Bluetooth	v4.1 Bluetooth Low Energy 2.4GHz
BLE Certified Module	SPBTLE-RF
Technology	Bluetooth Smart sensor and hub device.
BLE Chipset	ST BlueNRG-MS
Antenna	On Board
RF Conn/ Antenna	Chip Antenna
Internal High Speed Clock	32MHZ crystal oscillator
External Low Power Clock	32.768KHZ
Tx power	+ 4 dBm
Rx sensitivity	-88 dBm
link budget	92dB
Data Rate Bluetooth	1Mb/s
Host Interface BT	SPI
CE qualified	CE qualified
FCC/IC Certified	FCC/IC Certified
BQE Qualified	BQE qualified (in progress)
Processor	ARM® 32-bit Cortex®-M4 CPU with FPU
Microcontroller	STM32L476RG
Sensors	
Accelerometer, Gyroscope	LSM6DS3
Magnetic sensor	LIS3MDL
Pressure sensor	LPS25H
Relative humidity & temperature	HTS221
Digital MEMS Microphone	MP34DT01-M
Ambient Light Sensor	APDS-9250
User Input	
RG LED	LTST-C195KGJRKT

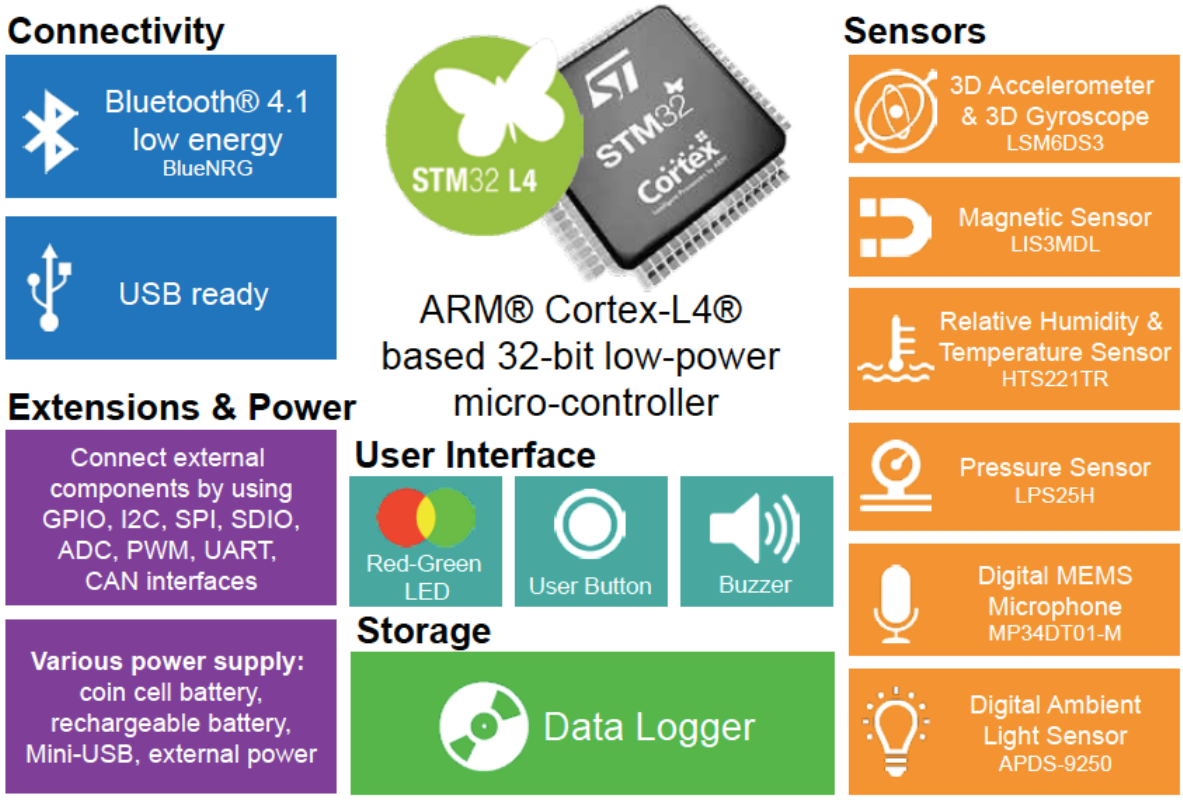
User Button	TL1014
Buzzer	ME05140SMC03
Data Logger	4Mbit SPI_Flash
Serial Flash	AT25XE041B-MHN-T
Mounting Type	Two 14pins/1.27 pitch female
Pin-Header Connector	PS3M34-114GBOTB-U
Extension Interface	
GPIO	18
I2C	2
SPI	2
USART	2
UART	2
ADC (12 bit)	4 ch
USB	OTG FS
PWM	5
SDIO	1
CAN (2.0B Active)	1
Power Interface	
Cell Battery	2 < Vin < 3.6
Coin Cell Battery	CR2025 , CR2032
Rechargeable Battery	Yes (external board)
Mini - USB	Yes (on Carrier Board)
External Power	4.5v < Vin < 7v
Dimensions	
SIMBA	20mm * 30mm
SIMBA height with Battery	10.43mm * 7.5mm
Battery Holder	20 * 22.50

1.3 Block Diagram

The system based on 6 main block's:

- Connectivity
- Micro Controller
- Extensions & Power
- Sensors
- Data Logger
- User Interface

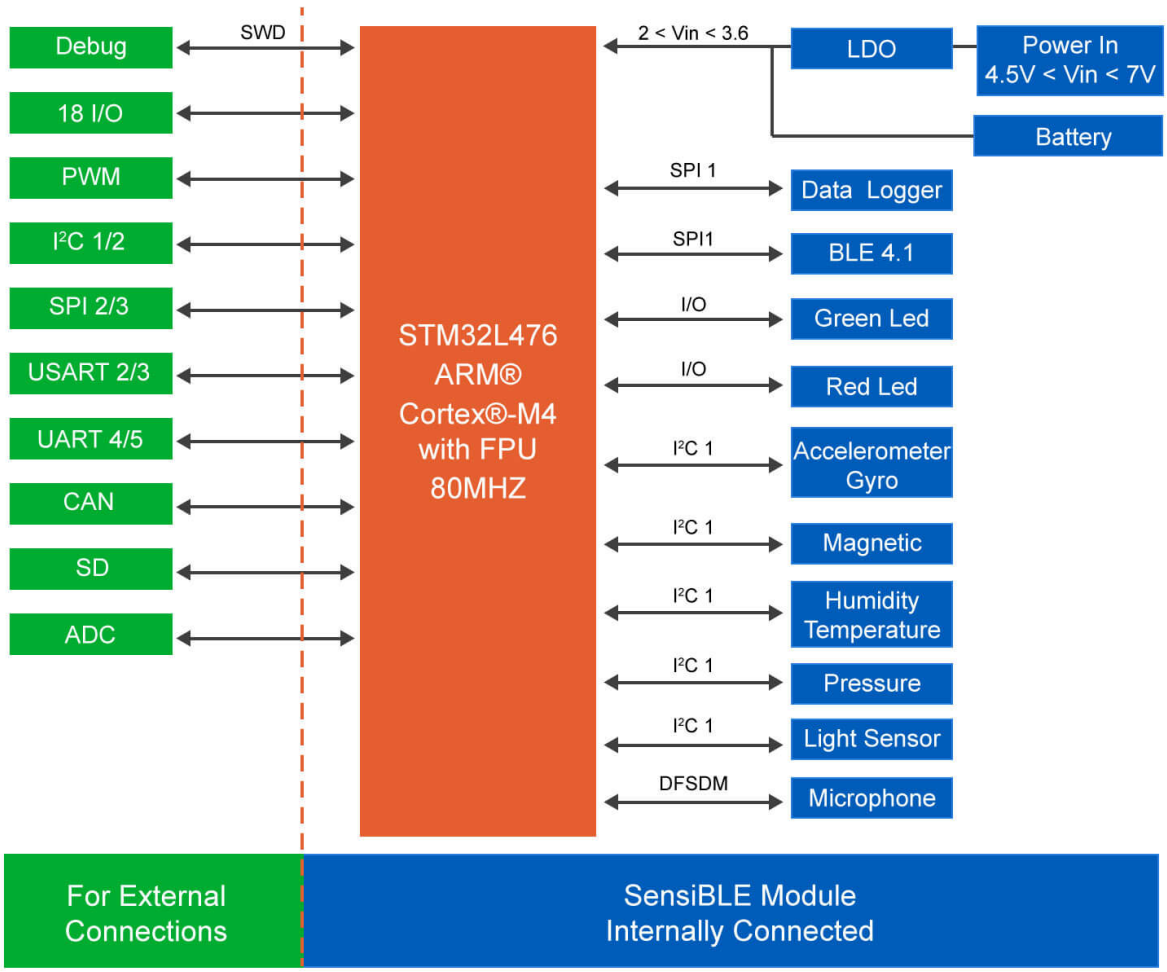
Figure 1 SensiBLE Block Diagram



2 Main Hardware Components

This section summarizes the main hardware building blocks of the *Sensi*BLE Module.
Part of the Connectivity used by the *Sensi*BLE module for internal connection between MCU and Sensors.
Microphone using DFSDM interface, Sensors connected to MCU using I^2C1, while BLE module and Data Logger connected via SPI1.

Figure 2 SensiBLE Internal & External Connections Diagram



Rest of unused Interfaces is free for user to interconnect with external world:

- 18 I/O
- PWM
- I^2C1, I^2C2
- SPI2, SPI3
- USART 2, USART3
- UART4, UART5
- CAN
- SD
- ADC

2.1 Microcontroller

2.1.1 STM32L476

The *Sensi*BLE module contains ST's STM32L476xx MCU. The STM32L476RG device are the ultra-low-power microcontrollers based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

2.2 Bluetooth

2.2.1 SPBTLE-RF

The *Sensi*BLE module contains ST's SPBTLE-RF. The SPBTLE-RF is an easy to use Bluetooth® Smart master/slave network processor module, compliant with Bluetooth® v4.1. The SPBTLE-RF B-SmarT module supports multiple roles simultaneously, and can act at the same time as Bluetooth Smart sensor and hub device.

2.3 Sensors

The *Sensi*BLE module contains verity of sensors :

- ST's 3D accelerometer and 3D gyroscope
- ST's 3-Axis Magnetometer
- ST's humidity and temperature
- ST's pressure sensor
- ST's digital microphone
- Avago's Digital RGB, IR and Ambient Light Sensor

2.3.1 LSM6DS3: inertial module: 3D accelerometer and 3D gyroscope

The LSM6DS3 is a system-in-package featuring a 3D digital accelerometer and a 3D digital gyroscope. Enabling always-on low-power features for an optimal motion experience.

2.3.2 LIS3MDL: 3-Axis Magnetometer

The LIS3MDL is an ultra low-power high-performance 3-Axis Magnetometer. This device offers the unique flexibility for designers to implement movement and position detection in space-constrained products such as personal navigation devices.

2.3.3 HTS221TR: humidity and temperature

The HTS221 is an ultra compact sensor for relative humidity and temperature. It includes a sensing element consists of a polymer dielectric planar capacitor structure and a mixed signal ASIC to provide the measurement information through digital serial interfaces.

2.3.4 LPS25H: pressure sensor

The LPS25H is an ultra compact absolute piezoresistive pressure sensor. It includes a monolithic sensing element capable to detect.

2.3.5 MP34DT01-M: digital microphone

The MP34DT01-M is an ultra-compact, low-power, omnidirectional, digital MEMS microphone built with a capacitive sensing element and an IC interface.
The sensing element, capable of detecting acoustic waves, is manufactured using a specialized silicon micromachining process dedicated to produce audio sensors.

2.3.6 APDS-9250: Digital RGB, IR and Ambient Light Sensor

The Avago APDS-9250 is a low-voltage digital RGB, IR and ambient light sensor device that converts light intensity to digital output signal. The color-sensing feature is useful in applications such as LED RGB backlight control, solid-state lighting, reflected LED color sampler and fluorescent light color temperature detection. With the IR sensing feature, the device can be used to read the IR content in certain lighting condition and detect the type of light source.

2.4 Data Logger

2.4.1 AT25XE041B

The *Sensi*BLE module contains Adesto® AT25XE041B . Adesto's AT25XE041B is a serial flash memory device.
Flexible erase architectures with page erase and block erase sizes make this memory ideal for data storage applications. AT25XE products feature ultra low-energy operation for active current, Program and Erase operations, as well as improved standby energy consumption. The device contains a specialized One-Time Programmable (OTP) security register usable for unique device serialization, system-level electronic serial number storage, and locked key storage.

2.5 User Interface

The *Sensi*BLE module contains verity of user interfaces :

- TongKeElectronics's Buzzer (PB11)
- IL SWITCH's Button (PC13)
- Lite-On's RG-LED (Led G @ PA5, Led R @ PC6)

2.5.1 LTST-C195KGJRKT Magnetic Buzzer

TongKE Electronics Buzzer based on Electro-Magnetic Acoustic Transducer for non-contact sound generation and reception using electromagnetic mechanisms.

2.5.2 SS304BS Button

IL SWITCH's is a Side push Surface Horizontal operating direction button.

2.5.3 LTST-C195KGJRKT Dual color chip LED

Lite-On's SMD Red/Green LED based 2 separate LED's in a package, allows two colors (red and green), while only having 4 pins (Dual set cathode and anode) miniature sizes and special configurations for space-sensitive applications. The color of the LED depends on the polarity of the connection, allowing separate and both colors at the same time.

3 External Connectors

The *Sensi*BLE exposes two low profile connectors. First J1 is 14 pin while Second J2 is 13 pin Board to Board connectors. The recommended mating connectors for Custom board interfacing are:

Pin Name: J1, J2

J1 - 14 pins 1row 1.27 Female
J2 - 13 pins 1row 1.27 Female

Pin #:	Pin Number
Schematic Name:	MCU name description
Type:	Pin type & direction
	S – Power Pin and/or Ground Pin
	I/O – GPIO
Func (#):	Function Number 1 to 4
Description:	Description of the Pin

3.1 Pin Mux

Table 3.1 and Table 3.2 explain function of connectivity pins in *Sensi*BLE module as well Pin MUX and alternate function available.

Table 3.1 - J1 *Sensi*BLE Module – Alternate Function

Pin #	Schematic Name	Type	Func1	Func2	Func3	Func4	Description
1	+5V_USB	S					Input voltage from USB +5V
2	VDD	S					+3.3V from voltage regulator
3	PB1	I/O	TIM3_CH4	TIM3_CH3N	ADC12_16		
4	PC4	I/O	ADC12_13	USART3_TX			
5	PB12	I/O	SPI2_NSS				
6	PB13	I/O	SPI2_SCK	I2C2_SCL			
7	PB14	I/O	SPI2_MISO	I2C2_SDA			
8	PC3	I/O	SPI2_MOSI	ADC123_14			
9	PA3	I/O	USART2_RX	TIM2_CH4	TIM5_CH4	TIM15_CH2	
10	PA2	I/O	USART2_TX	TIM2_CH3 TIM5_CH3	TIM15_CH1	ADC12_7	
11	JTCK/SW CLK	I/O					Serial clk pin SWD
12	JTMS/SW DAT	I/O					Serial data pin SWD
13	nReset	I/O					Reset pin
14	GND	S					Ground pin

Table 3.2 - J2 *Sensi*BLE Module – Alternate Function

	Schematic Name	Type	Func1	Func2	Func3	Func4	Description
1	PB5	I/O	TIM3_CH2		-	-	
2	GND	S	-	-	-	-	Ground pin
3	PA12	I/O	OTG_FS_DP	CAN1_TX			CAN/USB
4	PA11	I/O	OTG_FS_DM	CAN1_RX			CAN/USB
5	PA10	I/O	TIM1_CH3	OTG_ID			
6	PD2	I/O	SDMMC_CMD	UART5_RX			SDIO_CMD
7	PC12	I/O	SDMMC_CK	UART5_TX		SPI3_MOSI	SDIO_CLK
8	PC11	I/O	SDMMC_D3	USART3_RX	UART4_RX	SPI3_MISO	SDIO DATA3
9	PC10	I/O	SDMMC_D2	USART3_TX	UART4_TX	SPI3_SCK	SDIO DATA2
10	PC9	I/O	SDMMC_D1	TIM3_CH4	TIM8_CH4		SDIO DATA1
11	PC8	I/O	SDMMC_D0	TIM3_CH3	TIM8_CH3		SDIO DATA0
12	I2C1_SCL	I/O	I2C1_SCL				I2C1 bus clock
13	I2C1_SDA	I/O	I2C1_SDA				I2C1 bus data

4 Microcontroller

4.1 STM32L476

4.1.1 General Description

The STM32L476xx are the ultra-low-power microcontrollers based on the high performance ARM Cortex-M4, 32-bit RISC core operating at a frequency of up to 80 MHz.
The Cortex-M4 core features a Floating-point unit (FPU) single precision, which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L476 embed high-speed memories (Flash memory up to 1 Mbyte, up to 128 Kbyte of SRAM), an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix. The STM32L476 embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer fast 12-bit ADCs (5 Msps), an internal voltage reference buffer, a low-power RTC, two general-purpose 32-bit timer, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and two 16-bit low-power timers. The Micro Controller support digital filter for external sigma delta modulators (DFSDM).

In addition, 1 capacitive sensing button is available.

They also feature standard and advanced communication interfaces.

- Two I2Cs (I2C1 connected internally to Sensors).
- Three SPIs (SPI1 connected internally to BLE and Serial Flash).
- Two USARTs, two UARTs.
- One SDMMC
- One CAN
- One USB OTG full-speed

The STM32L476xx operates in the -40 to +85 C (+105 C junction), -40 to +105 C (+125 C junction) and -40 to +125 C (+130 C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low power applications.

4.1.2 Features

- Core: ARM® 32-bit Cortex®-M4 CPU
  - Frequency up to 80 MHz
  - FPU - Floating Point Unit
  - DSP instructions
  - Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait-state execution from Flash memory
  - MPU – Memory Protecting Unit

  - 100DMIPS/1.25DMIPS/MHz (Dhrystone 2.1)
  - 14-channel DMA controller
  - True random number generator
  - CRC calculation unit, 96-bit unique ID

- Memories
  - Up to 1 MB Flash, 2 banks read-while-write, proprietary code readout protection
  - Up to 128 KB of SRAM including 32 KB with hardware parity check

- Ultra-low-power with FlexPowerControl
  - 300 nA in VBAT mode: supply for RTC and 32x32-bit backup registers
  - 30 nA Shutdown mode (5 wakeup pins)
  - 120 nA Standby mode (5 wakeup pins)
  - 420 nA Standby mode with RTC
  - µA Stop 2 mode, 1.4 µA Stop 2 with RTC
  - 100 µA/MHz run mode
  - Batch acquisition mode (BAM)
  - 4 µs wakeup from Stop mode
  - Brown out reset (BOR) in all modes except shutdown
  - Interconnect matrix

- Clock Sources
  - 4 to 48 MHz crystal oscillator
  - 32 kHz crystal oscillator for RTC (LSE)
  - Internal 16 MHz factory-trimmed RC (±1%)
  - Internal low-power 32 kHz RC (±5%)
  - Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25 % accuracy)
  - 3 PLLs for system clock, USB, audio, ADC
  - RTC with HW calendar, alarms and calibration

- 1 capacitive sensing channels: support touchkey

- Timers
  - 16x timers: 2 x 16-bit advanced motor-control, 2 x 32-bit and 5 x 16-bit general purpose, 2x 16-bit basic, 2x low-power 16-bit timers (available in Stop mode), 2x watchdogs, SysTick timer

- digital filters for sigma delta modulator

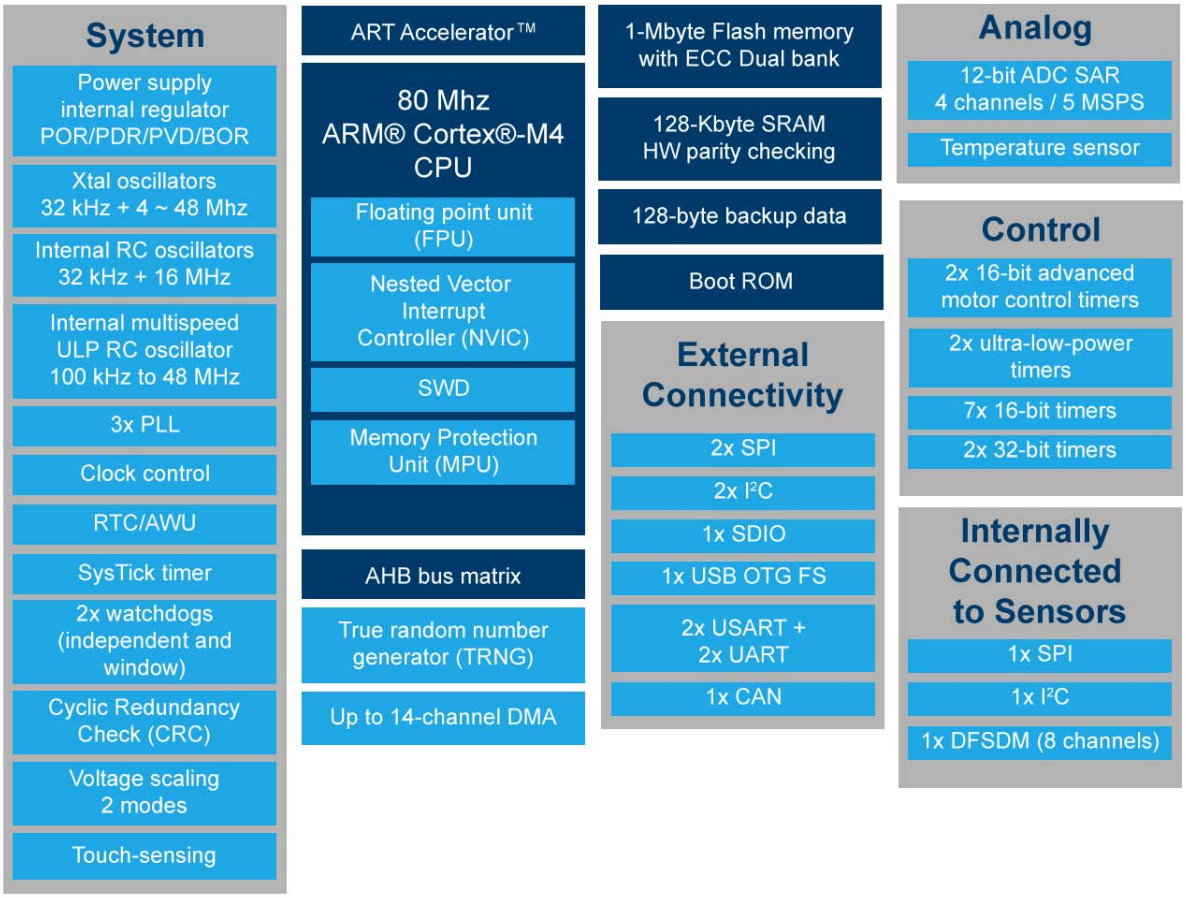
- Analog
  - Rich analog peripherals (independent supply)
  - 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
- Communication:
  - 10x communication interfaces
  - USB OTG 2.0 full-speed, LPM and BCD
  - 2x I2C FM+(1 Mbit/s), SMBus/PMBus
  - 2x USARTs (ISO 7816, LIN, IrDA, modem)
  - 2x USARTs (ISO 7816, LIN, IrDA, modem)
  - 2x SPIs

– CAN (2.0B Active)
– SDMMC interface

- Development support: serial wire debug (SWD).
- 1.71 V to 3.6 V power supply
- -40 °C to 85/105/125 °C temperature range

4.1.3 Block Diagram

Figure 3 SensiBLE's MCU Block Diagram



(*) Some of the peripherals are connected internally on-board sensors, others are available at extension connector (list).

5 Bleutooth

5.1 SPBTLE-RF

5.1.1 General Description

The SPBTLE-RF is a single-mode Bluetooth low energy master/slave network processor module compliant with Bluetooth® v4.1.

The SPBTLE-RF B-SmarT module integrates a 2.4 GHz RF radio the ST BlueNRG-MS on which a complete power-optimized stack for Bluetooth single mode protocol runs, providing

- Master, slave role support
- GAP: central, peripheral, observer or broadcaster roles
- ATT/GATT: client and server
- SM: privacy, authentication and authorization
- L2CAP
- Link Layer: AES-128 encryption and decryption

The BlueNRG-MS radio embeds nonvolatile Flash memory allows on-field stack upgrading.

In addition, according the Bluetooth specification v4.1 the SPBTLE-RF B-SmarT module provides:

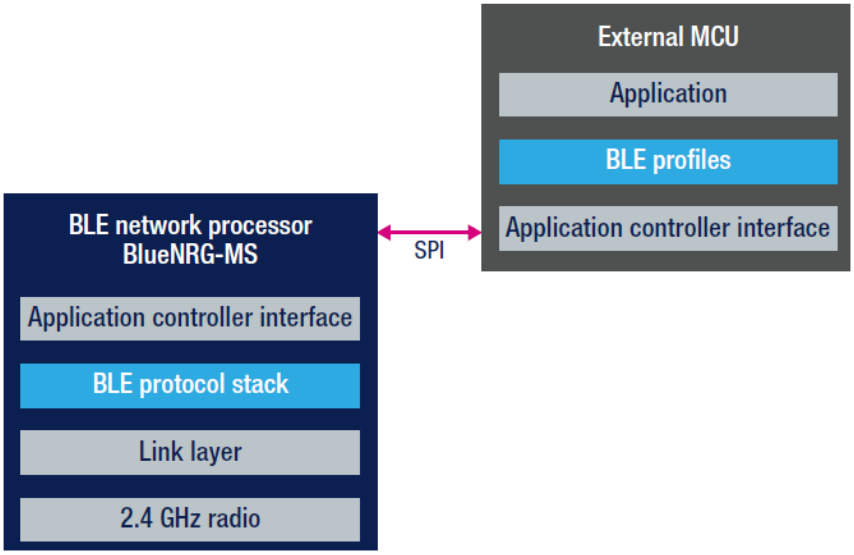
- Multiple roles simultaneously support
- Support simultaneous advertising and scanning
- Support being slave of up to two masters simultaneously
- Privacy V1.1
- Low duty cycle directed advertising
- Connection parameters request procedure
- LE Ping
- 32 bits UUIDs
- L2CAP connection oriented channels

The SPBTLE-RF B-SmarT module is equipped with Bluetooth low energy profiles in C

source code.

Application resides in the *Sensi*BLE's host application processor STM32L476, is interfaced with the SPBTLE-RF B-SmarT module through an application controller interface protocol, which is based on a standard SPI interface.

Figure 4 Embedded Bluetooth Low Energy Protocol Stack



The entire Bluetooth Smart stack and protocols are embedded in the BLE Module.

The *Sensi*BLE enables wireless connectivity, not requiring any RF experience or expertise. It provides a complete RF platform in a tiny form factor and being a certified solution optimizes the time to market of the final applications.

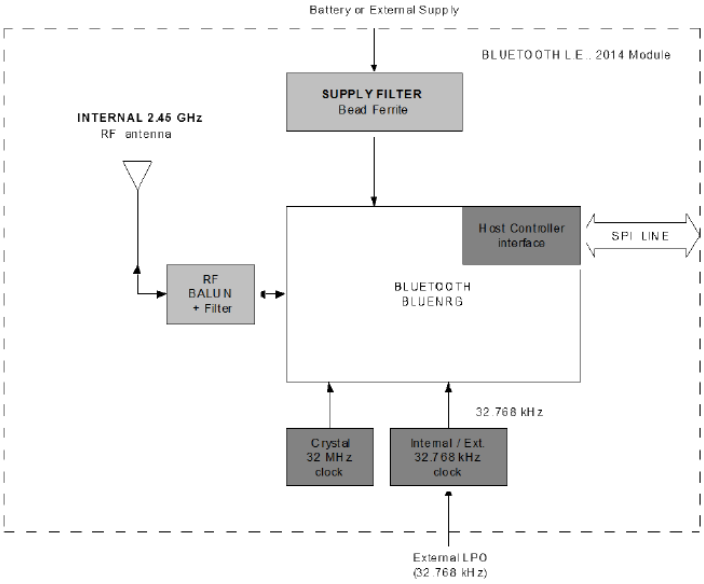
5.1.2 Features

- Bluetooth v4.1 compliant
  - Supports master and slave modes
  - Multiple roles supported simultaneously
- Embedded Bluetooth low energy protocol stack
  - GAP, GATT, SM, L2CAP, LL, RFPHY
- Bluetooth low energy profiles provided separately
- Bluetooth radio performance:
  - Embedded ST BlueNRG-MS
  - Tx power: + 4 dBm
  - Rx sensitivity: - 88 dBm
  - Provides up to 92 dB link budget with excellent link reliability
- Host interface
  - SPI, IRQ, and RESET
  - On-field stack upgrading available via SPI

- AES security co-processor
- Certification
  - CE qualified
  - FCC, IC modular approval certified
  - BQE qualified (in progress)
- On-board chip antenna
- Operating supply voltage: from 1.7 to 3.6 V
- Operating temperature range: -40 °C to 85 °C

5.1.3 Block Diagram

Figure 5 SPBTLE-RF HW Application Block Diagram



5.1.4 SPBTLE-RF Connections and Signals :

SPBTLE-RF Bluetooth NRG Certified Module soldered on top of *Sensi*BLE PCB to gain the Certification done previously by the SPBTLE-RF. The module connected by SPI1.

Figure 6 SPBTLE-RF Schematic Connections

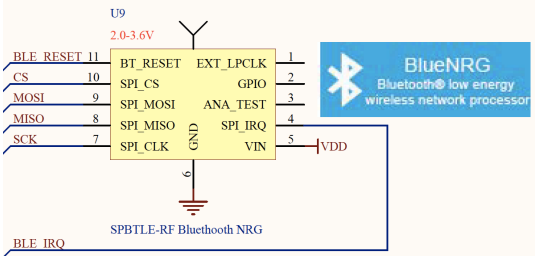


Table 1 SPBTLE-RF Pin Assignment

Name	Type	Pin #	Description	V max Tolerant
SPI Interface				
SPI_IRQ	O	4	SPI IRQ (slave has data for master	Vin
SPI_CLK	I	7	SPI Clock (max. 8 MHZ)	Vin
SPI_MISO	O	8		Vin
SPI_MOSI	I	9		Vin
SPI_CS	I	10		Vin
Power and Ground				
Vin		5	Vin	(1.7V – 3.6V max)
GND		6	GND	
Reset				
BT_Reset	I	11	Reset Input (active low < 0.35Vin)	(1.7V – 3.6V max)
LPO				
EXT_LPCLK	I	1	Not connected	
GPIO2	I/O	2	Not connected	
ANA TEST 0	I	3	Not connected	

6 Sensors

6.1 3D accelerometer and 3D gyroscope

6.1.1 General Description

The LSM6DS3 is a system-in-package featuring both high-performance 3-axis digital accelerometer and 3-axis digital gyroscope.

The integrated power-efficient modes are able to reduce the power consumption down to 1.25 mA in high-performance mode, combining always-on low-power features with superior sensing precision for an optimal motion experience for the consumer thanks to ultra-low noise performance for both the gyroscope and accelerometer.

The LSM6DS3 delivers best-in-class motion sensing that can detect orientation and gestures in order to empower application developers with features and capabilities that are more sophisticated than simply orienting their devices to portrait and landscape mode.

The event-detection interrupts enable efficient and reliable motion tracking and contextual awareness, implementing hardware recognition of free-fall events, 6D orientation, tap and double-tap sensing, activity or inactivity, and wakeup events.

The LSM6DS3 supports main OS requirements, offering real, virtual and batch mode sensors. In addition, the LSM6DS3 can efficiently run the sensor-related features specified in Android, saving power and enabling faster reaction time. In particular, the LSM6DS3 has been designed to implement hardware features such as significant motion, tilt, pedometer functions, time stamping and to support the data acquisition of an external magnetometer with ironing correction (hard, soft).

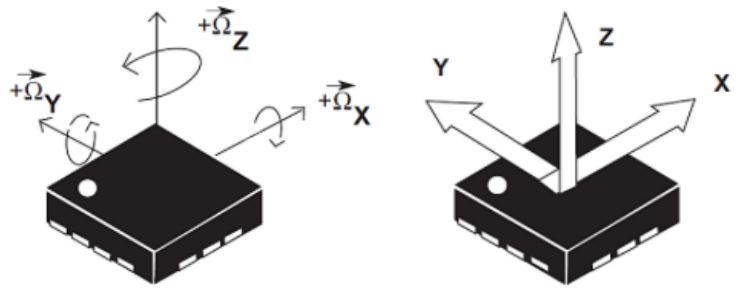
6.1.2 Features

- Power consumption: 0.9 mA in combo normal mode and 1.25 mA in combo high-performance mode up to 1.6 kHz.
- “Always-on” experience with low power consumption for both accelerometer and gyroscope
- Smart FIFO up to 8 kbyte data buffering based on features set
  - 100% efficiency with flexible configurations and partitioning
  - possibility to store timestamp
- Event-detection interrupts (fully configurable):
  - free-fall
  - wakeup
  - 6D orientation
  - tap and double-tap sensing
  - activity / inactivity recognition
- Specific IP blocks with negligible power consumption and high-performance:
  - pedometer functions: step detector and step counters
  - tilt detection (Android compliant)
  - significant motion (Android compliant)

- Data rate synchronization with external trigger for reduced sensor access and enhanced fusion
- Compliant with Android K and L
- Hard, soft ironing for external magnetic sensor corrections
- ±2/±4/±8/±16 g full scale
- ±125/±245/±500/±1000/±2000 dps full scale
- Analog supply voltage: 1.71 V to 3.6 V
- Independent IOs supply (1.62 V)
- Compact footprint, 2.5 mm x 3 mm x 0.83 mm
- SPI/I2C serial interface with main processor data synchronization feature
- Embedded temperature sensor
- ECOPACK®, RoHS and “Green” compliant

6.1.3 Block Diagram

Figure 7 LSM6DS3 HW Application Diagram



The LSM6DS3 has three operating modes available:

- only accelerometer active and gyroscope in power-down
- only gyroscope active and accelerometer in power-down
- both accelerometer and gyroscope sensors active with independent ODR

6.1.4 Connections and Signals

Figure 8 LSM6DS3 Schematic Connections

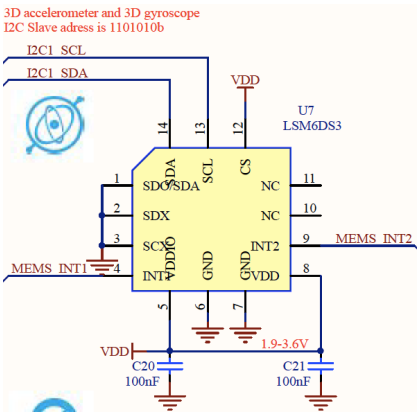


Table 2 LSM6DS3 Pin Assignment

Pin#	Name	Mode 1 function	Mode 2 Function
1	SDO/SA0	SPI 4-wire interface serial data output (SDO) I^2C Least significant bit of the device address (SA0)	SPI 4-wire interface serial data output (SDO) I^2C Least significant bit of the device address (SA0)
2	SDx	Connect to VDDIO or GND	I^2C Serial data master (MSDA)
3	SCx	Connect to VDDIO or GND	I^2C Serial data master (MSDA)
4	INT1	Programmable interrupt 1	
5	$VDDIO^{(1)}$	Power supply for I/O pins	
6	GND	0 V supply	
7	GND	0 V supply	
8	$VDD^{(2)}$	Power suppl	
9	INT2	Programmable interrupt 2 (INT2)/Data enable (DEN)	Programmable interrupt 2 (INT2)/Data enable (DEN)/ I^2C master external synchronization signal (MDRDY)
10	$NC^{(3)}$	Leave unconnected	
11	$NC^{(3)}$	Leave unconnected	
12	CS	I^2C /SPI mode selection (1:SPI idle mode / I^2C communication enabled; 0:SPI communication mode/ I^2C disabled)	I^2C /SPI mode selection (1:SPI idle mode / I^2C communication enabled; 0:SPI communication mode/ I^2C disabled)
13	SCL	I^2C serial clock (SCL) SPI serial port clock (SPC)	I^2C serial clock (SCL) SPI serial port clock (SPC)
14	SDA	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)

6.2 Magnetic Sensor

6.2.1 General Description

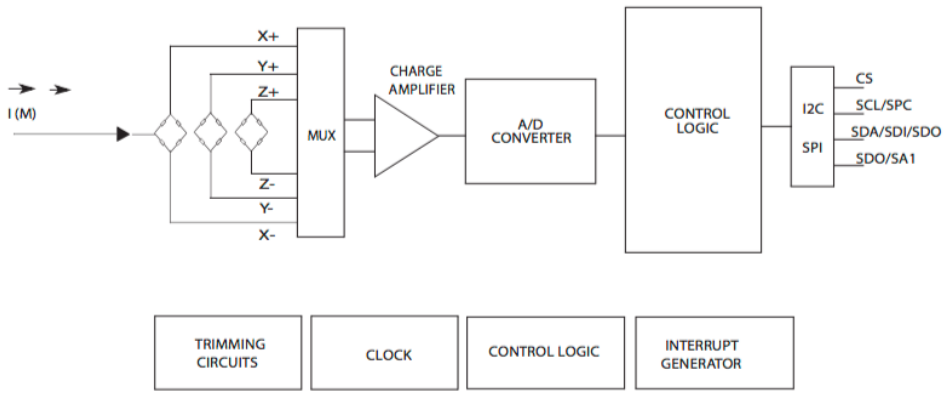
The *Sensi*BLE module contains ST's LIS3MDL. The LIS3MDL is an ultra-low-power high-performance three-axis magnetic sensor.
The LIS3MDL has user-selectable full scales of ±4/ ±8/ ±12/ ±16 gauss.
The self-test capability allows the user to check the functioning of the sensor in the final application.
The device may be configured to generate interrupt signals for magnetic field detection.

6.2.2 Features

- Wide supply voltage, 1.9 V to 3.6 V
- Independent IO supply (1.8 V)
- ±4/ ±8/ ±12/ ±16 gauss selectable magnetic full scale
- Continuous and single-conversion modes
- 16-bit data output
- Interrupt generator
- Self-test
- I2C digital output interface
- Power-down mode/ low-power mode
- ECOPACK® , RoHS and "Green" compliant

6.2.3 Block Diagram

Figure 9 LIS3MDL Block Diagram



6.2.4 Connections and Signals

Figure 10 LIS3MDL Schematic Connections

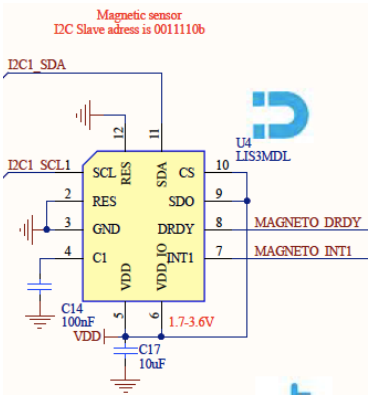


Table 3 LIS3MDL Pin Assignment

Pin#	Name	Function
1	SCL SPC	I^2C Serial clock (SCL) SPI serial port clock (SPC)
2	Reserved	Connect to GND
3	GND	Connect to GND
4	C1	Capacitor connection (C1=100nf)
5	Vdd	Power supply
6	Vdd_IO	Power supply for I/O pins
7	INT	interrupt
8	DRDY	Data Ready
9	SDO SA1	SPI serial data output (SDO) I^2C less significant bit of the device address (SA1)
10	CS	SPI enable /SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI commication mode / I^2C disabled)
11	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
12	Reserved	Connect to GND

6.3 Humidity and Temperature Sensor

6.3.1 General Description

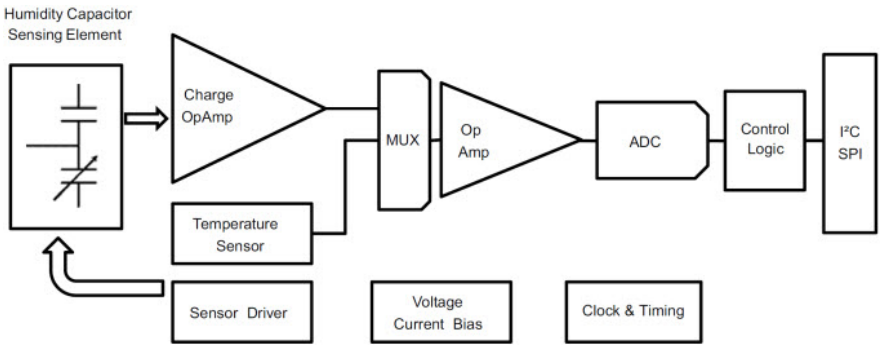
The *Sensi*BLE module contains ST's HTS221. The HTS221 is an ultra compact sensor for relative humidity and temperature. It includes a sensing element and a mixed signal ASIC to provide the measurement information through digital serial interfaces.
The sensing element consists of a polymer dielectric planar capacitor structure capable of detecting relative humidity variations.

6.3.2 Features

- 0 to 100% relative humidity range
- Supply voltage: 1.7 to 3.6 V
- Low power consumption: 2 µA @ 1 Hz ODR
- Selectable ODR from 1 Hz to 12.5 Hz
- High rH sensitivity: 0.004% rH/LSB
- Humidity accuracy: ± 3.5% rH, 20 to +80% rH
- Temperature accuracy: ± 0.5 °C,15 to +40 °C
- Embedded 16-bit ADC
- 16-bit humidity and temperature output data
- I²C interfaces
- Factory calibrated
- Tiny 2 x 2 x 0.9 mm package
- ECOPACK® compliant

6.3.3 Block Diagram

Figure 11 HTS221 Block Diagram



6.3.4 Connections and Signals

Figure 12 HTS221 Schematic Connections

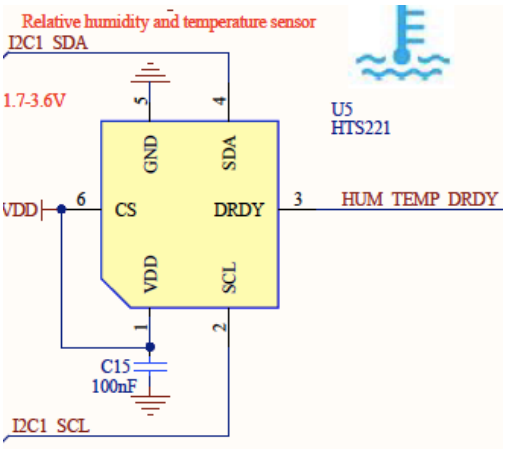


Table 4 HTS221 Pin Assignment

Pin #	Name	Function
1	Vdd	Power Supply
2	SCL	I^2C serial clock (SCL)
3	DRDY	Data Ready output signal
4	SDA	I^2C serial data (SDA)
5	GND	Ground
6	SPI enable	I^2C /SPI mode selection 1: SPI idle mode / I^2C communication enabled

6.4 Pressure Sensor

6.4.1 General Description

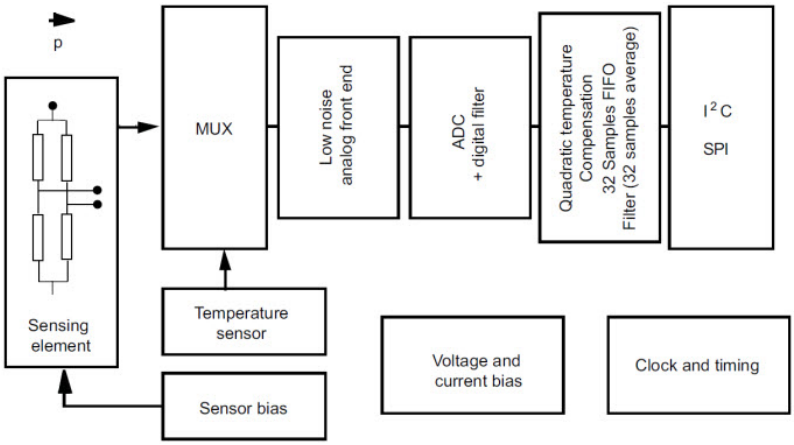
The *Sensi*BLE module contains ST's LPS25H. The LPS25H is an ultra compact absolute piezoresistive pressure sensor. It includes a monolithic sensing element and an IC interface able to take the information from the sensing element and to provide a digital signal.
The sensing element consists of a suspended membrane realized inside a single mono-silicon substrate.

6.4.2 Features

- 260 to 1260 mbar absolute pressure range
- High-resolution mode: 1 Pa RMS
- Low power consumption:
- Low resolution mode: 4 µA
- High resolution mode: 25 µA
- High overpressure capability: 20x full scale
- Embedded temperature compensation
- Embedded 24-bit ADC
- Selectable ODR from 1 Hz to 25 Hz
- I²C interfaces
- Embedded FIFO
- Supply voltage: 1.7 to 3.6 V
- High shock survivability: 10,000 g
- Small and thin package
- ECOPACK® lead-free compliant

6.4.3 Block Diagram

Figure 13 LPS25H Block Diagram



6.4.4 Connections and Signals

Figure 14 LPS25H Schematic Connections

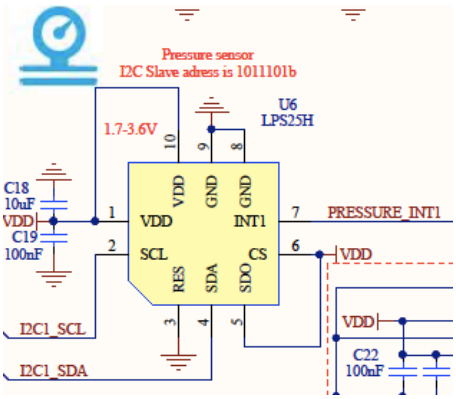


Table 5 LPS25H Pin Assignment

Pin Number	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	SCL SPC	I^2C Serial clock (SCL) SPI serial port clock (SPC)
3	Reserved	Connect to GND
4	SDA SDI SDI/SDO	I^2C Serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input/output (SDI/SDO)
5	SDO SA0	4-wire SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
6	CS	SPI enable I^2C / SPI mode selection (1: SPI idle mode / communication enabled; 0: SPI communication mode / I^2C disabled)
7	INT_DRDY	Interrupt or Data Ready
8	GND	0V supply
9	GND	0V supply
10	VDD	Power supply

6.5 Digital Microphone

6.5.1 General Description

The *Sensi*BLE module contains ST's MP34DT01-M. The MP34DT01-M is an ultra-compact, low-power, omnidirectional, digital MEMS microphone built with a capacitive sensing element and an IC interface.
The sensing element, capable of detecting acoustic waves. Able to provide a digital signal externally in PDM format.
The MP34DT01-M has an acoustic overload point of 120 dBSPL with a 61 dB signal-to-noise ratio and –26 dBFS sensitivity.

6.5.2 Features

- Single supply voltage
- Low power consumption
- 120 dBSPL acoustic overload point
- 61 dB signal-to-noise ratio
- Omnidirectional sensitivity
  - 26 dBFS sensitivity
- PDM output
- HCLGA package
- Top-port design
- SMD-compliant
- EMI-shielded
- ECOPACK®,RoHS, and "Green" compliant

6.5.3 Block Diagram

TBD

6.5.4 Connections and Signals

Figure 15 MP34DT01-M Schematic Connections

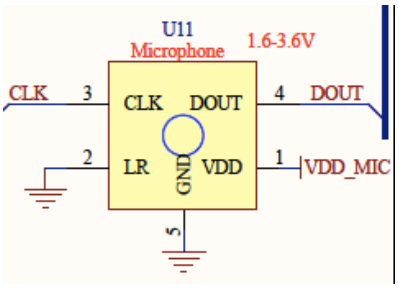


Table 6 MP34DT01-M Pin Assignment

Pin #	Pin name	Function
1	Vdd	Power supply
2	LR	Left/Right channel selection
3	CLK	Synchronization input clock
4	DOUT	Left/Right PDM data output
5 (ground ring)	GND	0 V Supply

6.6 Digital RGB, IR and Ambient Light Sensor

6.6.1 General Description

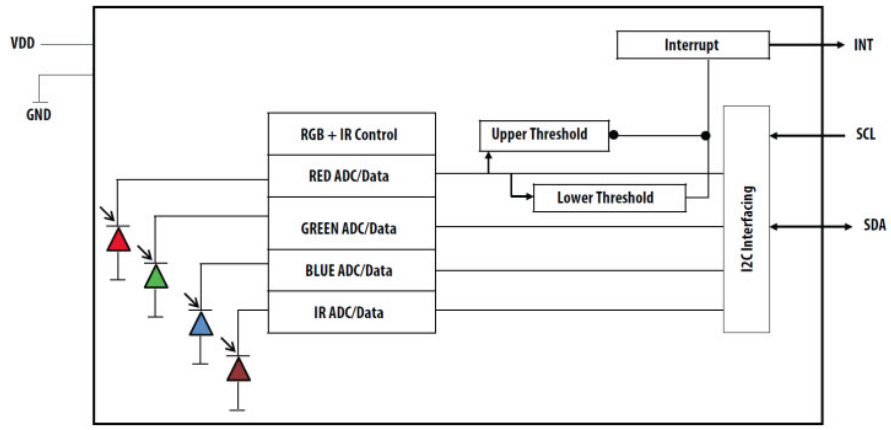
The *Sensi*BLE module contains Avago's APDS-9250. The Avago APDS-9250 is a low-voltage digital RGB, IR and ambient light sensor device that convert light intensity to digital output signal. The device supports I2C-bus interface and has a programmable interrupt controller that takes minimal micro-controller (MCU) resources. The color-sensing feature is useful in applications such as LED RGB backlight control, solid-state lighting, reflected LED color sampler and fluorescent light color temperature detection. With the IR sensing feature, the device can be used to read the IR content in certain lighting condition and detect the type of light source.

6.6.2 Features

- Colour and Ambient Light Sensing (CS-RGB and ALS)
  - Accuracy of Correlated Color Temperature (CCT)
  - Individual channels for Red, Green, Blue and Infared
  - Approximates Human Eye Response with Green Channel
  - Red, Green, Blue, Infrared and ALS Sensing
  - High Sensitivity in low lux condition - Ideally suited for Operation Behind Dark Glass
  - Wide Dynamic Range: 18,000,000: 1
  - Up to 20-Bit Resolution
- Power Management
  - Low Active Current - 130 µA typical
  - Low Standby Current - 1µA typical
- I2C-bus Fast Mode Compatible Interface
  - Up to 400kHz (I2C Fast-Mode)
  - Dedicated Interrupt Pin

6.6.3 Block Diagram

Figure 16 APDS-9250 Block Diagram



6.6.4 Connections and Signals

Figure 17 APDS-9250 Schematic Connections

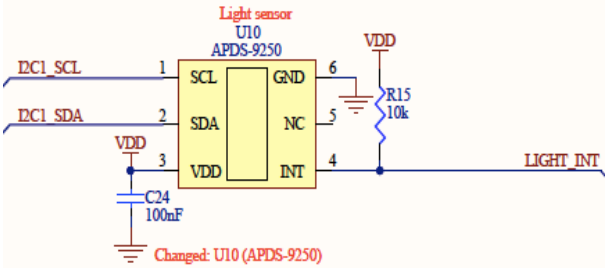


Table 7 APDS-9250 Pin Assignment

Pin	Name	Type	Description
1	SCL	I	I^2C Serial Clock input Terminal – Clock Signal for I2C Serial Data
2	SDA	I/O	Serial Data I/O for I^2C
3	VDD	Supply	Power Supply Voltage
4	INT	O	Interrupt – Open Drain
5	NC		No Connect
6	GND	Ground	Power Supply Ground. All Voltage and reference to GND.

7 Serial Flash

7.1 AT25XE041B

7.1.1 Description

The Adesto® AT25XE041B is a serial interface Flash memory device designed for use in applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the AT25XE041B, with its page erase granularity it is ideal for data storage as well, eliminating the need for additional data storage devices. The erase block sizes of the AT25XE041B have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own erase regions, the wasted and unused memory space that occurs with large sectored and large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density. The device also contains a specialized OTP (One-Time Programmable) Security Register that can be used for purposes such as unique device serialization, system-level Electronic Serial Number (ESN) storage, locked key storage, etc. The AT25XE041B supports read, program, and erase operations.

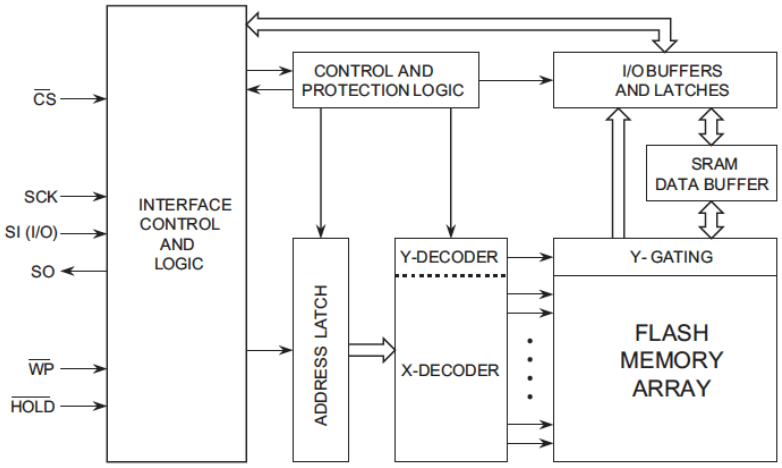
7.1.2 Features

- Single 1.65V - 3.6V Supply
- Serial Peripheral Interface (SPI) Compatible
  - Supports SPI Modes 0 and 3
  - Supports Dual-I/O Operation
- 85MHz Maximum Operating Frequency
  - Clock-to-Output (tV) of 6 ns
- Flexible, Optimized Erase Architecture for Code + Data Storage Applications
  - Uniform 4-Kbyte Block Erase
  - Uniform 32-Kbyte Block Erase
  - Uniform 64-Kbyte Block Erase
  - Full Chip Erase
- Hardware Controlled Locking of Protected Sectors via WP Pin
- 128-byte, One-Time Programmable (OTP) Security Register
  - 64 bytes factory programmed with a unique identifier
  - 64 bytes user programmable
- Flexible Programming
  - Byte/Page Program (1 to 256 Bytes)
  - Dual-Input Byte/Page Program (1 to 256 Bytes)
  - Sequential Program Mode Capability
- Fast Program and Erase Times
  - 2ms Typical Page Program (256 Bytes) Time
  - 45ms Typical 4-Kbyte Block Erase Time
  - 360ms Typical 32-Kbyte Block Erase Time

  - 720ms Typical 64-Kbyte Block Erase Time
- Automatic Checking and Reporting of Erase/Program Failures
- Software Controlled Reset
- JEDEC Standard Manufacturer and Device ID Read Methodology
- Low Power Dissipation
  - 200nA Ultra Deep Power Down current (Typical)
  - 5µA Deep Power-Down Current (Typical)
  - 25uA Standby current (Typical)
  - 3.5mA Active Read Current (Typical)
- Endurance: 100,000 Program/Erase Cycles
- Data Retention: 20 Years
- Complies with Full Industrial Temperature Range

7.1.3 Block Diagram

Figure 18 AT25XE041B Block Diagram



7.1.4 Connections and Signals

Figure 19 APDS-9250 Schematic Connections

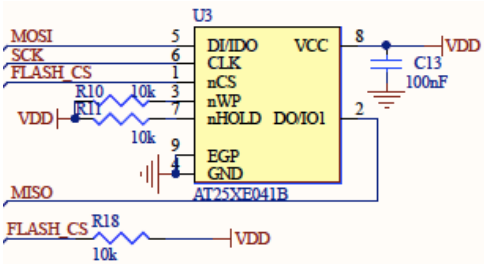


Table 8 AT25XE041B Pin Assignment

Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	**CHIP SELECT:** Asserting the $\overline{CS}$ pin selects the device. When the $\overline{CS}$ pin is deasserted, the device will be deselected and normally be placed in standby mode (not Deep Power-Down mode), and the SO pin will be in a high-impedance state. When the device is deselected, data will not be accepted on the SI pin. A high-to-low transition on the $\overline{CS}$ pin is required to start an operation, and a low-to-high transition is required to end an operation. When ending an internally self-timed operation such as a program or erase cycle, the device will not enter the standby mode until the completion of the operation.	Low	Input
SCK	**SERIAL CLOCK:** This pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command, address, and input data present on the SI pin is always latched in on the rising edge of SCK, while output data on the SO pin is always clocked out on the falling edge of SCK.	-	Input
SI (I/O_0)	**SERIAL INPUT:** The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched in on the rising edge of SCK. With the Dual-Output Read commands, the SI Pin becomes an output pin (I/O_0) in conjunction with other pins to allow two bits of data on (I/O_{1-0}) to be clocked out on every falling edge of SCK. To maintain consistency with the SPI nomenclature, the SI (I/O_0) pin will be referenced as the SI pin unless specifically addressing the Dual-I/O modes in which case it will be referenced as I/O_0. Data present on the SI pin will be ignored whenever the device is deselected (CS is deasserted).	-	Input/ Output
SO (I/O_1)	**SERIAL OUTPUT:** The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK. With the Dual-Output Read commands, the SO Pin remains an output pin (I/O_1) in conjunction with other pins to allow two bits of data on (I/O_{1-0}) to be clocked out on every falling edge of SCK. To maintain consistency with the SPI nomenclature, the SO (I/O_1) pin will be referenced as the SO pin unless specifically addressing the Dual-I/O modes in which case it ise referenced as I/O_1. The SO pin will be in a high-impedance state whenever the device is deselected (CS is deasserted).	-	Input/ Output
$\overline{WP}$	**WRITE PROTECT:** The $\overline{WP}$ pin controls the hardware locking feature of the device. Please refer to "Protection Commands and Features" on page 17 for more details on protection features and the $\overline{WP}$ pin. The $\overline{WP}$ pin is internally pulled-high and may be left floating if hardware controlled protection will not be used. However, it is recommended that the $\overline{WP}$ pin also be externally connected to V_{CC} whenever possible.	Low	Input
$\overline{HOLD}$	**HOLD:** The $\overline{HOLD}$ pin is used to temporarily pause serial communication without deselecting or resetting the device. While the $\overline{HOLD}$ pin is asserted, transitions on the SCK pin and data on the SI pin will be ignored, and the SO pin will be in a high-impedance state. The CS pin must be asserted, and the SCK pin must be in the low state in order for a Hold condition to start. A Hold condition pauses serial communication only and does not have an effect on internally self-timed operations such as a program or erase cycle. Please refer to "Hold" on page 35 for additional details on the Hold operation.The $\overline{HOLD}$ pin is internally pulled-high and may be left floating if the Hold function will not be used. However, it is recommended that the $\overline{HOLD}$ pin also be externally connected to V_{CC} whenever possible.	Low	Input
V_{CC}	**DEVICE POWER SUPPLY:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	-	Power
GND	**GROUND:** The ground reference for the power supply. GND should be connected to the system ground.	-	Power

8 Absolute Maximum Characteristics

TBD

9 Operational Characteristics

9.1 Power supplies

TBD

9.2 Power Consumption

TBD

10 DC Electrical Characteristics

TBD

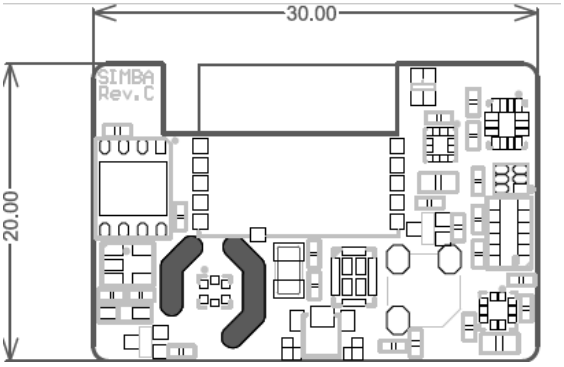
11 Environmental Specifications

TBD

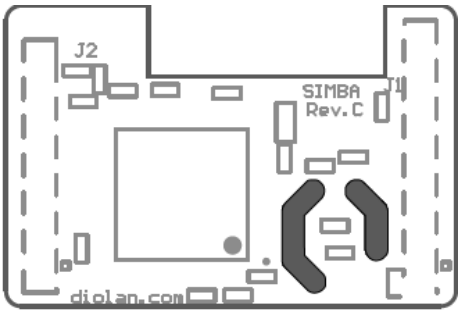
12 Mechanical Drawings

12.1 *Sensi*BLE Module: SIMBA

Figure 20 SensiBLE Top and Down View [mm]



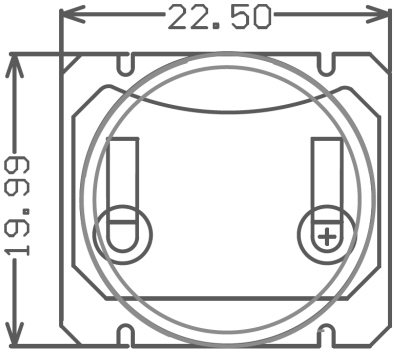
Top View [mm]



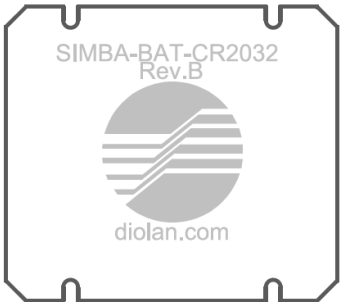
Down View

12.2 Battery Holder: SIMBA-BAT-CR2032

Figure 21 SensiBLE Battery Holder Top and Down View [mm]



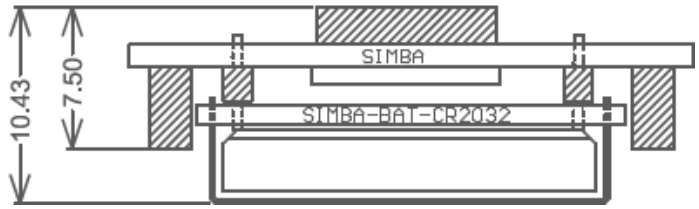
Top View [mm]



Down View

12.3 *Sensi*BLE Module with Coin Battery: SIMBA-PRO

Figure 22 SensiBLE Module with Coin Battery Side View [mm]



Side View [mm]

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

SensiEDGE:
SIMBA-PRO