STLQ020

Datasheet

200 mA ultra-low quiescent current LDO

DFN6-2x2

Flip-Chip4

SOT323-5L

Features

- Operating input voltage range: 2 V to 5.5 V
- Output current up to 200 mA
- Ultra-low quiescent current:
  - 300 nA typ. at no load
  - 100 µA typ. at 200 mA load
- Controlled I_q in dropout conditions
- Very low-dropout voltage: 160 mV at 200 mA
- Output voltage accuracy: 2% at room temperature, 3% in full temperature range
- Output voltage versions: from 0.8 V to 4.5 V, with 50 mV step and adjustable
- Logic-controlled electronic shutdown
- Output discharge feature (optional)
- Internal overcurrent and thermal protections
- Temperature range: from -40 °C to +125 °C
- Packages: DFN6-2x2, SOT323-5L, Flip-Chip4

Applications

- Smartphones/tablets
- Image sensors
- Wearable accessories
- Healthcare devices
- Metering

Maturity status link
STLQ020

Description

The STLQ020 is a 200 mA low-dropout voltage regulator, able to work with an input voltage ranging from 2 V to 5.5 V.

The typical dropout voltage at maximum load is 160 mV.

The ultra-low quiescent current, which is just 0.3 µA at no load, extends battery-life of applications requiring very long standby time.

Even though the device intrinsic consumption is ultra-low, STLQ020 is able to provide fast transient response and good PSRR performance, thanks to its adaptive biasing circuit.

Enable pin puts the STLQ020 in shutdown mode, reducing total current consumption to 5 nA.

The STLQ020 is designed to keep the quiescent current under control and at a low value also during dropout operation, helping to extend even more the operating time of battery- powered devices.

It also includes short-circuit constant-current limiting and thermal protection.

Several small package options are available.

1 Block diagram

Figure 1. **Block diagram (fixed version)**

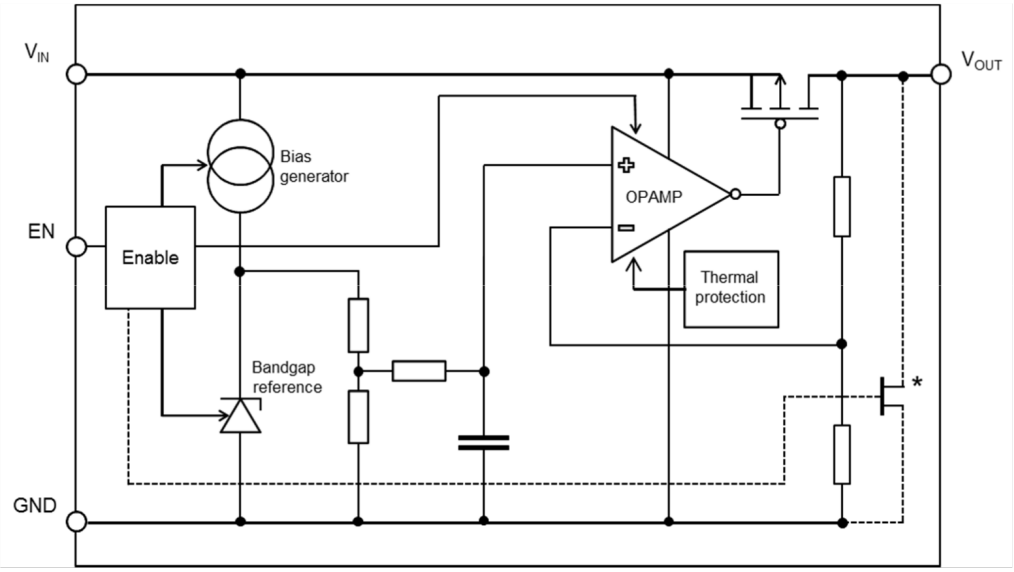
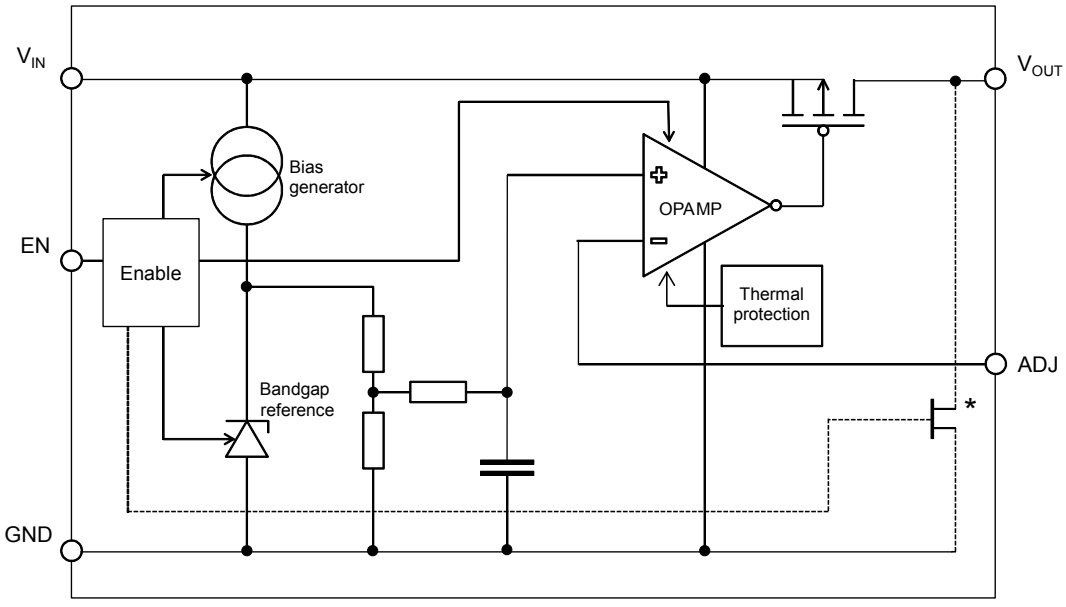


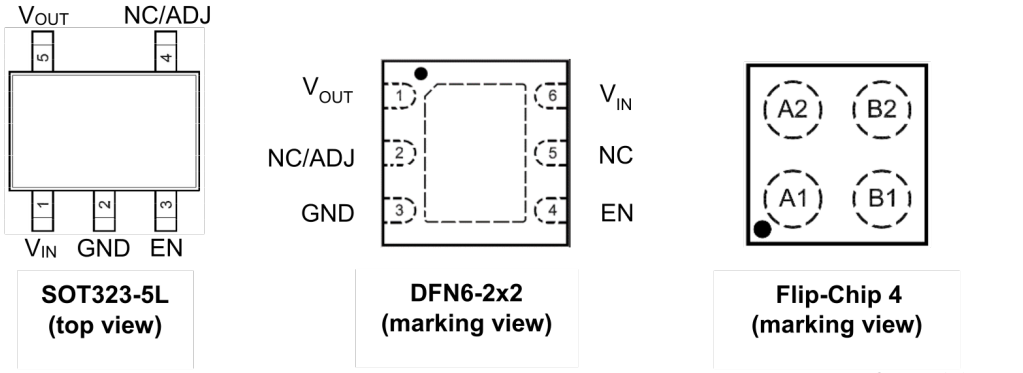
Figure 2. **Block diagram (adjustable version)**



Note: (*) output discharge function is optional.

2 Pin configuration

Figure 3. **Pin configuration**



AMG240320171202MT

Table 1. **Pin description**

Symbol	SOT323-5L	DFN6-2x2	Flip-Chip4	Description
V_{IN}	1	6	A1	LDO supply voltage
V_{OUT}	5	1	A2	LDO output voltage
GND	2	3	B2	Ground
EN	3	4	B1	Enable input: set V_{EN} = high to turn on the device; V_{EN} = low to turn off the device. Not internally pulled-up, don't leave floating.
NC/ADJ	4	2	-	Adjustable pin (only on ADJ version). Connect to external resistor divider. Not connected on the fixed version
NC	-	5	-	Not internally connected: it can be connected to GND
Exposed pad	-	Exposed pad	-	Must be connected to GND

3 Typical application diagram

Figure 4. **Typical application diagram (fixed version)**

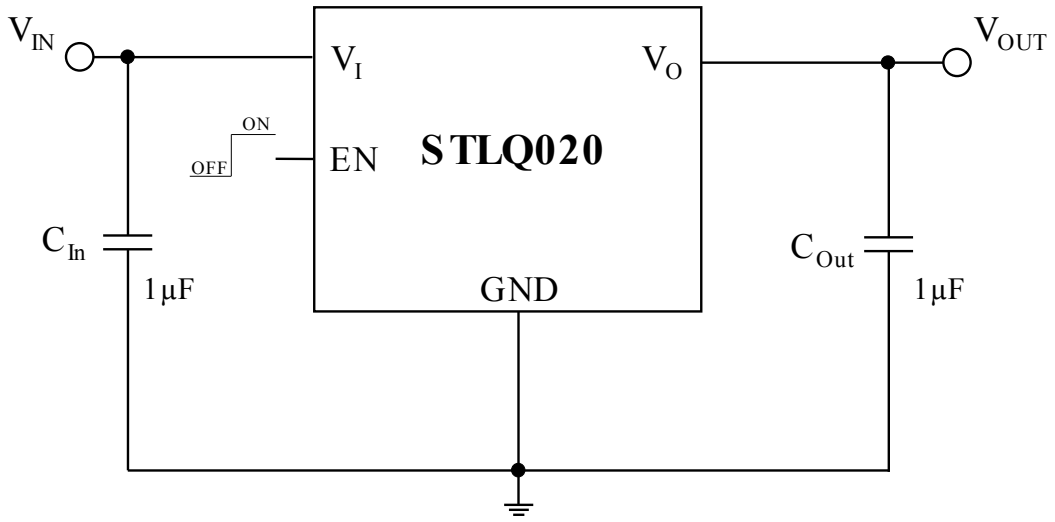


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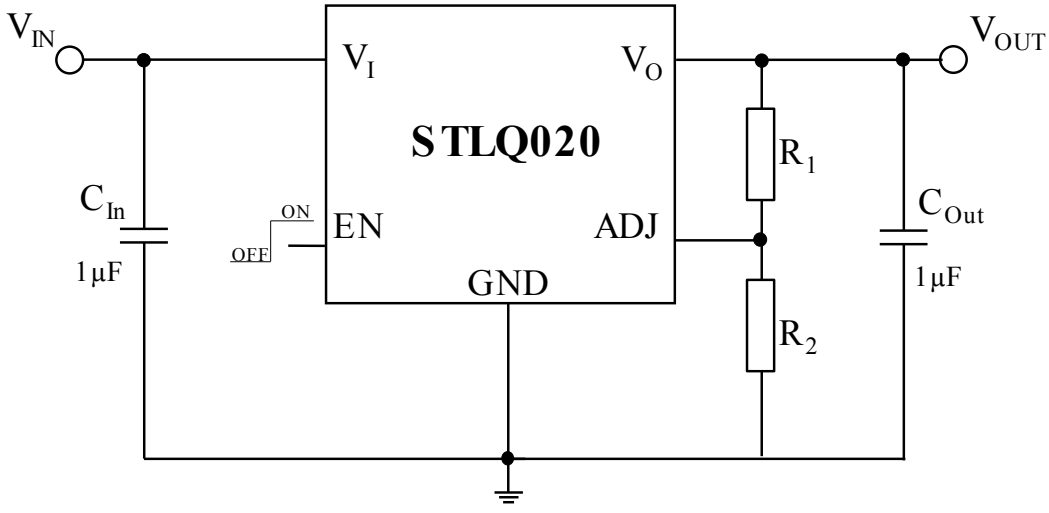
Figure 5. **Typical application diagram (adjustable version)**



Adjustable version

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Note: R_1 and R_2 are calculated according to the following formula: $R_1 = R_2 \times (V_{OUT} / V_{ADJ} - 1)$.

4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input supply voltage	-0.3 to 7	V
V_{OUT}	Output voltage	-0.3 to V_{IN} + 0.3	V
V_{ADJ}	Adjustable pin voltage	-0.3 to 2	V
I_{OUT}	Output current	Internally limited	A
EN	Enable pin voltage	-0.3 to V_{IN} + 0.3	V
P_D	Power dissipation	Internally limited	W
ESD	Charged device model	±500	V
	Human body model	±2000	
T_{J-OP}	Operating junction temperature	-40 to 125	°C
T_{J-MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature	-55 to 150	°C

Table 3. Thermal data

Symbol	Parameter	DFN6-2x2	Flip-Chip4	SOT323-5L	Unit
R_{thjc}	Thermal resistance, junction-to-case	15		130	°C/W
R_{thja}	Thermal resistance, junction-to-ambient	65	180	250	°C/W

5 Electrical characteristics

T_J = 25 °C, V_{IN} = V_{OUT} + 0.5 V or 2 V, whichever is greater; V_{EN} = V_{IN}; C_{IN} = 1 µF; C_{OUT} = 1 µF; I_{OUT} = 1 mA.

Table 4. Electrical characteristics (fixed version)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		2		5.5	V
V_{OUT}	Output voltage accuracy	T_J = 25 °C	-2		2	%
		-40 °C < T_J < 125 °C	-3		3	
$\Delta V_{OUT\%}/\Delta V_{IN}$	Static line regulation	V_{OUT} + 0.5 V < V_{IN} < 5.5 V (1)		0.005		%/V
		-40 °C < T_J < 125 °C			0.05	
$\Delta V_{OUT\%}/\Delta I_{OUT}$	Static load regulation	1 mA < I_{OUT} < 0.2 A; T_J = 25 °C		0.0015		%/mA
		-40 °C < T_J < 125 °C			0.005	
V_{DROP}	Dropout voltage (2)	V_{OUT} = 2.5 V; I_{OUT} = 0.2 A		160		mV
		V_{OUT} = 2.5 V; I_{OUT} = 20 mA		15		mV
eN	Output noise voltage	f = 10 Hz to 100 kHz		135		$\mu V_{RMS}/V_{OUT}$
SVR	Supply voltage rejection	V_{OUT} = 2.5 V; V_{RIPPLE} = 0.2 Vpp		52		dB
		I_{OUT} = 10 mA; f = 100 Hz				
		V_{OUT} = 2.5 V; V_{RIPPLE} = 0.2 Vpp		35		
		I_{OUT} = 10 mA ; f = 1 kHz				
		V_{OUT} = 2.5 V; V_{RIPPLE} = 0.2 Vpp		45		
		I_{OUT} = 10 mA; f = 10 kHz				
I_q	Quiescent current	I_{OUT} = 0 A		300		nA
		I_{OUT} = 0 A; -40 °C < T_J < 125 °C			1000	
		I_{OUT} = 0.2 A		100		µA
		I_{OUT} = 0.2 A; -40 °C < T_J < 125 °C			150	
	Shutdown current	V_{EN} = 0 V, V_{IN} = V_{OUT} + 0.5 V (1)		0.005	0.05	µA
I_{SC}	Short-circuit current	V_{OUT} = 0 V		380		mA
R_{LOW} (3)	Output discharge resistance	V_{EN} = 0 V		100		Ω
V_{EN}	Enable input logic low	-40 °C < T_J < 125 °C			0.4	V
	Enable input logic high		1.2			
I_{EN}	Enable pin input current	V_{EN} = V_{IN}; 1.25 < V_{IN} < 6.0 V		1		nA
T_{SHDN}	Thermal shutdown (4)	I_{OUT} > 1 mA		160		°C
	Hysteresis			20		

1. *V_{IN} = V_{OUT} + 0.5 V or 2 V, whichever is greater.*
2. *Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.*
3. *On specific version only.*
4. *The thermal protection is not active when the load current is lower than 1 mA.*

T_J = 25 °C, V_{IN} = 2 V, V_{EN} = V_{IN}; C_{IN} = 1 µF; C_{OUT} = 1 µF; I_{OUT} = 1 mA.

Table 5. Electrical characteristics (adjustable version)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		2		5.5	V
V_{ADJ}	Reference voltage accuracy	T_J = 25 °C	0.784	0.8	0.816	V
		-40 °C < T_J < 125 °C	-3		3	%
I_{ADJ}	Adjustable pin current			1		nA
$\Delta V_{ADJ\%}/\Delta V_{IN}$	Static line regulation	2 V< V_{IN} < 5.5 V		0.005		%/V
		-40 °C < T_J < 125 °C			0.05	
$\Delta V_{ADJ\%}/\Delta I_{OUT}$	Static load regulation	1 mA < I_{OUT} < 0.2 A; T_J = 25 °C		0.0015		%/mA
		-40 °C < T_J < 125 °C			0.005	
V_{DROP}	Dropout voltage (1)	V_{OUT} = 2.0 V; I_{OUT} = 0.2 A		200		mV
		V_{OUT} = 2.0 V; I_{OUT} = 20 mA		20		mV
eN	Output noise voltage	f = 10 Hz to 100 kHz		135		$\mu V_{RMS}/V_{OUT}$
SVR	Supply voltage rejection	V_{OUT} = 2.5 V; V_{RIPPLE} = 0.2 Vpp I_{OUT} = 10 mA; f = 100 Hz		60		dB
		V_{OUT} = 2.5 V; V_{RIPPLE} = 0.2 Vpp I_{OUT} = 10 mA ; f = 1 kHz		40		
		V_{OUT} = 2.5 V; V_{RIPPLE} = 0.2 Vpp I_{OUT} = 10 mA; f = 10 kHz		60		
I_q	Quiescent current	I_{OUT} = 0 A		300		nA
		I_{OUT} = 0 A; -40 °C < T_J < 125 °C			1000	
		I_{OUT} = 0.2 A		80		µA
		I_{OUT} = 0.2 A; -40 °C < T_J < 125 °C			150	
	Shutdown current	V_{EN} = 0 V, V_{IN} = 2 V		0.005	0.05	µA
I_{SC}	Short-circuit current	V_{OUT} = 0 V		380		mA
R_{LOW} (2)	Output discharge resistance	V_{EN} = 0 V		100		Ω
V_{EN}	Enable input logic low	-40 °C < T_J < 125 °C			0.4	V
	Enable input logic high		1.2			
I_{EN}	Enable pin input current	V_{EN} = V_{IN}; 1.25 < V_{IN} < 5.5 V		1		nA
T_{SHDN}	Thermal shutdown (3)	I_{OUT} > 1 mA		160		°C
	Hysteresis			20		

1. *Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.*
2. *On specific version only.*
3. *The thermal protection is not active when the load current is lower than 1 mA.*

6 Typical characteristics

The following plots are referred to the typical application circuit and, unless otherwise noted, at T_A = 25 °C.

Figure 6. Output voltage vs. temperature

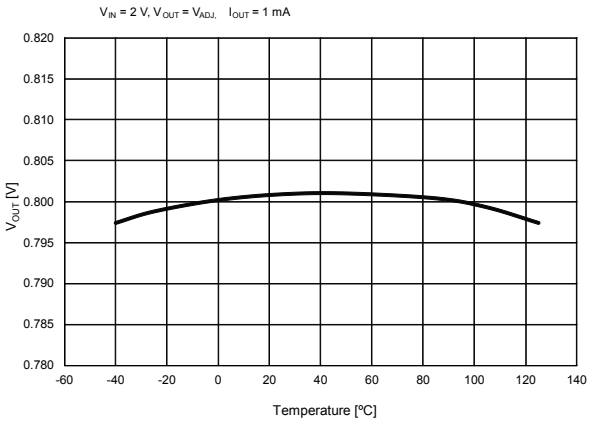


Figure 7. Output voltage vs. temperature

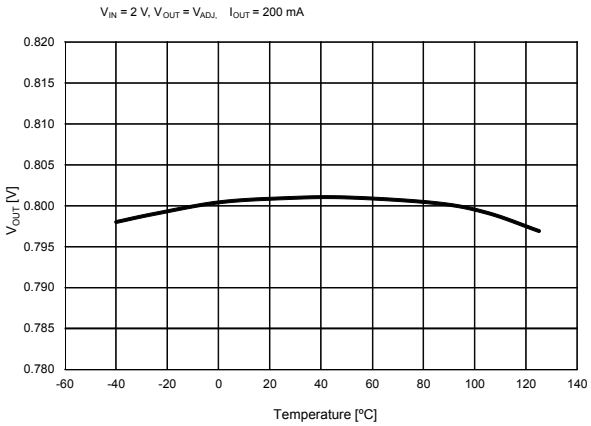


Figure 8. Output voltage vs. temperature

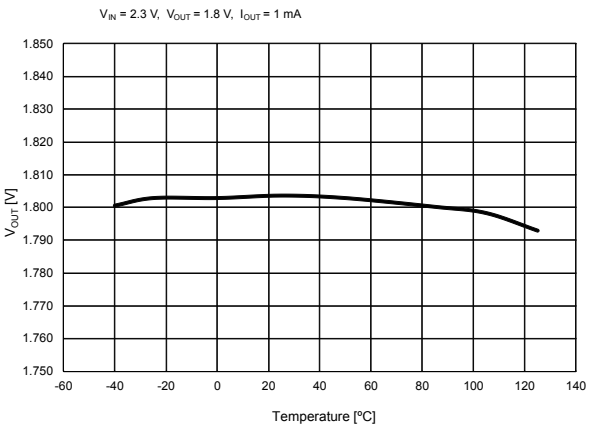


Figure 9. Output voltage vs. temperature

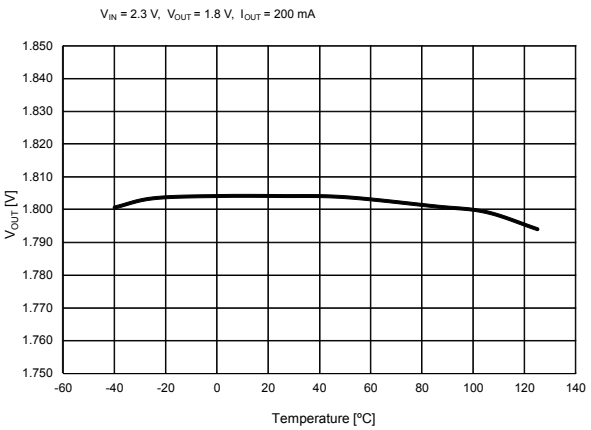


Figure 10. Line regulation vs. temperature

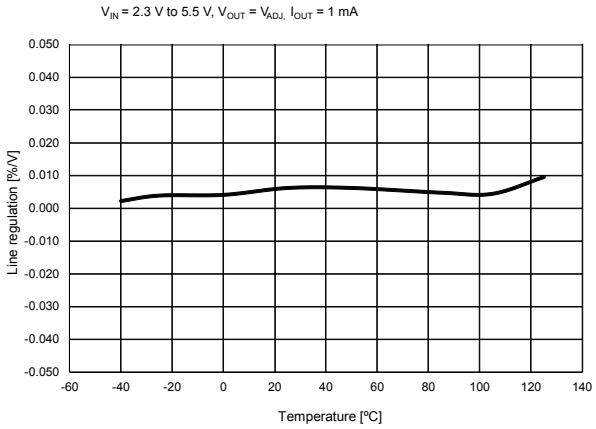


Figure 11. Load regulation vs. temperature

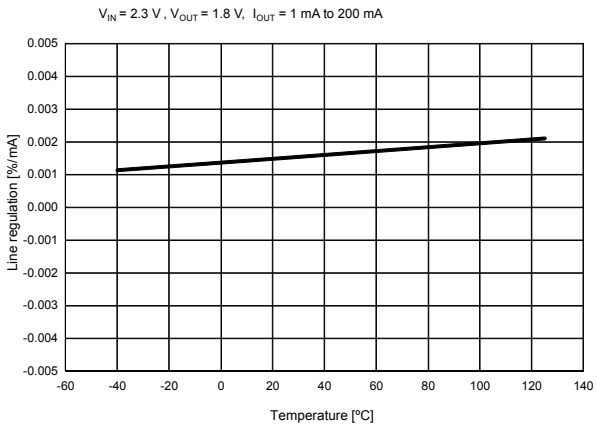


Figure 12. Short-circuit current vs. temp.

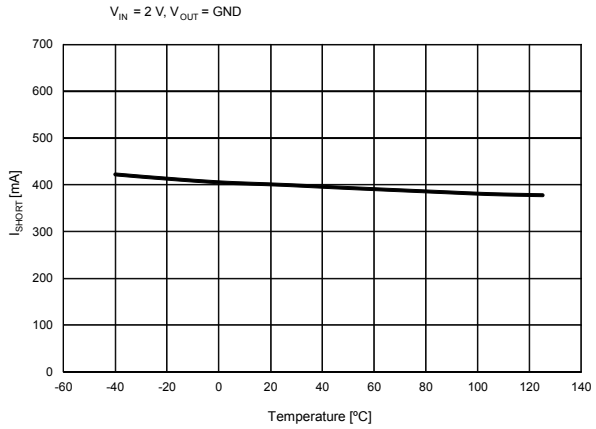


Figure 13. Quiescent current vs. temperature

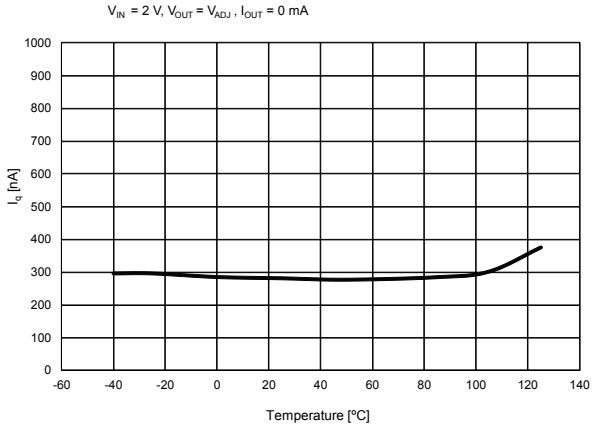


Figure 14. Quiescent current vs. temperature

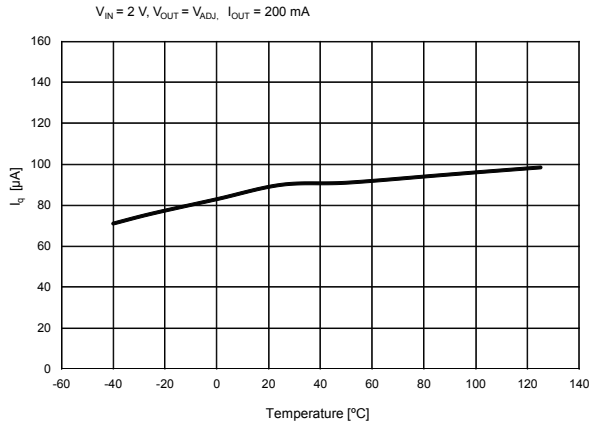


Figure 15. Shutdown current vs. temperature

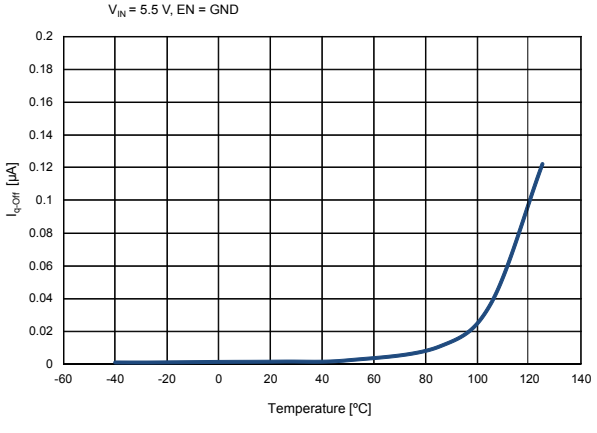


Figure 16. Quiescent current vs. load current

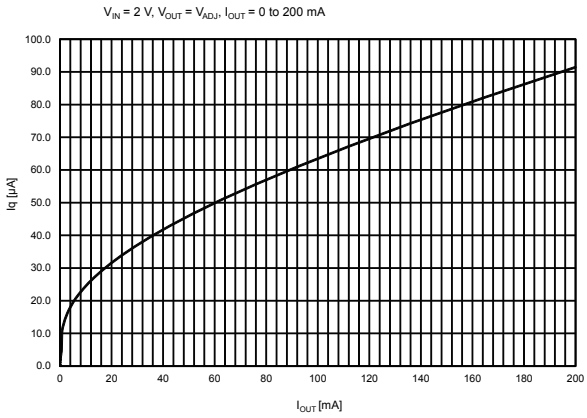


Figure 17. Quiescent current vs. load current (magnification)

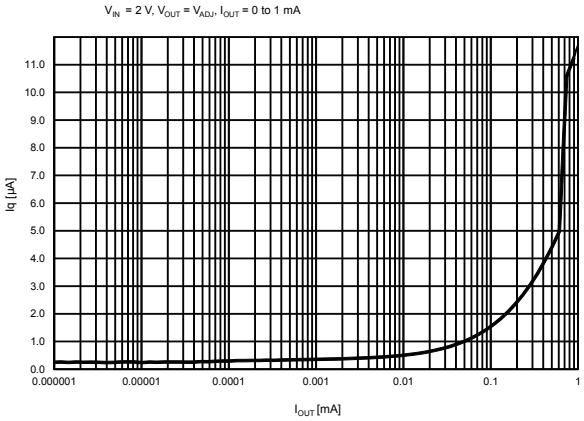


Figure 18. Quiescent current vs. input voltage

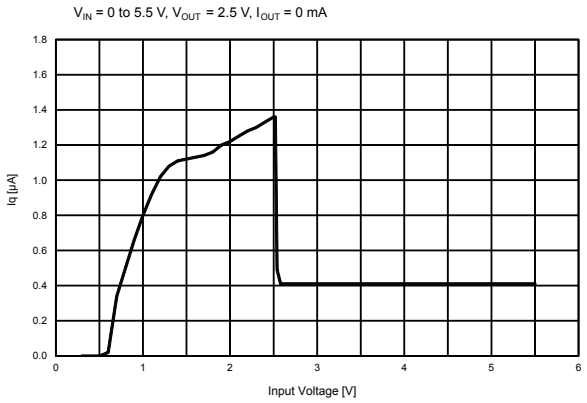


Figure 19. Output voltage vs. input voltage

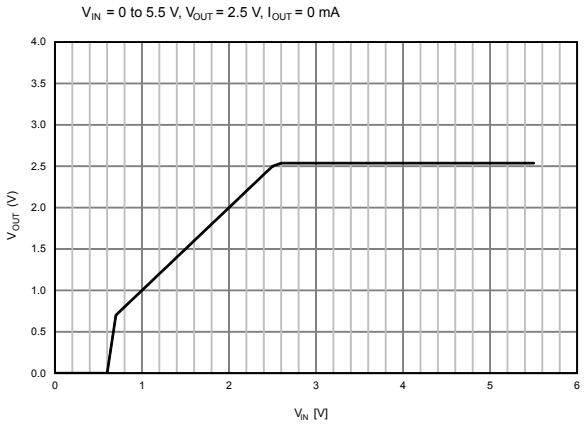


Figure 20. Enable pin current vs. temperature

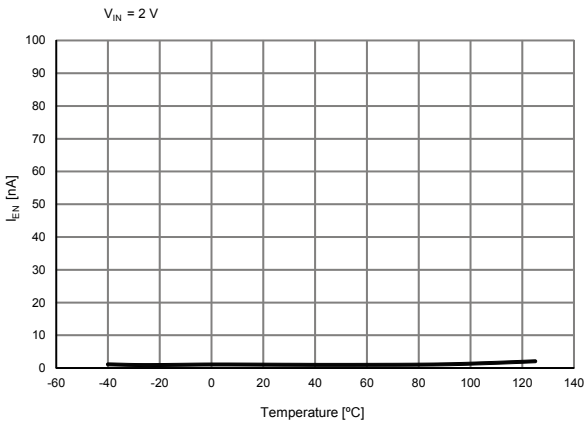


Figure 21. Dropout voltage vs. temperature

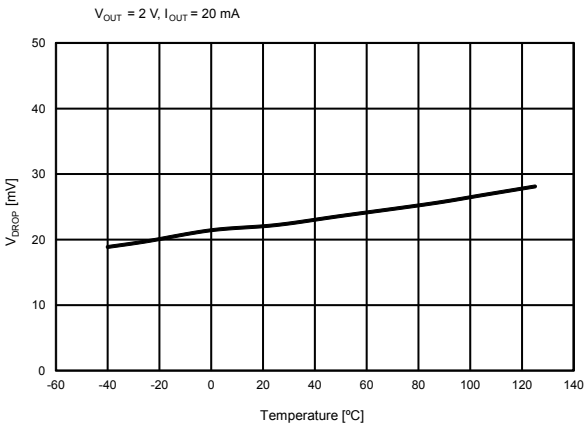


Figure 22. Dropout voltage vs. temperature

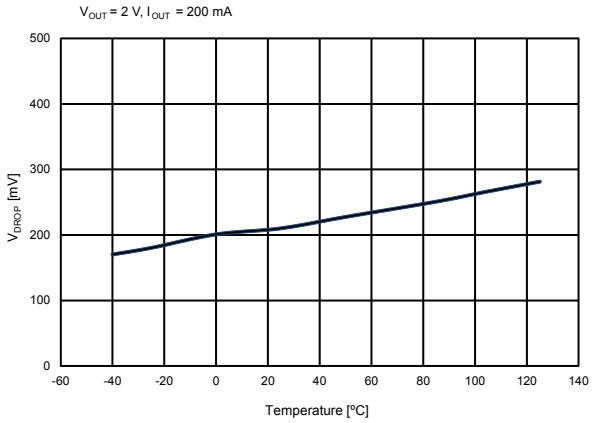


Figure 23. Enable threshold vs. temperature

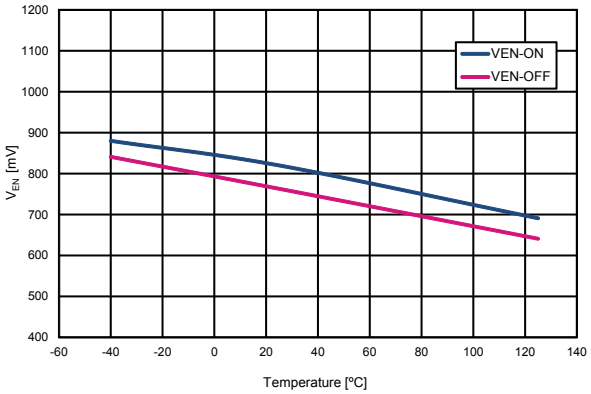


Figure 24. PSRR vs. frequency

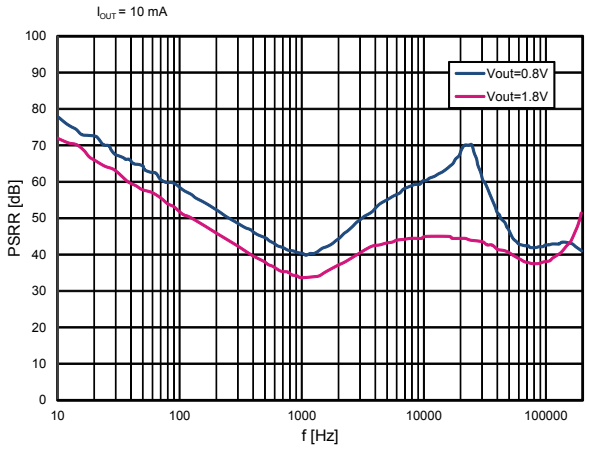


Figure 25. Line transient (t_{rise} = 5 µs)

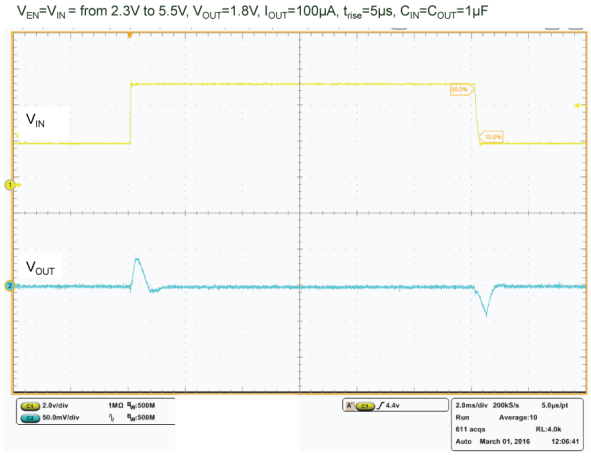


Figure 26. Line transient (t_{rise} = 1 µs)

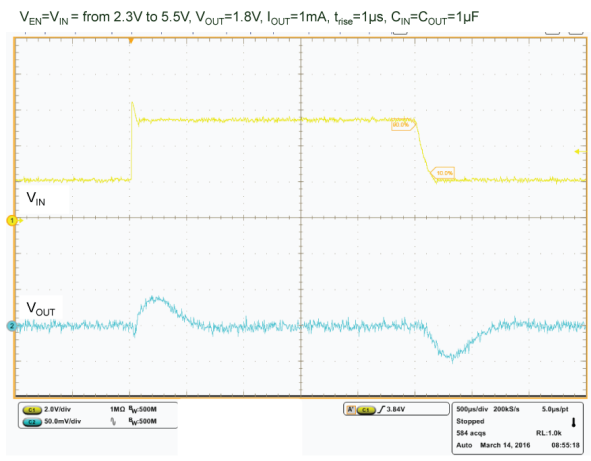


Figure 27. Line transient

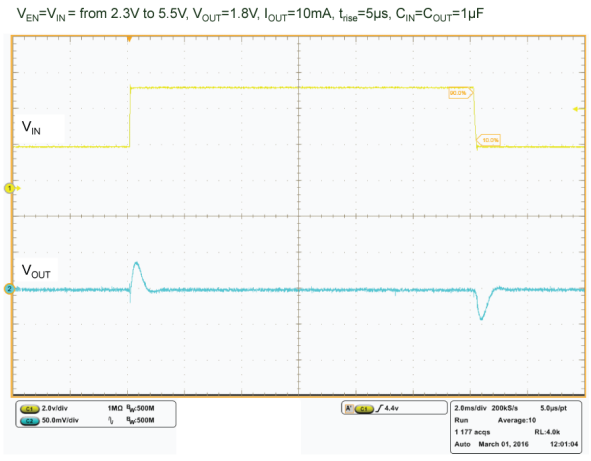


Figure 28. Load transient

V_{EN}= V_{IN}=2.3V, I_{OUT}=from 0mA to 10mA, V_{OUT}=1.8V, t_{rise}=5µs, C_{IN}=C_{OUT}=1µF

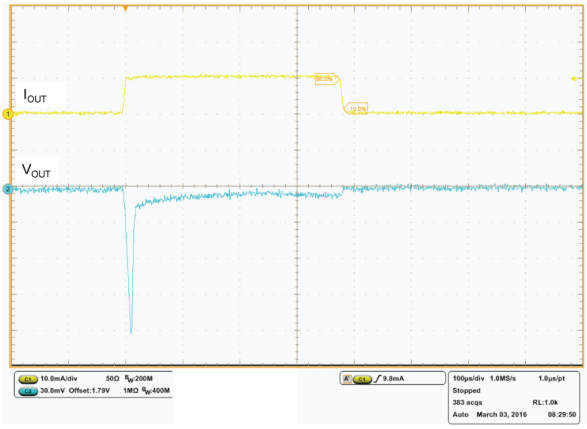


Figure 29. Load transient (t_{rise} = 5 µs)

V_{EN}= V_{IN}=2V, I_{OUT}=from 0mA to 10mA, V_{OUT}=V_{ADJ}, t_{rise}=5µs, C_{IN}=C_{OUT}=1µF

Figure 30. Load transient (V_{OUT} = 1.8 V)

V_{EN}= V_{IN}=2.3V, I_{OUT}=from 1mA to 200mA, V_{OUT}=1.8V, t_{rise}=5µs, C_{IN}=C_{OUT}=1µF

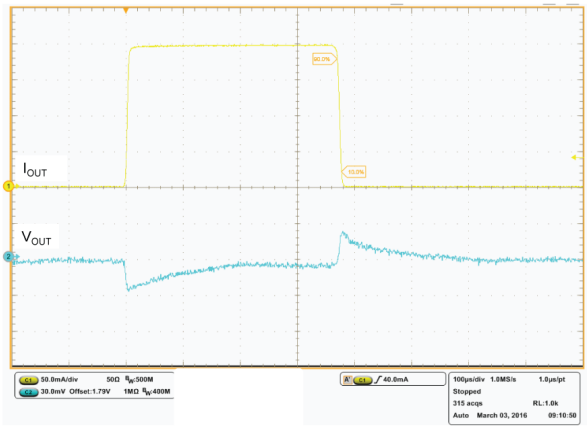


Figure 31. Load transient (V_{OUT} = V_{ADJ})

V_{EN}= V_{IN}=2V, I_{OUT}=from 1mA to 200mA, V_{OUT}=V_{ADJ}, t_{rise}=5µs, C_{IN}=C_{OUT}=1µF

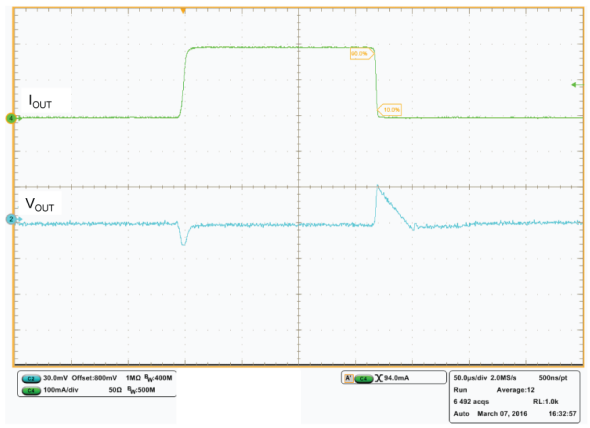


Figure 32. Startup transient

V_{EN}=V_{IN} = from 0V to 2.3V, V_{OUT}=1.8V, I_{OUT}=200mA, t_{rise}=10µs, C_{IN}=C_{OUT}=1µF

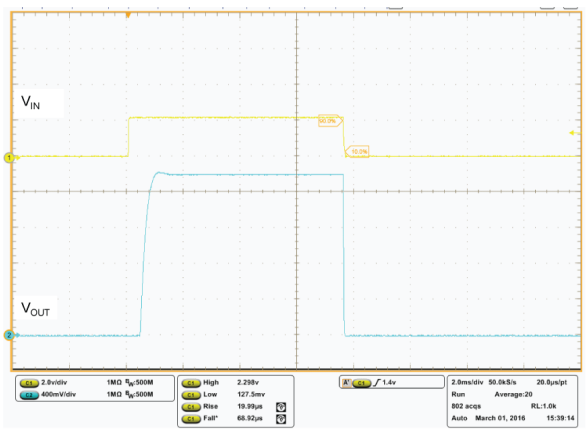
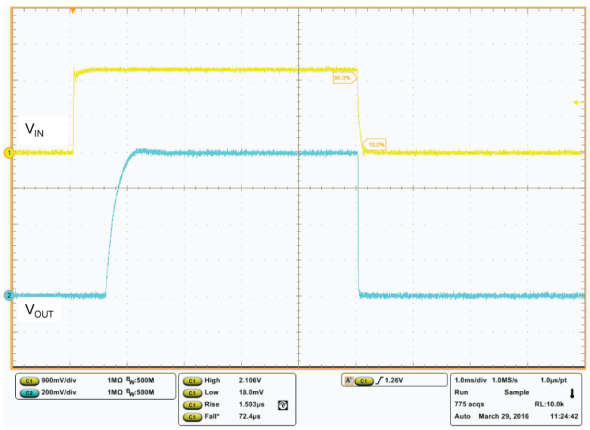


Figure 33. Startup transient (t_{rise} = 10 µs)

V_{IN}=V_{EN}=from 0V to 2V, V_{OUT}=V_{ADJ}, I_{OUT}=200mA, t_{rise}=1µs, C_{IN}=C_{OUT}=1µF



7 Application information

7.1 External capacitors

The STLQ020 voltage regulator requires external low ESR capacitors to assure the control loop stability. These capacitors must be selected to meet the requirements of minimum capacitance and equivalent series resistance defined in the following chapters. Input and output capacitors should be located as close as possible to the relevant pins.

Input capacitor

An input capacitor, with a minimum value of 1 µF, must be located as close as possible to the input pin of the device and returned to a clean analog ground. A good quality, low-ESR ceramic capacitor is suggested. It helps to ensure stability of the control loop, reduces the effects of inductive sources and improves ripple rejection. Capacitance higher than 1 µF can be chosen in case of fast load transients in application.

Output capacitor

STLQ020 requires a low-ESR capacitor connected on its output, to keep the control loop stable and reduce the risk of ringing and oscillations. The control loop is designed to be stable with any good quality ceramic capacitor (such as X5R/X7R types) with a minimum value of 1 µF and equivalent series resistance in the [3 – 500 mΩ] range. It is important to highlight that the output capacitor must maintain its capacitance and ESR in the stable region over the full operating temperature, load and input voltage ranges, to assure stability. Therefore, capacitance and ESR variations must be taken into account in the design phase to ensure the device works in the expected stability region. There is no maximum limit to the output capacitance, provided that the above conditions are respected.

7.2 Output voltage adjustment (adjustable version)

In the adjustable version, available on the DFN6-2x2 and SOT323-5L packages, the output voltage can be adjusted to any voltage, starting from 0.8 V (V_{ADJ}) up to the input voltage minus the voltage drop (V_{DROP}) across the internal power pass element, by connecting a resistor divider between the ADJ pin and the output, allowing the remote voltage sensing.

The resistor divider should be selected using the following equation:

Equation 1

$V_{OUT} = V_{ADJ} (1 + R_1 / R_2)$

with V_{ADJ} = 0.8 V (typ.) and $V_{OUT} < V_{IN}$-$V_{DROP(MAX)}$

For best accuracy and stability the resistor divider should be designed in order to allow that a current of at least 500 nA flows across it. The current flowing into the ADJ pin is typically less than 1 nA, therefore causing negligible change in final the output voltage.

7.3 Enable pin operation

This is a logic control pin, CMOS level-compatible, which can be used to turn On/Off the regulator.It is active high, so when it is pulled down, the device enters the shutdown mode, drastically reducing the current consumption, to less just few nA.

Since it is not internally pulled-up, when the enable feature is not used, this pin must not be left floating. It can be tied to V_{IN} to keep the regulator output in ON state all the time.

To assure reliable operation, the signal source used to drive the EN pin, must be able to swing above and below the specified thresholds listed in the electrical characteristics table (V_{EN}).

7.4 Power dissipation

A proper PCB design is recommended, to ensure that the device internal junction temperature is kept below 125°C, in all the operating condition.

Depending on the package option, the thermal energy generated by the device flows from the die surface to the PCB copper area through the package leads, solder bumps and/or exposed pad.

The PCB copper area acts as a heat sink. The footprint copper pads should be as wider as possible to spread and dissipate the heat to the surrounding environment. Thermal vias to the inner or backside copper layers improve the overall thermal performance of the device.

The power dissipation of the LDO depends on the input voltage, output voltage and output current, and is given by:

Equation 2

$P_D = (V_{IN} - V_{OUT}) I_{OUT}$

The junction temperature of the device is:

Equation 3

$T_{J\_MAX} = T_A + R_{thJA} \times P_D$

where: T_{J_MAX} is the maximum junction of the die, 125 °C; T_A is the ambient temperature; R_{thJA} is the thermal resistance junction-to-ambient.

With the above equation it is possible to calculate the maximum allowable power dissipation, therefore the maximum load current for a certain voltage drop. Appropriate de-rating of the operating condition can be applied accordingly.

7.5 Protection features

Current limit

The STLQ020 embeds a constant-current limit circuit, which acts in case of overload or short-circuit on the output, clamping the load current to a safe value (typ. 380 mA).

Normal operation is restored if the overload disappears, but prolonged operation in current limit may lead to high power dissipation inside the LDO and subsequently to thermal shutdown.

Thermal protection

An internal thermal feedback loop disables the output voltage if the die temperature reaches approximately 160 °C. This feature protects the device from excessive temperature that could lead to permanent damage to the LDO.

Once the thermal protection is triggered and the device is shut down, normal operation is automatically recovered if the die temperature falls below 140 °C (thermal protection hysteresis of 20 °C typically)

Important note: to keep the device power consumption below 500 nA in low load/no load condition, the internal thermal protection is kept disabled for load current below 1 mA.

Current and thermal limit protections are designed to protect the LDO from excessive power dissipation and not intended to replace a proper thermal and electrical design of the application.

Continuous operation above the maximum ratings may lead to permanent damage to the device.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 SOT323-5L package information

Figure 34. SOT323-5L package outline

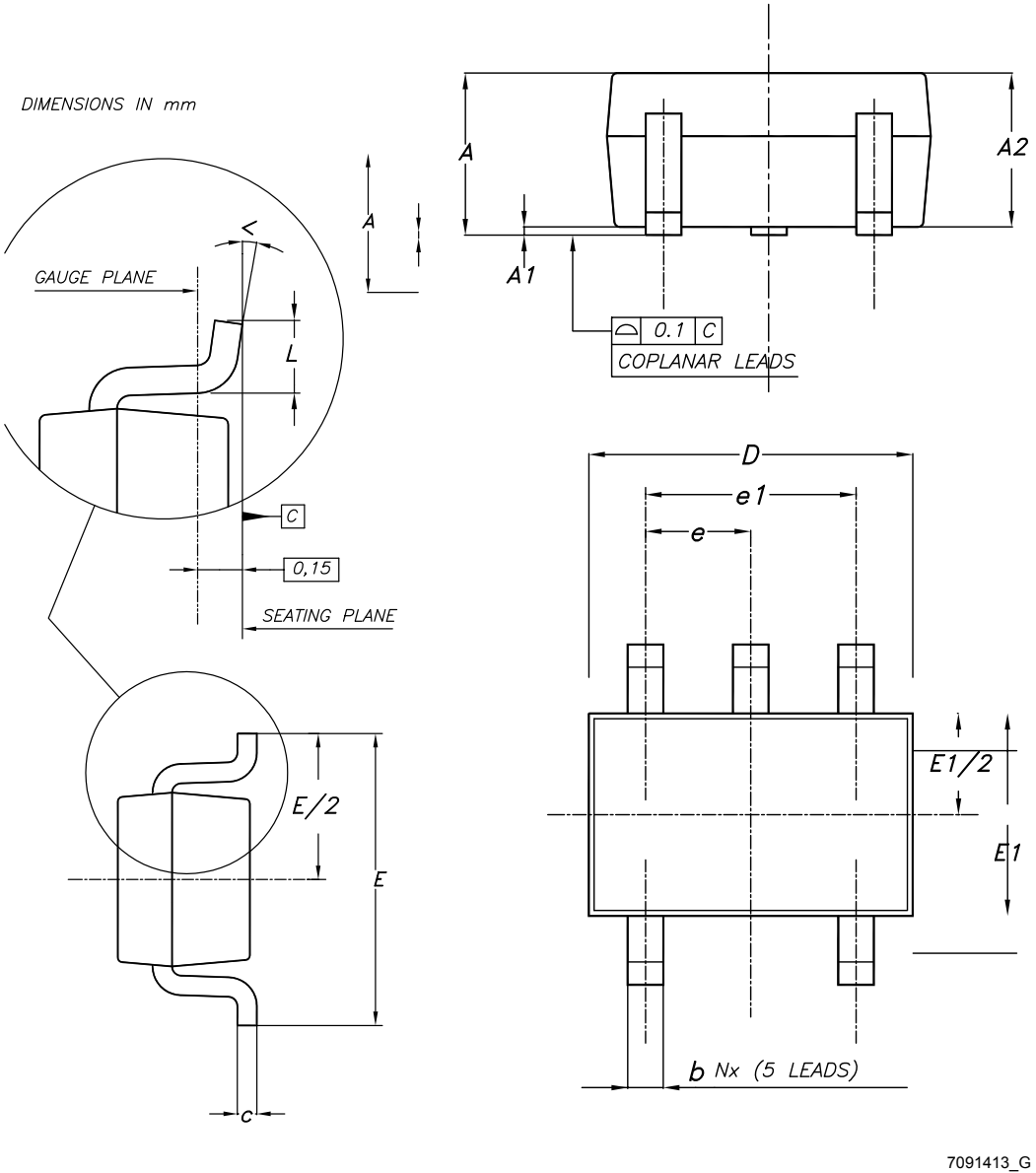
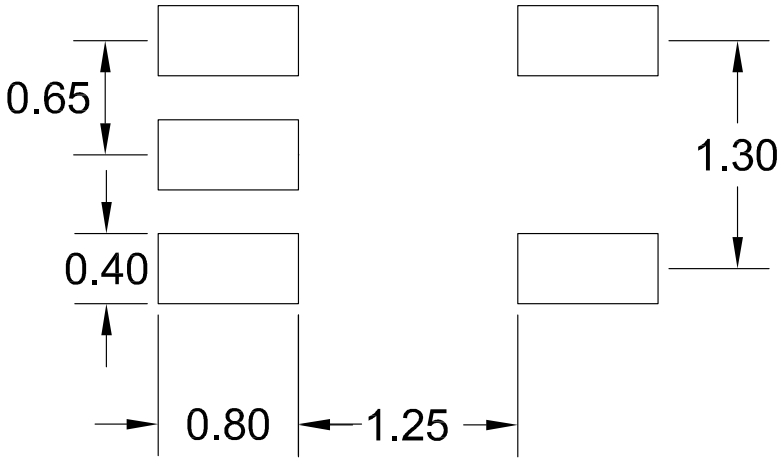


Table 6. **SOT323-5L package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.10
A1	0		0.10
A2	0.80	0.90	1
b	0.15		0.30
c	0.10		0.22
D	1.80	2	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e		0.65	
e1		1.30	
L	0.26	0.36	0.46
<	0°		8°

Figure 35. **SOT323-5L recommended footprint**



8.1.1 SOT323-5L tape and reel information

Figure 36. **SOT323-5L tape outline**

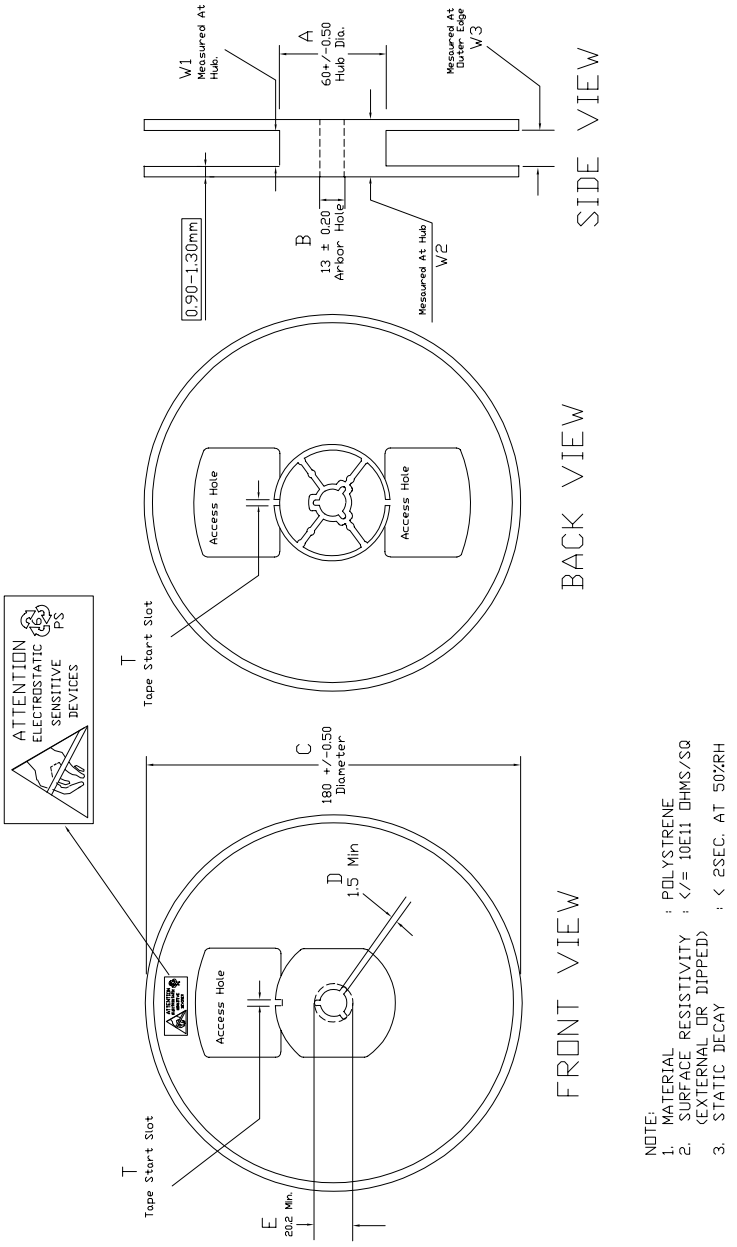
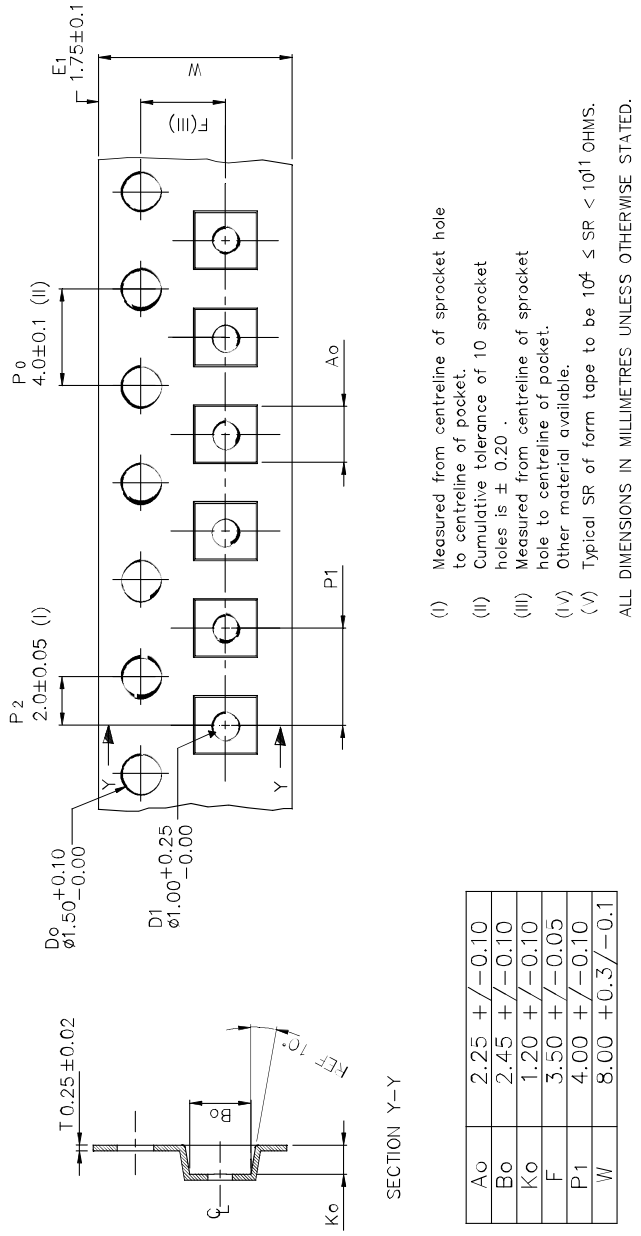


Figure 37. **SOT323-5L reel outline**



Ao	2.25 +/−0.10
Bo	2.45 +/−0.10
Ko	1.20 +/−0.10
F	3.50 +/−0.05
P1	4.00 +/−0.10
W	8.00 +0.3/−0.1

8.2 Flip-Chip4 package information

Figure 38. **Flip-Chip4 package outline**

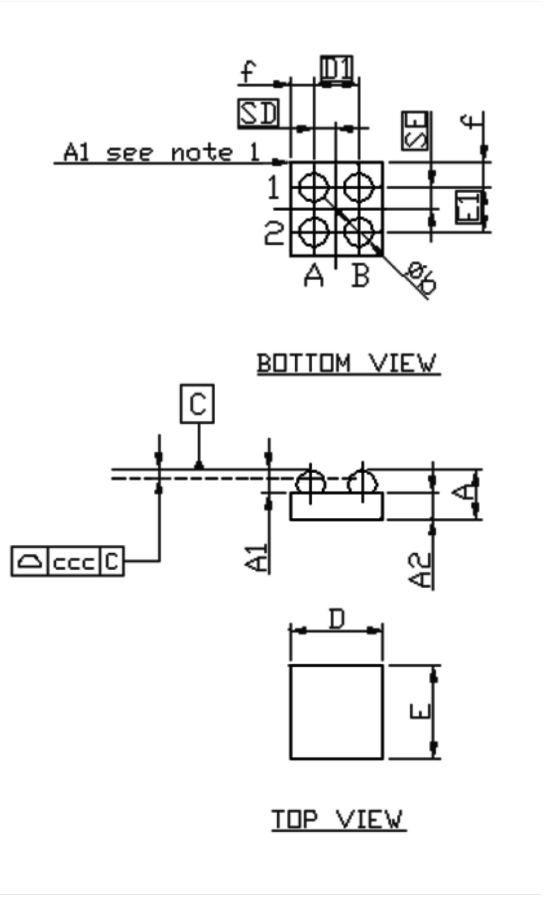
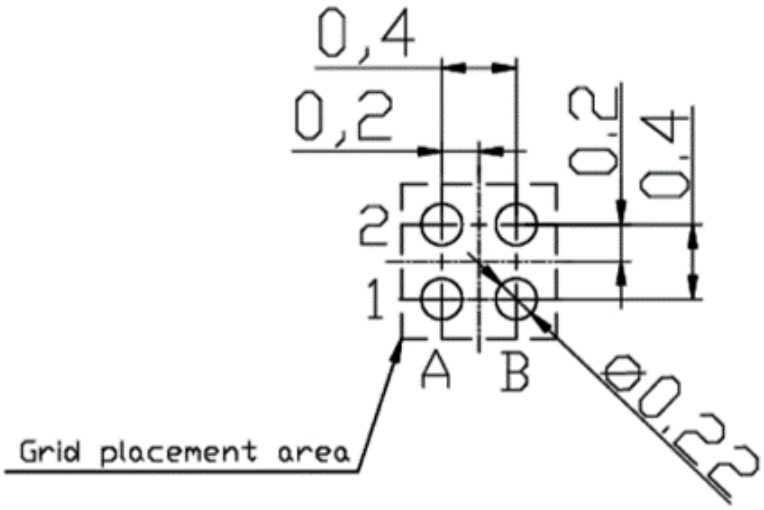


Table 7. **Flip-Chip4 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.51	0.56	0.61
A1	0.17	0.20	0.23
A2	0.34	0.36	0.38
b	0.23	0.26	0.29
D	0.743	0.773	0.803
D1		0.40	
E	0.743	0.773	0.803
E1		0.40	
SD		0.20	
SE		0.20	
f		0.187	
ccc		0.075	

Figure 39. **Flip-Chip4 recommended footprint**



8.2.1 Flip-Chip4 reel information

Figure 40. **Flip-Chip4 reel outline**

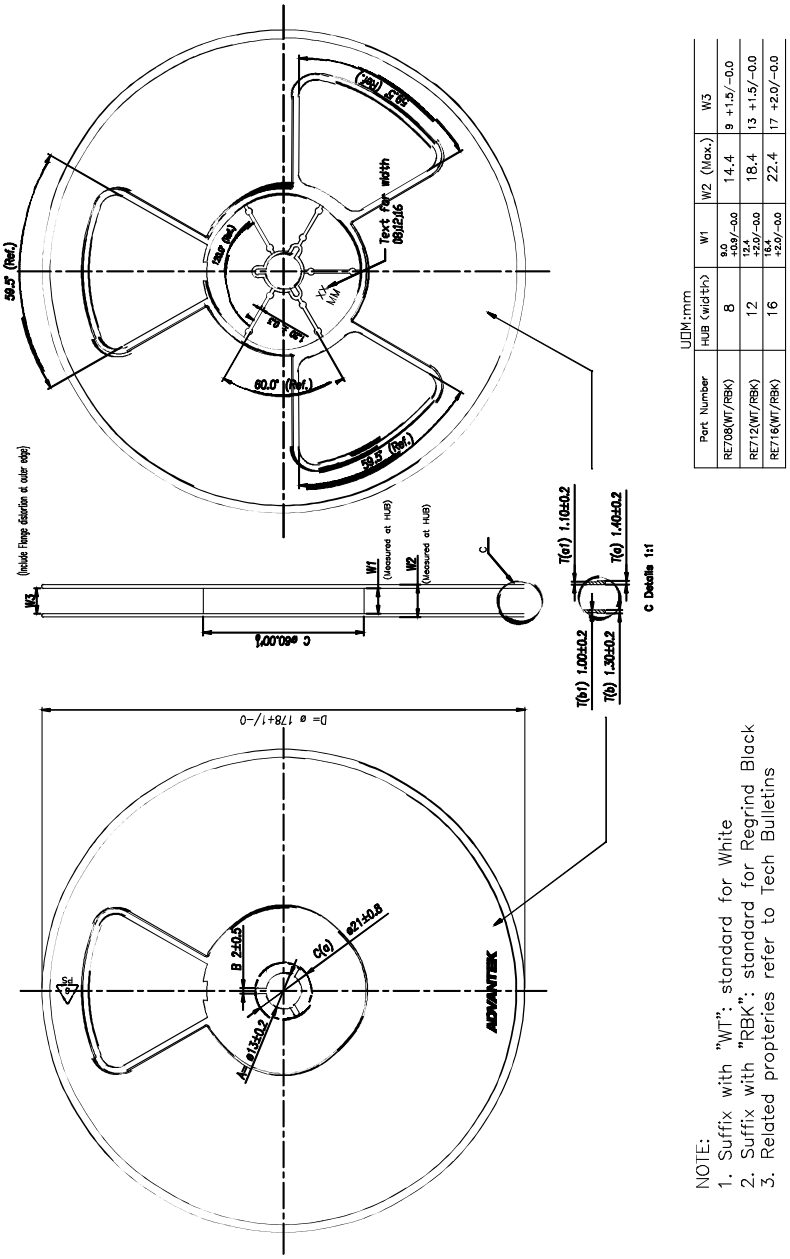
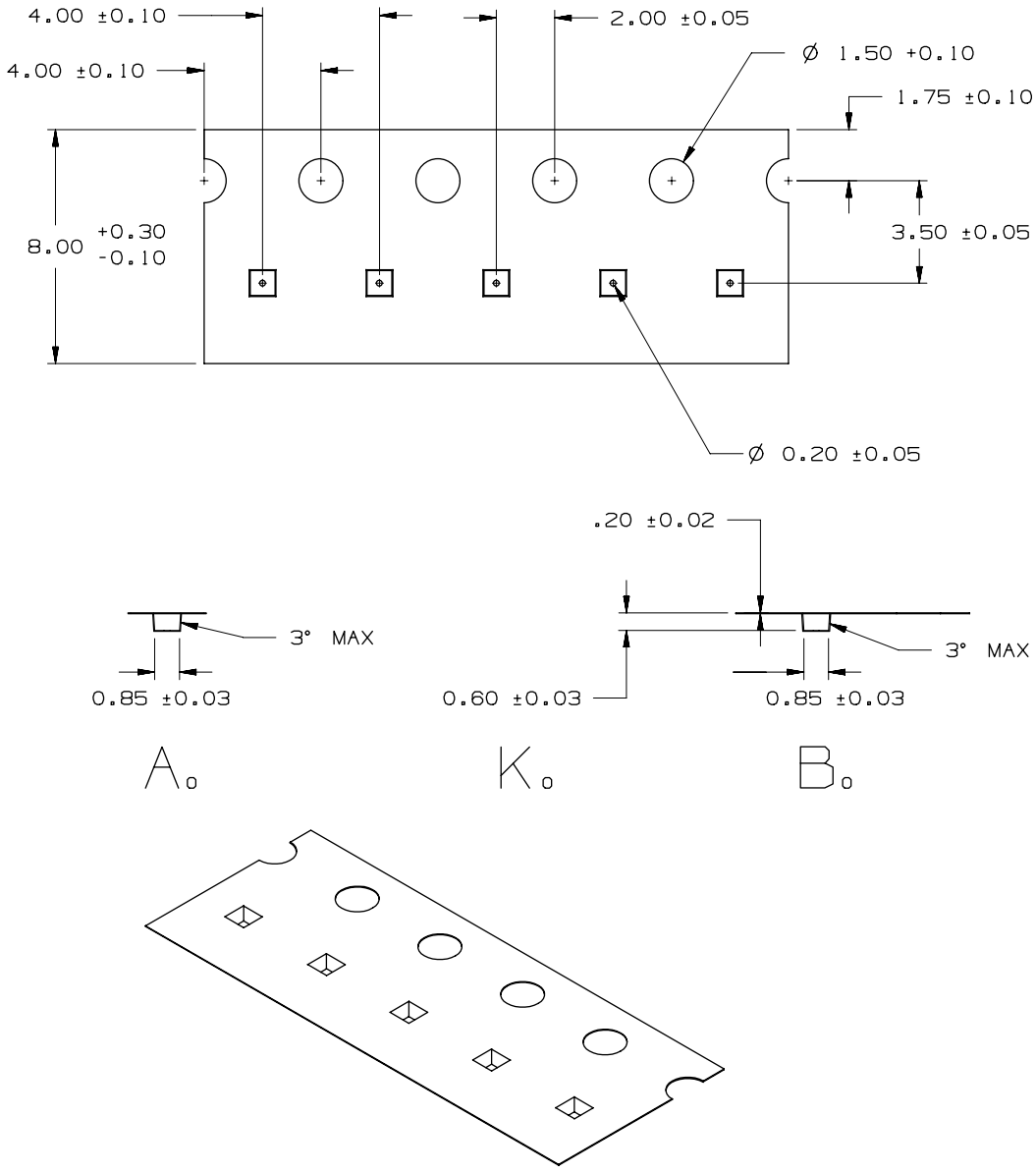
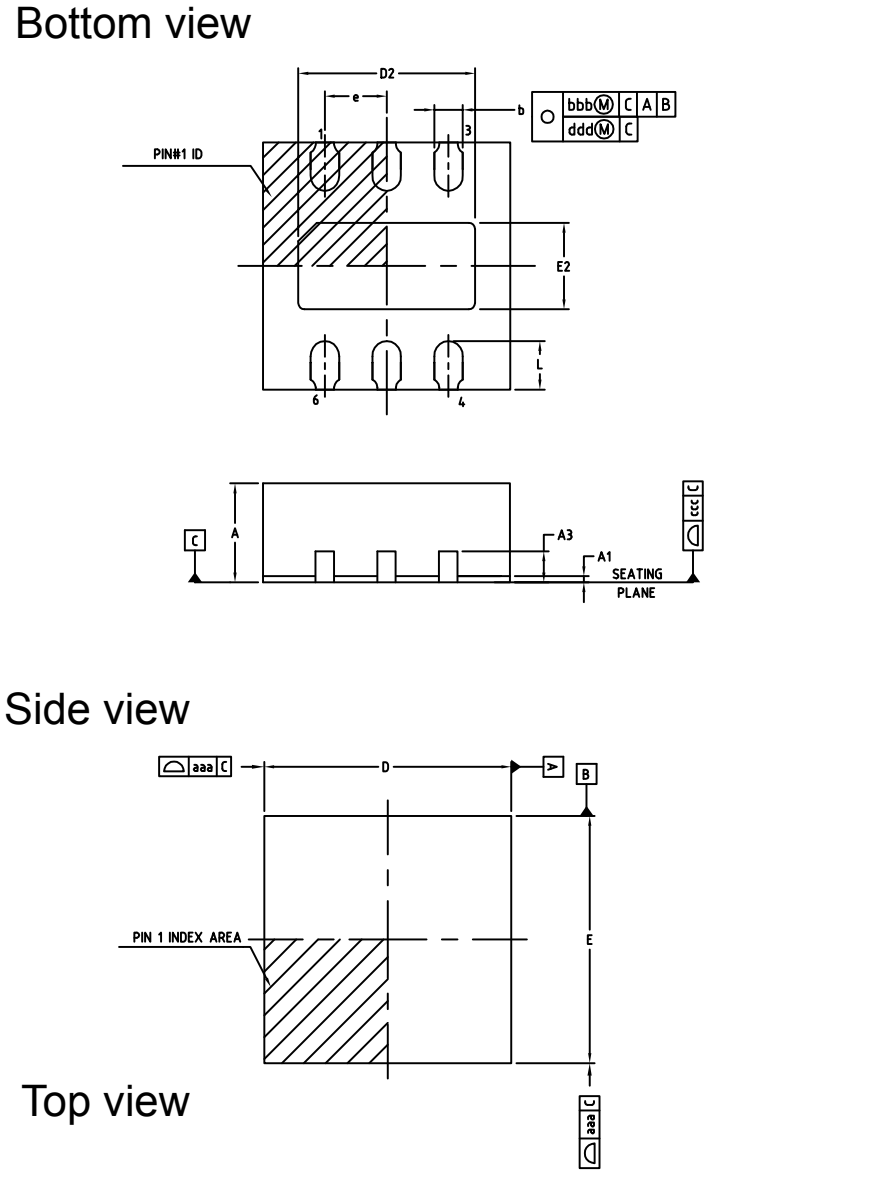


Figure 41. **Flip-Chip4 tape outline**



8.3 DFN6 2x2 package information

Figure 42. **DFN6 2x2 package outline**

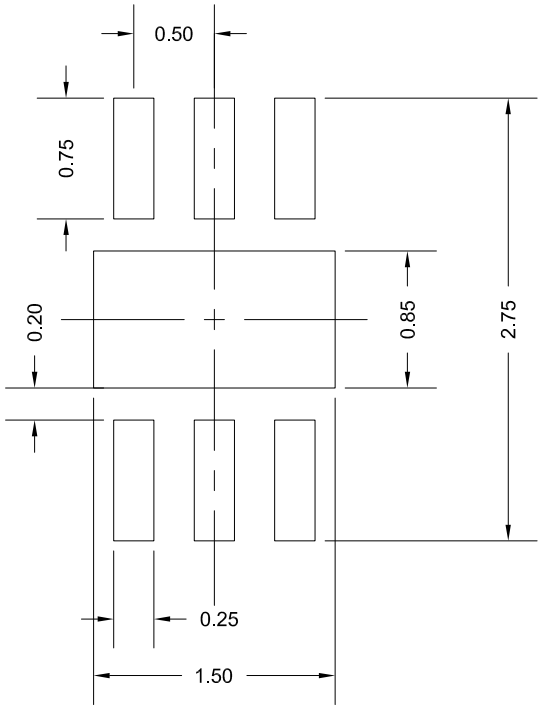


DM00205706

Table 8. **DFN6 2x2 package mechanical data**

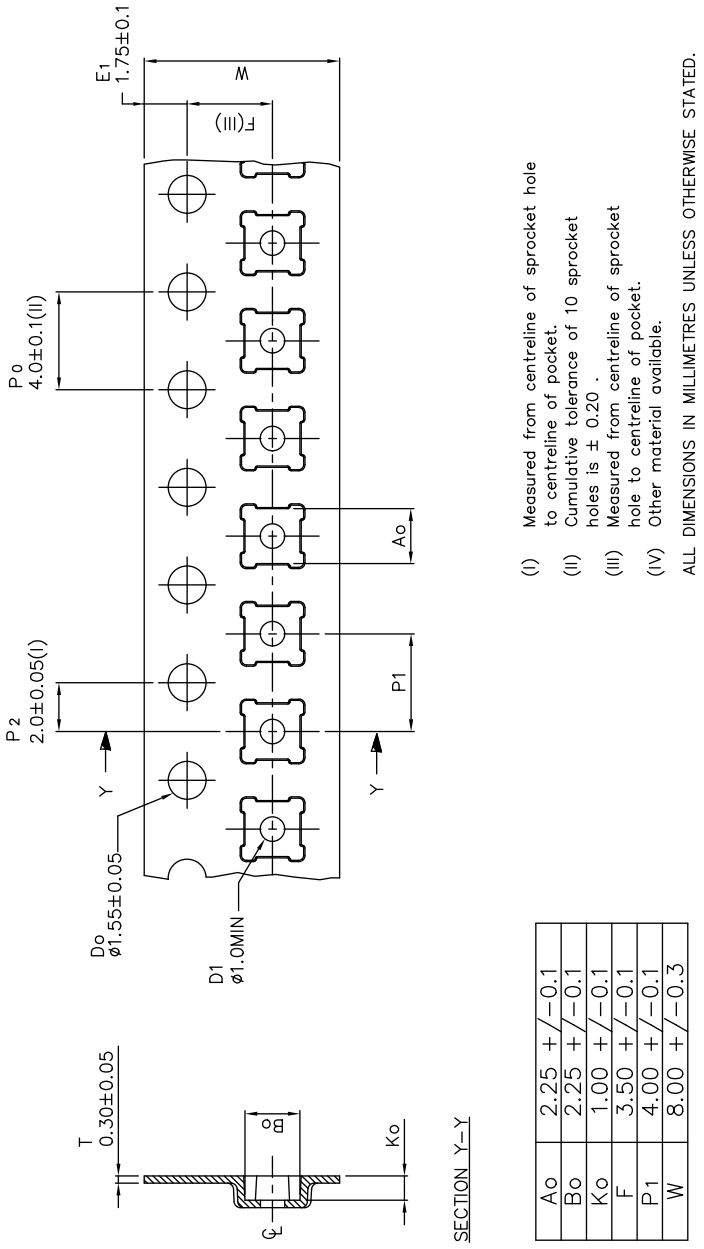
Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00	0.02	0.05
A3	0.10	0.20	0.30
b	0.18	0.23	0.28
D	1.90	2.00	2.10
D2	1.33	1.43	1.53
E2	0.68	0.78	0.88
e		0.50	
E	1.90	2.00	2.10
L	0.25	0.35	0.45
N		6	

Figure 43. **DFN6 2x2 recommended footprint**



8.3.1 DFN6 2x2 tape information

Figure 44. **DFN6 2x2 tape outline**



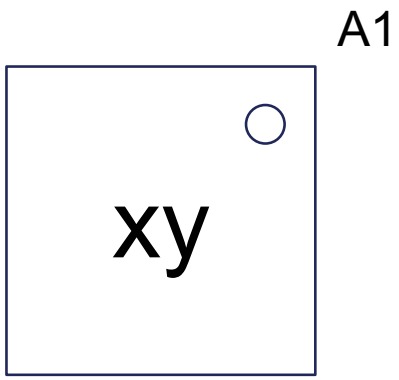
Ao	2.25 +/−0.1
Bo	2.25 +/−0.1
Ko	1.00 +/−0.1
F	3.50 +/−0.1
P1	4.00 +/−0.1
W	8.00 +/−0.3

9 Ordering information

Table 9. **Order codes**

Order code	Package	Output voltage	Marking	Packing
STLQ020C18R	SOT323-5L	1.8 V	QLJ	Tape and reel
STLQ020C22R	SOT323-5L	2.2 V	QLS	Tape and reel
STLQ020C28R	SOT323-5L	2.8 V	QM3	Tape and reel
STLQ020C33R	SOT323-5L	3.3 V	QMB	Tape and reel
STLQ020J18R	Flip-Chip 4	1.8 V	LJ	Tape and reel
STLQ020J25R	Flip-Chip 4	2.5 V	LX	Tape and reel
STLQ020J30R	Flip-Chip 4	3.0 V	M7	Tape and reel
STLQ020J33R	Flip-Chip 4	3.3 V	MB	Tape and reel
STLQ020PU19R	DFN6-2x2	1.9 V	QLL	Tape and reel
STLQ020PU28R	DFN6-2x2	2.8 V	QM3	Tape and reel
STLQ020PU33R	DFN6-2x2	3.3 V	QMB	Tape and reel
STLQ020PUR	DFN6-2x2	ADJ	QAD	Tape and reel

Figure 45. **Marking composition (flip-chip)**



Revision history

Table 10. **Document revision history**

Date	Revision	Changes
27-Mar-2017	1	Initial release.
05-Dec-2017	2	Added: Section 6 Typical characteristics and Section 7 Application information.
07-Jun-2019	3	Added: order codes Table 9. Order codes and reel information Section 8.1.1 SOT323-5L tape and reel information, Section 8.2.1 Flip-Chip4 reel information and Section 8.3.1 DFN6 2x2 tape information
27-Oct-2021	4	Added new order codes Table 9. Order codes

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