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R5433V SERIES

Li-ION/POLYMER 3/4/5CELL PROTECTOR

OVERVIEWS

The R5433V Series are high voltage CMOS-based process protection ICs against over-charge and over-discharge of Li-ion/Li polymer secondary batteries. The R5433V series can detect over-charge voltage, over-discharge voltage of 3, 4 or 5-stacked cells of Li-ion/Li polymer batteries.

The R5433V consists of 10 voltage detectors, a voltage reference unit, an oscillator, a counter, delay circuits, and logic circuits.

When the over-charge voltage is detected, after the IC internally prefixed delay time, the output of C_{OUT} becomes "Hi-Z" or "H" depending on the output type. When the over-discharge voltage current is detected, after the setting delay time by the internal constant current source and an external capacitor, the output of D_{OUT} becomes "Hi-Z" or "H" depending on the output type.

After detecting over-charge, when the cell voltage becomes lower than the over-charge released voltage, the over-charge state is released and the output of C_{out} becomes "L". While after detecting over-discharge, when the cell voltage becomes equal or more than the over-discharge released voltage, then the over-discharge state is released, and the output of D_{OUT} becomes "L".

If breaking wire between the cell and protection board is occurred, the wire breaking is detected, and the output of C_{OUT} becomes "Hi-Z" or "H" depending on the output type. After detecting the breaking wire, the cell and the protection board is connected again, the breaking wire detector is released and the output of C_{OUT} becomes "L".

Further, the testing time shortening function of the protection circuit board is built in the IC. By setting voltage level of DS pin as same as V_{DD}, the output delay time of over-charge can be shortened into approximately 1/100. By setting DS pin at 3.0V, the output delay time of over-discharge can be shortened into approximately 1/100.

The output type of C_{OUT} and D_{OUT} can be designated as CMOS type or N-channel open drain type. The output type of the R5433VxxxAA is N-channel open drain type. The output type of the R5433VxxxAB is CMOS output type. The voltage level of the output of CMOS type is in between V_{SS} and the internal regulator output. Therefore, "H" level is the output of the internal regulator, approximately 3.6V.

FEATURES

- Manufactured with High Voltage Tolerant Process

  Absolute Maximum Rating : 30V
- Low supply current

  Under operation, for 5-cell : Typ. 6.0μA
- High accuracy detector threshold

  Over-charge detector (Topt=25°C) : ....±25mV

  Over-discharge detector   : ±2.5%
- Variety of detector threshold

Over-charge detector threshold ·····························3.6V-4.5V step of 0.005V ($V_{DET1}n$) (n=1,2,3,4,5)

Over-discharge detector threshold·······················2.0V-3.0V step of 0.005V ($V_{DET2}n$) (n=1,2,3,4,5)

Over-charge released voltage ····························$V_{DET1}n$-0.0V to 0.4V step of 0.05V ($V_{REL1}n$) (n=1,2,3,4,5)

Over-discharge released voltage ························$V_{DET2}n$+(0.0V to 0.7V, step of 0.1V) ($V_{REL2}n$) (n=1,2,3,4,5)
  up to 3.4V

- Setting of Output delay time

Over-charge detector Output Delay   ....:1.0s

Over-discharge detector Output Delay ....setting by an external capacitor C_{CT}

- Output Delay Time Shortening Function

  By setting voltage level of DS pin as same as V_{DD}, the output delay time of detect the over-charge voltage can be reduced

  into approximately 1/100.

  By forcing in the range from 2.8V to $V_{DD}/2$-0.5V to DS pin, the delay time for over-charge can be reduced into 4ms and the

  delay time for over-discharge can be reduced into approximately 1/100.

- Cell unbalance operation

If one of the stacked cells becomes over-charge, and another cell becomes over-discharge, the both outputs of C_{OUT} and

D_{OUT} becomes "Hi-Z" or "H" depending on the output type of the R5433V.

- 0V-battery charge.. Acceptable
- Over-charge/discharge released condition ...... By cell voltage
- Output of C_{OUT}/D_{OUT}

N-channel open drain type: Normal state "L" Detected state "Hi-Z"

CMOS output type: Normal state "L" Detected state "H"

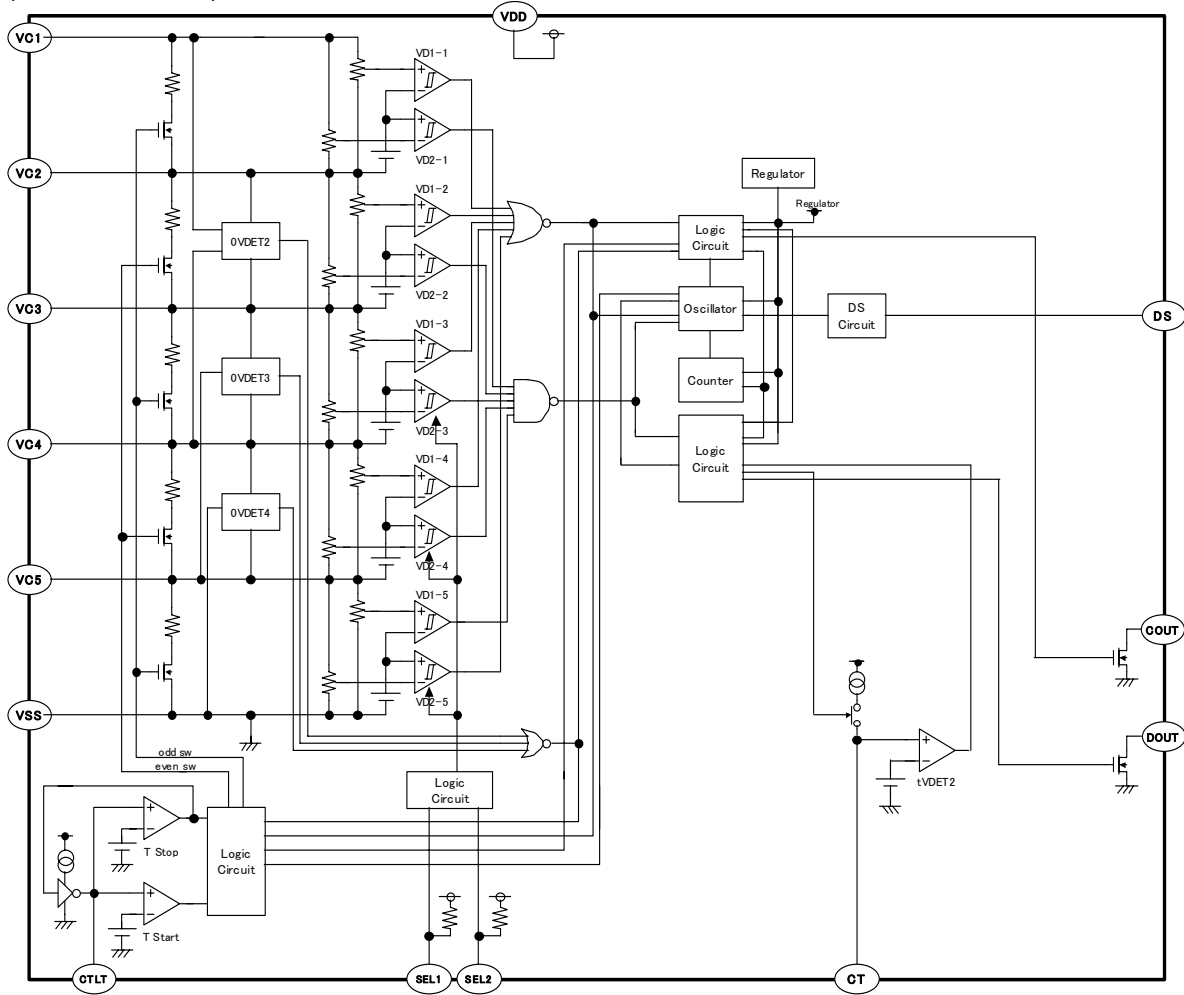CMOS output type: same as 3.6V output regulator CMOS output

- Breaking wire Detector Function

Breaking wire detector function between the protection circuit board and the battery pack
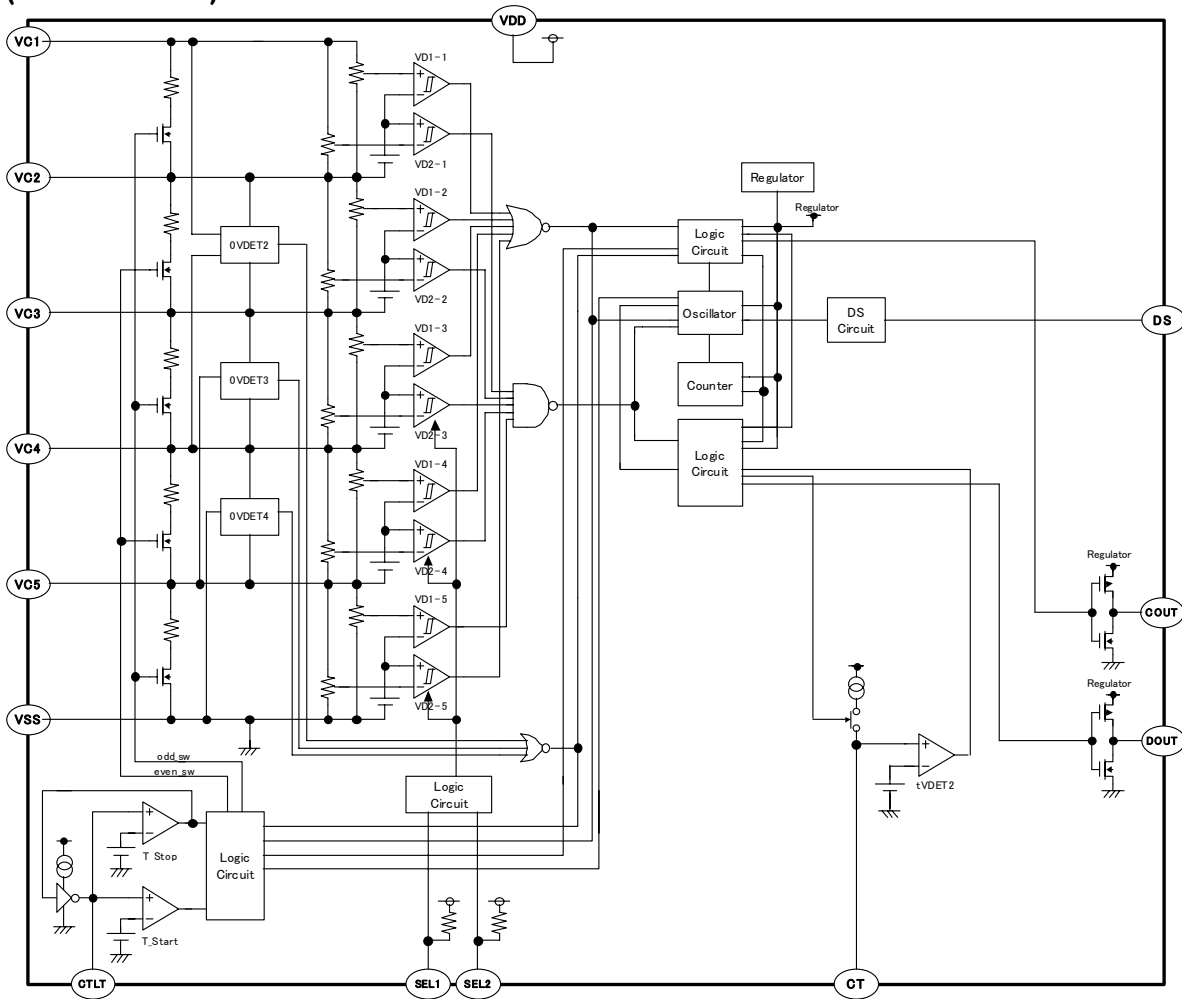
- Small package.. SSOP-16

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BLOCK DIAGRAMS

(R5433VxxxxA)

(R5433VxxxxB)

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SELECTION GUIDE

In the R5433Vxxxx Series, input threshold of over-charge, over-discharge, and output delay time can be designated according to the application.

Part Number is designated as follows:

(ex.)

R5433V 301AA ←Part Number

↑　↑↑↑

a　b c d

Code	Contents
a	Package Type　　V: SSOP-16
b	Serial Number for the R5433 Series designating input threshold for over-charge, over-discharge
c	Designation of Output delay option
d	Designation of version symbols.

*Function Table

Code	Output of C_{OUT}	Output of D_{OUT}	C_{OUT} output logic	D_{OUT} output logic
R5433VxxxAA	N-channel open drain	N-channel open drain	Normal state: "L" Detected state: "Hi-Z"	Normal state: "L" Detected state: "Hi-Z"
R5433VxxxAB	CMOS	CMOS	Normal state: "L" Detected state: "H"	Normal state: "L" Detected state: "H"

Delay Time table

Code	Over-charge detector output delay time tV_{DET1} (s)*1	Over-discharge detector output delay time tV_{DET2} (ms)*2
R5433VxxxAA	1.0	$3.64 \times C_{CT}$(nF)
R5433VxxxAB	1.0	$3.64 \times C_{CT}$(nF)

*1: Capacitor for CT pin: C_{CT}

*2: Refer to the item of "OPERATION"

Product name list

Code	Over charge detector threshold $V_{DET1n}(V)$ *1	Over charge Released voltage $V_{REL1n}(V)$ *1	Over discharge detector threshold $V_{DET2n}(V)$ *1	Over discharge Released voltage $V_{REL2n}(V)$ *1
R5433V301AA	4.220	4.150	2.300	2.300
R5433V301AB	4.220	4.150	2.300	2.300
R5433V302AB	4.220	4.150	2.700	2.700
R5433V401AA	4.250	4.050	2.300	3.000
R5433V401AB	4.250	4.050	2.300	3.000
R5433V402AA	4.220	4.150	2.300	3.000
R5433V402AB	4.220	4.150	2.300	3.000
R5433V403AA	4.220	4.150	2.500	3.200
R5433V403AB	4.220	4.150	2.500	3.200

*1: n=1,2,3,4,5

PIN CONFIGURATIONS

SSOP-16

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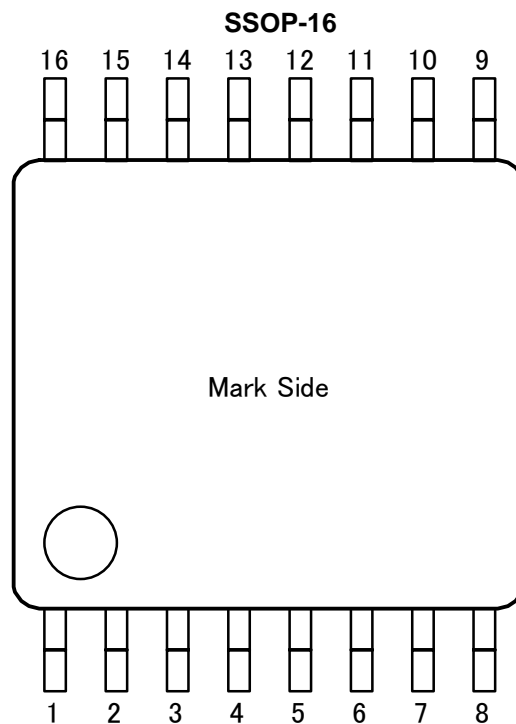
PIN DESCRIPTION

Pin No.	Symbol	Description
1	D_{OUT}	Output pin of over-discharge detection
2	C_{OUT}	Output pin of over-charge detection
3	SEL2	Selector pin for 3-cell/4-cell/5-cell protection
4	SEL1	Selector pin for 3-cell/4-cell/5-cell protection
5	DS	Output delay time shortening pin
6	CT	Capacitor setting pin for over-discharge delay time
7	CTLT	Capacitor setting pin for time interval of breaking wire detector function
8	V_{SS}	V_{SS} pin. Ground pin for the IC
9	NC	No Connection
10	NC	No Connection
11	V_{C5}	Positive terminal pin for Cell-5
12	V_{C4}	Positive terminal Pin for Cell-4
13	V_{C3}	Positive terminal Pin for Cell-3
14	V_{C2}	Positive terminal pin for Cell-2
15	V_{C1}	Positive terminal pin for Cell-1
16	V_{DD}	V_{DD} Pin

ABSOLUTE MAXIMUM RATINGS

Topt=25°C, V_{SS}=0V

Symbol	Item	Ratings	Unit
V_{DD}	Supply voltage	-0.3 to 30	V
V_{C1} V_{C2} V_{C3} V_{C4} V_{C5} V_{SEL1} V_{SEL2} V_{DS} V_{CTLT} V_{CT}	Input Voltage Positive input pin voltage for Cell-1 Positive input pin voltage for Cell-2 Positive input pin voltage for Cell-3 Positive input pin voltage for Cell-4 Positive input pin voltage for Cell-5 SEL1 pin voltage SEL2 pin voltage DS pin voltage CTLT pin voltage CT pin voltage	 V_{C2} –0.3 to V_{C2}+6.5 V_{C3} –0.3 to V_{C3}+6.5 V_{C4} –0.3 to V_{C4}+6.5 V_{C5} –0.3 to V_{C5}+6.5 –0.3 to 6.5 -0.3 to V_{DD}+0.3 -0.3 to V_{DD}+0.3 -0.3 to V_{DD}+0.3 -0.3 to 3.0 -0.3 to 3.0	V
V_{COUT} V_{DOUT}	Output voltage(R5433VxxxxA) C_{OUT} pin voltage D_{OUT} pin voltage	 -0.3 to 30 -0.3 to 30	V
VC_{OUT} VD_{OUT}	Output voltage(R5433VxxxxB) C_{OUT} pin voltage D_{OUT} pin voltage	 -0.3 to V_R+0.3 -0.3 to V_R+0.3	V
P_D	Power dissipation	685	mW
Topt	Operating temperature range	-40 to 85	°C
Tstg	Storage temperature range	-55 to 125	°C

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ELECTRICAL CHARACTERISTICS

R5433VxxxAA   Unless otherwise specified, Topt=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
V_{DD1}	Operating input voltage	Voltage defined as VDD-VSS	1.7		25.0	V	-
$V_{DET1}n$	CELLn Over-charge threshold (n=1,2,3,4,5)	Detect rising edge of supply voltage	VDET1n-0.025	VDET1n	VDET1n+0.025	V	A
$V_{REL1}n$	CELLn Over-charge released voltage(n=1,2,3,4,5)	Detect falling edge of supply voltage	V_{REL1n}-0.050	V_{REL1n}	V_{REL1n}+0.050	V	A
tV_{DET1}	Output delay of over-charge	$V_{DD}=V_{C1}$, $Vc_{CELL}n$=3.5V, V_{CELL1}=3.5V to 4.5V (n=2,3,4,5)	0.7	1.0	1.3	s	B
tV_{REL1}	Output delay of release from over-charge	$V_{DD}=V_{C1}$, $V_{CELL}n$=3.5V, VCELL1=4.5V to 3.5V (n=2,3,4,5)	11	16	21	ms	B
$V_{DET2}n$	CELLn Over-discharge threshold (n=1,2,3,4,5)	Detect falling edge of supply voltage	$V_{DET2n}\times$0.975	VDET2n	$V_{DET20}\times$1.025	V	C
$V_{REL2}n$	CELLn Released Voltage from Over-discharge (n=1,2,3,4,5)	Detect rising edge of supply voltage	$V_{REL2n}\times$0.975	VREL2n	$V_{REL2n}\times$1.025	V	C
I_{CT}	CT pin charge current	VDD=V_{C1}, VCELLn=3.5V(n=2,3,4,5) V_{CELL1}=3.5V to 1.5V	350	500	650	nA	D
V_{DCT}	CT pin detector threshold	$V_{DD}=V_{C1}$, $V_{CELL}n$=3.2V(n=2,3,4,5) V_{CELL1}=3.5V to 1.5V	1.48	1.80	2.22	V	E
tV_{DET2}	Output delay of over-discharge	$tV_{DET2}=C_{CT}$ x V_{DCT}/I_{CT}, C_{CT}=0.33uF	0.8	1.2	1.6	s	-
tV_{REL2}	Output delay of release from over-discharge	$V_{DD}=V_{C1}$, $V_{CELL}n$=3.5V V_{CELL1}=1.5V to 3.5V, (n=2,3,4,5)	0.7	1.2	1.7	ms	F
I_{CTLT}	CTLT pin charge current	$V_{DD}=V_{C1}$, $V_{CELL}n$=3.5V(n=1,2,3,4,5)	145	200	264	nA	G
V_{DTLT}	CTLT pin detector threshold	$V_{DD}=V_{C1}$ $V_{CELL}n$=3.2V(n=1,2,4,5) VC3,=VD1+0.25V	1.58	1.80	2.42	V	H
V_{RTLT}	CTLT pin released voltage	$V_{DD}=V_{C1}$ $V_{CELL}n$=3.2V(n=1,2,3,4,5)	0.07	0.13	0.19	V	H
tLT	Test interval of breaking wire detector	C_{CTLT}=3.3μF, TLT=C_{CTLT} x (V_{DCT}-V_{RTLT})/I_{CTLT}	21	30	39	s	-
V_{IH1}	SEL1 pin "H" input voltage	$V_{DD}=V_{C1}$, $V_{CELL}n$=3.2V (n=1,2,3,4,5)	7.7		V_{DD}+0.3	V	I
V_{IL1}	SEL1 pin "L" input voltage	$V_{DD}=V_{C1}$, $V_{CELL}n$=3.2V (n=1,2,3,4,5)	Vss-0.3		V_{SS}+1.0	V	I
V_{IH2}	SEL2 pin "H" input voltage	V_{DD}=VC1, $V_{CELL}n$=3.2V (n=1,2,3,4,5)	7.7		V_{DD}+0.3	V	J
V_{IL2}	SEL2 pin "L" input voltage	VDD=VC1, $V_{CELL}n$=3.2V (n=1,2,3,4,5)	V_{SS}-0.3		V_{ss}+1.0	V	J
V_{IH3}	DS pin "H" input voltage	VDD=VC1, $V_{CELL}n$=3.5V (n=2,3,4,5), $V_{CELL}n$=4.5V to 3.0V	14.0		V_{DD}+0.3	V	K
V_{IM3}	DS pin "Middle" input voltage	VDD=VC1, $V_{CELL}n$=3.5V (n=2,3,4,5), V_{CELL1}=4.5V to 3.0V (Max side) V_{CELL1}=3.5V to 1.5V (Min side)	2.8		5.9	V	K、L
V_{IL3}	DS pin "L" input voltage	VDD=VC1, $V_{CELL}n$=3.5V (n=2,3,4,5), V_{CELL1}=3.5V to 1.5V	Vss-0.3		0.9	V	L

*Note: VCELLn means Cell-n's voltage. n=1,2,3,4,5

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
VOL1	COUT N-channel ON voltage	I_{OL}=50μA, V_{DD}=VC1 V_{CELLn}=3.2V, (n=1,2,3,4,5)		0.1	0.5	V	M
VOL2	DOUT N-channel ON voltage	I_{OL}=50μA, V_{DD}=VC1 V_{CELLn}=3.2V, (n=1,2,3,4,5)		0.1	0.5	V	N
ILCOUT	COUT open-drain pin off leakage current	V_{DD}=VC1, V_{CELLn}=6.0V (n=1,2,3,4,5) COUT=30.0V	-0.2		0.2	μA	O
ILDOUT	DOUT open-drain pin off leakage current	V_{DD}=VC1, V_{CELLn}=1.5V, (n=1,2,3,4,5), COUT=30.0V	-0.2		0.2	μA	P
ISS1	Supply current1	VDD=VC1, COUT= VSS , DOUT = VSS, VCELLn=VDET1n-0.4V (n=1,2,3,4,5)		6.0	15.0	μA	a
ISS2	Supply current2	VDD=VC1, COUT= VSS , DOUT = VSS, VCELLn=1.5V (n=1,2,3,4,5)		5.0	13.0	μA	a

*Note: VCELLn means Cell-n's voltage. n=1,2,3,4,5

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R5433VxxxAB

Unless otherwise specified, Topt=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
VDD1	Operating input voltage	Voltage defined as VDD-VSS	1.7		25.0	V	-
VDET1n	CELLn Over-charge threshold (n=1,2,3,4,5)	Detect rising edge of supply voltage	VDET1n-0.025	VDET1n	VDET1n + 0.025	V	A
VREL1n	CELLn Over-charge released voltage(n=1,2,3,4,5)	Detect falling edge of supply voltage	V_{REL1n}-0.050	V_{REL1n}	V_{REL1n}+0.050	V	A
tVDET1	Output delay of over-charge	$V_{DD}=V_{C1}$, Vc_{ELLn}=3.5V, V_{CELL1}=3.5V to 4.5V (n=2,3,4,5)	0.7	1.0	1.3	s	B
tV_{REL1}	Output delay of release from over-charge	$V_{DD}=V_{C1}$, V_{CELLn}=3.5V, V_{CELL1}=4.5V to 3.5V (n=2,3,4,5)	11	16	21	ms	B
VDET2n	CELLn Over-discharge threshold (n=1,2,3,4,5)	Detect falling edge of supply voltage	$V_{DET2n}\times$0.975	VDET2n	$V_{DET20}\times$1.025	V	C
VREL2n	CELLn Released Voltage from Over-discharge (n=1,2,3,4,5)	Detect rising edge of supply voltage	$V_{REL2n}\times$0.975	VREL2n	$V_{REL2n}\times$1.025	V	C
ICT	CT pin charge current	$V_{DD}=V_{C1}$, V_{CELLn}=3.5V(n=2,3,4,5) V_{CELL1}=3.5V to 1.5V	350	500	650	nA	D
VDCT	CT pin detector threshold	$V_{DD}=V_{C1}$, V_{CELLn}=3.2V(n=2,3,4,5) V_{CELL1}=3.5V to 1.5V	1.48	1.80	2.22	V	E
tVDET2	Output delay of over-discharge	$tV_{DET2}=C_{CT}$ x V_{DCT}/I_{CT}, C_{CT}=0.33uF	0.8	1.2	1.6	s	-
tVREL2	Output delay of release from over-discharge	VDD=VC1, VCELLn=3.5V V_{CELL1}=1.5V to 3.5V, (n=2,3,4,5)	0.7	1.2	1.7	ms	F
ICTLT	CTLT pin charge current	$V_{DD}=V_{C1}$, V_{CELLn}=3.5V(n=1,2,3,4,5)	145	200	264	nA	G
VDTLT	CTLT pin detector threshold	$V_{DD}=V_{C1}$ V_{CELLn}=3.2V(n=1,2,4,5) VC3,=VD1+0.25V	1.58	1.80	2.42	V	H
VRTLT	CTLT pin released voltage	$V_{DD}=V_{C1}$ V_{CELLn}=3.2V(n=1,2,3,4,5)	0.07	0.13	0.19	V	H
tLT	Test interval of breaking wire detector	C_{CTLT}=3.3uF, TLT=C_{CTLT}x(VDCT-VRTLT)/ICTLT	21	30	39	s	-
VIH1	SEL1 pin "H" input voltage	VDD=VC1, V_{CELLn}=3.2V (n=1,2,3,4,5)	7.7		V_{DD}+0.3	V	I
VIL1	SEL1 pin "L" input voltage	VDD=VC1, V_{CELLn}=3.2V (n=1,2,3,4,5)	Vss -0.3		V_{SS}+1.0	V	I
VIH2	SEL2 pin "H" input voltage	VDD=VC1, V_{CELLn}=3.2V (n=1,2,3,4,5)	7.7		V_{DD}+0.3	V	J
VIL2	SEL2 pin "L" input voltage	VDD=VC1, V_{CELLn}=3.2V (n=1,2,3,4,5)	V_{SS} -0.3		V_{SS}+1.0	V	J
VIH3	DS pin "H" input voltage	VDD=VC1, V_{CELLn}=3.5V (n=2,3,4,5), V_{CELLn}=4.5V to 3.0V	14.0		V_{DD} +0.3	V	K
VIM3	DS pin "Middle" input voltage	VDD=VC1, V_{CELLn}=3.5V (n=2,3,4,5), V_{CELL1}=4.5V to 3.0V (Max side) V_{CELL1}=3.5V to 1.5V (Min side)	2.8		5.9	V	K、L
VIL3	DS pin "L" input voltage	VDD=VC1, V_{CELLn}=3.5V (n=2,3,4,5), V_{CELL1}=3.5V to 1.5V	Vss -0.3		0.9	V	L

*Note: VCELLn means Cell-n's voltage. n=1,2,3,4,5

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Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
VOL1	COUT N-channel ON voltage	I_{OL}=50μA, V_{DD}=VC1 V_{CELLn}=3.2V, (n=1,2,3,4,5)		0.1	0.5	V	M
VOL2	DOUT N-channel ON voltage	I_{OL}=50μA, V_{DD}=VC1 V_{CELLn}=3.2V, (n=1,2,3,4,5)		0.1	0.5	V	N
VR	Internal regulator voltage	I_{OH}=0μA, V_{DD}=VC1 , V_{CELL1}=1.5V, V_{CELLn}=3.2V, (n=2,3,4,5)	3.0	3.7	4.5	V	O
VOH1	COUT P-channel ON voltage	I_{OH}=-50μA, V_{DD}=VC1 , V_{CELL1}=4.5V, V_{CELLn}=3.2V, (n=2,3,4,5)	VR-0.5	VR-0.1		V	M
VOH2	DOUT P-channel ON voltage	I_{OH}=-50μA, V_{DD}=VC1 , V_{CELL1}=1.5V, V_{CELLn}=3.2V, (n=2,3,4,5)	VR-0.5	VR-0.1		V	N
ISS1	Supply current1	VDD=VC1, VCELLn=VDET1n-0.4V (n=1,2,3,4,5)		6.0	15.0	μA	a
ISS2	Supply current2	VDD=VC1, VCELLn=1.5V (n=1,2,3,4,5)		5.0	13.0	μA	a

*Note: VCELLn means Cell-n's voltage. n=1,2,3,4,5

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OPERATION

● VDET1n / Over-Charge Detectors (n=1, 2, 3, 4, 5)

While the cell is charged, the voltage between VC1 pin and VC2 pin (voltage of the Cell-1), the voltage between VC2 pin and VC3 pin (voltage of the Cell-2), the voltage between VC3 pin and VC4 pin (voltage of the Cell-3), the voltage of VC4 pin and VC5 pin (voltage of Cell-4), and the voltage between VC5 pin and VSS pin (voltage of the Cell-5) are supervised. If at least one of the cells' voltage becomes equal or more than the over-charge detector threshold, the over-charge is detected, and C$_{OUT}$ pin connected to an external pull up resistance outputs "H"-R5433VxxxAA or without pull-up resistance outputs "H"-R5433VxxxAB. As for the R5433VxxxAB, the output type of COUT pin is CMOS between VSS and internal regulator, and "H" voltage level is the output of the internal regulator, approximately 3.6V.

To reset the over-charge and make the C$_{OUT}$ pin level to "H" again after detecting over-charge, in such conditions that a time when all the cells' voltages becomes lower than the over-charge released voltage. The output voltage of C$_{OUT}$ pin becomes "L". The over-charge detectors have hysteresis.

Internal fixed output delay times for over-charge detection and release from over-charge exist. Even if one of cells keeps its level more than the over-charge detector threshold, and output delay time passes, over-charge voltage is detected. Even when the voltage of each cell becomes equal or higher level than V$_{DET1}$ if these voltages would be back to a level lower than the over-charge detector threshold within a time period of the output delay time, the over-charge is not detected. Besides, after detecting over-charge, each cell voltage is lower than the over-charge detector released voltage, even if just one of cells' voltage becomes equal or more than the over-charge released voltage within the released output delay time, over-charge is not released.

● VDET2n / Over-Discharge Detectors (n=1, 2, 3, 4, 5)

While the cells are discharged, the voltage between VC1 pin and VC2 pin (the voltage of Cell-1), the voltage between VC2 pin and VC3 pin (Cell-2 voltage), the voltage between VC3 pin and VC4 pin (Cell-3 voltage), the voltage between VC4 pin and VC5 pin (Cell-4 voltage), and the voltage between VC5 pin and Vss pin (Cell-5 voltage) are supervised.   If at least one of the cells' voltage becomes equal or less than the over-discharge detector threshold, the over-discharge is detected, and DOUT pin outputs "H".

R5433VxxxAA: Dout is connected to an external pull up resistance, and outputs "H".

R5433VxxxAB: Dout is not connected to any pull-up resistance, and outputs "H". The output type of DOUT pin is CMOS type between VSS and the internal regulator output. "H" level of DOUT is the output of the internal regulator, approximately 3.6V.

The condition to release over-discharge voltage detector is that after detecting over-discharge voltage, all the cells' voltage becomes higher than the over-discharge released voltage, DOUT pin becomes "L" level. The over-discharge detectors have hysteresis.

The output delay time for over-discharge detect is set with an external capacitor CCT connected to CT pin. If at least one of the cells' voltage becomes down to equal or lower than the over-discharge detector threshold, if the voltage of each cell would be back to a level higher than the over-discharge detector threshold within a time period of the output delay time, the over-discharge is not detected. Output delay time for release from over-discharge is also set internally.

After detecting over-discharge, supply current would be reduced and be into standby by halting unnecessary circuits.   The consumption current of the IC itself is reduced as small as possible.

● **SEL1, SEL2 pin**

    SEL1 and SEL2 pins are used as switch over 3-cell protector, 4-cell protector and 5-cell protector. If 4-cell protection is selected, by forcing VSS voltage level to SEL1 pin and forcing VDD voltage level to SEL2 pin, the operation of 5th cell's protection circuit stops, and the signal is shut down, therefore, even if the VC5 is shortened to GND, over-discharge is not detected and operates as a 4-cell protector IC.

    3-cell protection is selected, by forcing VDD voltage level to SEL1 pin, VSS voltage level to SEL2 pin, the operation of 5th cell and 4th cell stop, and the signal is cut off. Therefore, even if VC4, VC5 and VSS are shorted, over-discharge is not detected and operates as a 3-cell protector IC.

    Pull-up resistance is built in the SEL1 pin and SEL2 pin. If they are open, the level becomes VDD.

● **SEL1 and SEL2 pin input and operation mode**

SEL1 pin input	SEL2 pin input	Operation mode
"H"	"H"	5-cell protector
"L"	"H"	4-cell protector
"H"	"L"	3-cell protector
"L"	"L"	Prohibited

● **tVDET2 setting**

    CT pin is used for setting the output delay time of over-discharge (tVDET2) by connecting an external capacitor C_{CT}.

tVDET2 can be set according to the equation of $CV=i\Delta t$.

tVDET2 external capacitor C_{CT} setting

tVDET2 can be set as in the next formula.

$tVDET2(ms)=C_{CT}(nF)\times 3.64$

For example, if $C_{CT}=330nF$, tVDET2 =1201ms

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● **Breaking Wire Detector Function**

In the next figure, the breaking wire detector function is applied to the areas named as B+, B1, B2, B3, B4, and B-.
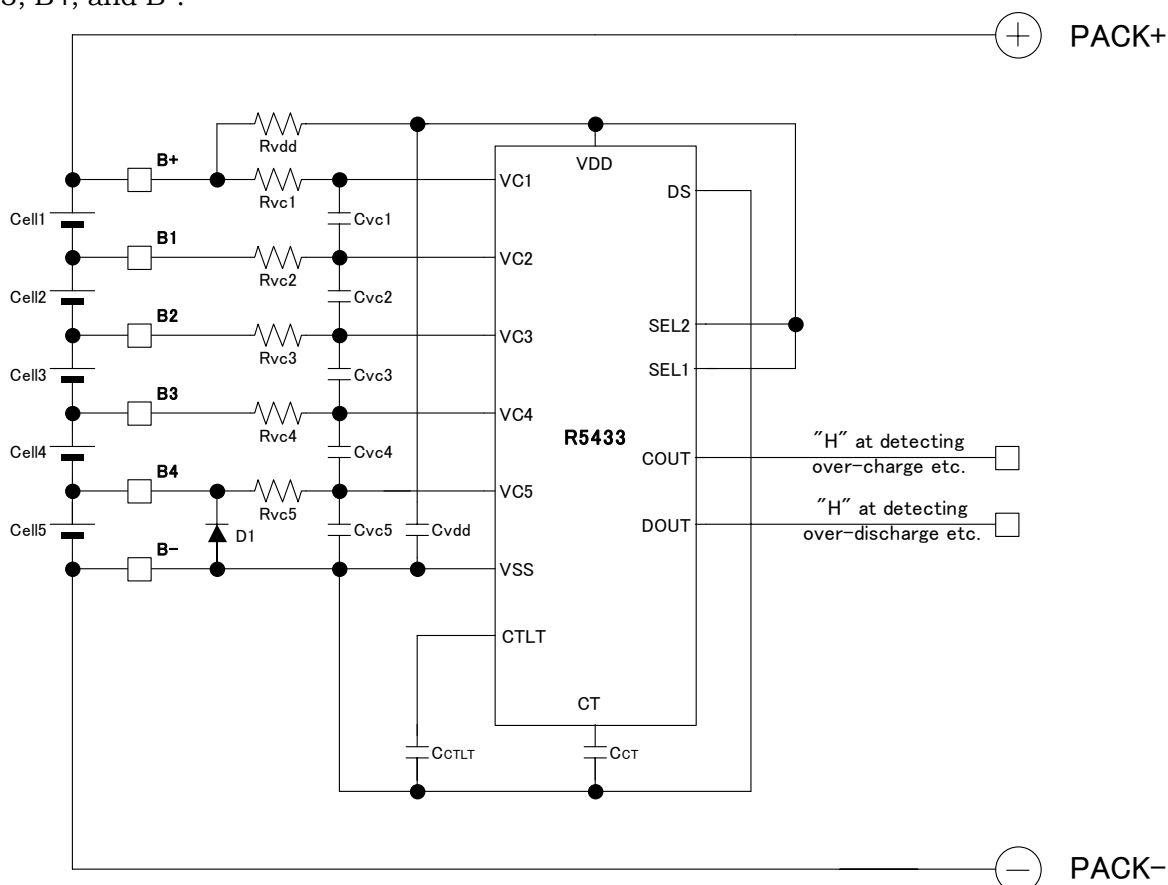
Breaking wire detector function for "B+" and "B-" as in 5-cell protector

If the breaking wire at "B+" is detected, the voltage between V_{C1} and V_{C2} becomes equal or less than 0V.

If the breaking wire at "B-" is detected, the voltage between V_{C5} and V_{SS} becomes equal or less than 0V.

The voltage shift is detected by the 0V-detector circuit.

If the breaking wire is detected, C_{OUT} pin connected to an external pull up resistance outputs "H"-R5433VxxxAA or without pull-up resistance outputs "H"-R5433VxxxAB. As for the R5433VxxxAB, the output type of C_{OUT} pin is CMOS between V_{SS} and internal regulator, and "H" voltage level is the output of the internal regulator, approximately 3.6V.

Breaking wire detector function for "B1", "B2", "B3", and "B4" as in 5-cell protector

In case of the 3.3uF capacitor is attached to the CTLT pin, breaking wire detector operates every 30 seconds. The breaking wire test time is for about 1s in 30 seconds. During the breaking wire testing, built in switch of V_{C1}, V_{C3}, V_{C5} cell, and the switch attached to the V_{C2} and V_{C4} turn on alternatively by the even_sw and the odd_sw signal. The internal impedance of the cell whose switch turns on becomes low. If the wire is broken,

VC shifts by the difference of internal impedance and the shift is detected by the comparator for VDET1. If the breaking wire is detected, the C_{OUT} pin of the R5433VxxxAA outputs "H" via an external pull-up resistance. While the output type of C_{OUT} pin of the R5433VxxxAB is CMOS between V_{SS} and internal regulator, and the "H" level is the output voltage of the internal regulator, approximately, 3.6V.

*Technical notes on breaking wire detector function

During the breaking wire test, even if the cell voltage becomes equal or more than the over-charge detector threshold, the over-charge detector does not operate. In this case, after the breaking wire test, if the cell voltage keeps its level equal or more than the over-charge detector threshold, then over-charge detector starts. Because of this reason, the output delay time of over-charge detector may be longer than tV_{DET1}.

During the breaking wire test, even if the cell voltage becomes equal or less than the over-discharge detector threshold, over-discharge detector does not operate. In this case, after the breaking wire test, if the cell voltage keeps its level equal or less than the over-discharge detector threshold, then over-discharge detector starts. Because of this reason, the output delay time of over-discharge may be longer than tV_{DET2}.

If over-charge is detected, the breaking wire test is cancelled. When the cell voltage becomes lower than the over-charge released voltage and over-charge is released, then breaking wire test is restarted.

If over-discharge is detected, the breaking wire test is cancelled. When the cell voltage is less than 3.0V, the breaking wire may not be detected.

When the B- wire is broken, the minimum input voltage of the IC is same as the input voltage of V_{C5} pin. Therefore, the output of C_{OUT} and D_{OUT} is more than V_{C5} pin voltage. If some external components are connected to C_{OUT} pin or D_{OUT} pin, and the GND level of the components is the negative terminal of the battery pack, then the voltage rating must be considered.

• DS (Delay shortening) function

By setting DS pin level as same as V_{DD}, over-charge detector output delay time can be shortened into about 1/100.

By forcing the voltage ranging from 2.8V to $V_{DD}/2-0.5$ to DS pin, the output delay time of over-charge can be shortened into approximately 4ms, and the output delay time of over-discharge can be shortened into approximately 1/100.

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TIMING CHART
(1)Timing diagram of over-charge and over-discharge operation
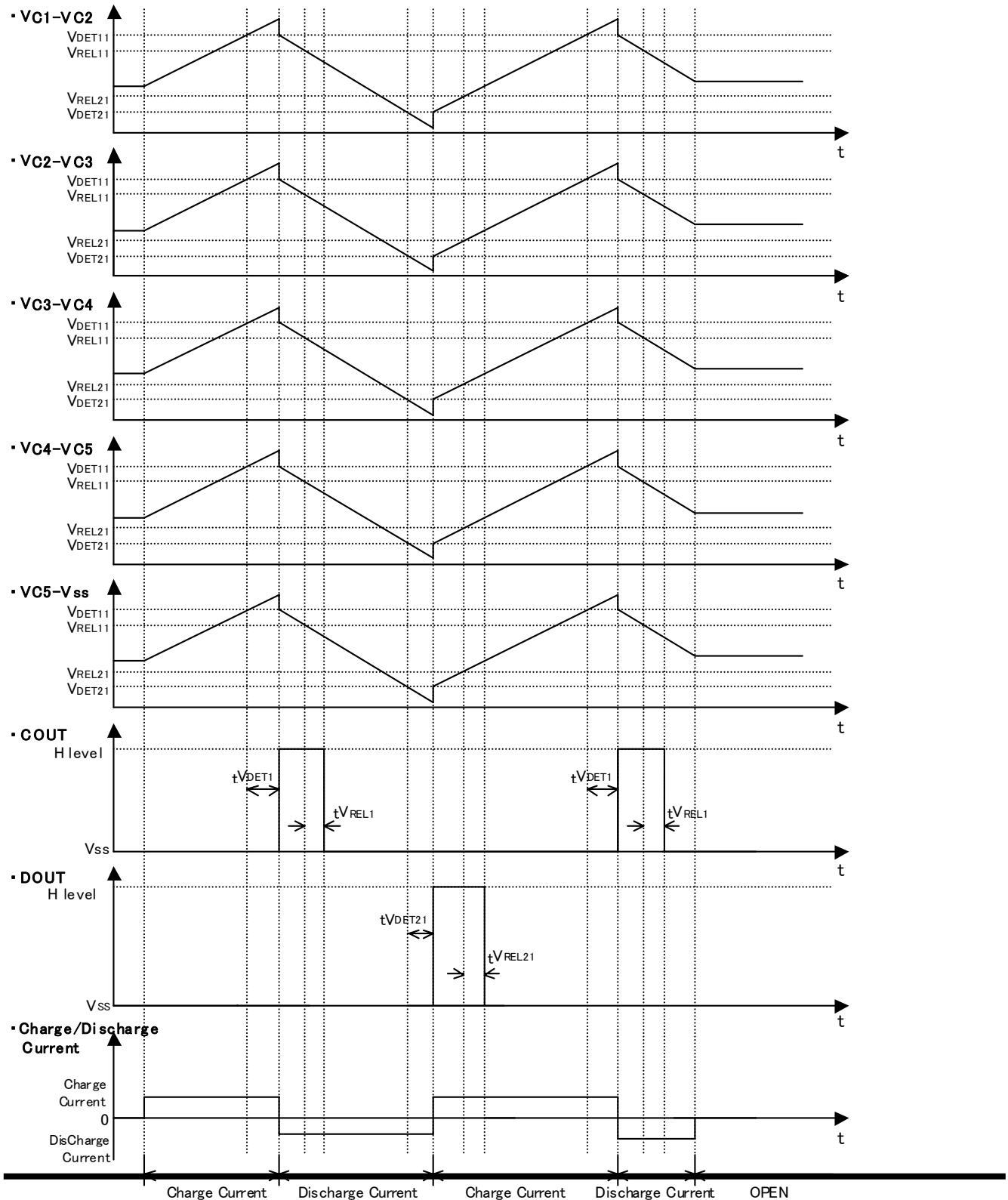
(2) Breaking wire detector operation

Breaking wire detector's operation of B1, B2, B3, and B4 for 5-cell protector

By attachment 3.3uF capacitor to the CTLT pin, breaking wire detector operates every 30 seconds. The built in switch of V_{C1}, V_{C3}, V_{C5} cell, and the switch attached to the V_{C2} and V_{C4} turn on alternatively by the even_sw and the odd_sw signal.

The internal impedance of the cell whose switch turns on becomes low by the low resistance connected to the switch in serial. If the wire is broken, the difference of internal impedance of the IC, VC value shifts, and the comparator, COMP for V_{DET1} detects the breaking wire, then, the output of C_{OUT} of the R5433VxxxAA becomes "H". The R5433VxxxAA outputs "H" from C_{OUT} via an external pull-up resistor. Without the pull-up resistance, the R5433VxxxAB, C_{OUT} outputs "H". The output type of C_{OUT} of R5433VxxxAB is CMOS between V_{SS} and internal regulator.

The timing chart of breaking wire of B2 is shown below:
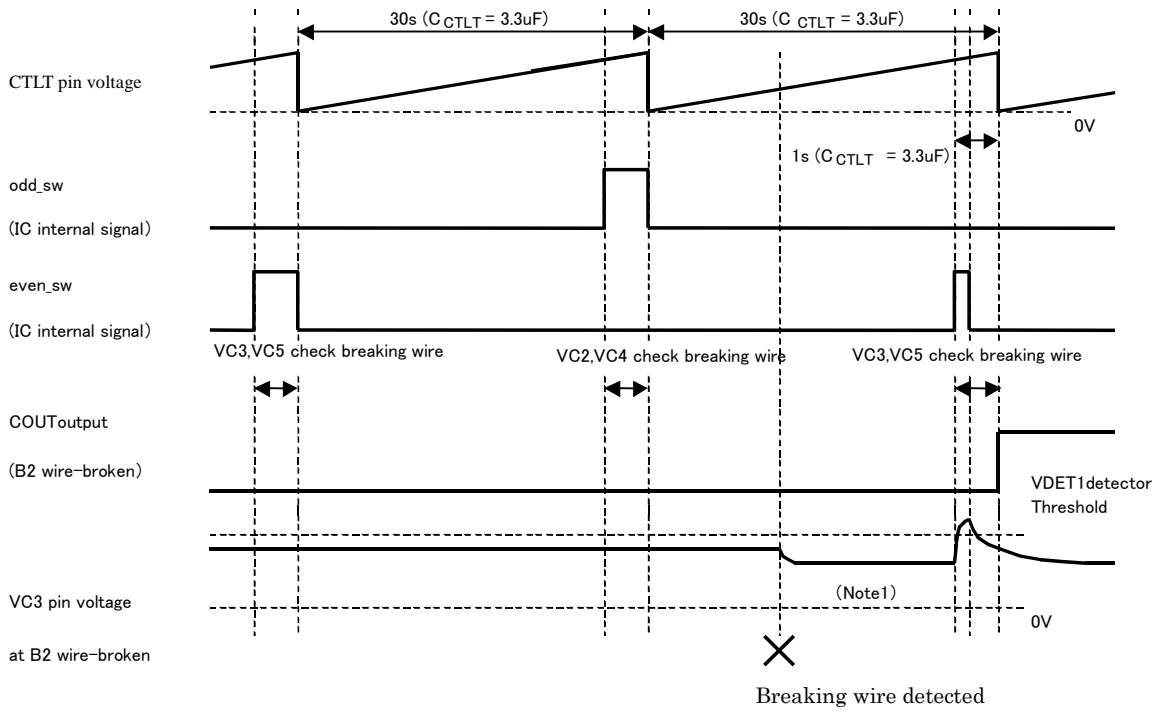
(Note1) The change of VC is not always increasing. Depending on the cell balance or the internal impedance, the VC increases or decreases.

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TYPICAL APPLICATION AND TECHNICAL NOTES

*Circuit example (R5433VxxxAA)
5-cell protection
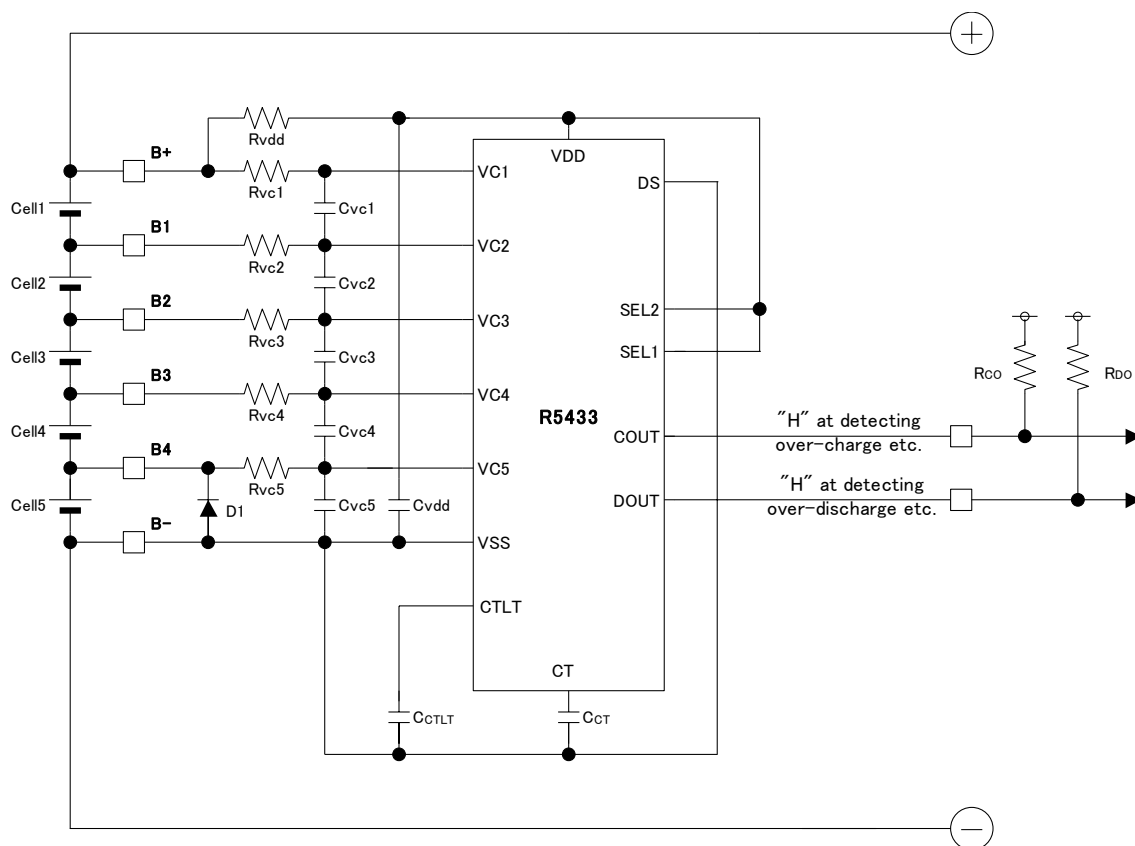
R5433VxxxAA

*Circuit example (for 4-cell protection)

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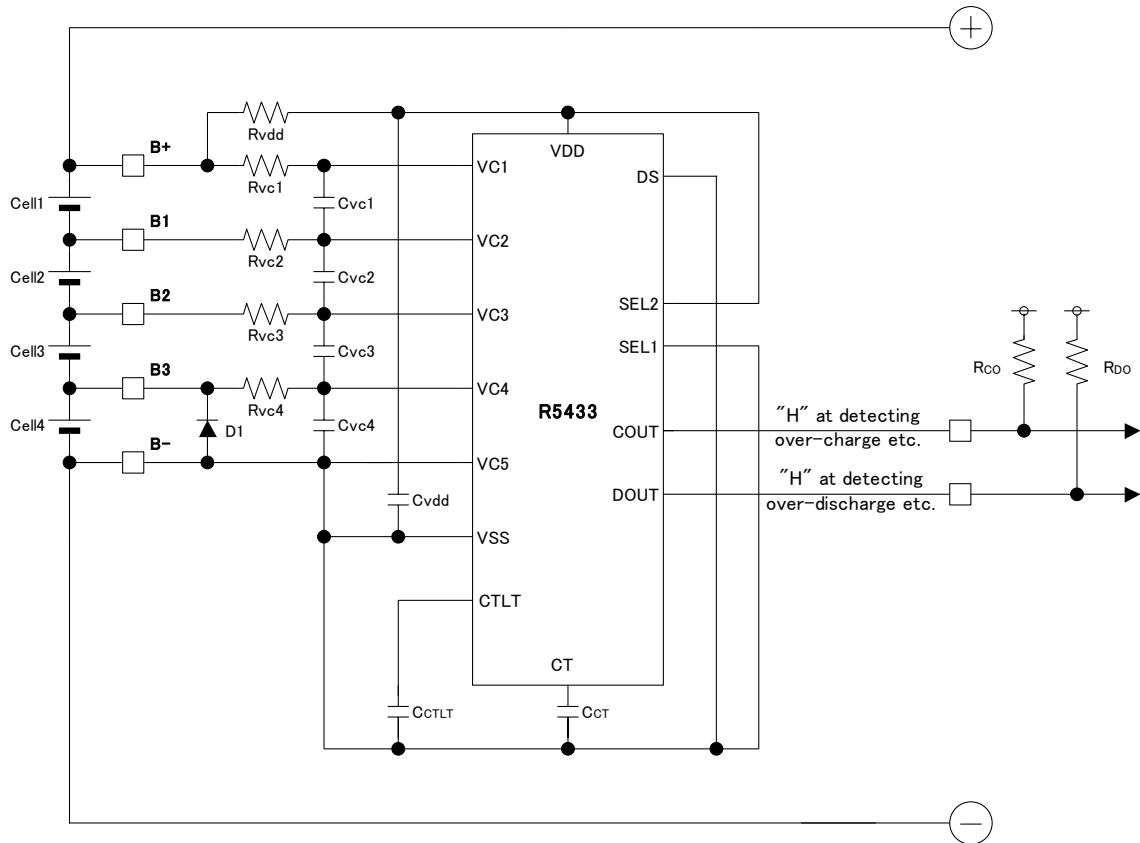
R5433VxxxAA

*Circuit example (for 3-cell protection)
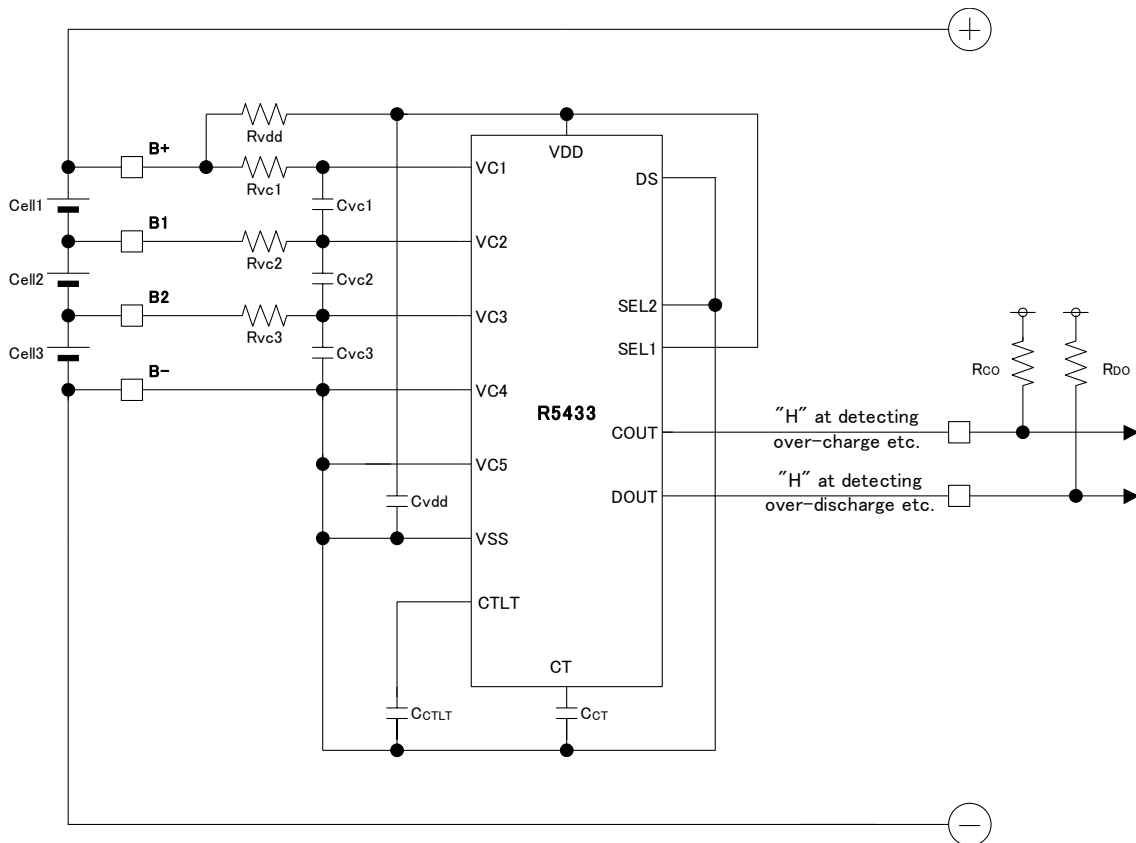
R5433VxxxAB

＊**Circuit Example (for 5-cell protection)**
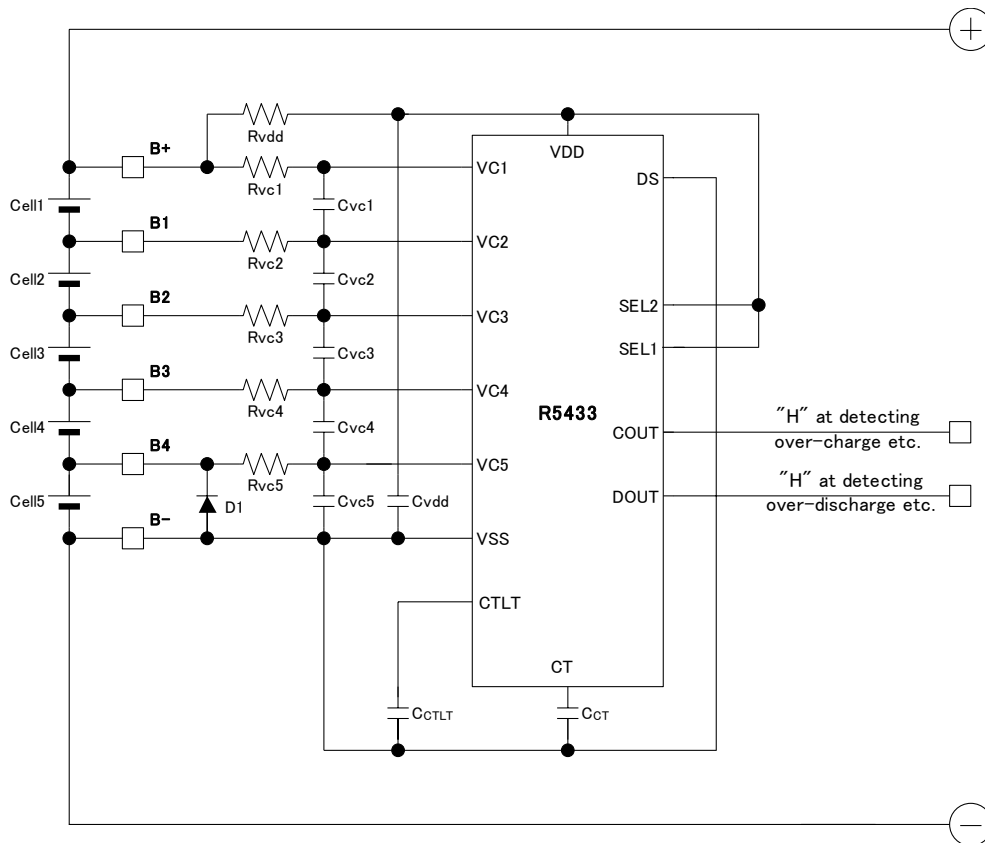
RICOH

R5433VxxxAB

＊Circuit Example (for 4-cell protection)

R5433VxxxAB

∗ Circuit Example (for 3-cell protection)

RICOH
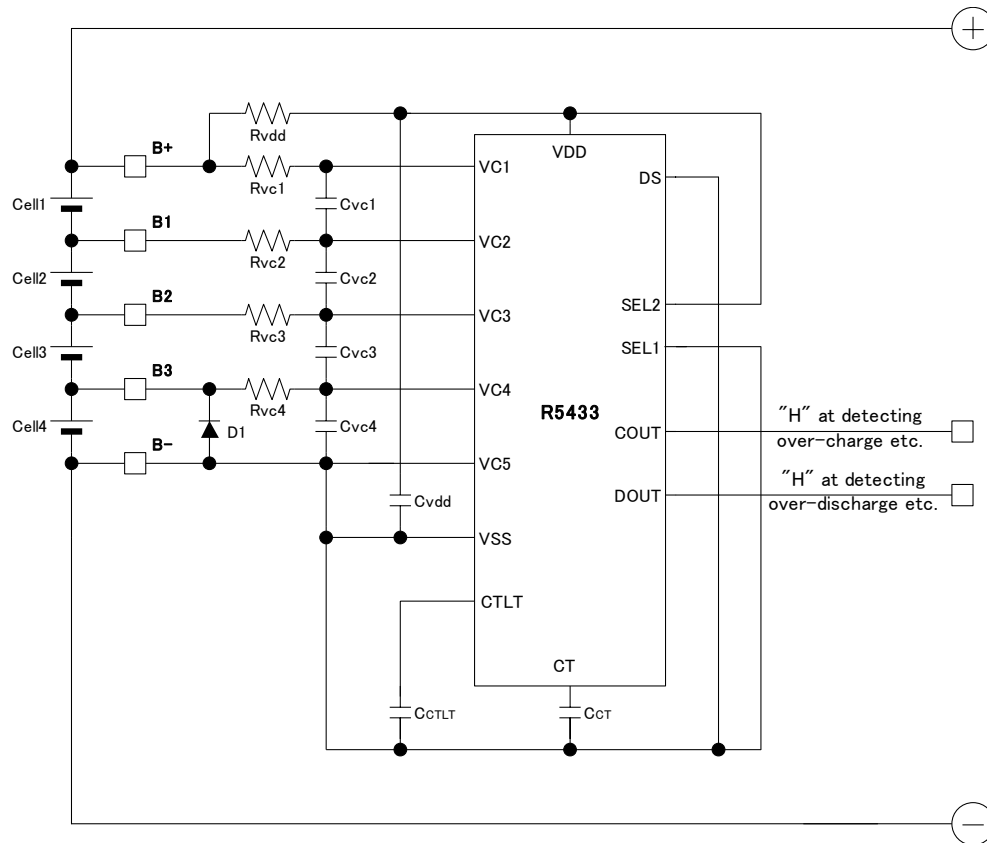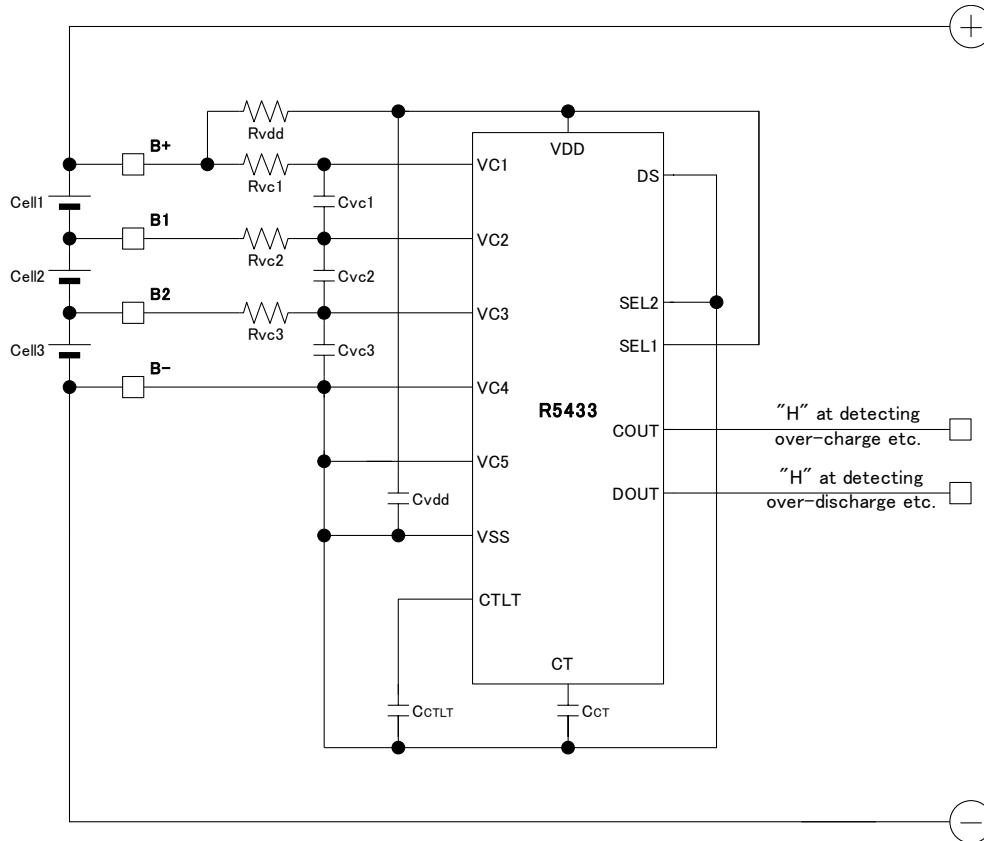
External Components values

Symbol	Value	Unit	Estimated Range	Reference Technical Notes #
Rvdd	1000	Ω	510 to 1000	*1
R_{VC1}	1000	Ω	1000	*2
R_{VC2}	1000	Ω	1000	*2
R_{VC3}	1000	Ω	1000	*2
R_{VC4}	1000	Ω	1000	*2
R_{VC5}	1000	Ω	1000	*2
R_{CO}	10	MΩ	*3	*3
R_{DO}	10	MΩ	*3	*3
Cvdd	0.1	μF	0.1 to 1.0	*1
C_{VC1}	0.1	μF	0.1	*2
C_{VC2}	0.1	μF	0.1	*2
C_{VC3}	0.1	μF	0.1	*2
C_{VC4}	0.1	μF	0.1	*2
C_{VC5}	0.1	μF	0.1	*2
C_{CT}	0.33	μF	0.01 to 1.00	*4
C_{CTLT}	3.3	μF	3.3	*5
D_1	*6	*6	*6	*6

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Technical Notes on the external circuits and components

*1) The voltage fluctuation is stabilized with Rvdd and Cvdd. If a small Rvdd is set, in the case of the large transient may happen to the cell voltage, by the flowing current, the IC may be unstable. If a large Rvdd is set, by the consumption current of the IC itself, the voltage difference between VDD pin and VC1 pin is generated, and unexpected operation may result. Therefore, the appropriate value range of Rvdd is from 510Ω to 1kΩ. To make a stable operation of the IC, the appropriate value range of Cvdd is from 0.1μF to 1.0μF.

*2) R_{VC1} to R_{VC10} and C_{VC1} to C_{VC5} stabilize the voltage fluctuation. If large R_{VC1} to R_{VC5} is set, the detector threshold will be high because of the internal conduction current of the IC. The operation error of breaking wire detector function may happen easily by the distribution of the ICs or environment. If small R_{VC1} to R_{VC5} is set, the noise immunity will be worse. Therefore the appropriate value of R_{VC1} to R_{VC5} is 1kΩ. To make stable operation, use 0.1μF as C_{VC1} to C_{VC5}.

*3) If small R_{CO} or R_{DO} is set, when the output of C_{OUT} or D_{OUT} is "L", the consumption current of protection circuit board increases. If large R_{CO} or R_{DO} is set, when the output of COUT or DOUT is "Hi-Z", the speed for pull-down the gate of the charge FET becomes slow and turning off the FET will be slow.

*4) If the breaking wire detector function of V_{C2} to V_{C5} is used, use 0.33μF to 1μF as C_{CT}. If the breaking wire detector function is unnecessary, use a capacitor of 0.01μF or more.

*5) If the breaking wire detector of V_{C2} to V_{C5} is used, use 3.3μF as C_{CTLT}. If the breaking wire detector of V_{C2} to V_{C5} is not necessary, short the CTLT pin to V_{SS}.

*6) If B- wire is broken, the internal regulator voltage may be close to V_{DD}. In such condition, if B- is reconnected, the over voltage stress is forced to the device connected to the internal regulator, and IC might be damaged. To prevent this situation, connect a diode as in the external components position. Choose the diode with Vf range is from 0.55V to 0.8V@25°C, 1mA load.

The typical application circuit diagrams are just examples. This circuit performance largely depends on the PCB layout and external components. In the actual application, fully evaluation is necessary.

Over-voltage and the over current beyond the absolute maximum rating should not be forced to the protection IC and external components.

Ricoh cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Ricoh product. If technical notes are not complied with the circuit which is used Ricoh product, Ricoh is not responsible for any damages and any accidents.

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TEST CIRCUITS

M
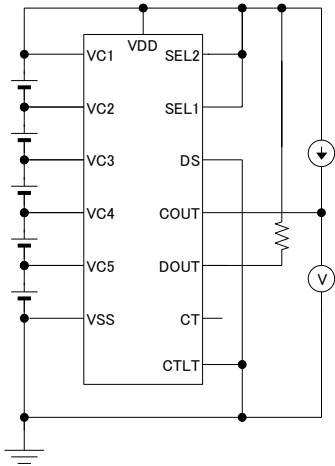
N
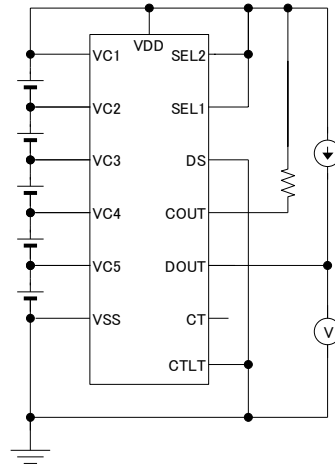
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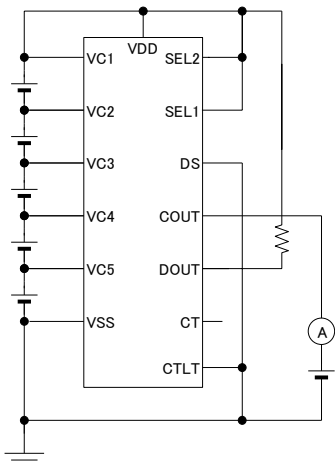
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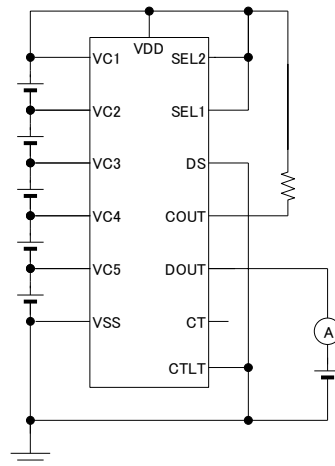
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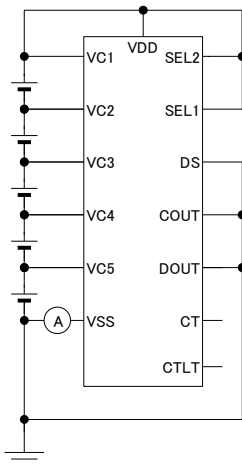
●R5433VxxxAB

A

B

C

D

E

F

G

H

I

J

K

L

M

N

O

a

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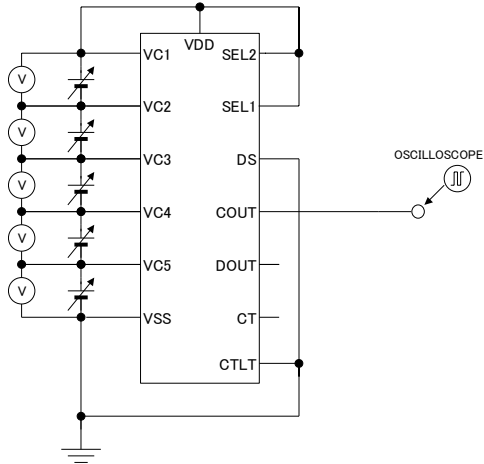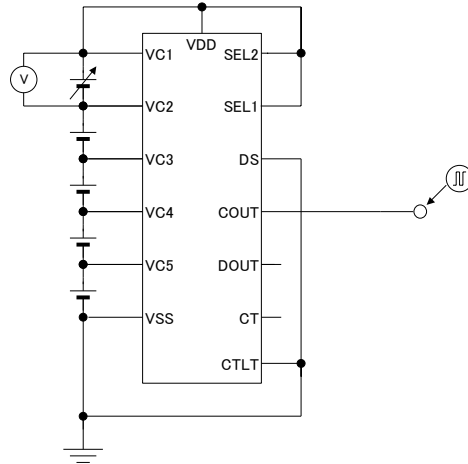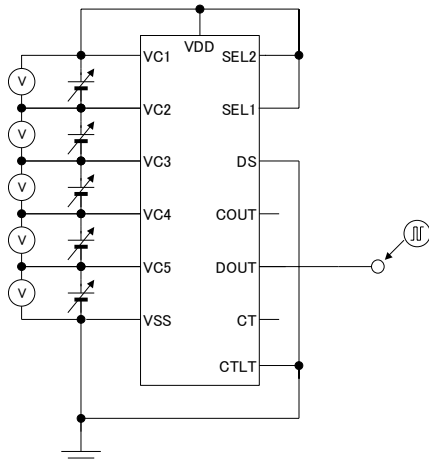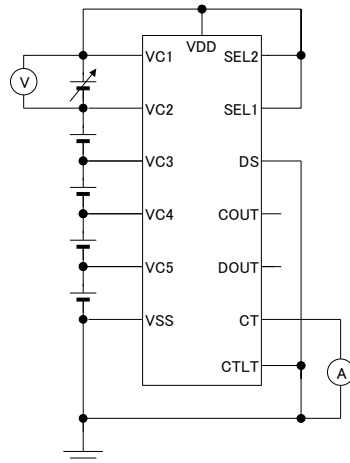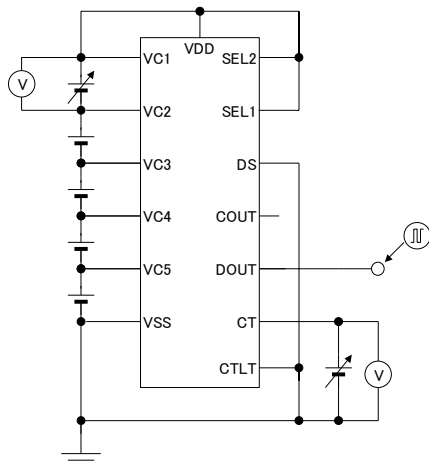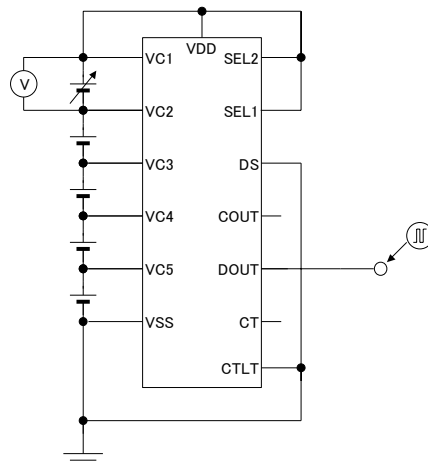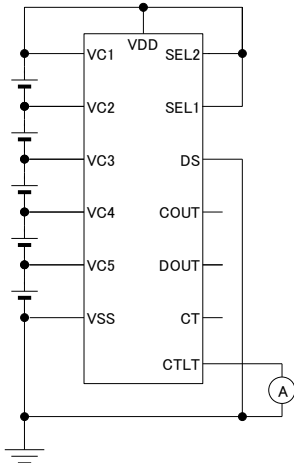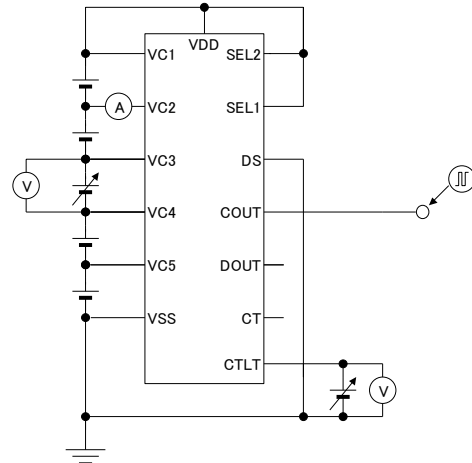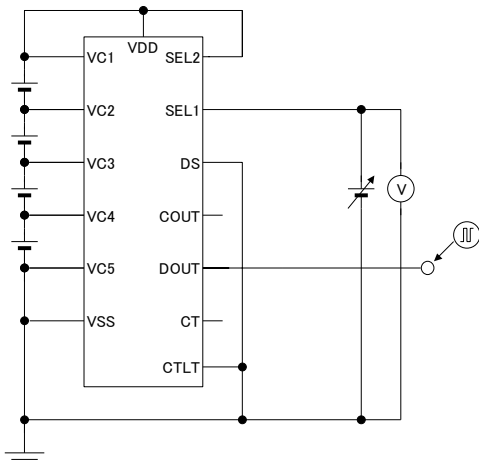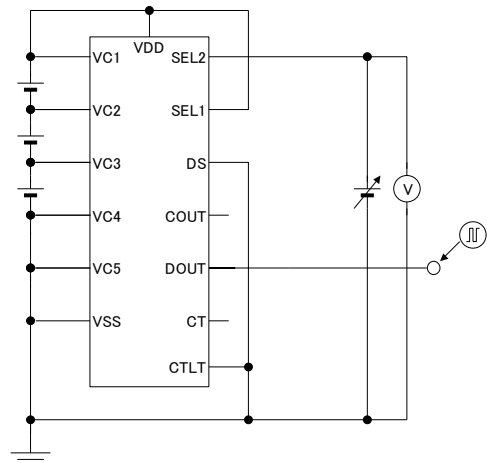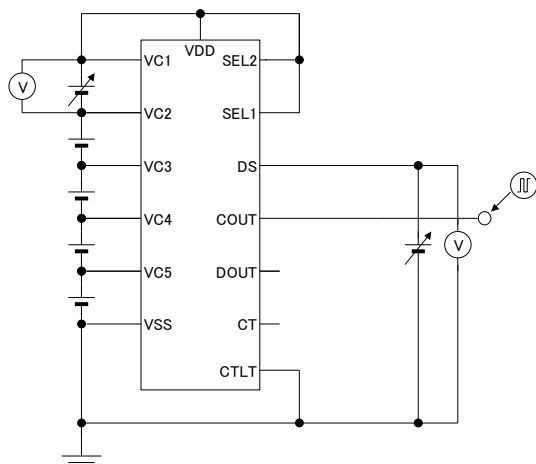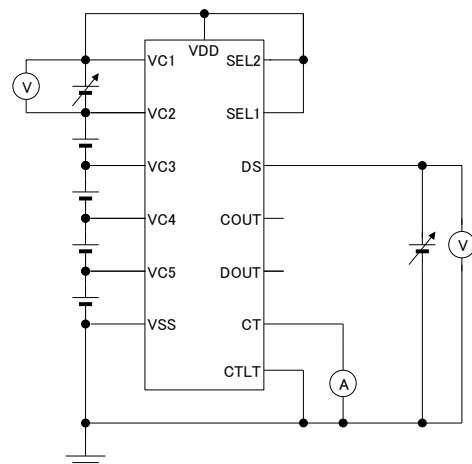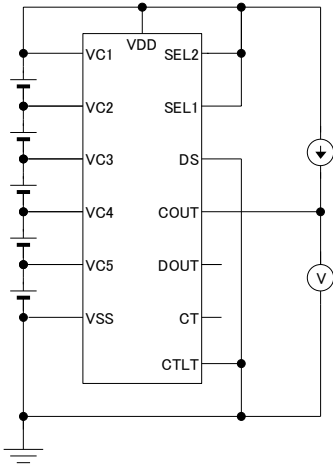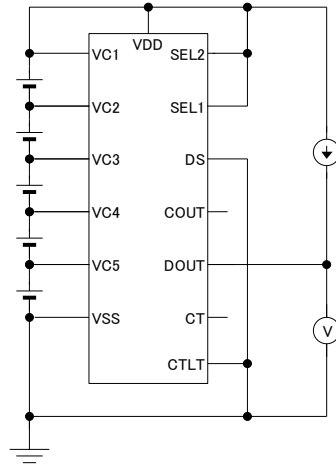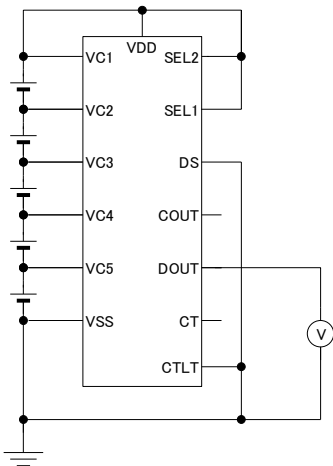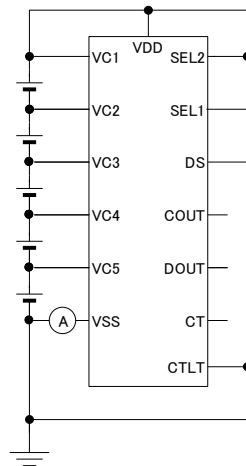
TYPICAL CHARACTERISTICS

● **Part1. Temperature Characteristics**

1)Cell-n Over-charge detector threshold
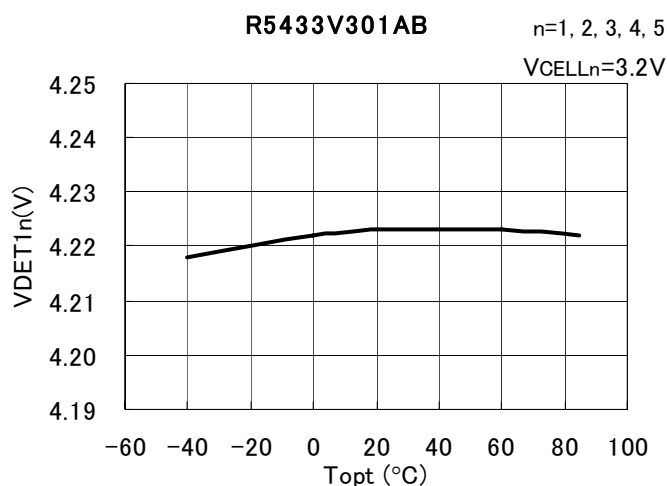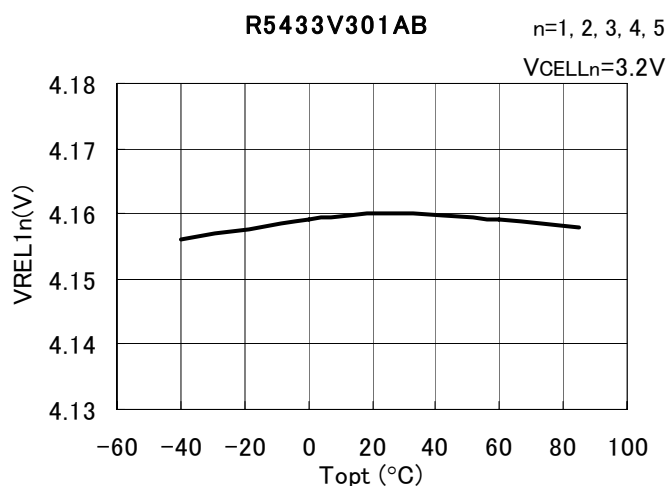
R5433V301AB   n=1, 2, 3, 4, 5

$V_{CELLn}=3.2V$

2) Cell-n Over-charge released voltage

R5433V301AB   n=1, 2, 3, 4, 5

$V_{CELLn}=3.2V$

3) Cell-n Output delay time of Over-charge detector

R5433V301AB   n=2, 3, 4, 5

$V_{CELLn}=3.2V$, $V_{CELL1}=3.2V{\rightarrow}4.5V$

4) Cell-n output delay time for release from over-charge

R5433V301AB   n=2, 3, 4, 5

$V_{CELLn}=3.2V$, $V_{CELL1}=4.5V{\rightarrow}3.2V$

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5) Cell-n over-discharge detector threshold

R5433V301AB   n=1, 2, 3, 4, 5

VCELLn=3.2V

6) Cell-n released voltage from over-discharge

R5433V301AB   n=1, 2, 3, 4, 5

VCELLn=3.2V
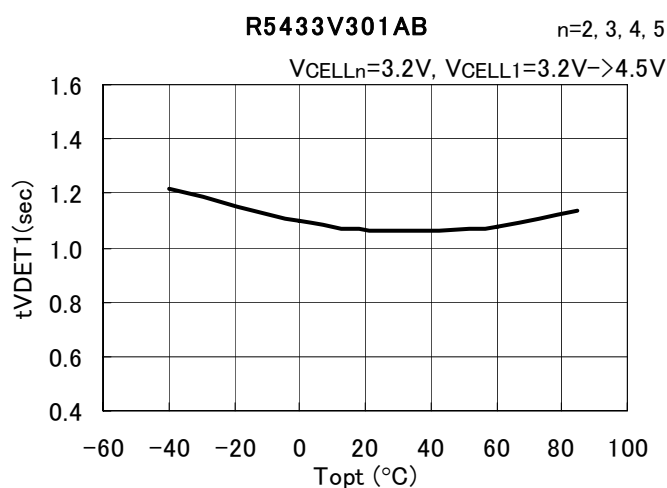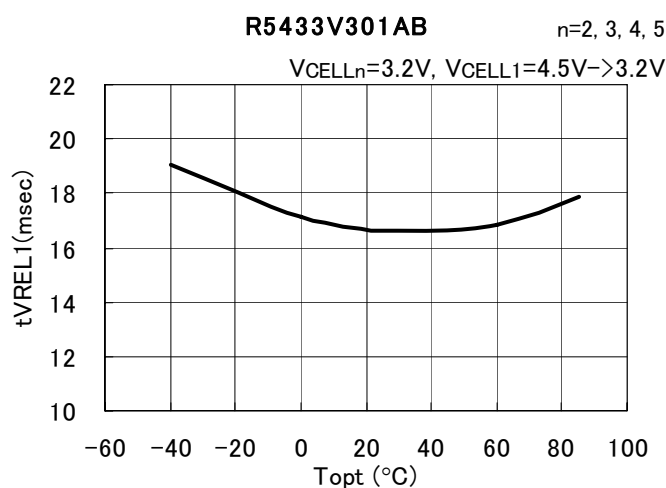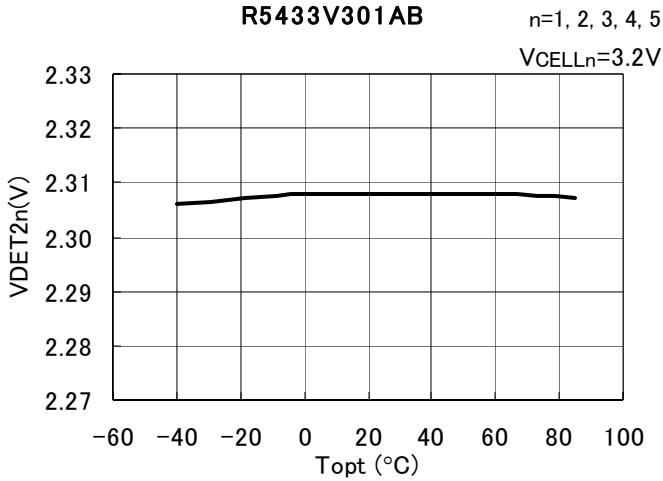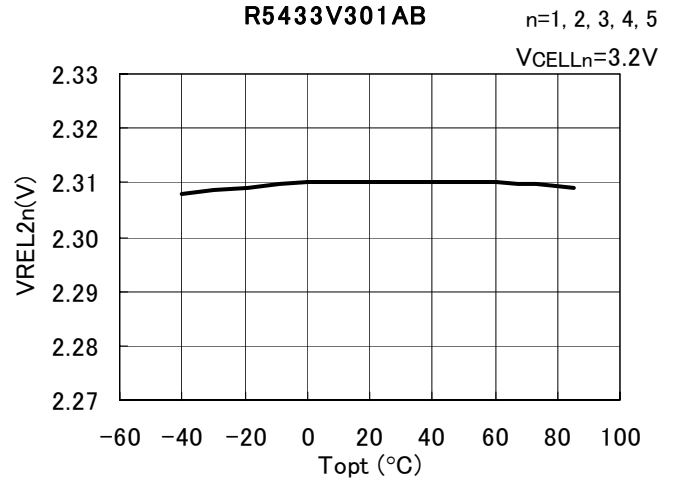
7) Cell-n over-discharge output delay time

R5433V301AB   n=2, 3, 4, 5

VCELLn=3.2V, VCELL1=3.2V−>1.5V, C1=33nF

8) Cell-n over-discharge released delay time

R5433V301AB   n=2, 3, 4, 5

VCELLn=3.2V, VCELL1=1.5V−>3.2V

9) CTLT charge current

R5433V301AB   n=1, 2, 3, 4, 5

VCELLn=3.2V
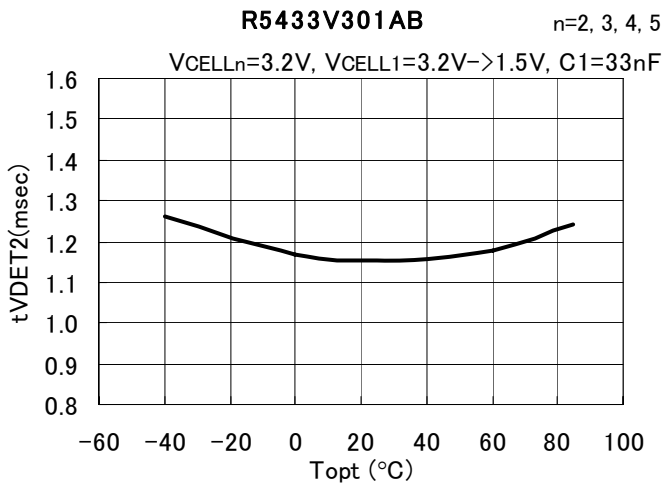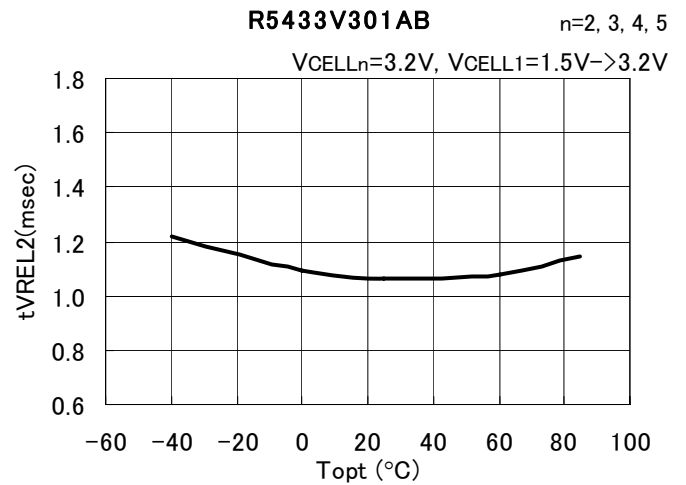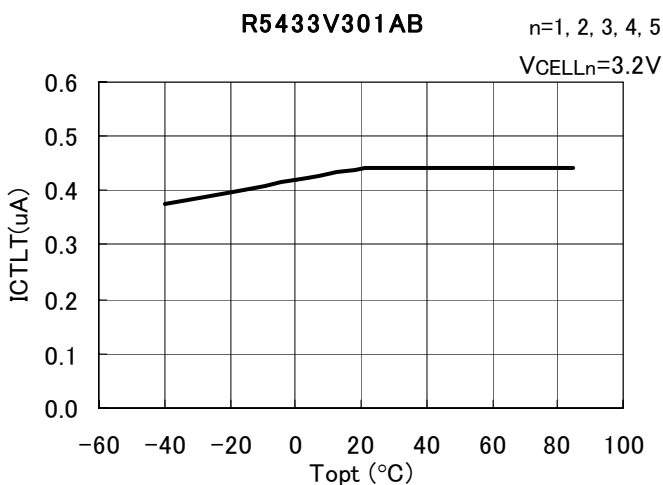
10) CTLT detector threshold

R5433V301AB   n=1, 2, 3, 4, 5

VCELLn=3.2V

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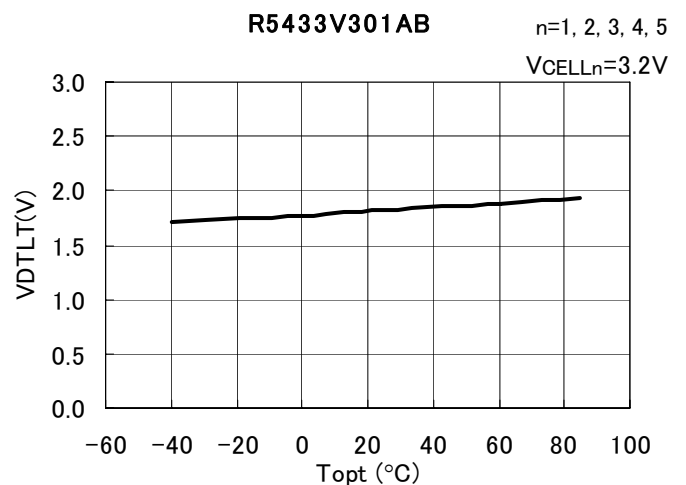
11) CTLT released voltage

R5433V301AB

n=1, 2, 3, 4, 5

V_{CELLn}=3.2V
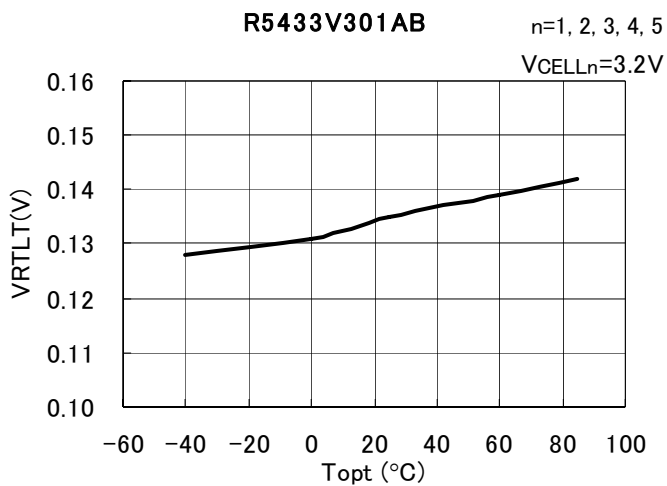
12) Breaking wire test interval time
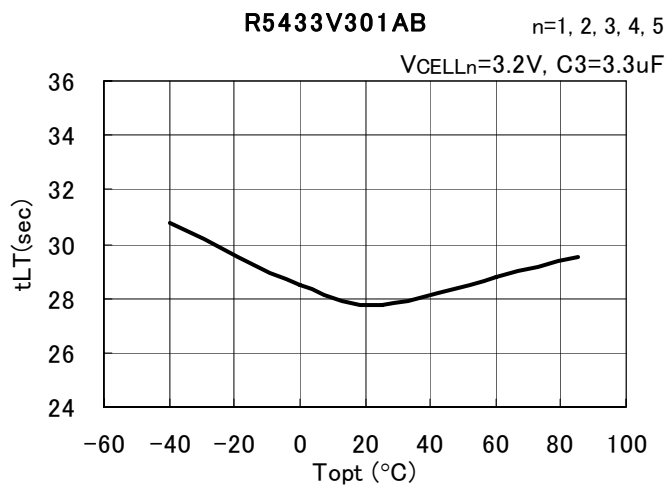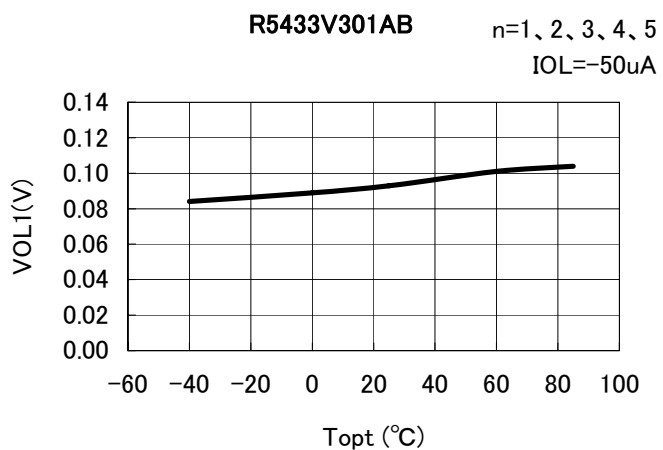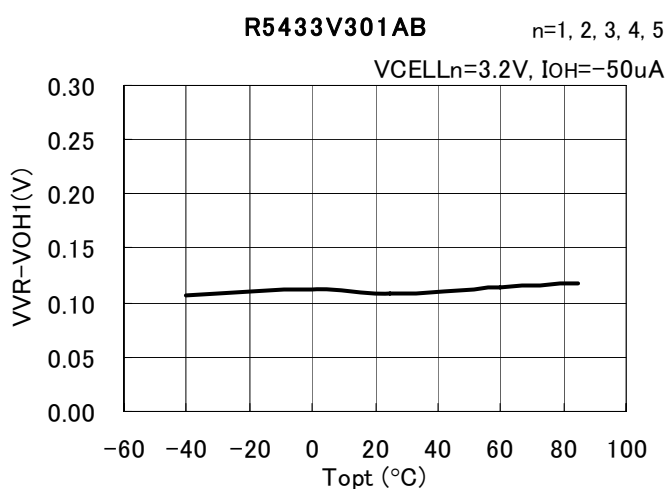
R5433V301AB

n=1, 2, 3, 4, 5

V_{CELLn}=3.2V, C3=3.3uF

13) C_{OUT} N-channel on voltage

R5433V301AB

n=1、2、3、4、5

I_{OL}=−50uA

14) C_{OUT} P-channel on voltage

R5433V301AB

n=1, 2, 3, 4, 5

V_{CELLn}=3.2V, I_{OH}=−50uA

15) DOUT N-channel on voltage

R5433V301AB   n=1, 2, 3, 4, 5

VCELLn=3.2V, $I_{OL}=-50uA$

16) D$_{OUT}$ P-channel on voltage

R5433V301AB   n=1, 2, 3, 4, 5

VCELLn=3.2V, $I_{OH}=-50uA$

17) VR V output voltage

R5433V301AB   n=1, 2, 3, 4, 5

VCELLn=3.2V

18) Supply Current 1

R5433V301AB   n=1, 2, 3, 4, 5

VCELLn=3.2V

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19) Supply current 2

R5433V301AB   n=1, 2, 3, 4, 5
V_{CELLn}=1.5V
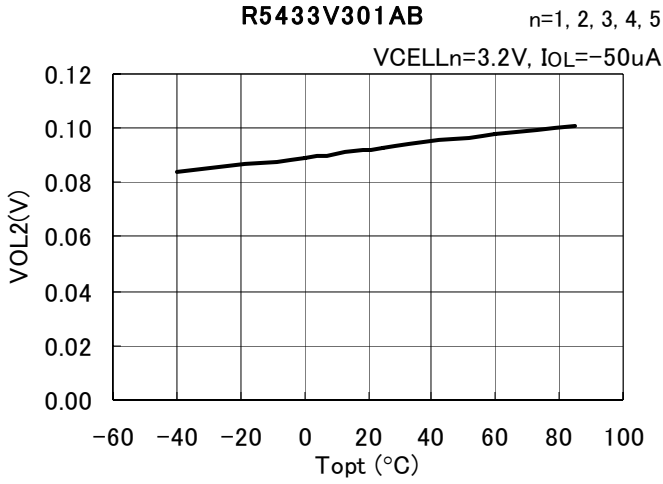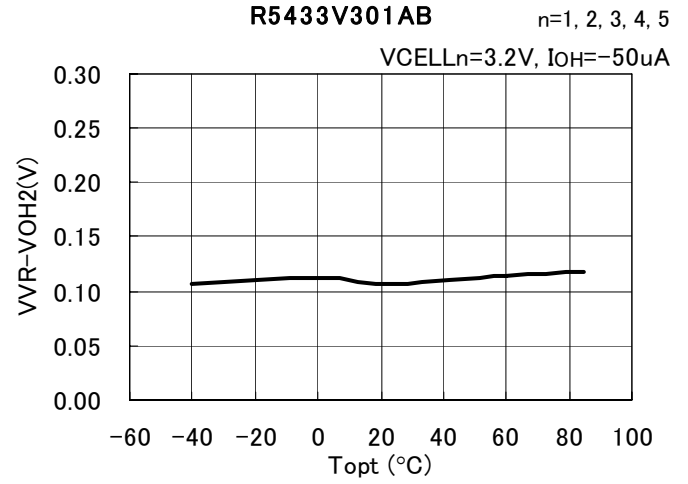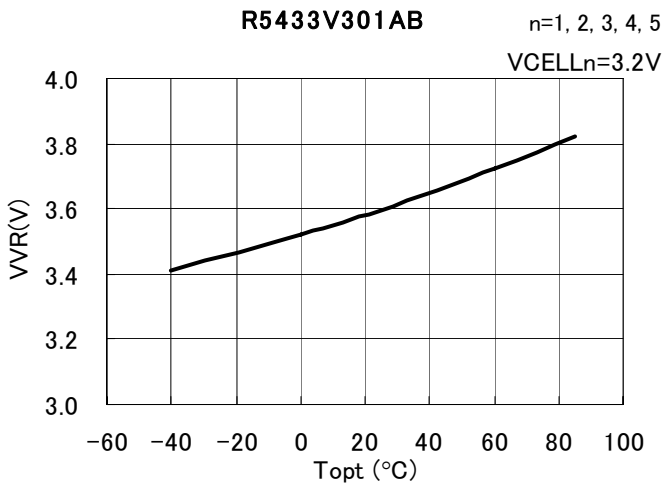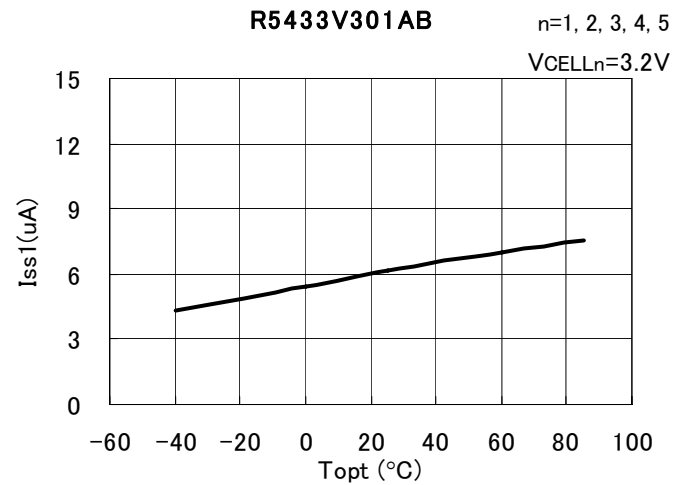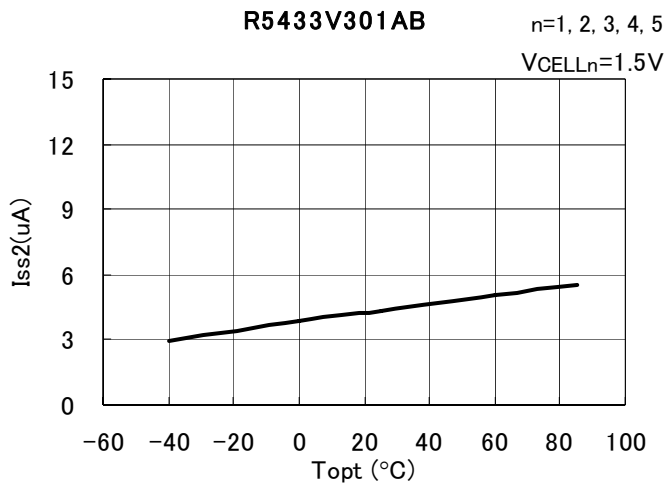
• **Part 2. Output Delay Time V$_{DD}$ dependence**

Over-charge detector output delay time
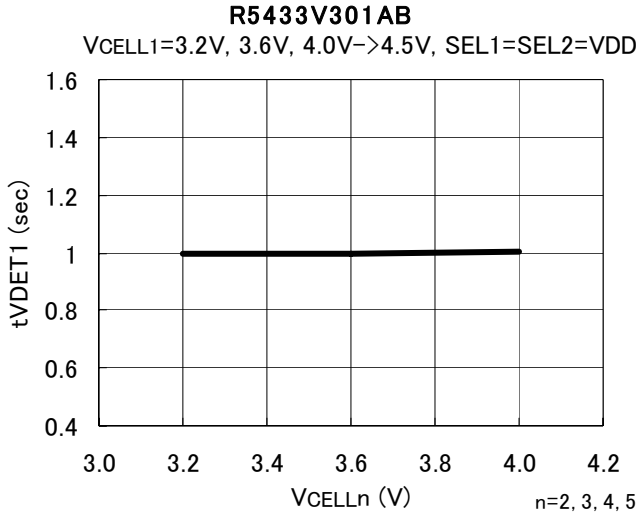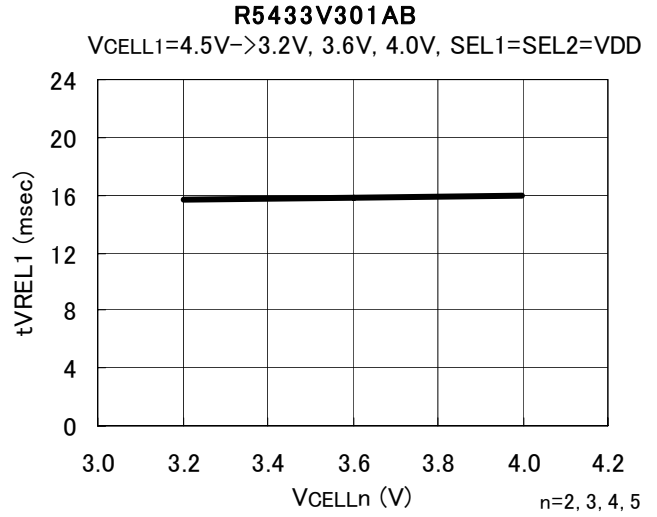
R5433V301AB
V$_{CELL1}$=3.2V, 3.6V, 4.0V–>4.5V, SEL1=SEL2=VDD

Over-charge released delay time

R5433V301AB
V$_{CELL1}$=4.5V–>3.2V, 3.6V, 4.0V, SEL1=SEL2=VDD

Over-discharge detector output delay time

R5433V301AB
V$_{CELL1}$=3.2V, 3.6V, 4.0V–>2.0V, SEL1=SEL2=VDD

Over-discharge released delay time

R5433V301AB
V$_{CELL1}$=2.0V–>3.2V, 3.6V, 4.0V, SEL1=SEL2=VDD

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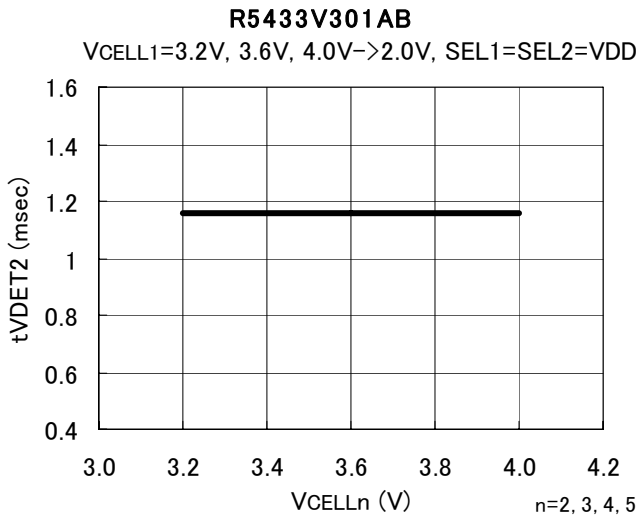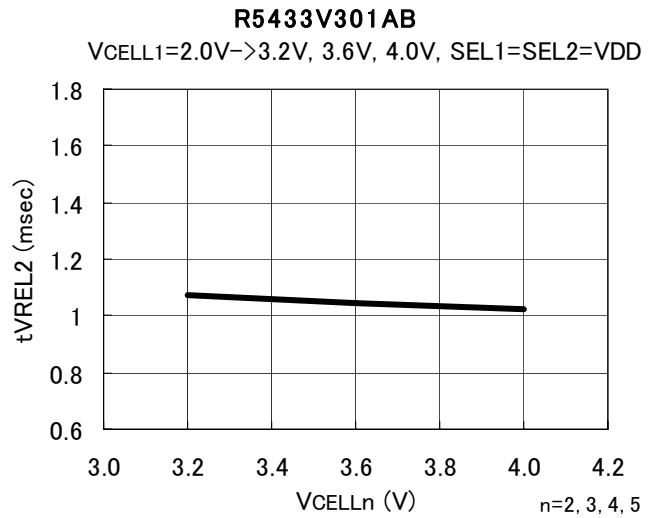
● **Part3. Supply current VDD dependence (R5433V301AB)**
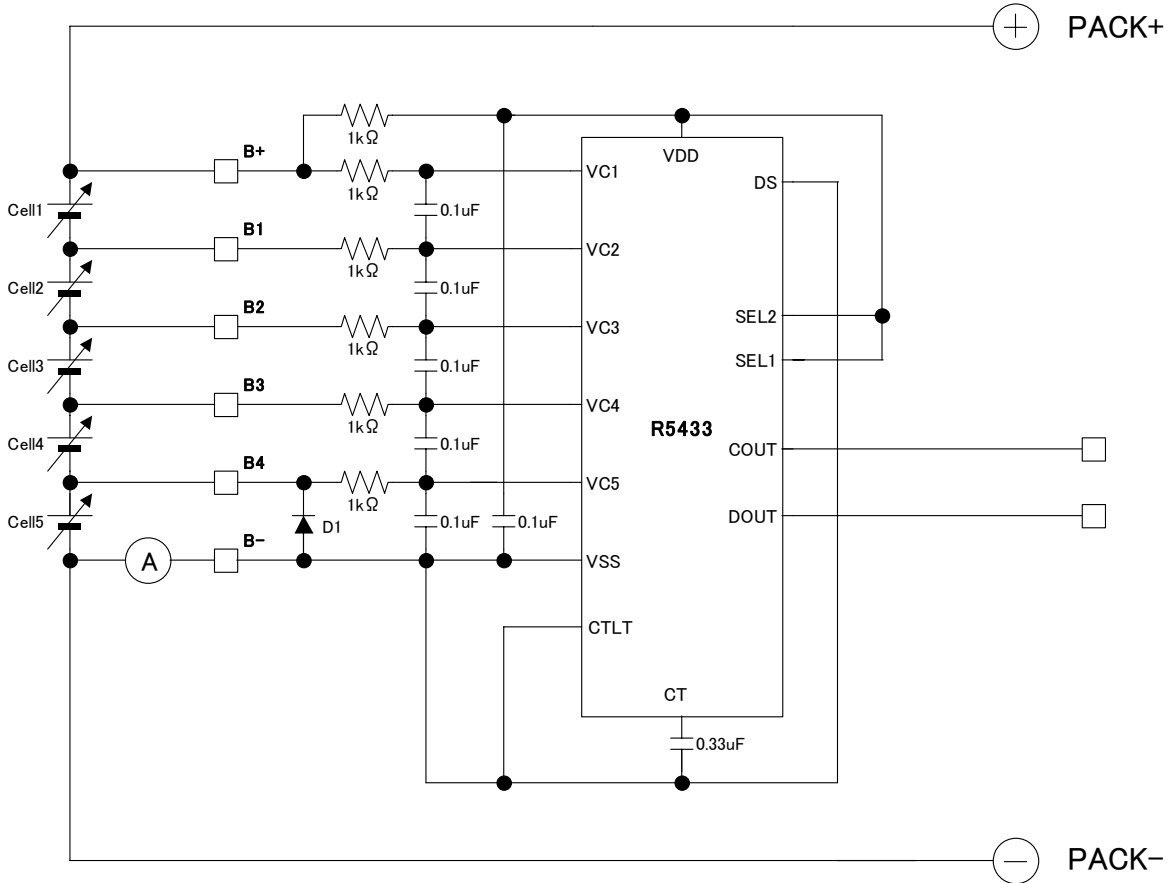
Supply current for 5-cell protection

R5433V301AB

V_{CELL1}=3.2V, 3.6V, 4.0V→2.0V, SEL1=SEL2=VDD
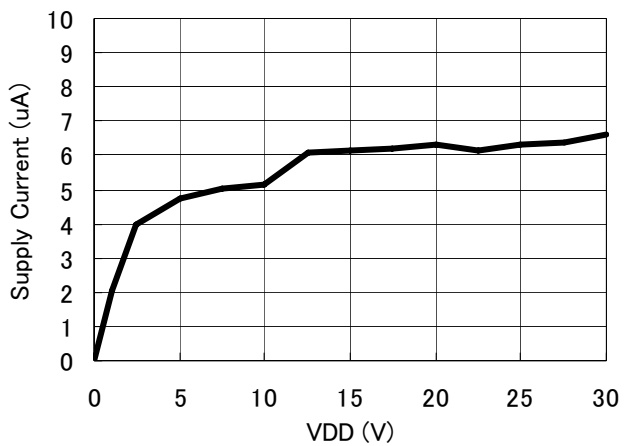
● **Part4. External resistance dependence (R5433V301AB)**

RICOH
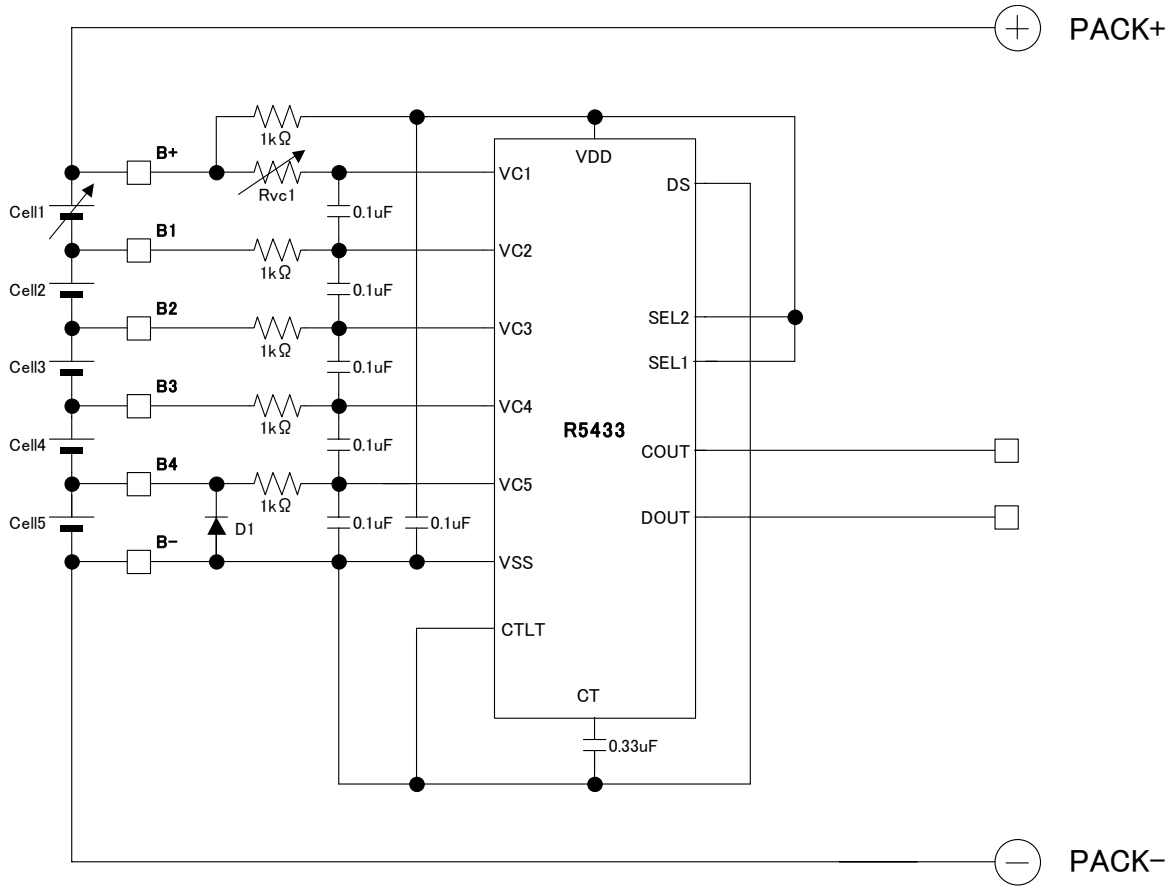
Over-charge/ Released from over-charge vs. R1 (Cell1)
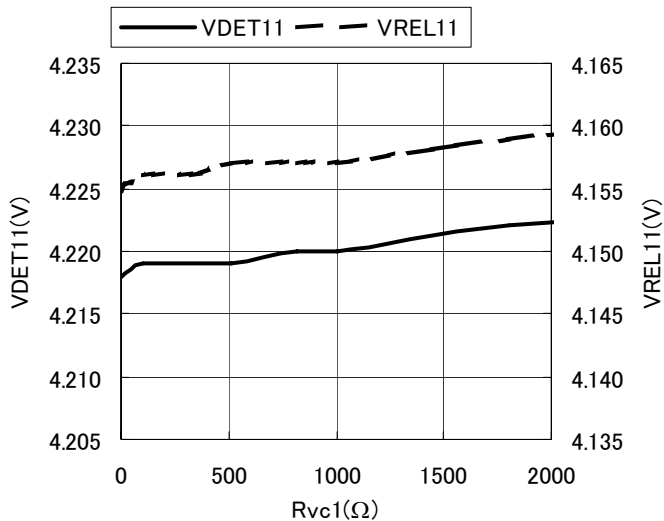
Over-discharge/Released from over-discharge vs. R1 (Cell1)

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PACKAGE DIMENSIONS

● **SSOP-16P (0.65mm pitch)**

Unit: mm

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RoHS Compliant
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Ricoh is committed to reducing the environmental loading materials in electrical devices with a view to contributing to the protection of human health and the environment.
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