MAX40007

nanoPower Op Amp in Ultra-Tiny WLP and SOT23 Packages

General Description

The MAX40007 is a single operational amplifier that provides a maximized ratio of gain bandwidth (GBW) to supply current and is ideal for battery-powered applications such as portable instrumentation, portable medical equipment, and wireless handsets.

This CMOS op amp features an ultra-low supply current of only 700nA (typ), ground-sensing inputs, and rail-to-rail outputs; operating from a single 1.7V to 5.5V supply, allowing the amplifier to be powered by the same 1.8V, 2.5V, or 3.3V nominal supply that powers the microcontroller. The MAX40007 amplifier is unity-gain stable with a 20kHz GBW product.

The ultra-low supply current, low operating voltage, and rail-to-rail output capabilities make this operational amplifier ideal for use in single lithium ion (Li+), two-cell NiCd or alkaline battery systems.

The MAX40007 is available in a 6-pin SOT23 package and an ultra-tiny 6-bump, 1.1mm x 0.76mm wafer-level package (WLP) with a bump pitch of 0.35mm. The amplifier is specified over the -40°C to 125°C operating temperature range.

Applications

- Fitness Wearables
- Mobile Phones
- Notebook and Tablet Computers
- Portable Medical Devices
- Portable Instrumentation

Benefits and Features

- Ultra-Low-Power Preserves Battery Life
  - 700nA Typical Supply Current
- Single 1.7V to 5.5V Supply Voltage Range
  - Amplifier Can be Powered From the Same 1.8V/2.5V/3.3V/5V System Rails
- Tiny Packages Save Board Space
  - 1.1mm x 0.76mm WLP-6 with 0.35mm Bump Pitch
  - SOT23-6 Package
- Precision Specifications for Buffer/Filter/Gain Stages
  - Low 300μV Input Offset Voltage
  - Rail-to-Rail Output Voltage
  - 20kHz BW
  - Low 40pA Input Bias Current
  - Unity-Gain Stable
- -40°C to 125°C Temperature Range

***Ordering Information* appears at end of data sheet.**

19-8735; Rev 1; 1/18

Absolute Maximum Ratings

V_{DD} to V_{SS} .... -0.3V to +6V
IN+, IN- to V_{SS} .... V_{SS} -0.3V to V_{DD} + 0.3V
IN+ to IN- .... ±V_{DD}
OUT to V_{SS} .... V_{SS} -0.3V to V_{DD} + 0.3V
Continuous Current Into Any Input Pin .... ±10mA
Continuous Current Into Output Pin .... ±30mA
Output Short-Circuit Duration to V_{DD} or V_{SS} 10s

Continuous Power Dissipation (T_A = +70°C)
- 6-Bump WLP (derate 10.19mW/°C at 70°C) 816mW
- SOT23-6 (derate 4.30mW/°C at 70°C) 347.80mW

Operating Temperature Range .... -40°C to +125°C
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

WLP
- Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 98.06°C/W

SOT23
- Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 230°C/W
- Junction-to-Case Thermal Resistance (θ_{JC}) .... 76°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

V_{DD} = +3V, V_{SS} = 0V, V_{CM} = 0.5V, V_{OUT} = V_{DD}/2, R_L = 1MΩ to V_{DD}/2, **T_A = +25°C**, unless otherwise noted. (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSRR tests		1.7		5.5	V
Supply Current	I_{DD}	At 25°C			0.7	0.9	µA
Input Offset Voltage	V_{OS}	V_{SS} - 0.1V < CMIR < V_{DD} - 1.1V			±0.3	±1.3	mV
Input Bias Current (Note 3)	I_B				±40	±100	pA
Input Offset Current (Note 3)	I_{OS}				±5	±50	pA
Input Capacitance		Either input, over entire common mode range			1.5		pF
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by the CMRR test		V_{SS} - 0.1V		V_{DD} -1.1	V
Common-Mode Rejection Ratio	CMRR	DC, (V_{SS} - 0.1) ≤ V_{CM} ≤ (V_{DD} - 1.1V)		70	92		dB
		AC, 100mV_{PP} 1kHz, with output at V_{DD}/2			72		
Power-Supply Rejection Ratio	PSRR	DC, +1.7V ≤ V_{DD} ≤ +5.5V		75	100		dB
		AC, 100mV_{PP} 1kHz, superimposed on V_{DD}/2			75		
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = V_{SS} + 25mV to V_{DD} - 25mV		75	110		dB
Output Voltage Swing	V_{OH}	Swing high specified as $V_{DD} - V_{OUT}$	R_L = 100kΩ		3.2	8	mV
			R_L = 10kΩ		32	70	
	V_{OL}	Swing low specified as V_{OUT} - V_{SS}	R_L = 100kΩ		2.9	8	
			R_L = 10kΩ		27	70	
Gain-Bandwidth Product	GBW	A_V = 1, C_L = 20pF			15		kHz
Phase Margin	φM	C_L = 20pF			56		°

Electrical Characteristics (continued)

V_{DD} = +3V, V_{SS} = 0V, V_{CM} = 0.5V, V_{OUT} = V_{DD}/2, R_L = 1MΩ to V_{DD}/2, **T_A = +25°C**, unless otherwise noted. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slew Rate	SR	V_{OUT} = 1V_{P-P} step, A_V = 1V/V		12		V/ms
Settling Time		100mV step, 0.1% settling, A_V = 1		74		μs
Input Voltage Noise	e_n	f = 1kHz		513		nV/√Hz
Input Current Noise	i_n	f = 1kHz		0.004		pA/√Hz
Output Short-Circuit Current		Shorted to V_{SS} (sourcing)		10		mA
		Shorted to V_{DD} (sinking)		10		mA
Power-On Time	t_{ON}			0.13		ms
Stable Capacitive Load	C_L	No sustained oscillations		20		pF

Electrical Characteristics

V_{DD} = +3V, V_{SS} = 0V, V_{CM} = 0.5V, V_{OUT} = V_{DD}/2, R_L = 1MΩ to V_{DD}/2, **T_A = +40°C to +125°C**, unless otherwise noted. (Note 2)

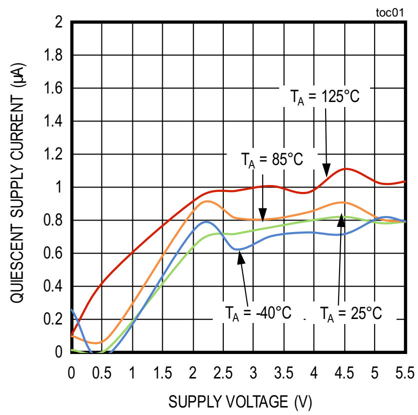
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSRR tests		1.7		5.5	V
Supply Current	I_{DD}	T_A = -40°C to 85°C				1.2	μA
		T_A = -40°C to 125°C				1.4	
Input Offset Voltage	V_{OS}	T_A = -40°C to 125°C				±4.5	mV
Input Offset Voltage Temperature Coefficient	TCV_{OS}				6.4	36.6	μV/°C
Input Bias Current (Note 3)	I_B				0.7	7	nA
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by the CMRR test		V_{SS} - 0.1		V_{DD} -1.1	V
Common-Mode Rejection Ratio	CMRR	DC, (V_{SS} - 0.1) ≤ V_{CM} ≤ (V_{DD} - 1.1V)		70			dB
		AC, 100mV_{P-P} 1kHz, with output at V_{DD}/2			63		
Power-Supply Rejection Ratio	PSRR	+1.7V ≤ V_{DD} ≤ +5.5V, -40°C ≤ T_A ≤ +125°C		75			dB
		AC, 100mV_{P-P} 1kHz, superimposed on V_{DD}			40		
Large-Signal Voltage Gain	A_{VOL}	V_{OUT} = 50mV to V_{DD} - 50mV, R_L = 1MΩ		75			dB
Output Voltage Swing	V_{OH}	Swing high specified as V_{DD} - V_{OUT}	R_L = 100kΩ		8		mV
			R_L = 10kΩ		70		
	V_{OL}	Swing low specified as V_{OUT} - V_{SS}	R_L = 100kΩ		8		
			R_L = 10kΩ		70		

Note 2: All devices are production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 3: Guaranteed by design and bench characterization.

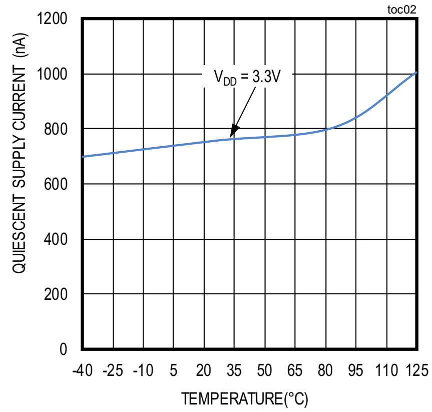
Typical Operating Characteristics

(V_{DD} = +3V, V_{SS} = 0V, V_{CM} = 0V, R_L = 100kΩ to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

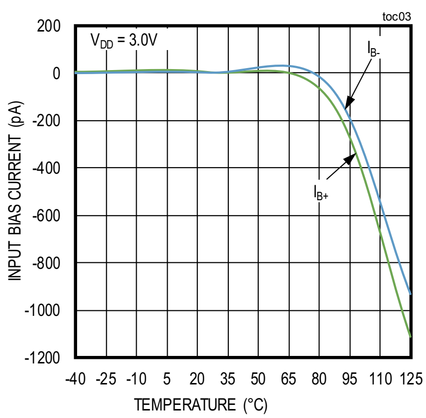
SUPPLY CURRENT vs. SUPPLY VOLTAGE



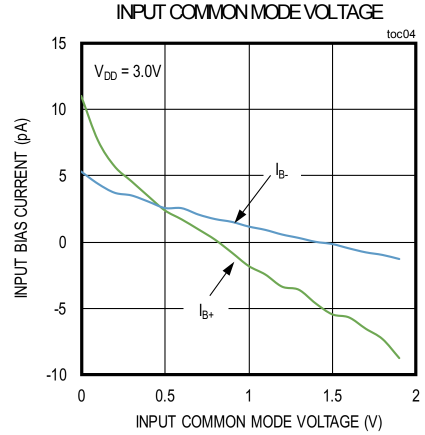
SUPPLY CURRENT
vs. TEMPERATURE



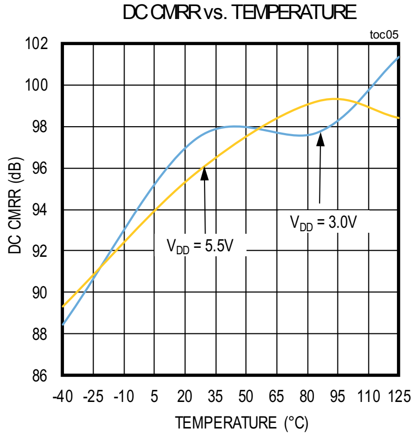
INPUT BIAS CURRENTS vs. TEMPERATURE



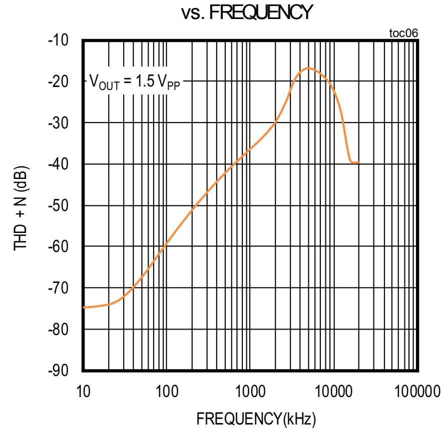
INPUT BIAS CURRENTS vs.
INPUT COMMON MODE VOLTAGE



DC CMRR vs. TEMPERATURE

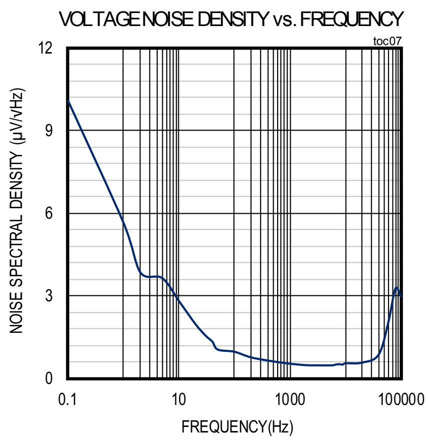


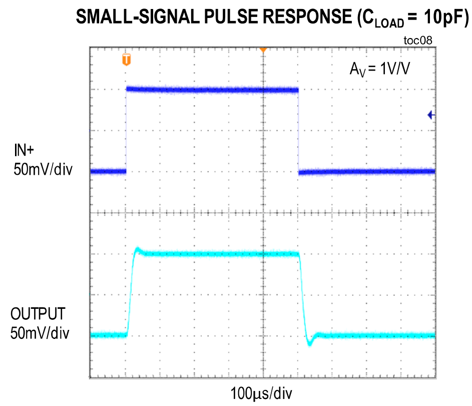
TOTAL HARMONIC DISTORTION PLUS NOISE
vs. FREQUENCY

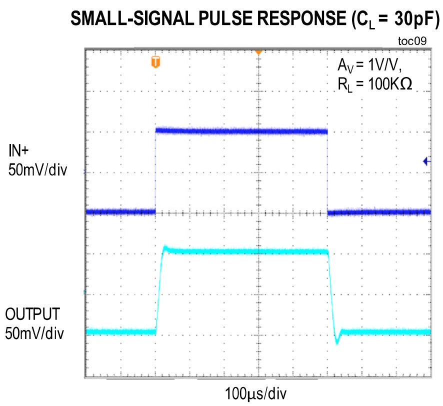


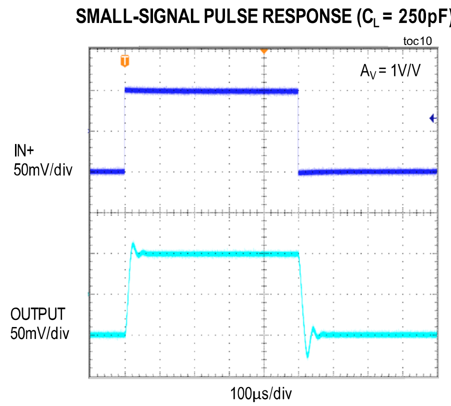
Typical Operating Characteristics (continued)

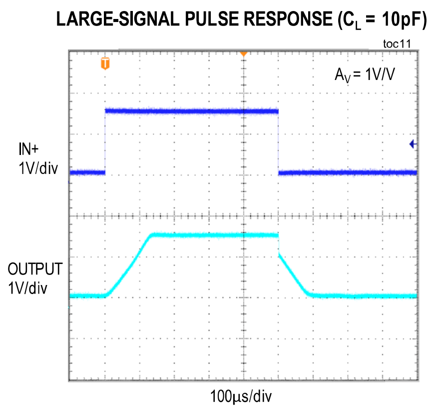
(V_{DD} = +3V, V_{SS} = 0V, V_{CM} = 0V, R_L = 100kΩ to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

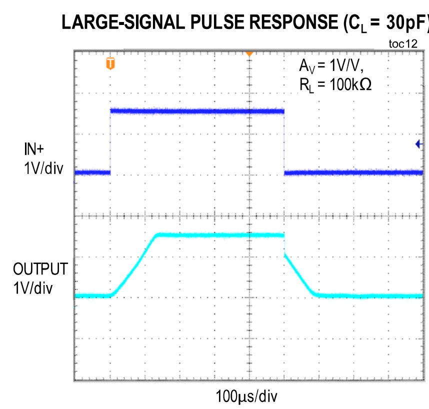






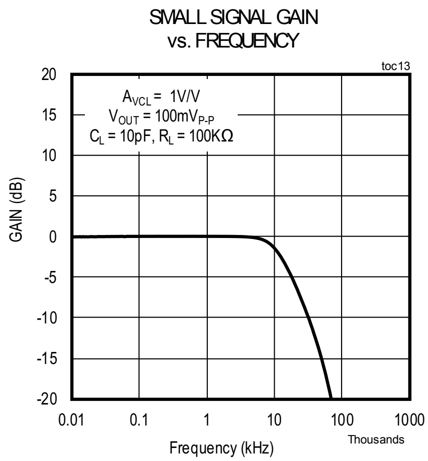


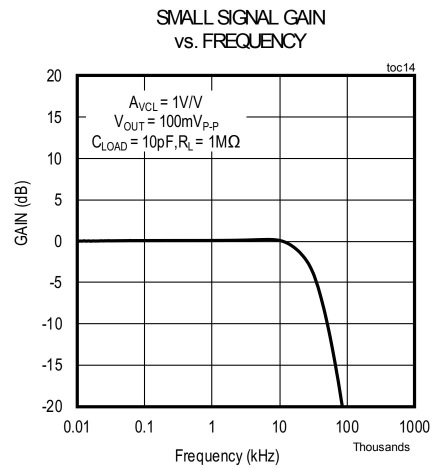


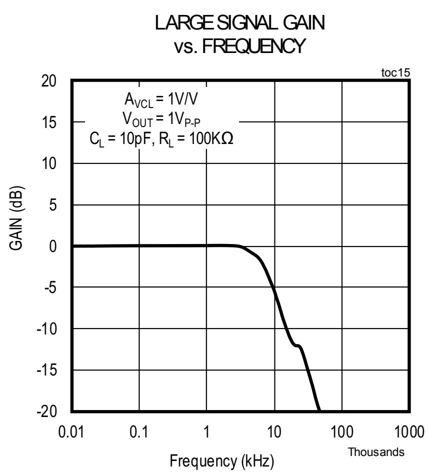


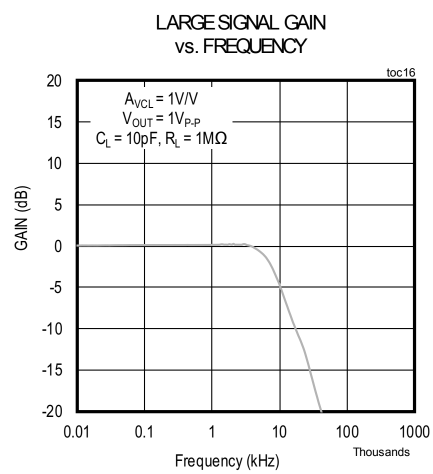
Typical Operating Characteristics (continued)

(V_{DD} = +3V, V_{SS} = 0V, V_{CM} = 0V, R_L = 100kΩ to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

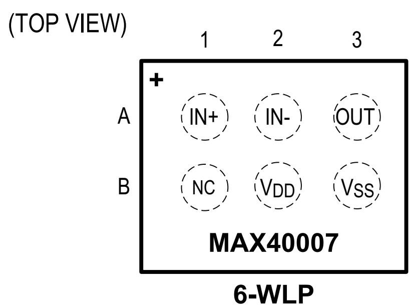


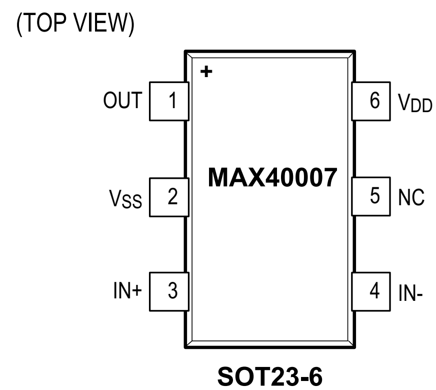






Pin Configurations

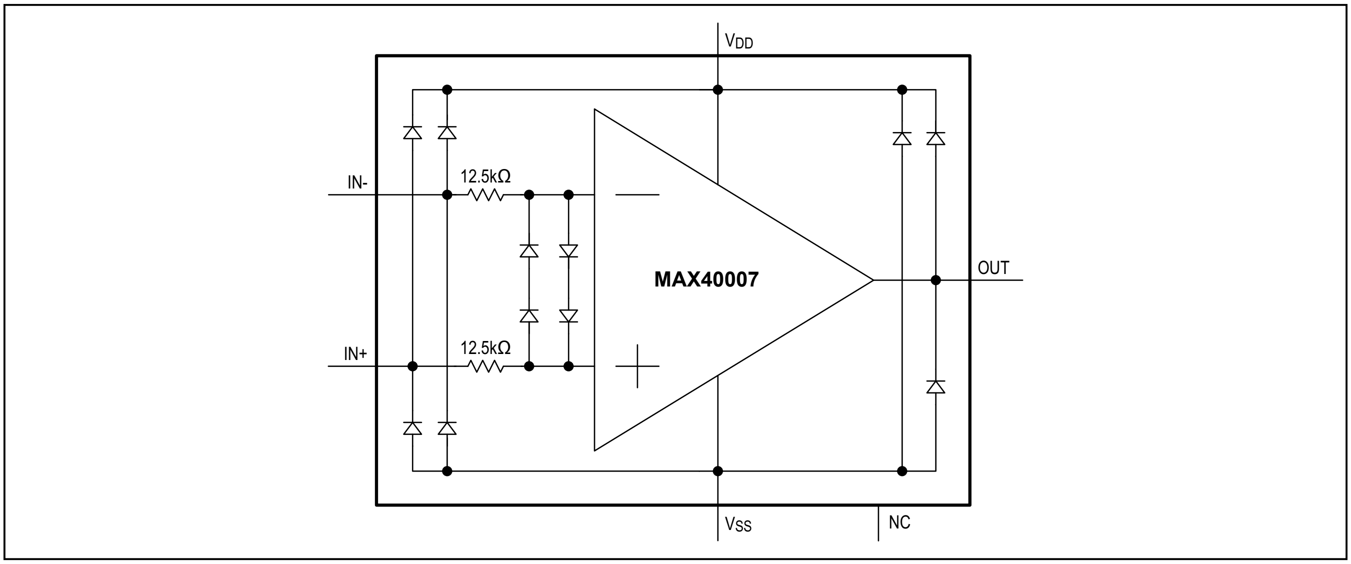




Pin Description

BUMP (WLP)	6-SOT23	NAME	FUNCTION
A1	3	IN+	Non-Inverting Amplifier Input.
A2	4	IN-	Inverting Amplifier Input.
A3	1	OUT	Amplifier Output.
B1	5	NC	No Connection. Internally connected.
B2	6	V_{DD}	Positive Power Supply Input.
B3	2	V_{SS}	Negative Power Supply Input. Connect V_{SS} to 0V in single-supply application.

Functional (or Block) Diagram



Detailed Description

The MAX40007 is an ultra-low-power op amp ideal for battery-powered applications and features a maximized ratio of GBW to supply current, low operating supply voltage, and low input bias current. The MAX40007 is ideal for general-purpose, low-current, low-voltage continuously powered portable applications. The MAX40007 consumes an ultra-low 700nA (typ) supply current and has a 0.3mV (typ) offset voltage. This device is unity-gain stable with a 20kHz GBW product, driving capacitive loads up to 20pF.

Applications Information

Ground Sensing

The common-mode input range of the MAX40007 extends down to V_{SS}, and offers excellent common-mode rejection. This op amp is guaranteed not to exhibit phase reversal when either input is overdriven.

Power Supplies and Layout

The MAX40007 operates from a single +1.7V to +5.5V power supply. Bypass the power supplies with a 0.1μF ceramic capacitor placed close to V_{DD} and V_{SS} pins. Adding a solid Ground plane improves performance generally by decreasing the noise at the op amp's inputs However, in very high impedance circuits, it may be worth removing the ground plane under the IN- pin to reduce the stray capacitance and help avoid reducing the phase margin. To further decrease stray capacitance, minimize PCB lengths and resistor leads, and place external components close to the amplifier's pins.

Input Differential Voltage Protection

The MAX40007's inputs are protected from large differential voltages by the network shown in Figure 1. This is done to prevent gradual degradation of the input offset voltage. In normal operation, the amplifier inputs are at almost the same voltage at all times so these components are transparent to normal operation. Using this amplifier as a comparator, however, is not recommended—the inputs will start to draw "bias current' when the differential voltage exceeds about 1V. While this will not damage the amplifier in any way, it is not usually a desirable feature for a comparator. Maxim does make comparators with similar speed and power performance as these amplifiers, such as the MAX40002/3/4/5.

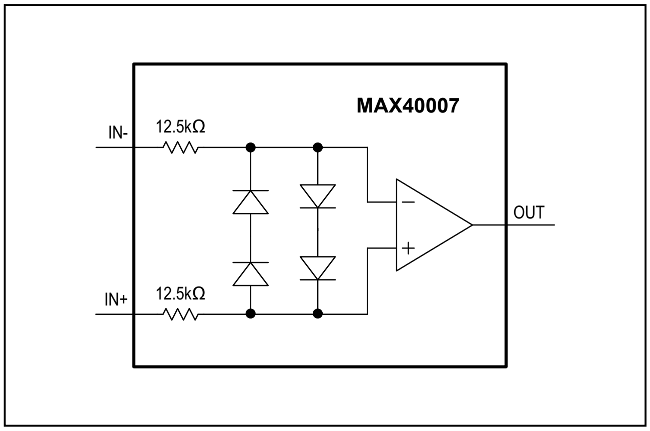


Figure 1. Input Protection Scheme

Stability

This MAX40007 maintains stability in its minimum gain configuration while driving capacitive loads up to 20pF or so. Larger capacitive loading is achieved using the techniques described in the Capacitive Load Stability section below.

Although this amplifier is primarily designed for low-frequency applications, good layout can still be extremely important, especially if very high-value resistors are being used—as is likely in ultra-low-power circuitry. However, some stray capacitance may be unavoidable; and it may be necessary to add a 2pF to 10pF capacitor across the feedback resistor, as shown in Figure 2. Select the smallest capacitor value that ensures stability so that BW and settling time are not significantly impacted.

Capacitive Load Stability

Driving large capacitive loads can cause instability in amplifiers. The MAX40007 is stable with capacitive loads up to 20pF. Stability with higher capacitive loads can be achieved by adding an isolation resistor in series with the op-amp output as shown in Figure 2 below. This resistor improves the circuit's phase margin by isolating the load capacitor from the amplifier's inverting input. The graph in the *Typical Operating Characteristics* gives the stable operation region for capacitive load versus isolation resistors.

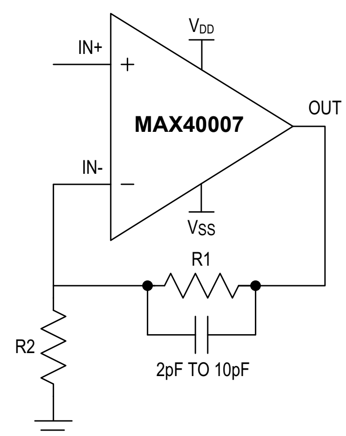


Figure 2. Compensation for Feedback Node Capacitance

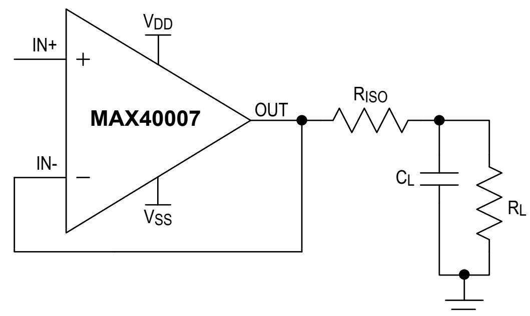


Figure 3. R_{ISO} Improving Capacitive Load Drive Capability of Op Amp

Ordering Information

PART	TEMP RANGE	PIN PACKAGE	TOP MARK
MAX40007ANT+	-40°C to +125°C	6-WLP	+2
MAX40007AUT+	-40°C to +125°C	6-SOT23	+ACUV

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6-WLP	N60D1+1	**21-100086**	Refer to **Application Note 1891**
6-SOT23	U6+1	**21-0058**	**90-0175**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/16	Initial release	—
1	1/18	Updated *Ordering Informaiton* table	9

