GaAs, pHEMT, MMIC, 1/2 W, 18 GHz to 44 GHz, Power Amplifier

Data Sheet **ADPA7002**

FEATURES

Output P1dB: 28 dBm (typical at 34 GHz to 44 GHz)
P_{SAT}: 29.5 dBm (typical at 24 GHz to 34 GHz)
Gain: 15 dB (typical at 34 GHz to 44 GHz)
IP3: 38 dBm (typical)
Integrated power detector
Supply voltage: 5 V at 700 mA
16-terminal, 6 mm × 6 mm, ceramic, high frequency, air cavity package

APPLICATIONS

Military
Test instrumentation
Communications

FUNCTIONAL BLOCK DIAGRAM

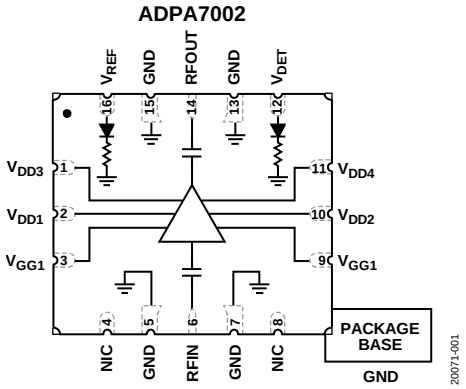

Figure 1.

GENERAL DESCRIPTION

The ADPA7002 is a gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC), 28 dBm (1/2 W) power amplifier, with an integrated temperature compensated on-chip power detector that operates between 18 GHz and 44 GHz. The ADPA7002 provides 15 dB of small signal gain and 30 dBm of saturated output power (P_{SAT}) at 32 GHz from a 5 V supply. With an IP3 of 38 dBm, the ADPA7002 is ideal for linear applications such as electronic countermeasure and instrumentation applications demanding >28 dBm of efficient P_{SAT}. The RF inputs and outputs are internally matched and dc blocked for ease of integration into higher level assemblies. The ADPA7002 is housed in a 6 mm × 6 mm, ceramic leadless chip with heat sink (LCC_HS) that exhibits low thermal resistance and is compatible with surface-mount manufacturing techniques.

Rev. 0 **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **Technical Support** **www.analog.com**

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REVISION HISTORY

12/2019—Revision 0: Initial Version

SPECIFICATIONS

18 GHz TO 20 GHz FREQUENCY RANGE

T_A = 25°C, drain voltage (V_{DD}) = 5 V, and quiescent drain current (I_{DQ}) = 700 mA for nominal operation, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		18		20	GHz	
GAIN			15		dB	
Flatness			±0.5		dB	
Variation over Temperature			0.026		dB/°C	
NOISE FIGURE			11		dB	
RETURN LOSS						
Input			8		dB	
Output			13		dB	
OUTPUT						
Power for 1 dB Compression	P1dB		25.5		dBm	
Saturated Output Power	P_{SAT}		27.5		dBm	
Third-Order Intercept	IP3		36.5		dBm	Measurement taken at output power (P_{OUT}) per tone = 12 dBm
POWER ADDED EFFICIENCY	PAE		12.5		%	Measured at P_{SAT}
SUPPLY						
Quiescent Drain Current	I_{DQ}		700		mA	Adjust V_{GG1} between −1.5 V to 0 V to achieve the desired I_{DQ}
Drain Voltage	V_{DD}	4	5		V	

20 GHz TO 24 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 700 mA for nominal operation, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		20		24	GHz	
GAIN		15	17		dB	
Flatness			±0.5		dB	
Variation over Temperature			0.026		dB/°C	
NOISE FIGURE			8		dB	
RETURN LOSS						
Input			12		dB	
Output			12		dB	
OUTPUT						
Power for 1 dB Compression	P1dB	24	27		dBm	
Saturated Output Power	P_{SAT}		28.5		dBm	
Third-Order Intercept	IP3		37		dBm	Measurement taken at P_{OUT} per tone = 12 dBm
POWER ADDED EFFICIENCY	PAE		14		%	Measured at P_{SAT}
SUPPLY						
Quiescent Drain Current	I_{DQ}		700		mA	Adjust V_{GG1} between −1.5 V to 0 V to achieve the desired I_{DQ}
Drain Voltage	V_{DD}	4	5		V	

24 GHz TO 34 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 700 mA for nominal operation, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		24		34	GHz	
GAIN		15	17		dB	
Flatness			±0.7		dB	
Variation over Temperature			0.012		dB/°C	
NOISE FIGURE			5.8		dB	
RETURN LOSS						
Input			14		dB	
Output			14		dB	
OUTPUT						
Power for 1 dB Compression	P1dB	24.5	28		dBm	
Saturated Output Power	P_{SAT}		29.5		dBm	
Third-Order Intercept	IP3		38		dBm	Measurement taken at P_{OUT} per tone = 12 dBm
POWER ADDED EFFICIENCY	PAE		16		%	Measured at P_{SAT}
SUPPLY						
Quiescent Drain Current	I_{DQ}		700		mA	Adjust V_{GG1} between −1.5 V to 0 V to achieve the desired I_{DQ}
Drain Voltage	V_{DD}	4	5		V	

34 GHz TO 44 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 700 mA for nominal operation, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		34		44	GHz	
GAIN		13.5	15.5		dB	
Flatness			±0.9		dB	
Variation over Temperature			0.024		dB/°C	
NOISE FIGURE			5		dB	
RETURN LOSS						
Input			15		dB	
Output			16		dB	
OUTPUT						
Power for 1 dB Compression	P1dB	24	27		dBm	
Saturated Output Power	P_{SAT}		28.5		dBm	
Third-Order Intercept	IP3		38.5		dBm	Measurement taken at P_{OUT} per tone = 12 dBm
POWER ADDED EFFICIENCY	PAE		10		%	Measured at P_{SAT}
SUPPLY						
Quiescent Drain Current	I_{DQ}		700		mA	Adjust V_{GG1} between −1.5 V to 0 V to achieve the desired I_{DQ}
Drain Voltage	V_{DD}	4	5		V	

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_{DDX}	6.0 V
V_{GG1}	−1.6 V to 0 V
RF Input Power (RFIN)	25 dBm
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derate 69 mW/°C above 85°C)	6.21 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−40°C to +85°C
Nominal Junction (T_A = 85°C, V_{DD} = 5 V, I_{DQ} = 700 mA)	135.75°C
Junction to Maintain 1,000,000 Hour Mean Time to Failure (MTTF)	175°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	Class 1A (passed 500 V)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 6. Thermal Resistance

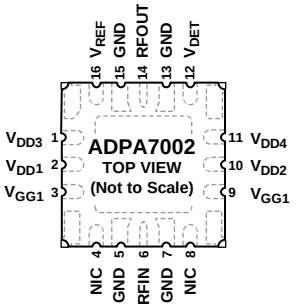
Package Type	θ_{JC}	Unit
EH-16-1[1]	14.5	°C/W

[1] Thermal resistance (θ_{JC}) is determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel, through the ground pin, to the PCB, and the ground pin is held constant at the operating temperature of 85°C.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NO INTERNAL CONNECTION. THESE PINS HAVE NO INTERNAL CONNECTIONS. CONNECT TO GROUND.
2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO RF AND DC GROUND.

20071-002

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 10, 11	V_{DD3}, V_{DD1}, V_{DD2}, V_{DD4}	Drain Biases. External bypass capacitors are required.
3, 9	V_{GG1}	Gate Bias Controls. External bypass capacitors are required.
4, 8	NIC	No Internal Connection. These pins have no internal connections. Connect to ground.
5, 7, 13, 15	GND	Ground. These pins must be connected to RF and dc ground.
6	RFIN	RF Signal Input. This pin is ac-coupled and matched to 50 Ω.
12	V_{DET}	Detector Diode to Measure RF Output Power. Output power detection via this pin requires the application of a dc bias voltage through an external series resistor. Used in combination with the V_{REF} pin, the difference voltage ($V_{REF} - V_{DET}$) is a temperature compensated dc voltage that is proportional to the RF output power.
14	RFOUT	RF Signal Output. This pin is ac-coupled and matched to 50 Ω.
16	V_{REF}	Reference Diode for Temperature Compensation of V_{DET} RF Output Power Measurements.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

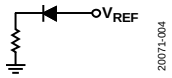


Figure 4. V_{REF} Interface Schematic

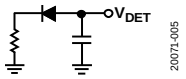


Figure 5. V_{DET} Interface Schematic

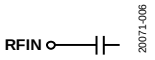


Figure 6. RFIN Interface Schematic

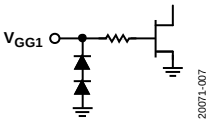


Figure 7. V_{GG1} Schematic

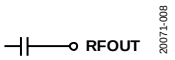


Figure 8. RFOUT Interface Schematic

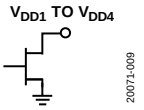


Figure 9. V_{DD1} to V_{DD4} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

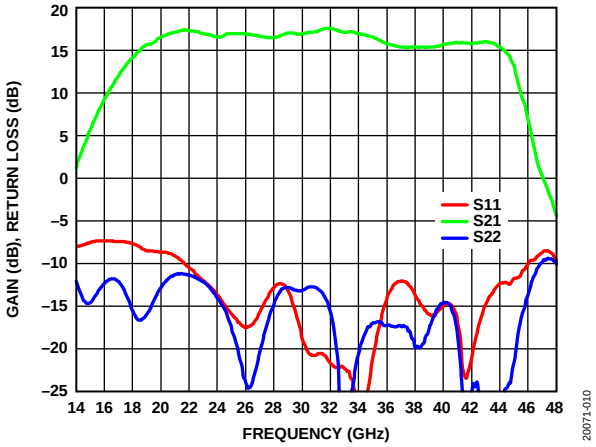


Figure 10. Gain and Return Loss vs. Frequency

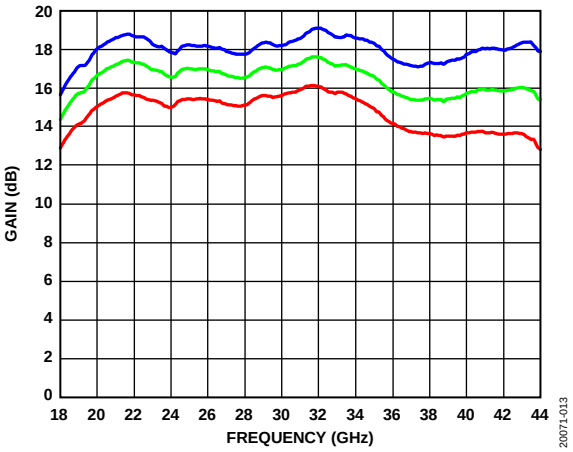


Figure 13. Gain vs. Frequency for Various Temperatures

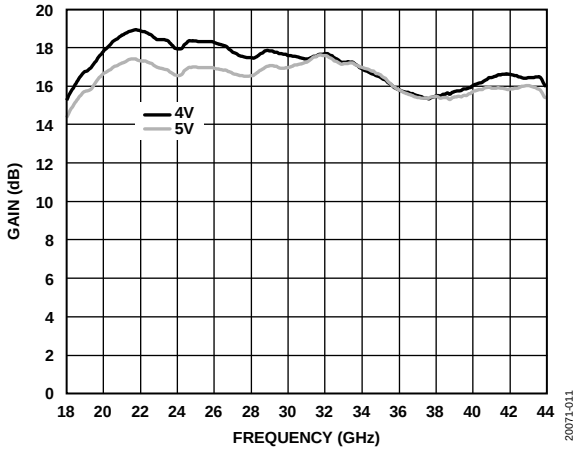


Figure 11. Gain vs. Frequency for Various Drain Voltages

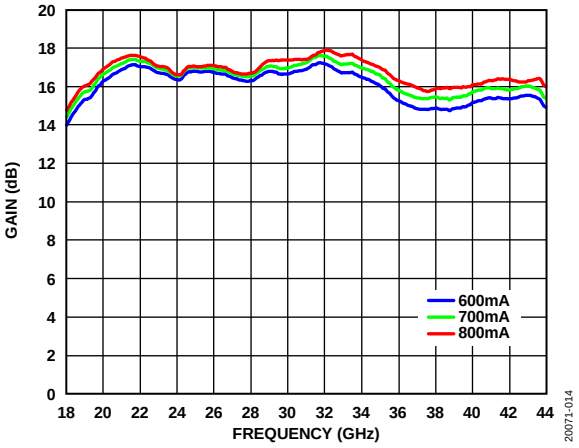


Figure 14. Gain vs. Frequency for Various Quiescent Drain Currents

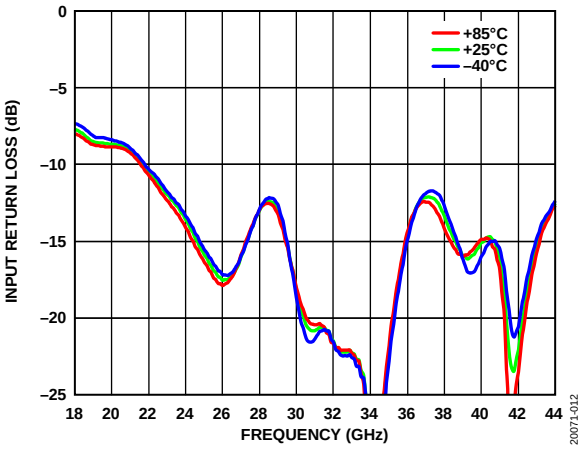


Figure 12. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 700 mA

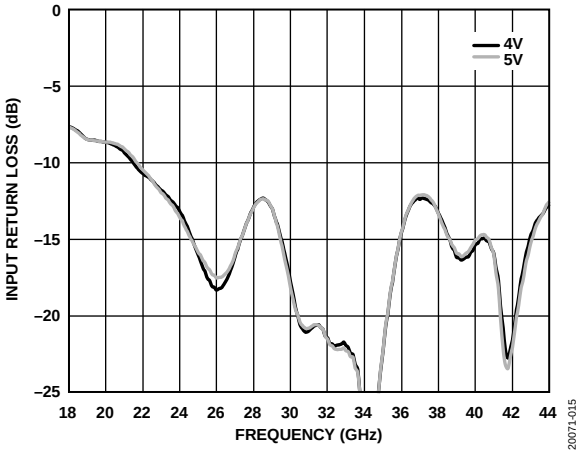


Figure 15. Input Return Loss vs. Frequency for Various Drain Voltages

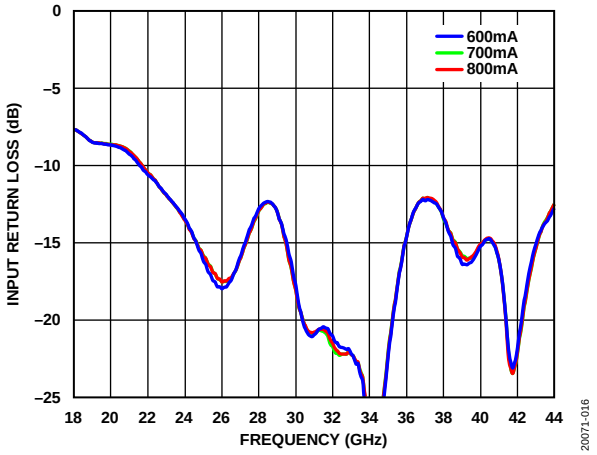


Figure 16. Input Return Loss vs. Frequency for Various Quiescent Drain Currents

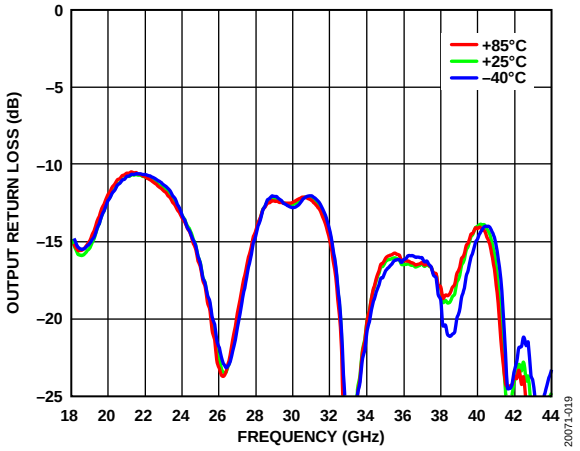


Figure 19. Output Return Loss vs. Frequency for Various Temperatures

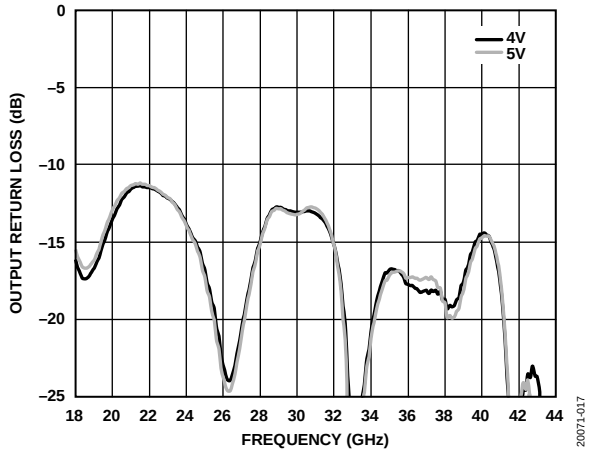


Figure 17. Output Return Loss vs. Frequency for Various Drain Voltages

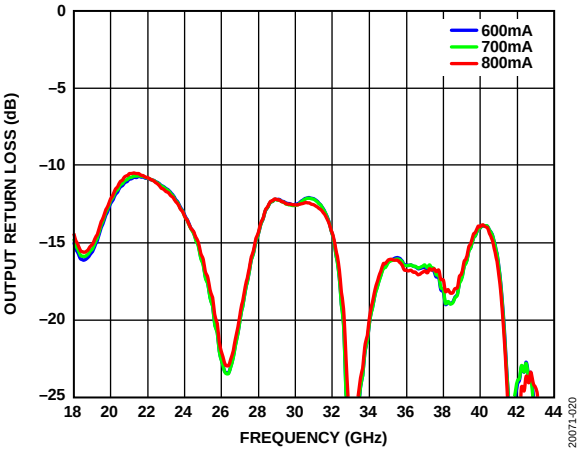


Figure 20. Output Return Loss vs. Frequency for Various Quiescent Drain Currents

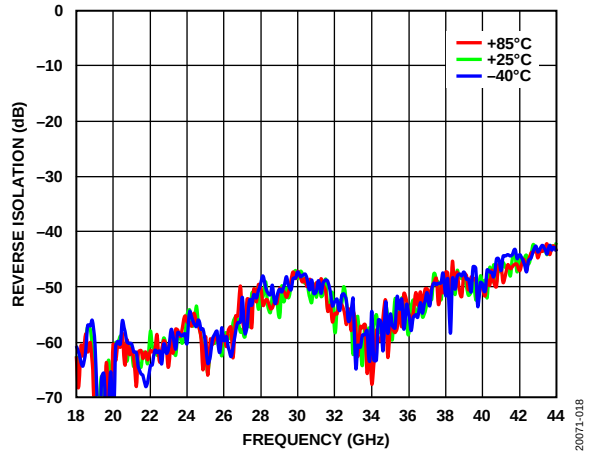


Figure 18. Reverse Isolation vs. Frequency for Various Temperatures

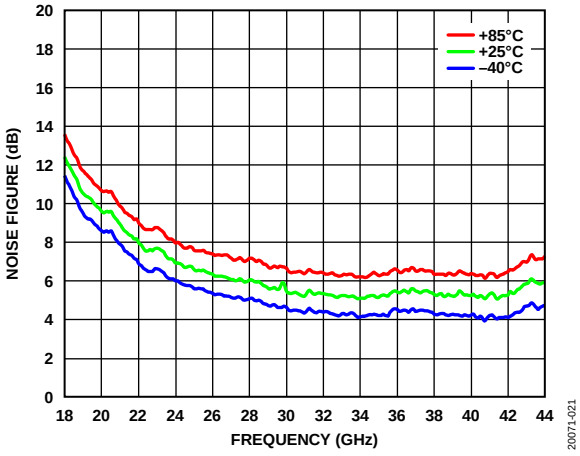


Figure 21. Noise Figure vs. Frequency for Various Temperatures

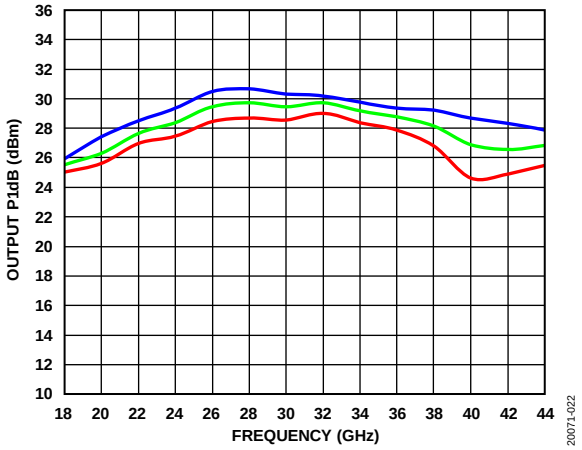


Figure 22. Output P1dB vs. Frequency for Various Temperatures

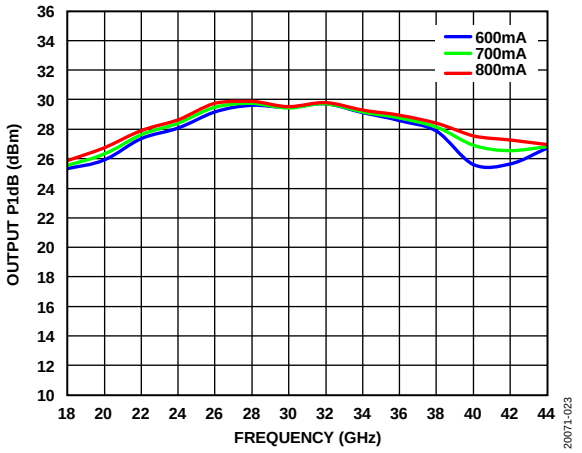


Figure 23. Output P1dB vs. Frequency for Various Currents

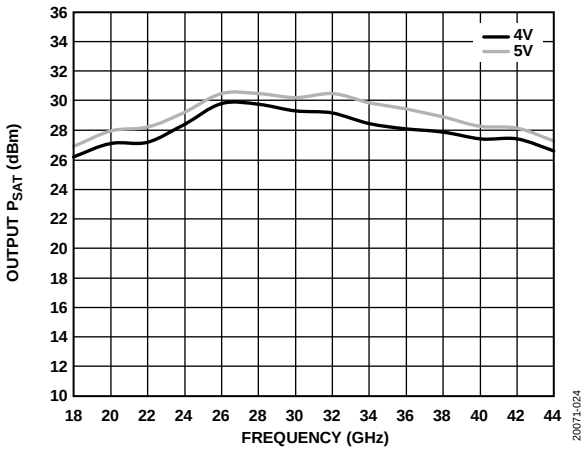


Figure 24. Output P_{SAT} vs. Frequency for Various Drain Voltages

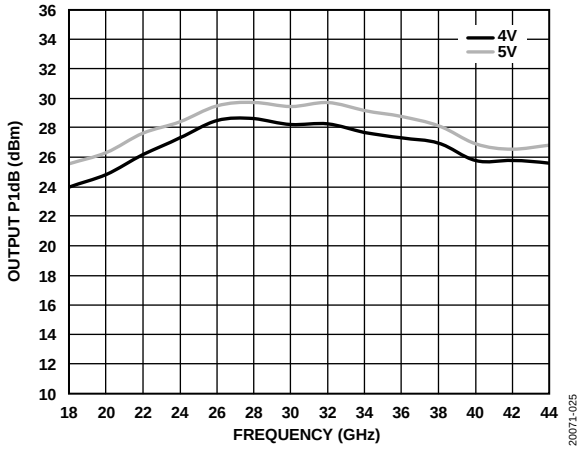


Figure 25. Output P1dB vs. Frequency for Various Drain Voltages

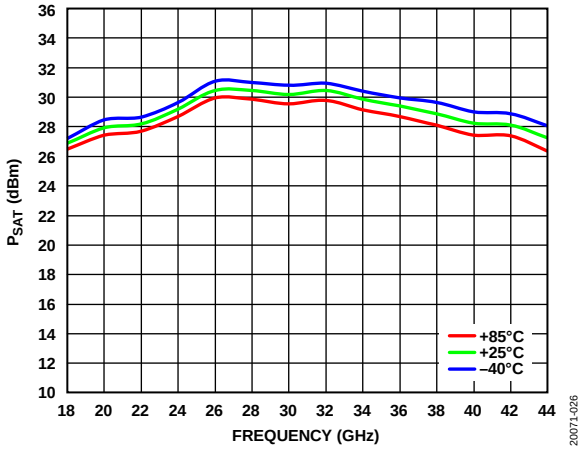


Figure 26. P_{SAT} vs. Frequency for Various Temperatures

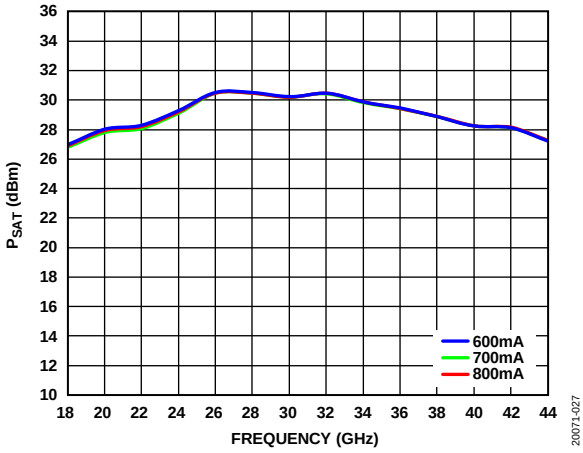


Figure 27. P_{SAT} vs. Frequency for Various Quiescent Drain Currents

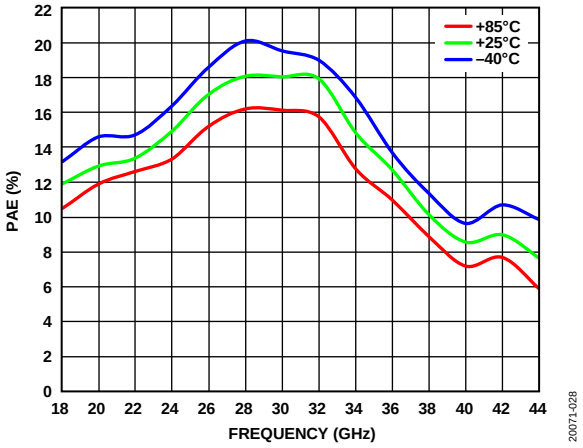


Figure 28. PAE vs. Frequency over Temperature, PAE Measured at P_{SAT}

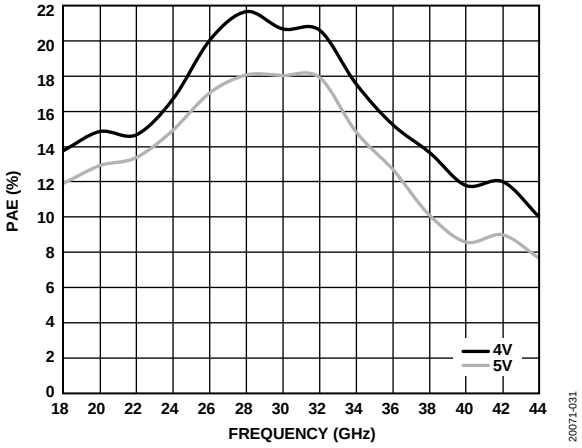


Figure 31. PAE vs. Frequency for Various Drain Voltages, PAE Measured at P_{SAT}

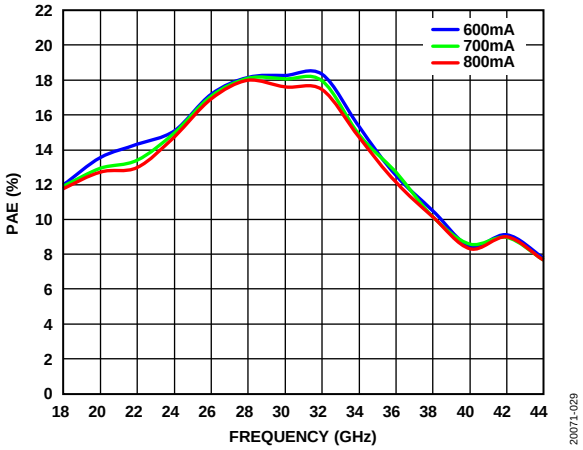


Figure 29. PAE vs. Frequency for Various Quiescent Drain Currents, PAE Measured at P_{SAT}

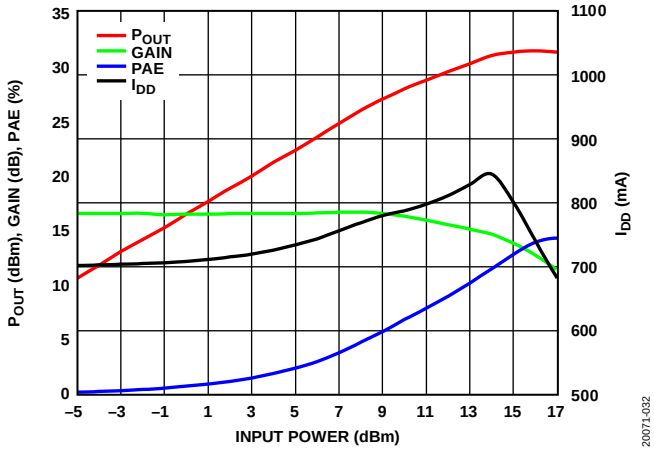


Figure 32. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, Frequency = 22 GHz

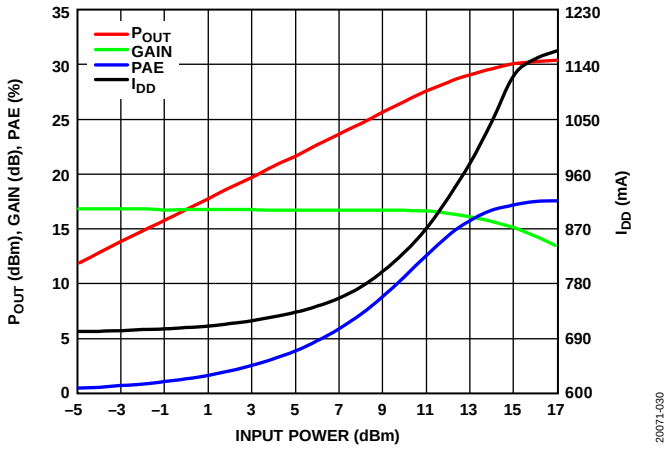


Figure 30. P_{OUT}, Gain, PAE, and Drain Currents (I_{DD}) vs. Input Power, Frequency = 26 GHz

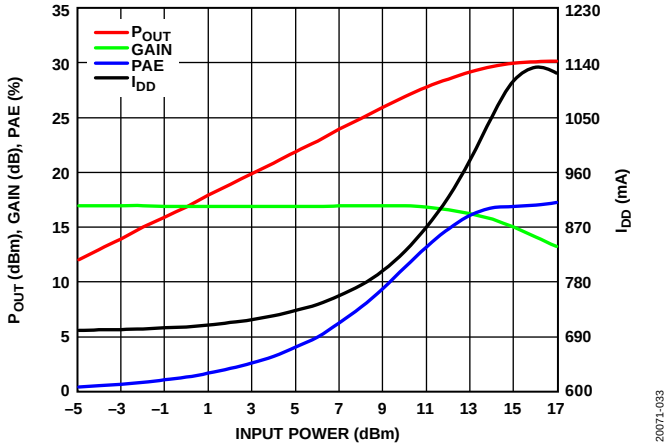


Figure 33. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, Frequency = 30 GHz

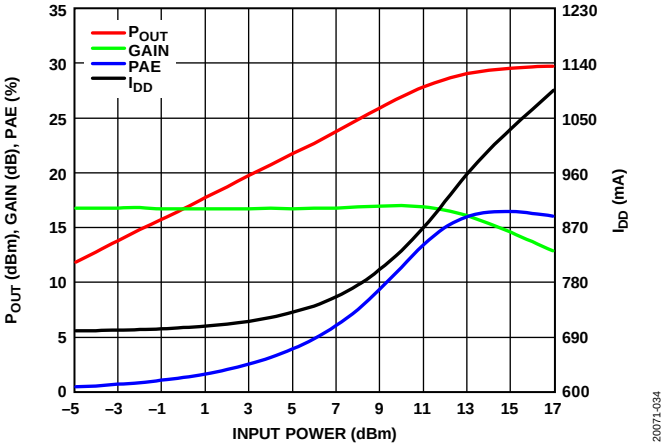


Figure 34. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, Frequency = 34 GHz

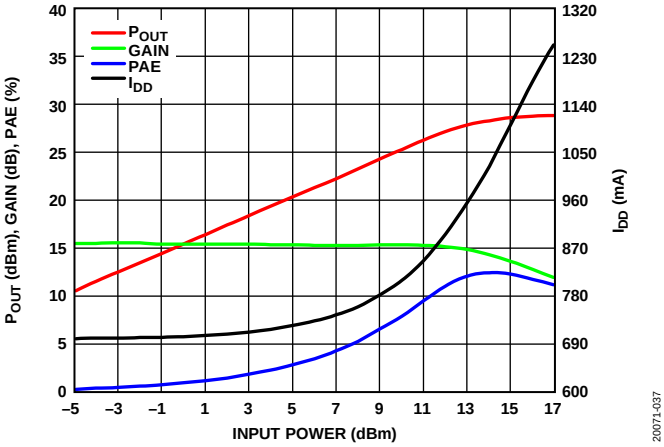


Figure 37. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, Frequency = 38 GHz

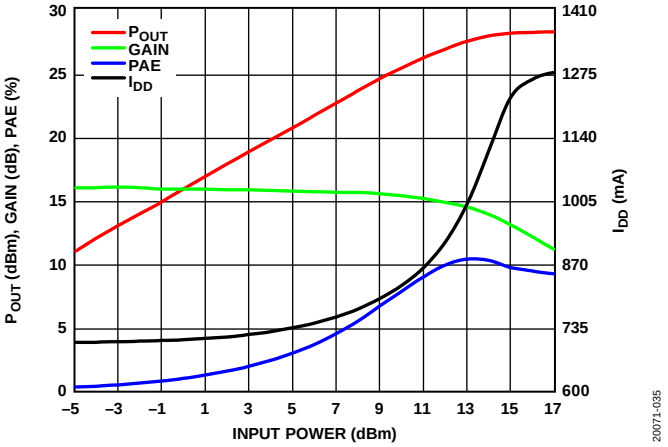


Figure 35. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, Frequency = 42 GHz

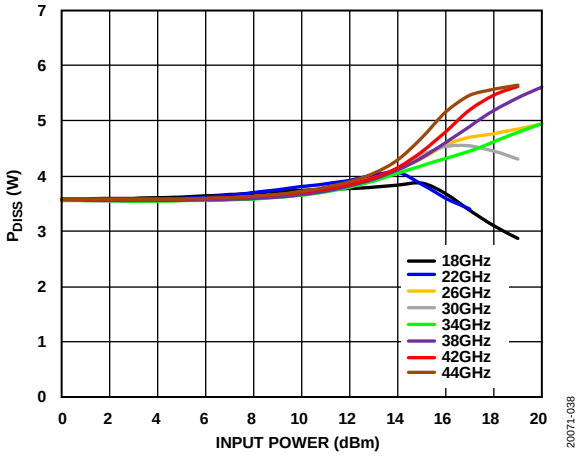


Figure 38. P_{DISS} vs. Input Power, T_A = 85°C

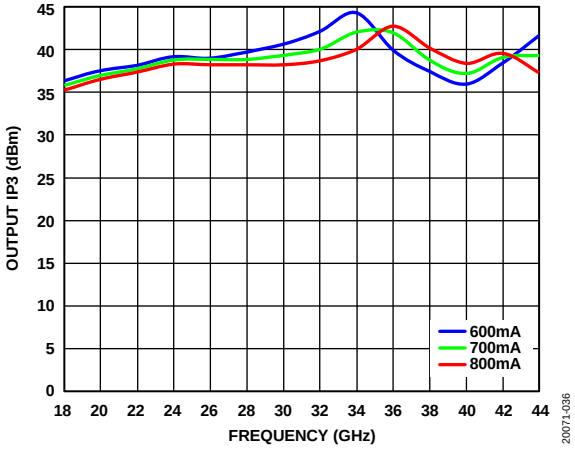


Figure 36. Output IP3 vs. Frequency for Various Drain Currents, P_{OUT} per Tone = 12 dBm

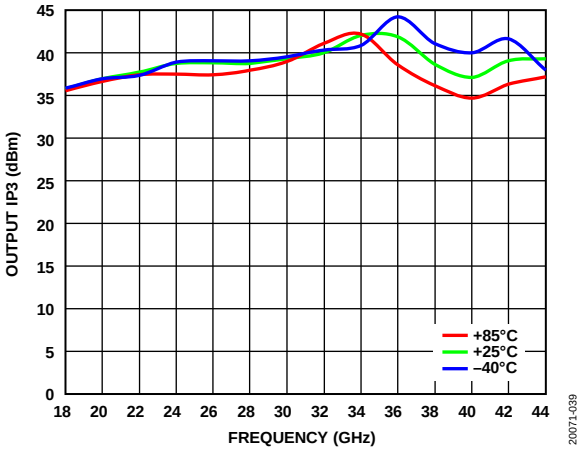


Figure 39. Output IP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 12 dBm, I_{DD} = 700 mA

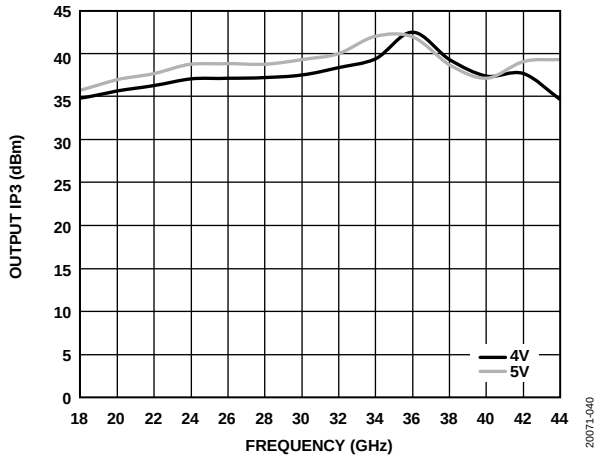


Figure 40. Output IP3 vs. Frequency for Various Drain Voltages, P_{OUT} per Tone = 12 dBm

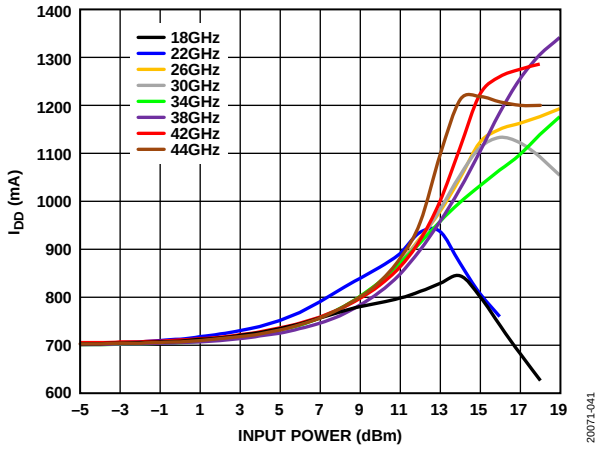


Figure 41. I_{DD} vs. Input Power over Various Frequencies

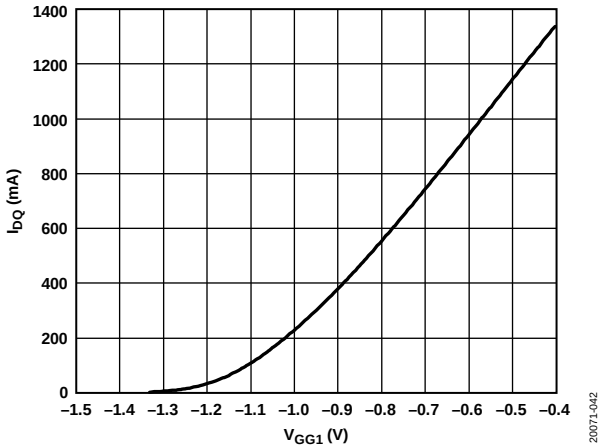


Figure 42. I_{DQ} vs. V_{GG1}

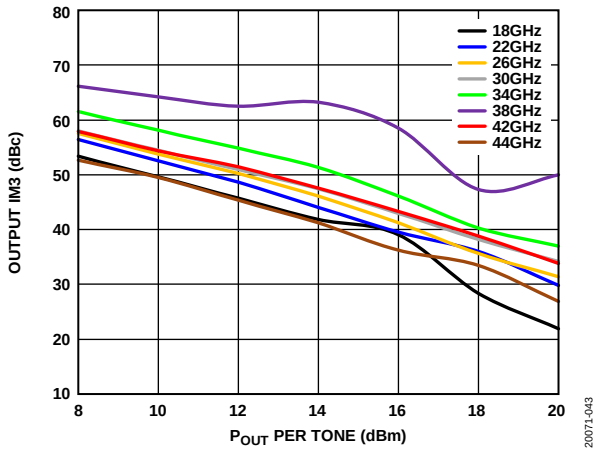


Figure 43. Output Third-Order Intermodulation (IM3) vs. P_{OUT} per Tone for Various Frequencies at V_{DD} = 4 V

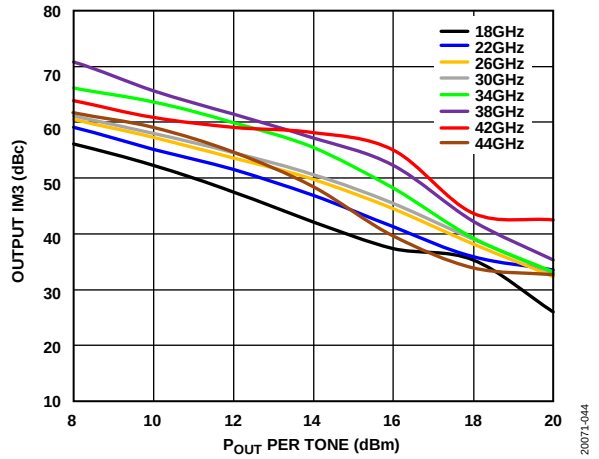


Figure 44. Output IM3 vs. P_{OUT} per Tone for Various Frequencies at V_{DD} = 5 V

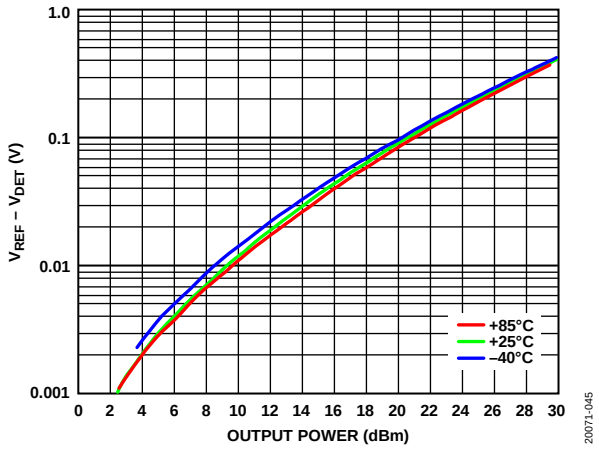


Figure 45. $V_{REF} - V_{DET}$ vs. Output Power at Various Temperatures, Frequency = 32 GHz

CONSTANT I_{DD} OPERATION

T_A = 25°C, V_{DD} = 5 V, and I_{DD} = 800 mA for nominal operation, unless otherwise noted. Figure 46 through Figure 49 are biased with the HMC980LP4E active bias controller. See the Biasing the ADPA7002 with the HMC980LP4E section for biasing details.

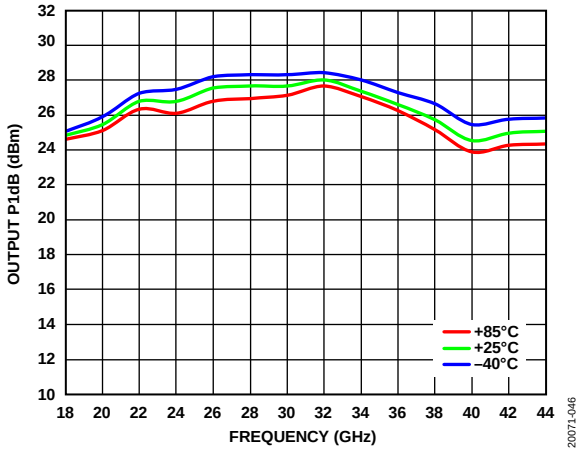


Figure 46. Output P1dB vs. Frequency for Various Temperatures, Data Measured with Constant I_{DD}

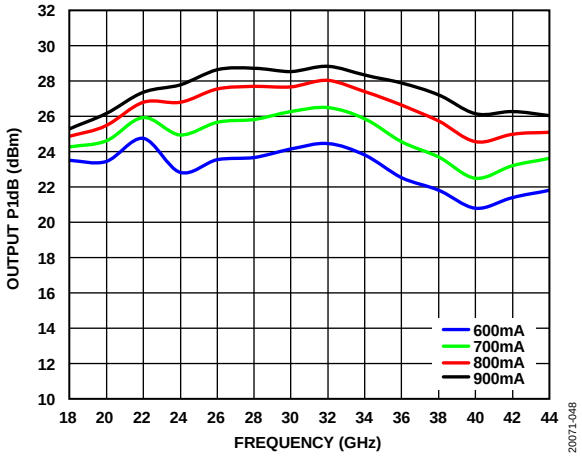


Figure 48. Output P1dB vs. Frequency for Various Supply Currents, Data Measured with Constant I_{DD}

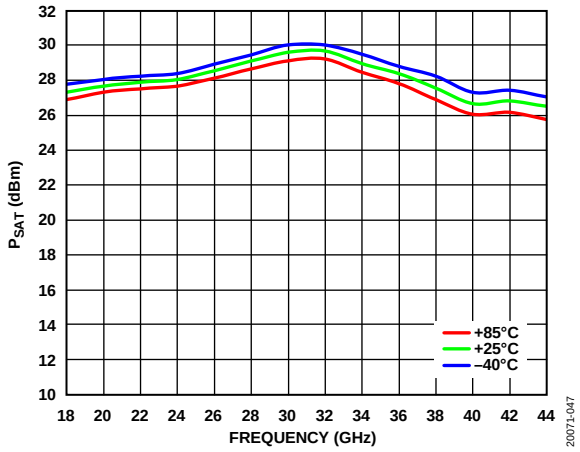


Figure 47. P_{SAT} vs. Frequency for Various Temperatures, Data Measured with Constant I_{DD}

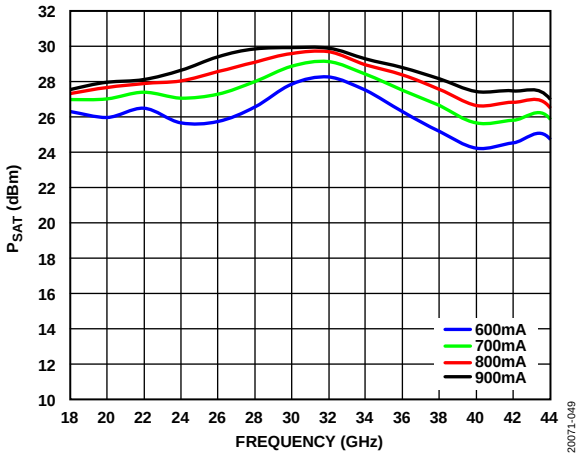


Figure 49. P_{SAT} vs. Frequency for Various Supply Currents Data Measured with Constant I_{DD}

THEORY OF OPERATION

The architecture of the ADPA7002, a medium power amplifier, is displayed in Figure 50. The ADPA7002 uses a cascaded, three-stage amplifier operating in quadrature between two 90° hybrids.

A portion of the RF output signal is directionally coupled to a diode to detect the RF output power. When the diode is dc biased, the diode rectifies the RF power and makes the RF power available for measurement as dc voltage at the V_{DET} pin. Temperature compensation is accomplished by referencing a symmetrical diode circuit that is not coupled to the RF output that contains a dc voltage output at the V_{REF} pin. The difference of $V_{REF} - V_{DET}$ provides a temperature compensated signal that is proportional to the RF output.

The 90° hybrids ensure that the input and output return losses are >12 dB. See the application circuits in the Applications Information section for further details on biasing the various blocks.

To obtain optimal performance from the ADPA7002 and to avoid damaging the device, follow the recommended biasing sequences described in the Biasing Procedures section.

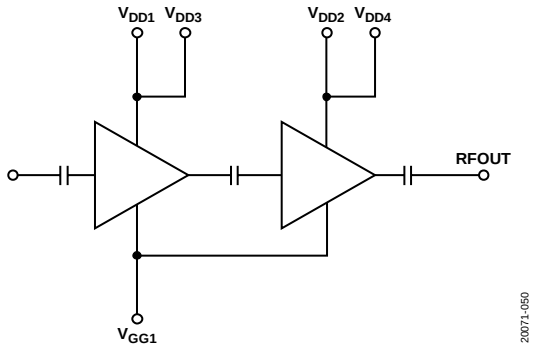


Figure 50. Simplified Architecture of the ADPA7002

APPLICATIONS INFORMATION

Figure 51 and Figure 52 show the two recommended typical application circuits for the ADPA7002. Pin 3 and Pin 9 are V_{GG1} gate bias control pins that are connected internally. V_{DD1} and V_{DD2}, Pin 2 and Pin 10, are drain bias pins for the driver stage that are internally connected. V_{DD3} and V_{DD4}, Pin 1 and Pin 11, are drain bias pins for the output stage that also internally connect.

The gate bias voltage can be applied to either Pin 3 or Pin 9. The drain bias can be applied to either V_{DD1} and V_{DD3} or V_{DD2} and V_{DD4}, which results in two possible bias configuration options. With Bias Option 1 (see Figure 51), the drain and gate voltages are applied to Pin 9, Pin 10, and Pin 11 on the south side of the device. With Bias Option 2 (see Figure 52), the drain and gate voltages are applied to Pin 1, Pin 2, and Pin 3 on the north side of the device. Capacitive bypassing is required for all pins in use.

The power supply decoupling capacitors shown in Figure 51 and Figure 52 represent the configuration used to characterize and qualify the device. There may be a scope to reduce the number of capacitors, but the scope varies from system to system. It is recommended to first remove or combine the largest capacitors that are farthest from the device.

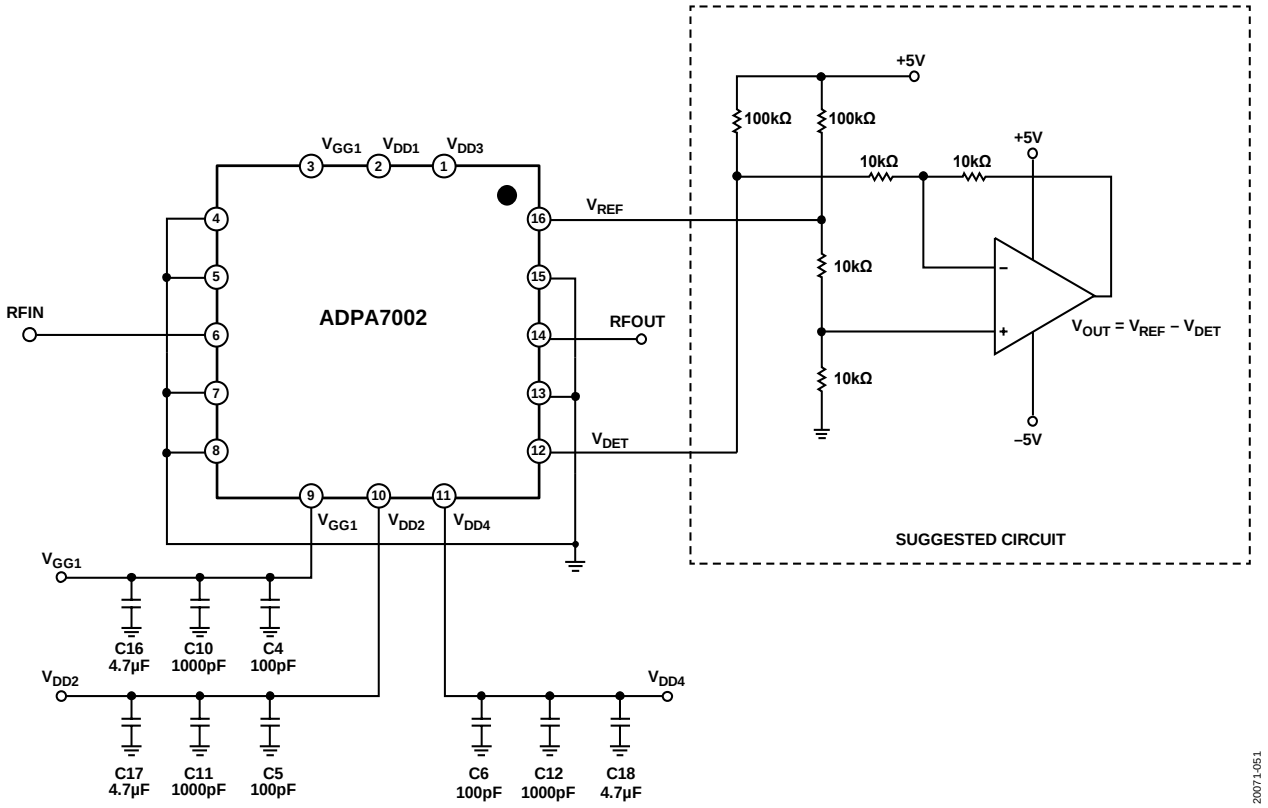


Figure 51. Bias Option 1

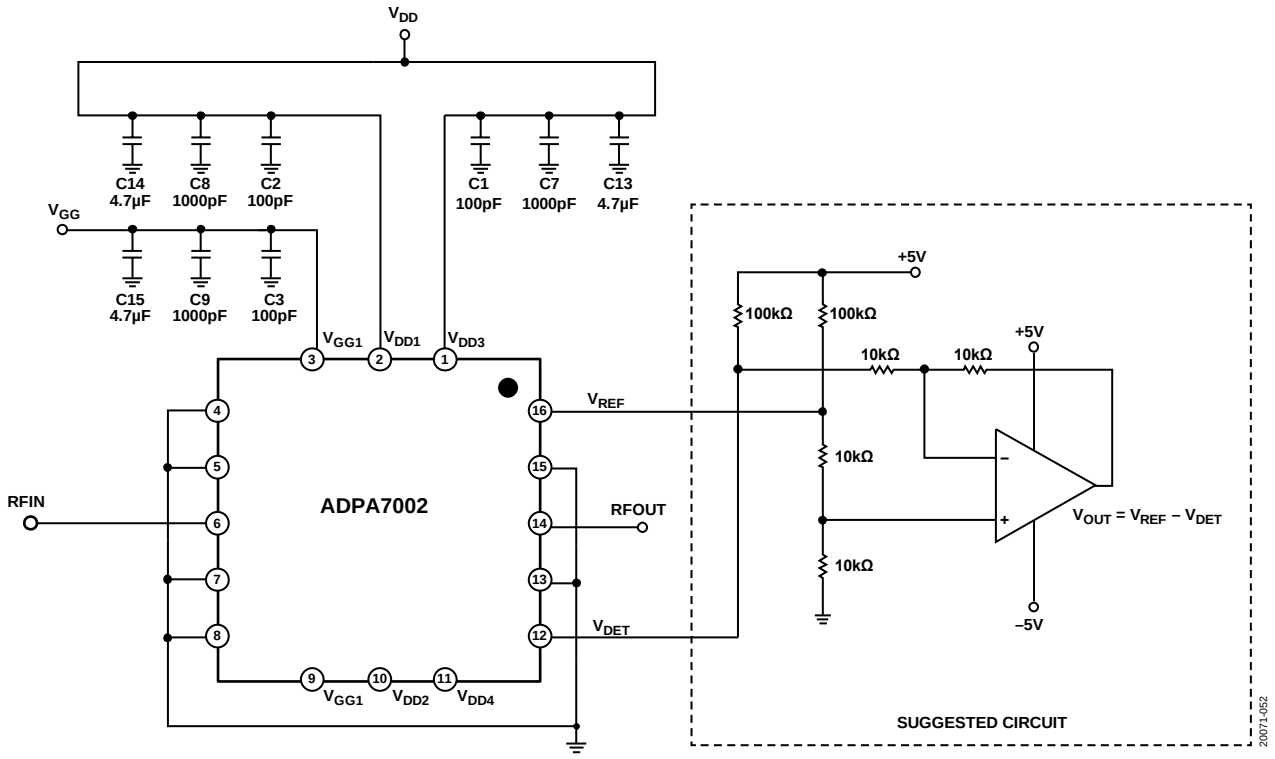


Figure 52. Bias Option 2

BIASING PROCEDURES

Adhere to the following bias sequence during power-up:

1. Connect GND to the RF and dc ground.
2. Set the V_{GG1} pin voltage to −1.5 V.
3. Set the drain bias voltage pins (V_{DDX}) to 5 V.
4. Increase the V_{GG1} pin voltage to achieve I_{DQ} = 700 mA.
5. Apply the RF signal.

Adhere to the following bias sequence during power-down:

1. Turn off the RF signal.
2. Decrease V_{GG1} to −1.5 V to achieve I_{DQ} = 0 mA (approximately).
3. Decrease the drain bias voltage pins (V_{DDX}) to 0 V.
4. Decrease the V_{GG1} pin voltages to 0 V.

The simplified bias pin connections to the dedicated gain stages are shown in Figure 50.

Table 8. Power Selection Table[1, 2]

I_{DQ} (mA)	Gain (dB)	P1dB (dBm)	OIP3 (dBm)	P_{DISS} (W)	V_{GG1} (V)
600	17.2	30.04	40.6	3	−0.73
700	17.7	30.24	38.7	3.5	−0.67
800	18.0	30.25	37.0	4	−0.62

[1] Data taken at the following nominal bias conditions: V_{DD} = 5 V, T_A = 25°C.
[2] Adjust V_{GG1} from −1.5 V to 0 V to achieve the desired drain current.

The nominal bias conditions are recommended to optimize overall performance of the ADPA7002. Unless otherwise noted, the data in the Typical Performance Characteristics section is taken using the nominal bias conditions. If operating at different bias conditions, the performance of the ADPA7002 can differ from the data in Table 1, Table 2, Table 3, and Table 4. Table 8 shows how gain, P1dB, and OIP3 vary with the bias current at 34 GHz.

BIASING THE ADPA7002 WITH THE HMC980LP4E

The HMC980LP4E is an active bias controller designed to meet the bias requirement for depletion mode amplifiers like the ADPA7002. The HMC980LP4E provides constant current biasing over temperature, provides device to device variation, properly sequences the gate and drain voltages to ensure safe operation, and offers self protection in the event of a short circuit. The HMC980LP4E contains an internal charge pump that generates negative voltage needed for the ADPA7002 gate and that can be used as an external negative voltage source.

For more information regarding the usage of HMC980LP4E, refer to the HMC980LP4E data sheet and the AN-1363 Application Note.

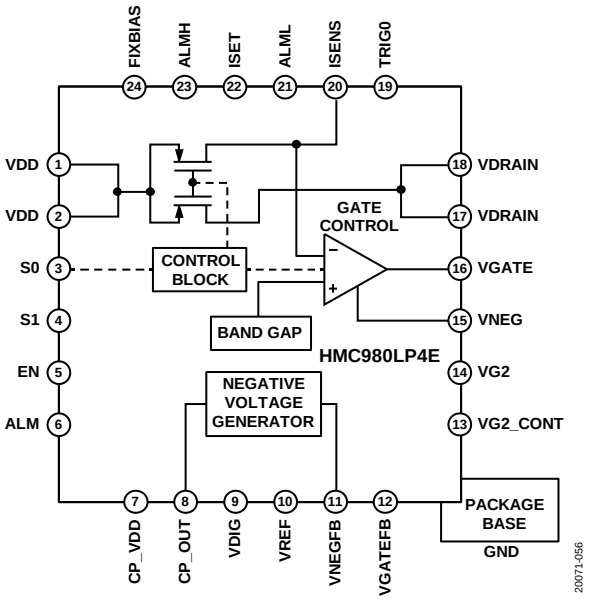


Figure 53. Functional Diagram of HMC980LP4E

Application Circuit Setup

Figure 54 shows a schematic of an application circuit using the HMC980LP4E to control the drain current of the ADPA7002 biased at 800 mA. In this example, the negative gate control voltage is generated by HMC980LP4E. Figure 55 shows an application circuit using an external negative supply.

In the application circuit, the ADPA7002 drain voltage and drain current are set by the following equations:

$$VDRAIN = VDD - (IDRAIN \times 0.85\ \Omega)$$

$$VDRAIN = 5.68\ V - (800\ mA \times 0.85\ \Omega)$$

$$VDRAIN = 5\ V$$

and

$$IDRAIN = (150\ \Omega)/(R10)$$

$$IDRAIN = (150\ \Omega)/(187\ \Omega)$$

$$IDRAIN = 0.802\ A$$

where:
VDRAIN is the drain voltage, or V_{DD}.
VDD is the supply voltage to the HMC980LP4E.
IDRAIN is the output current from Pin 17 and Pin 18 on the HMC980LP4E.

Limiting VGATE to Meet the ADPA7002 V_{GG1} AMR Requirement

When using the ADPA7002 with the HMC980LP4E, limit the minimum voltages for VNEG and VGATE to −1.5 V to keep the voltages within the absolute maximum ratings limit for the V_{GG1} pins. To limit the minimum voltages for VNEG and VGATE, set the R15 resistor and the R16 resistor to 732 kΩ and 632 kΩ, respectively. Refer to the AN-1363 Application Note for more information and for the R15 and R16 calculations.

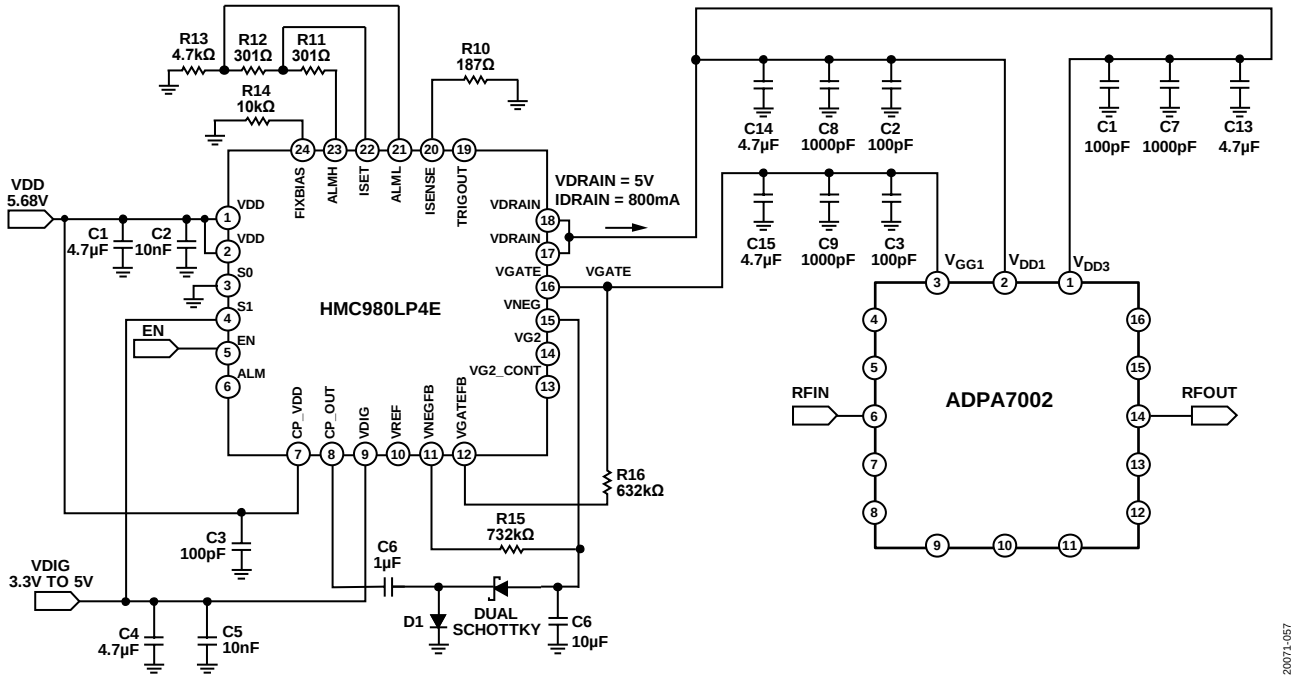


Figure 54. Application Circuit using the HMC980LP4E to Control the Drain Current of the ADPA7002

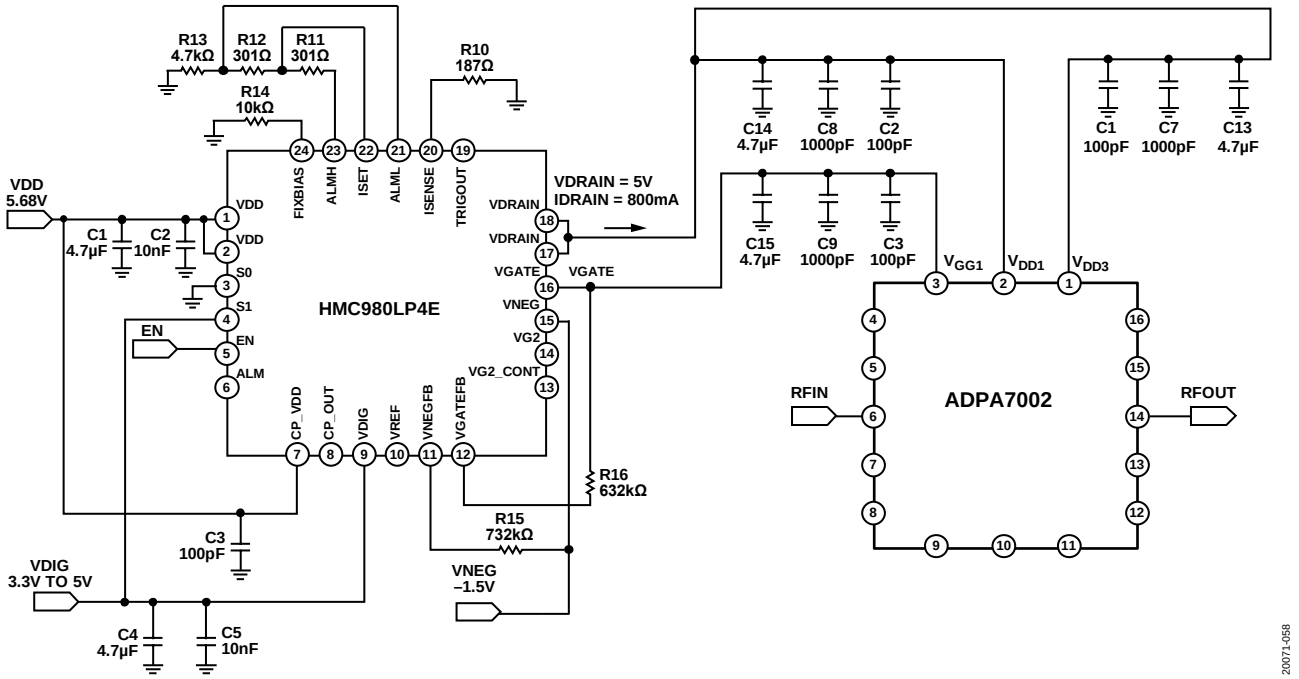


Figure 55. Application Circuit using the HMC980LP4E to Control the Drain Current of the ADPA7002 with an External Negative Voltage Source

HMC980LP4E Bias Sequence

To prevent damage to HMC980LP4E, properly sequence the dc supply. Adhere to the following power-up sequence steps:

1. Set the VDIG pin (Pin 9) to 3.3 V.
2. Set the S1 pin (Pin 4) to 3.3 V.
3. Set the VDD pin (Pin 1) to 5.68 V.
4. Set the VNEG pin (Pin 15) to −1.5 V. This step is not needed if using internally generated voltage.
5. Set the EN pin (Pin 5) to 3.3 V. Transitioning from 0 V to 3.3 V turns on the VGATE pin (Pin 16) and the VDRAIN pin (Pin 17).

Adhere to the following power-down sequence steps:

1. Set EN to 0 V. Transitioning from 3.3 V to 0 V turns off VDRAIN and VGATE.
2. Set VNEG to 0 V. This step is not required if using internally generated voltage.
3. Set VDD to 0 V.
4. Set S1 to 0 V.
5. Set VDIG to 0 V.

When the HMC980LP4E bias control circuit is set up, the ADPA7002 bias can be toggled on and off by applying the VDIG pin voltage (3.3 V) or by applying 0 V to the EN pin. When the EN pin is set to the VDIG voltage, the VGATE pin drops to −1.5 V, and the VDRAIN pin is turned on at +5 V. VGATE rises in voltage until IDRAIN equals 800 mA. The closed control loop then regulates IDRAIN at 800 mA. When EN is set to 0 V, VGATE is automatically set to −1.5 V and VDRAIN is set to 0 V (see Figure 56 and Figure 57).

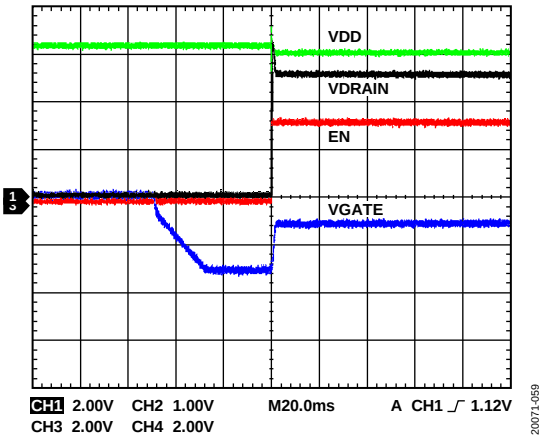


Figure 56. Turn On—HMC980LP4E Outputs to the ADPA7002

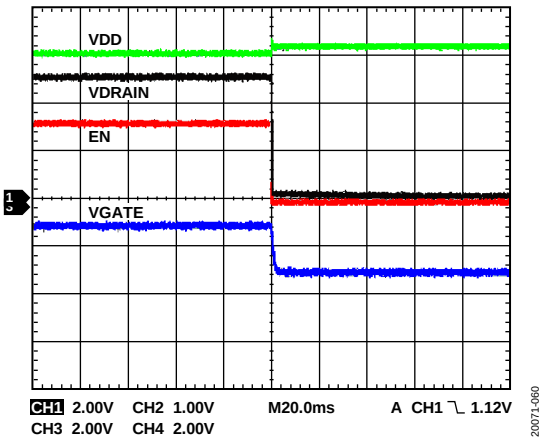


Figure 57. Turn Off—HMC980LP4E Outputs to the ADPA7002

Constant Drain Current Biasing vs. Constant Gate Voltage Biasing

The HMC980LP4E uses closed loop feedback to continuously adjust VGATE to maintain a constant gate current bias over dc supply variation, temperature variation, and part to part variation. The constant drain current bias method reduces calibration procedure time and maintains consistent performance over time.

In comparison to a constant gate voltage bias where the current increases when RF power is applied, a constant drain current has a slightly lower output P1dB. RF performance is lower due to a lower drain current at high input power levels as the HMC980LP4E reaches 1 dB compression.

The output P1dB performance for the constant drain current bias improves if the bias current setpoint is increased. By increasing the bias current setpoint to approximately 1 A (see Figure 61), the output P1dB and output power increases up to the level achievable with constant gate voltage biasing. Figure 59 shows a P_{OUT} vs. an input power (P_{IN}) response with a constant current bias where the bias current setpoint has increased.

The current and temperature limit of I_{DD} under the constant current operation is typically set by the thermal limitations in the absolute maximum ratings table (see Table 5) and by the maximum continuous power dissipation specification. Increasing the I_{DD} does not indefinitely increase the output P1dB as the power dissipation increases. Therefore, consider the trade-off between power dissipation and output P1dB performance when using constant drain current biasing.

Testing the HMC980LP4E

After biasing the ADPA7002 with the HMC980LP4E at the application nodes, compare the results to Figure 58 through Figure 61 to verify that the biasing procedure is correct. Note the measurements in Figure 58 through Figure 61 are of the die (the ADPA7002CHIP), but the ADPA7002 measurements are similar.

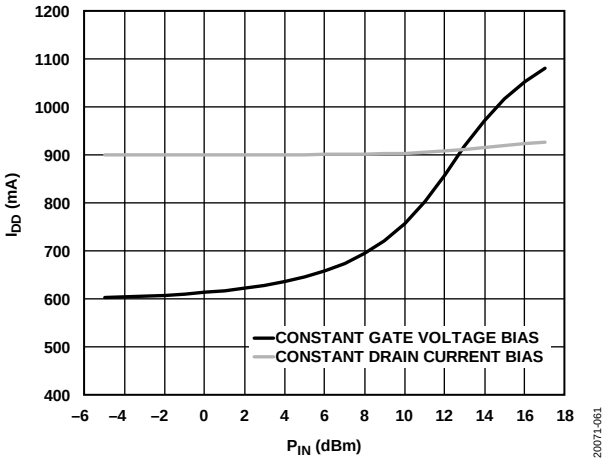


Figure 58. I_{DD} vs. P_{IN}, V_{DD} = 5 V, Frequency = 32 GHz, Constant Current Bias and Constant Voltage Bias

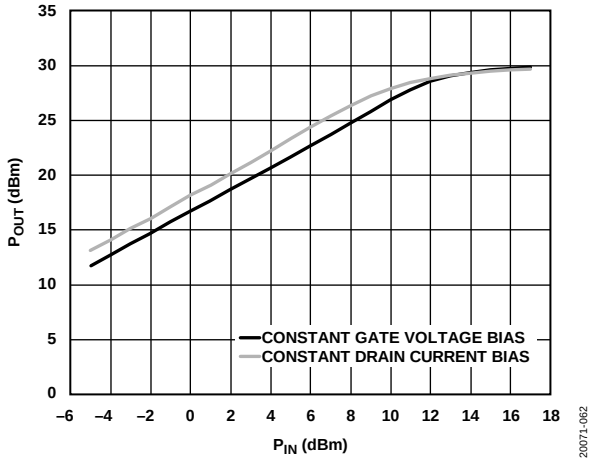


Figure 59. P_{OUT} vs. P_{IN}, V_{DD} = 5 V, Frequency = 32 GHz, Constant Current Bias and Constant Voltage Bias

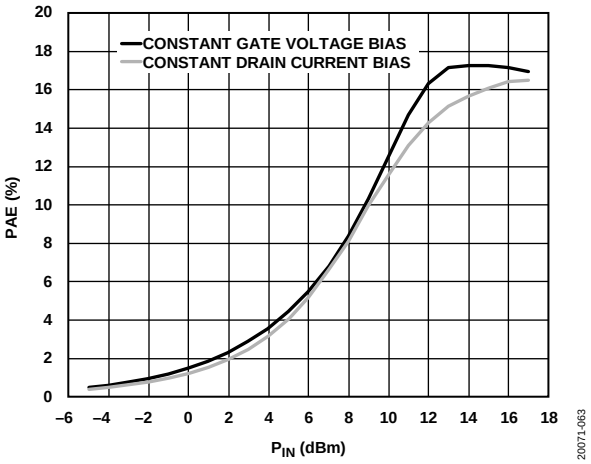


Figure 60. PAE vs. P_{IN}, V_{DD} = 5 V, Frequency = 32 GHz, Constant Current Bias and Constant Voltage Bias

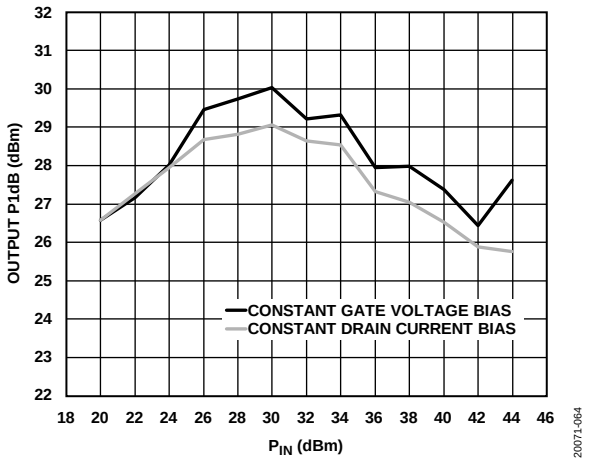


Figure 61. Output P1dB vs. P_{IN}, V_{DD} = 5 V, Frequency = 32 GHz Constant Current Bias and Constant Voltage Bias

OUTLINE DIMENSIONS

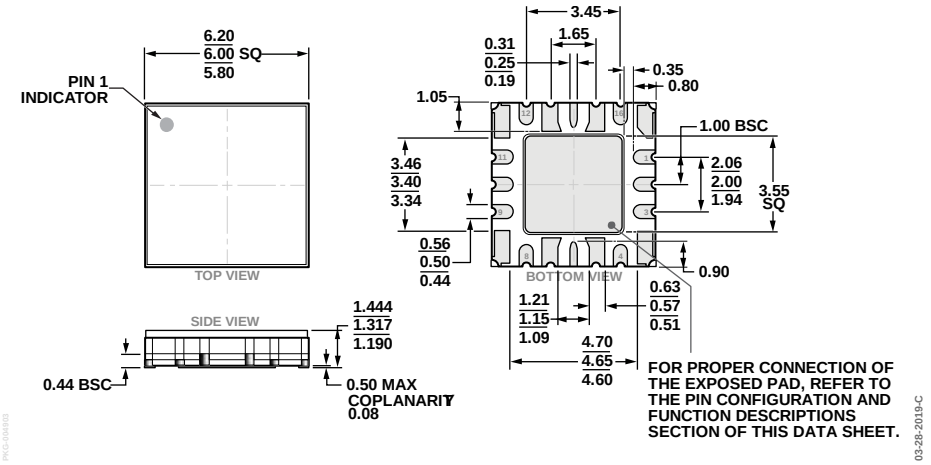


Figure 62. 16-Terminal Ceramic Leadless Chip with Heat Sink [LCC_HS]
(EH-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Moisture Sensitivity Level (MSL) Rating[2]	Package Description	Package Option
ADPA7002AEHZ	−40°C to +85°C	MSL3	16-Terminal Ceramic LCC_HS	EH-16-1
ADPA7002AEHZ-R7	−40°C to +85°C	MSL3	16-Terminal Ceramic LCC_HS	EH-16-1
ADPA7002-EVALZ			Evaluation PCB	

[1] Z = RoHS Compliant Part.
[2] See the Absolute Maximum Ratings section for further information on the MSL rating.

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ADPA7002C-KIT ADPA7002CHIP ADPA7002-EVALZ ADPA7002AEHZ ADPA7002AEHZ-R7