

# 74AUP1G74

Low-power D-type flip-flop with set and reset;  
positive-edge trigger

Rev. 14 — 14 July 2023

Product data sheet

## 1. General description

The 74AUP1G74 is a single positive edge triggered D-type flip-flop with individual data (D), clock (CP), set ( $\overline{SD}$ ) and reset ( $\overline{RD}$ ) inputs, and complementary Q and  $\overline{Q}$  outputs. Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device ensures very low static and dynamic power consumption across the entire  $V_{CC}$  range from 0.8 V to 3.6 V.

This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

## 2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- CMOS low power dissipation
- High noise immunity
- Overvoltage tolerant inputs to 3.6 V
- Low static power consumption;  $I_{CC} = 0.9 \mu\text{A}$  (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Low noise overshoot and undershoot < 10 % of  $V_{CC}$
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 5000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74AUP1G74DC</a>	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	<a href="#">SOT765-1</a>
<a href="#">74AUP1G74GT</a>	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	<a href="#">SOT833-1</a>
<a href="#">74AUP1G74GF</a>	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	<a href="#">SOT1089</a>
<a href="#">74AUP1G74GN</a>	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	<a href="#">SOT1116</a>
<a href="#">74AUP1G74GS</a>	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	<a href="#">SOT1203</a>
<a href="#">74AUP1G74GX</a>	-40 °C to +125 °C	X2SON8	plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 × 0.8 × 0.32 mm	<a href="#">SOT1233-2</a>

### 4. Marking

Table 2. Marking codes

Type number	Marking code <sup>[1]</sup>
74AUP1G74DC	p74
74AUP1G74GT	p74
74AUP1G74GF	54
74AUP1G74GN	54
74AUP1G74GS	54
74AUP1G74GX	54

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

### 5. Functional diagram

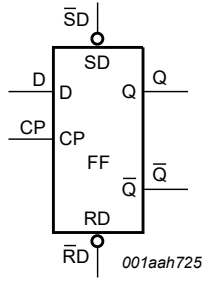


Fig. 1. Logic symbol

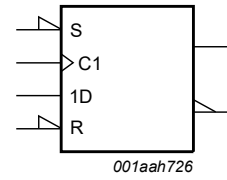


Fig. 2. IEC logic symbol

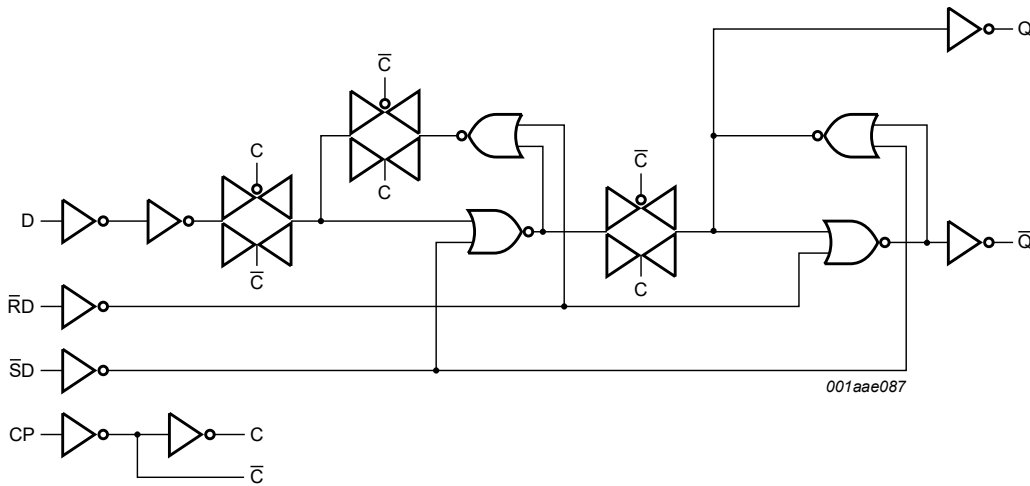
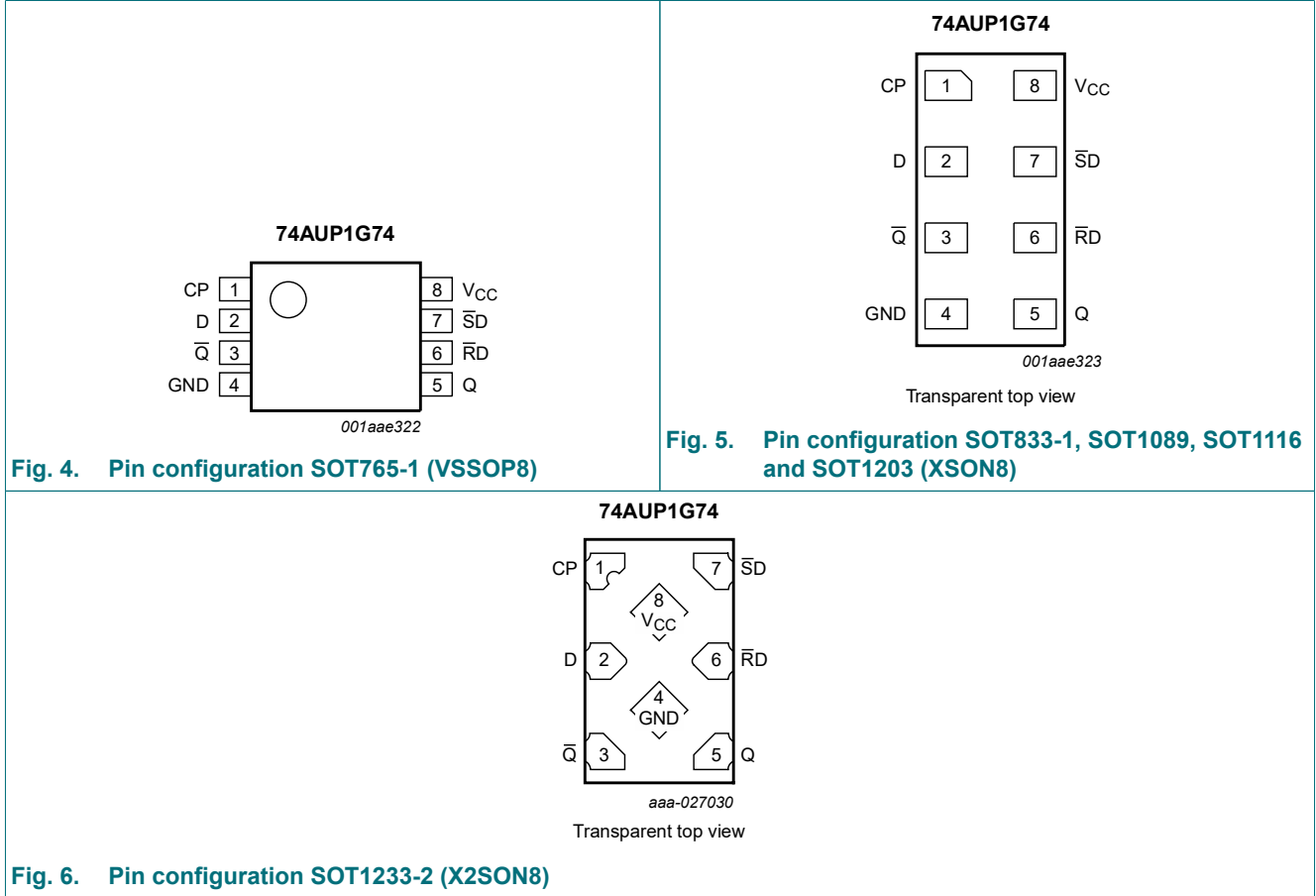


Fig. 3. Logic diagram

## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
CP	1	clock input
D	2	data input
Q̄	3	complement output
GND	4	ground (0 V)
Q	5	true output
RD̄	6	asynchronous reset input (active LOW)
SD̄	7	asynchronous set input (active LOW)
V <sub>CC</sub>	8	supply voltage

## 7. Functional description

**Table 4. Function table for asynchronous operation**

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input				Output	
SD	RD	CP	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

**Table 5. Function table for synchronous operation**

H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH CP transition;

$\bar{Q}_{n+1}$ ,  $Q_{n+1}$  = state after the next LOW-to-HIGH CP transition.

Input				Output	
SD	RD	CP	D	$Q_{n+1}$	$\bar{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

## 8. Limiting values

**Table 6. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$V_I$	input voltage		[1]	+4.6	V
$V_O$	output voltage	Active mode and Power-down mode	[1]	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±20	mA
$I_{CC}$	supply current		-	+50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to $+125$ °C SOT765-1 (VSSOP8) [2] SOT833-1 (XSON8) [3] SOT1089 (XSON8) [4] SOT1116 (XSON8) [5] SOT1203 (XSON8) [6] SOT1233-2 (X2SON8) [7]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT765-1 (VSSOP8) package:  $P_{tot}$  derates linearly with 4.9 mW/K above 99 °C.

[3] For SOT833-1 (XSON8) package:  $P_{tot}$  derates linearly with 3.1 mW/K above 68 °C.

[4] For SOT1089 (XSON8) package:  $P_{tot}$  derates linearly with 4.0 mW/K above 88 °C.

[5] For SOT1116 (XSON8) package:  $P_{tot}$  derates linearly with 4.2 mW/K above 90 °C.

[6] For SOT1203 (XSON8) package:  $P_{tot}$  derates linearly with 3.6 mW/K above 81 °C.

[7] For SOT1233-2 (X2SON8) package:  $P_{tot}$  derates linearly with 7.7 mW/K above 118 °C.

## 9. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		0.8	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	Active mode	0	$V_{CC}$	V
		Power-down mode; $V_{CC} = 0$ V	0	3.6	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 0.8$ V to 3.6 V	-	200	ns/V

## 10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25</math> °C</b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 0.8$ V	$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 0.9$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.6	-	-	V
		$V_{CC} = 3.0$ V to 3.6 V	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 0.8$ V	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 0.9$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 3.0$ V to 3.6 V	-	-	0.9	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -20$ $\mu$ A; $V_{CC} = 0.8$ V to 3.6 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -1.1$ mA; $V_{CC} = 1.1$ V	$0.75 \times V_{CC}$	-	-	V
		$I_O = -1.7$ mA; $V_{CC} = 1.4$ V	1.11	-	-	V
		$I_O = -1.9$ mA; $V_{CC} = 1.65$ V	1.32	-	-	V
		$I_O = -2.3$ mA; $V_{CC} = 2.3$ V	2.05	-	-	V
		$I_O = -3.1$ mA; $V_{CC} = 2.3$ V	1.9	-	-	V
		$I_O = -2.7$ mA; $V_{CC} = 3.0$ V	2.72	-	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 20$ $\mu$ A; $V_{CC} = 0.8$ V to 3.6 V	-	-	0.1	V
		$I_O = 1.1$ mA; $V_{CC} = 1.1$ V	-	-	$0.3 \times V_{CC}$	V
		$I_O = 1.7$ mA; $V_{CC} = 1.4$ V	-	-	0.31	V
		$I_O = 1.9$ mA; $V_{CC} = 1.65$ V	-	-	0.31	V
		$I_O = 2.3$ mA; $V_{CC} = 2.3$ V	-	-	0.31	V
		$I_O = 3.1$ mA; $V_{CC} = 2.3$ V	-	-	0.44	V
		$I_O = 2.7$ mA; $V_{CC} = 3.0$ V	-	-	0.31	V
$I_O = 4.0$ mA; $V_{CC} = 3.0$ V	-	-	0.44	V		
$I_I$	input leakage current	$V_I = \text{GND}$ to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	$\pm 0.1$	$\mu$ A
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	$\pm 0.2$	$\mu$ A

## Low-power D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta I_{OFF}$	additional power-off leakage current	$V_I$ or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	$\pm 0.2$	$\mu$ A
$I_{CC}$	supply current	$V_I = GND$ or $V_{CC}$ ; $I_O = 0$ A; $V_{CC} = 0.8$ V to 3.6 V	-	-	0.5	$\mu$ A
$\Delta I_{CC}$	additional supply current	$V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 3.3$ V; per pin [1]	-	-	40	$\mu$ A
$C_I$	input capacitance	$V_{CC} = 0$ V to 3.6 V; $V_I = GND$ or $V_{CC}$	-	0.6	-	pF
$C_O$	output capacitance	$V_O = GND$ ; $V_{CC} = 0$ V	-	1.3	-	pF
<b><math>T_{amb} = -40</math> °C to <math>+85</math> °C</b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 0.8$ V	$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 0.9$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.6	-	-	V
		$V_{CC} = 3.0$ V to 3.6 V	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 0.8$ V	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 0.9$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 3.0$ V to 3.6 V	-	-	0.9	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -20$ $\mu$ A; $V_{CC} = 0.8$ V to 3.6 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -1.1$ mA; $V_{CC} = 1.1$ V	$0.7 \times V_{CC}$	-	-	V
		$I_O = -1.7$ mA; $V_{CC} = 1.4$ V	1.03	-	-	V
		$I_O = -1.9$ mA; $V_{CC} = 1.65$ V	1.30	-	-	V
		$I_O = -2.3$ mA; $V_{CC} = 2.3$ V	1.97	-	-	V
		$I_O = -3.1$ mA; $V_{CC} = 2.3$ V	1.85	-	-	V
		$I_O = -2.7$ mA; $V_{CC} = 3.0$ V	2.67	-	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 20$ $\mu$ A; $V_{CC} = 0.8$ V to 3.6 V	-	-	0.1	V
		$I_O = 1.1$ mA; $V_{CC} = 1.1$ V	-	-	$0.3 \times V_{CC}$	V
		$I_O = 1.7$ mA; $V_{CC} = 1.4$ V	-	-	0.37	V
		$I_O = 1.9$ mA; $V_{CC} = 1.65$ V	-	-	0.35	V
		$I_O = 2.3$ mA; $V_{CC} = 2.3$ V	-	-	0.33	V
		$I_O = 3.1$ mA; $V_{CC} = 2.3$ V	-	-	0.45	V
		$I_O = 2.7$ mA; $V_{CC} = 3.0$ V	-	-	0.33	V
	$I_O = 4.0$ mA; $V_{CC} = 3.0$ V	-	-	0.45	V	
$I_I$	input leakage current	$V_I = GND$ to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	$\pm 0.5$	$\mu$ A
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	$\pm 0.5$	$\mu$ A
$\Delta I_{OFF}$	additional power-off leakage current	$V_I$ or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	$\pm 0.6$	$\mu$ A
$I_{CC}$	supply current	$V_I = GND$ or $V_{CC}$ ; $I_O = 0$ A; $V_{CC} = 0.8$ V to 3.6 V	-	-	0.9	$\mu$ A
$\Delta I_{CC}$	additional supply current	$V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 3.3$ V; per pin [1]	-	-	50	$\mu$ A

## Low-power D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 0.8 V	0.75 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	0.70 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.6	-	-	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 0.8 V	-	-	0.25 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	-	-	0.30 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.9	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 0.8 V to 3.6 V	V <sub>CC</sub> - 0.11	-	-	V
		I <sub>O</sub> = -1.1 mA; V <sub>CC</sub> = 1.1 V	0.6 × V <sub>CC</sub>	-	-	V
		I <sub>O</sub> = -1.7 mA; V <sub>CC</sub> = 1.4 V	0.93	-	-	V
		I <sub>O</sub> = -1.9 mA; V <sub>CC</sub> = 1.65 V	1.17	-	-	V
		I <sub>O</sub> = -2.3 mA; V <sub>CC</sub> = 2.3 V	1.77	-	-	V
		I <sub>O</sub> = -3.1 mA; V <sub>CC</sub> = 2.3 V	1.67	-	-	V
		I <sub>O</sub> = -2.7 mA; V <sub>CC</sub> = 3.0 V	2.40	-	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.30	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 0.8 V to 3.6 V	-	-	0.11	V
		I <sub>O</sub> = 1.1 mA; V <sub>CC</sub> = 1.1 V	-	-	0.33 × V <sub>CC</sub>	V
		I <sub>O</sub> = 1.7 mA; V <sub>CC</sub> = 1.4 V	-	-	0.41	V
		I <sub>O</sub> = 1.9 mA; V <sub>CC</sub> = 1.65 V	-	-	0.39	V
		I <sub>O</sub> = 2.3 mA; V <sub>CC</sub> = 2.3 V	-	-	0.36	V
		I <sub>O</sub> = 3.1 mA; V <sub>CC</sub> = 2.3 V	-	-	0.50	V
		I <sub>O</sub> = 2.7 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.50	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = GND to 3.6 V; V <sub>CC</sub> = 0 V to 3.6 V	-	-	±0.75	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V	-	-	±0.75	μA
ΔI <sub>OFF</sub>	additional power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V to 0.2 V	-	-	±0.75	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = GND or V <sub>CC</sub> ; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 0.8 V to 3.6 V	-	-	1.4	μA
ΔI <sub>CC</sub>	additional supply current	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 3.3 V; per pin [1]	-	-	75	μA

[1] One input at V<sub>CC</sub> - 0.6 V, other input at V<sub>CC</sub> or GND.



## 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +85 °C		T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
<b>C<sub>L</sub> = 5 pF</b>										
t <sub>pd</sub>	propagation delay	CP to Q, $\bar{Q}$ ; see Fig. 7. [2]								
		V <sub>CC</sub> = 0.8 V	-	25.4	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	2.9	6.7	14.0	2.6	14.2	2.6	14.2	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	2.4	4.5	7.6	2.3	8.3	2.3	8.6	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.9	3.5	5.7	1.7	6.5	1.7	6.8	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	2.6	3.8	1.4	4.4	1.4	4.7	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.5	2.2	3.1	1.2	3.4	1.2	3.7	ns
		$\bar{S}D$ to Q, $\bar{Q}$ ; see Fig. 8. [2]								
		V <sub>CC</sub> = 0.8 V	-	19.6	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	2.7	5.6	11.0	2.5	11.4	2.5	11.5	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	2.4	4.0	6.3	2.2	6.9	2.2	7.3	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.0	3.3	4.9	1.7	5.6	1.7	5.9	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.9	2.7	3.7	1.7	4.0	1.7	4.2	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.8	2.5	3.2	1.5	3.6	1.5	3.8	ns
		$\bar{R}D$ to Q, $\bar{Q}$ ; see Fig. 8. [2]								
		V <sub>CC</sub> = 0.8 V	-	19.2	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	2.6	5.5	11.0	2.5	11.3	2.5	11.5	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	2.3	3.9	6.3	2.2	6.8	2.2	7.3	ns
V <sub>CC</sub> = 1.65 V to 1.95 V	1.9	3.2	5.0	1.8	5.6	1.8	5.9	ns		
V <sub>CC</sub> = 2.3 V to 2.7 V	1.9	2.6	3.6	1.7	4.1	1.7	4.3	ns		
V <sub>CC</sub> = 3.0 V to 3.6 V	1.8	2.4	3.3	1.5	3.6	1.5	3.8	ns		
f <sub>max</sub>	maximum frequency	CP; see Fig. 7.								
		V <sub>CC</sub> = 0.8 V	-	53	-	-	-	-	MHz	
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	203	-	170	-	170	-	MHz
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	347	-	310	-	300	-	MHz
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	435	-	400	-	390	-	MHz
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	550	-	490	-	480	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	619	-	550	-	510	-	MHz

Low-power D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +85 °C		T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
<b>C<sub>L</sub> = 10 pF</b>										
t <sub>pd</sub>	propagation delay	CP to Q, $\bar{Q}$ ; see Fig. 7. [2]								
		V <sub>CC</sub> = 0.8 V	-	28.9	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	3.1	7.5	15.8	2.9	16.1	2.9	16.1	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	2.7	5.1	8.7	2.4	9.4	2.4	9.8	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.5	4.1	6.5	2.2	7.2	2.2	7.6	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.0	3.2	4.6	1.8	5.3	1.8	5.6	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.8	2.8	3.8	1.6	4.1	1.6	4.4	ns
		SD to Q, $\bar{Q}$ ; see Fig. 8. [2]								
		V <sub>CC</sub> = 0.8 V	-	23.2	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	2.9	6.5	12.9	2.8	13.3	2.8	13.5	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	2.7	4.6	7.5	2.3	7.9	2.3	8.3	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.6	3.9	5.6	2.3	6.3	2.3	6.6	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.3	3.2	4.4	2.0	4.8	2.0	5.2	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.2	3.0	3.9	1.9	4.2	1.9	4.4	ns
		$\bar{R}\bar{D}$ to Q, $\bar{Q}$ ; see Fig. 8. [2]								
		V <sub>CC</sub> = 0.8 V	-	22.7	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	2.8	6.4	12.8	2.7	13.2	2.7	13.4	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	2.6	4.5	7.5	2.3	8.1	2.3	8.4	ns
V <sub>CC</sub> = 1.65 V to 1.95 V	2.5	3.3	5.8	2.3	6.3	2.3	6.7	ns		
V <sub>CC</sub> = 2.3 V to 2.7 V	2.2	3.2	4.4	2.0	4.9	2.0	5.2	ns		
V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	2.9	4.0	1.9	4.3	1.9	4.5	ns		
f <sub>max</sub>	maximum frequency	CP; see Fig. 7.								
		V <sub>CC</sub> = 0.8 V	-	52	-	-	-	-	MHz	
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	192	-	150	-	150	-	MHz
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	324	-	280	-	230	-	MHz
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	421	-	310	-	250	-	MHz
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	486	-	370	-	360	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	550	-	410	-	360	-	MHz

Low-power D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +85 °C		T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
<b>C<sub>L</sub> = 15 pF</b>										
t <sub>pd</sub>	propagation delay	CP to Q, $\bar{Q}$ ; see Fig. 7. [2]								
		V <sub>CC</sub> = 0.8 V	-	32.4	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	3.5	8.3	17.6	3.3	17.8	3.3	18.0	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	3.2	5.6	9.5	2.8	10.5	2.8	11.1	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.7	4.6	7.2	2.5	8.1	2.5	8.6	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.4	3.6	5.2	2.2	5.8	2.2	6.2	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.2	3.2	4.4	2.0	4.9	2.0	5.2	ns
		SD to Q, $\bar{Q}$ ; see Fig. 8. [2]								
		V <sub>CC</sub> = 0.8 V	-	26.7	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	3.3	7.3	14.7	3.1	15.2	3.1	15.4	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	3.2	5.2	8.3	2.9	9.0	2.9	9.5	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.8	4.3	6.4	2.5	7.1	2.5	7.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.8	3.7	5.1	2.2	5.5	2.2	5.8	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.5	3.5	4.6	2.4	5.0	2.4	5.2	ns
		$\bar{R}\bar{D}$ to Q, $\bar{Q}$ ; see Fig. 8. [2]								
		V <sub>CC</sub> = 0.8 V	-	26.1	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	3.2	7.2	14.5	3.1	15.0	3.1	15.2	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	3.1	5.1	8.4	2.7	9.2	2.7	9.7	ns
V <sub>CC</sub> = 1.65 V to 1.95 V	2.7	4.3	6.5	2.6	7.3	2.6	7.7	ns		
V <sub>CC</sub> = 2.3 V to 2.7 V	2.6	3.6	5.0	2.4	5.5	2.4	5.8	ns		
V <sub>CC</sub> = 3.0 V to 3.6 V	2.4	3.4	4.6	2.3	5.0	2.3	5.2	ns		
f <sub>max</sub>	maximum frequency	CP; see Fig. 7.								
		V <sub>CC</sub> = 0.8 V	-	50	-	-	-	-	MHz	
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	181	-	120	-	120	-	MHz
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	301	-	190	-	160	-	MHz
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	407	-	240	-	190	-	MHz
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	422	-	300	-	270	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	481	-	320	-	300	-	MHz

Low-power D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +85 °C		T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
<b>C<sub>L</sub> = 30 pF</b>										
t <sub>pd</sub>	propagation delay	CP to Q, $\bar{Q}$ ; see Fig. 7. [2]								
		V <sub>CC</sub> = 0.8 V	-	42.7	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	4.2	10.6	22.5	4.0	23.0	4.0	23.3	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	3.7	7.2	12.0	3.7	13.3	3.7	14.0	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	3.5	5.8	9.2	3.4	10.4	3.4	11.0	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	3.3	4.7	6.6	3.0	7.3	3.0	7.8	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	3.0	4.3	5.8	2.8	6.8	2.8	7.3	ns
		SD to Q, $\bar{Q}$ ; see Fig. 8. [2]								
		V <sub>CC</sub> = 0.8 V	-	37.0	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	4.0	9.5	19.8	3.8	20.8	3.8	21.1	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	3.8	6.7	10.9	3.7	12.0	3.7	12.7	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	3.7	5.6	8.4	3.5	9.3	3.5	9.9	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	3.7	4.8	6.6	3.2	7.2	3.2	7.6	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	3.4	4.6	6.0	3.1	6.8	3.1	7.1	ns
		$\bar{R}D$ to Q, $\bar{Q}$ ; see Fig. 8. [2]								
		V <sub>CC</sub> = 0.8 V	-	36.4	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	3.9	9.4	19.5	3.8	20.2	3.8	20.5	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	3.6	6.6	10.9	3.7	12.0	3.7	12.6	ns
V <sub>CC</sub> = 1.65 V to 1.95 V	3.5	5.5	8.5	3.5	9.5	3.5	10.1	ns		
V <sub>CC</sub> = 2.3 V to 2.7 V	3.5	4.7	6.5	3.2	7.1	3.2	7.6	ns		
V <sub>CC</sub> = 3.0 V to 3.6 V	3.3	4.4	6.1	3.1	7.1	3.1	7.5	ns		
f <sub>max</sub>	maximum frequency	CP; see Fig. 7.								
		V <sub>CC</sub> = 0.8 V	-	28	-	-	-	-	MHz	
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	145	-	70	-	70	-	MHz
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	185	-	120	-	110	-	MHz
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	270	-	150	-	120	-	MHz
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	290	-	190	-	170	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	315	-	200	-	190	-	MHz

Low-power D-type flip-flop with set and reset; positive-edge trigger

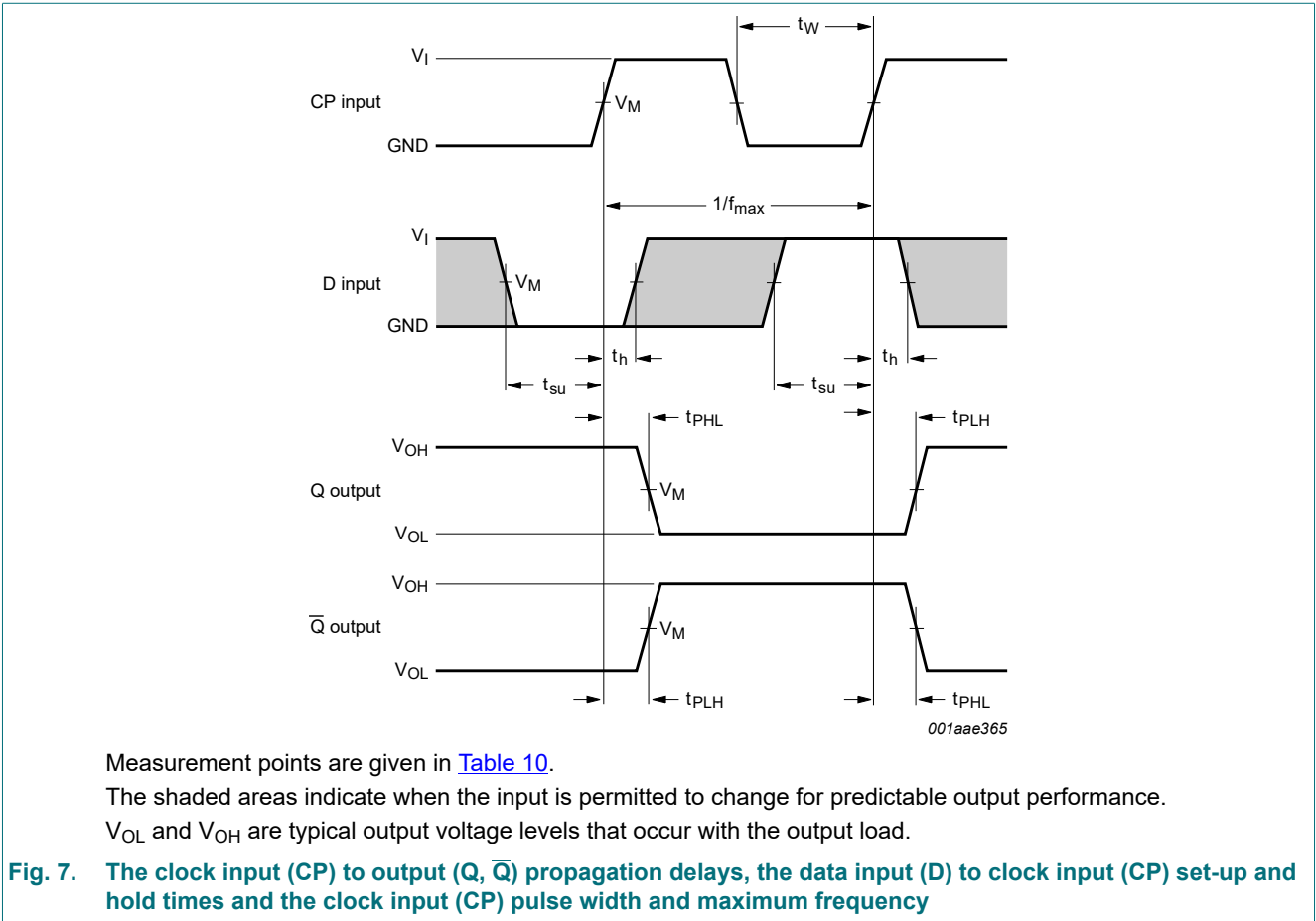
Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +85 °C		T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C <sub>L</sub> = 5 pF, 10 pF, 15 pF and 30 pF										
t <sub>su</sub>	set-up time	D to CP HIGH; see Fig. 7.								
		V <sub>CC</sub> = 0.8 V	-	3.4	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	0.6	-	1.2	-	1.2	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	0.3	-	0.6	-	0.6	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	0.4	-	0.5	-	0.5	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	0.2	-	0.4	-	0.4	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	0.3	-	0.4	-	0.4	-	ns
		D to CP LOW; see Fig. 7.								
		V <sub>CC</sub> = 0.8 V	-	3.0	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	0.5	-	1.2	-	1.2	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	0.3	-	0.7	-	0.7	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	0.4	-	0.7	-	0.7	-	ns
V <sub>CC</sub> = 2.3 V to 2.7 V	-	0.5	-	0.7	-	0.7	-	ns		
V <sub>CC</sub> = 3.0 V to 3.6 V	-	0.6	-	0.8	-	0.8	-	ns		
t <sub>h</sub>	hold time	D to CP; see Fig. 7.								
		V <sub>CC</sub> = 0.8 V	-	-1.9	-	-	-	-	-	ns
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	-0.3	-	0.5	-	0.5	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	-0.2	-	0.2	-	0.2	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-0.2	-	0.1	-	0.1	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-0.2	-	0.1	-	0.1	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-0.2	-	0.1	-	0.1	-	ns
t <sub>rec</sub>	recovery time	RD; see Fig. 8								
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	-0.5	-	-0.9	-	-0.9	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	-0.2	-	-0.6	-	-0.6	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-0.2	-	-0.4	-	-0.4	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-0.1	-	-0.1	-	-0.1	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-0.1	-	-0.1	-	-0.1	-	ns
		SD; see Fig. 8.								
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	-0.5	-	-0.3	-	-0.3	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	-0.4	-	-0.1	-	-0.1	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-0.3	-	0	-	0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-0.2	-	0.1	-	0.1	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-0.1	-	0.1	-	0.1	-	ns

Low-power D-type flip-flop with set and reset; positive-edge trigger

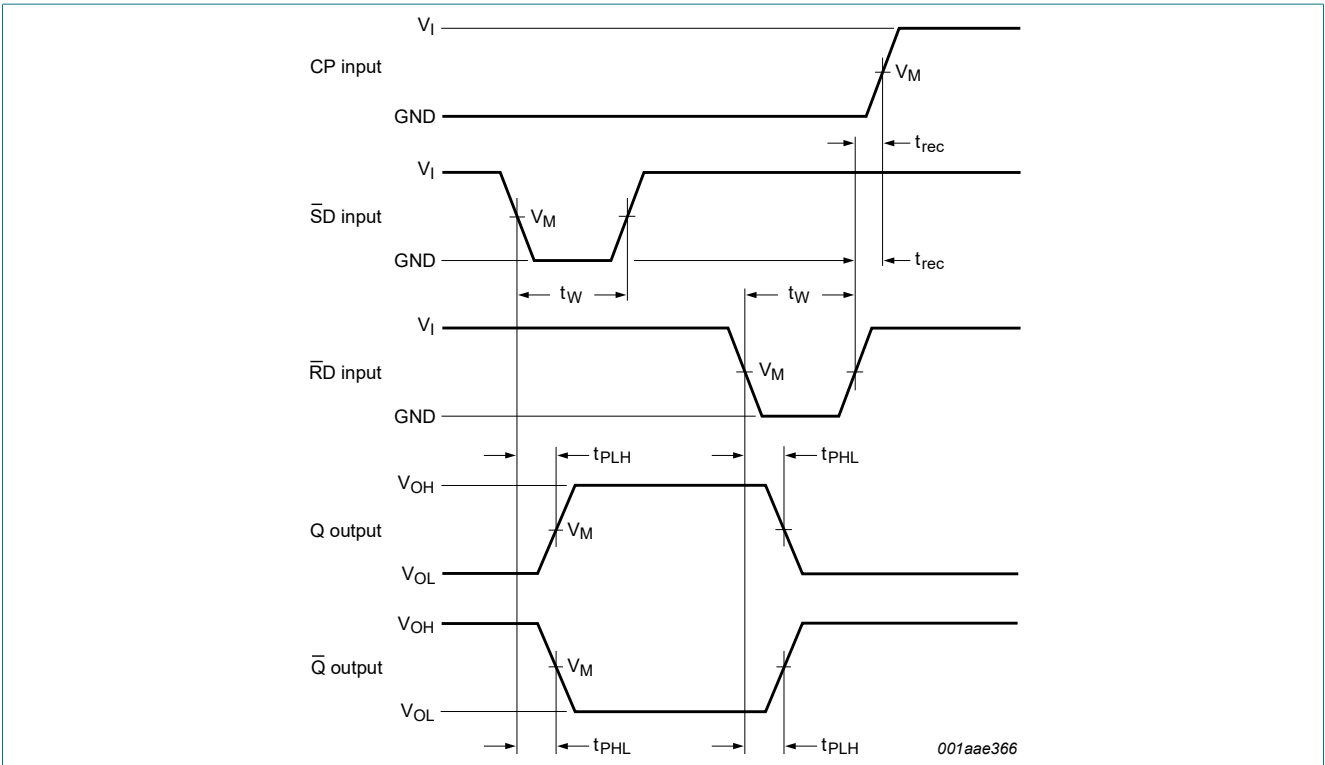
Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C			T <sub>amb</sub> = -40 °C to +85 °C		T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t <sub>w</sub>	pulse width	CP HIGH or LOW; see Fig. 7.								
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	2.1	-	2.7	-	2.7	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	1.1	-	1.5	-	1.5	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	0.9	-	1.6	-	1.6	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	0.6	-	1.7	-	1.7	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	0.6	-	1.9	-	1.9	-	ns
		$\overline{SD}$ or $\overline{RD}$ LOW; see Fig. 8.								
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	4.2	-	11.3	-	11.5	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	2.3	-	6.2	-	6.4	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	1.8	-	4.8	-	5.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	1.2	-	3.3	-	3.5	-	ns
V <sub>CC</sub> = 3.0 V to 3.6 V	-	1.1	-	2.6	-	2.8	-	ns		
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> [3]								
		V <sub>CC</sub> = 0.8 V	-	2.8	-	-	-	-	-	pF
		V <sub>CC</sub> = 1.1 V to 1.3 V	-	2.9	-	-	-	-	-	pF
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	3.0	-	-	-	-	-	pF
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	3.0	-	-	-	-	-	pF
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	3.5	-	-	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	3.9	-	-	-	-	-	pF

[1] All typical values are measured at nominal V<sub>CC</sub>.  
 [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
 [3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in V;  
 N = number of inputs switching;  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

11.1. Waveforms and test circuit



Low-power D-type flip-flop with set and reset; positive-edge trigger



Measurement points are given in [Table 10](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

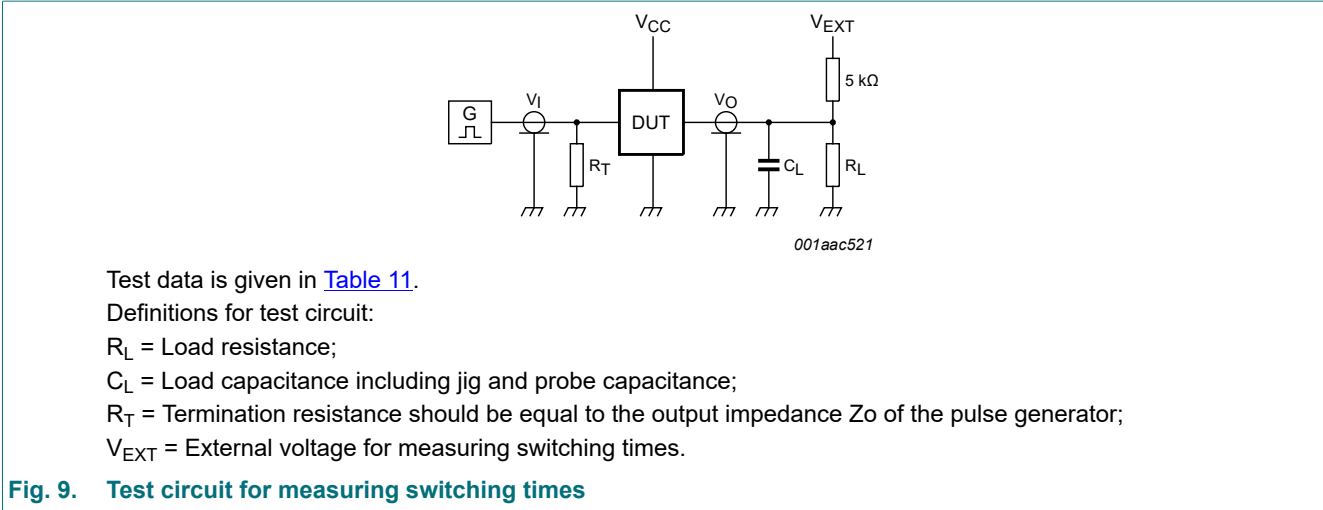
**Fig. 8.** The set input ( $\overline{SD}$ ) and reset input ( $\overline{RD}$ ) to output ( $Q$ ,  $\overline{Q}$ ) propagation delays, the set input ( $\overline{SD}$ ) and reset input ( $\overline{RD}$ ) pulse widths and the reset input ( $\overline{RD}$ ) to clock input ( $CP$ ) recovery time

**Table 10. Measurement points**

Supply voltage	Output	Input		
$V_{CC}$	$V_M$	$V_M$	$V_I$	$t_r = t_f$
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{CC}$	$\leq 3.0$ ns



Low-power D-type flip-flop with set and reset; positive-edge trigger



**Fig. 9. Test circuit for measuring switching times**

**Table 11. Test data**

Supply voltage	Load		$V_{EXT}$		
$V_{CC}$	$C_L$	$R_L$ [1]	$t_{PLH}$ , $t_{PHL}$	$t_{PZH}$ , $t_{PHZ}$	$t_{PZL}$ , $t_{PLZ}$
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times  $R_L = 5 \text{ k}\Omega$ .  
 For measuring propagation delays, setup and hold times and pulse width  $R_L = 1 \text{ M}\Omega$ .

12. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

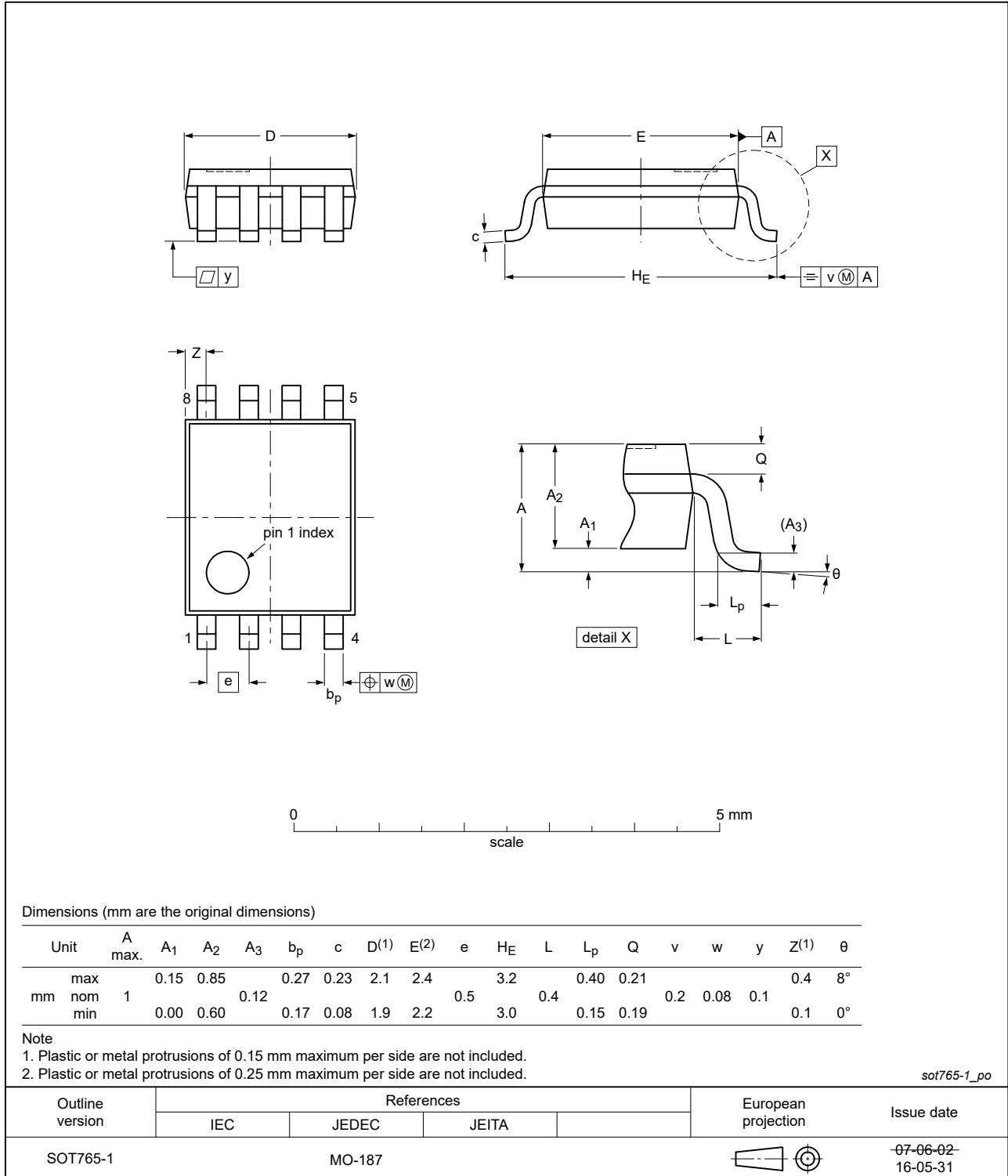


Fig. 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1



Fig. 11. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;  
8 terminals; body 1.35 x 1 x 0.5 mm

SOT1089



Fig. 12. Package outline SOT1089 (XSON8)

XSON8: extremely thin small outline package; no leads;  
8 terminals; body 1.2 x 1.0 x 0.35 mm

SOT1116

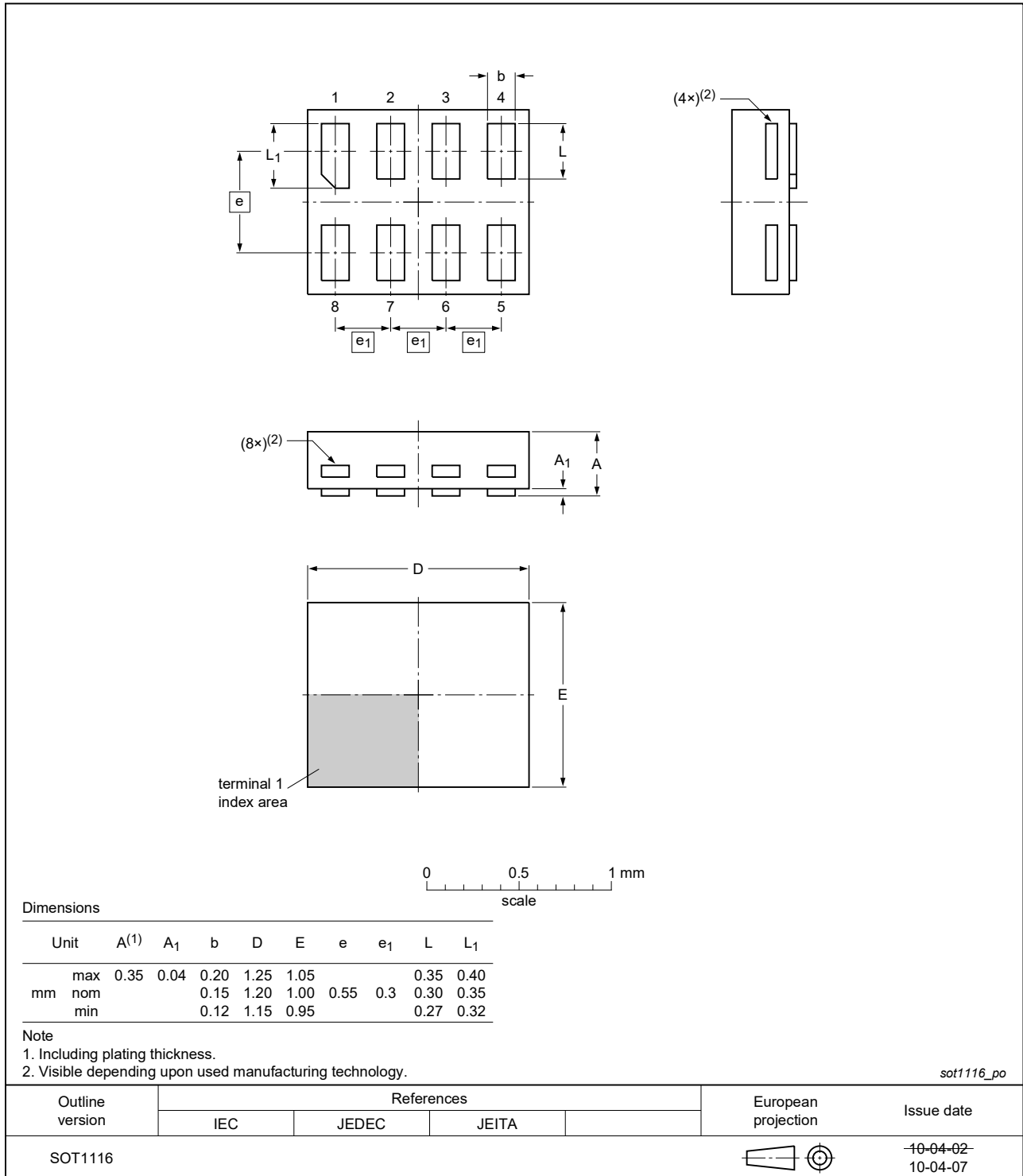


Fig. 13. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;  
8 terminals; body 1.35 x 1.0 x 0.35 mm

SOT1203



Fig. 14. Package outline SOT1203 (XSON8)

Low-power D-type flip-flop with set and reset; positive-edge trigger

X2SON8: plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 x 0.8 x 0.32 mm

SOT1233-2

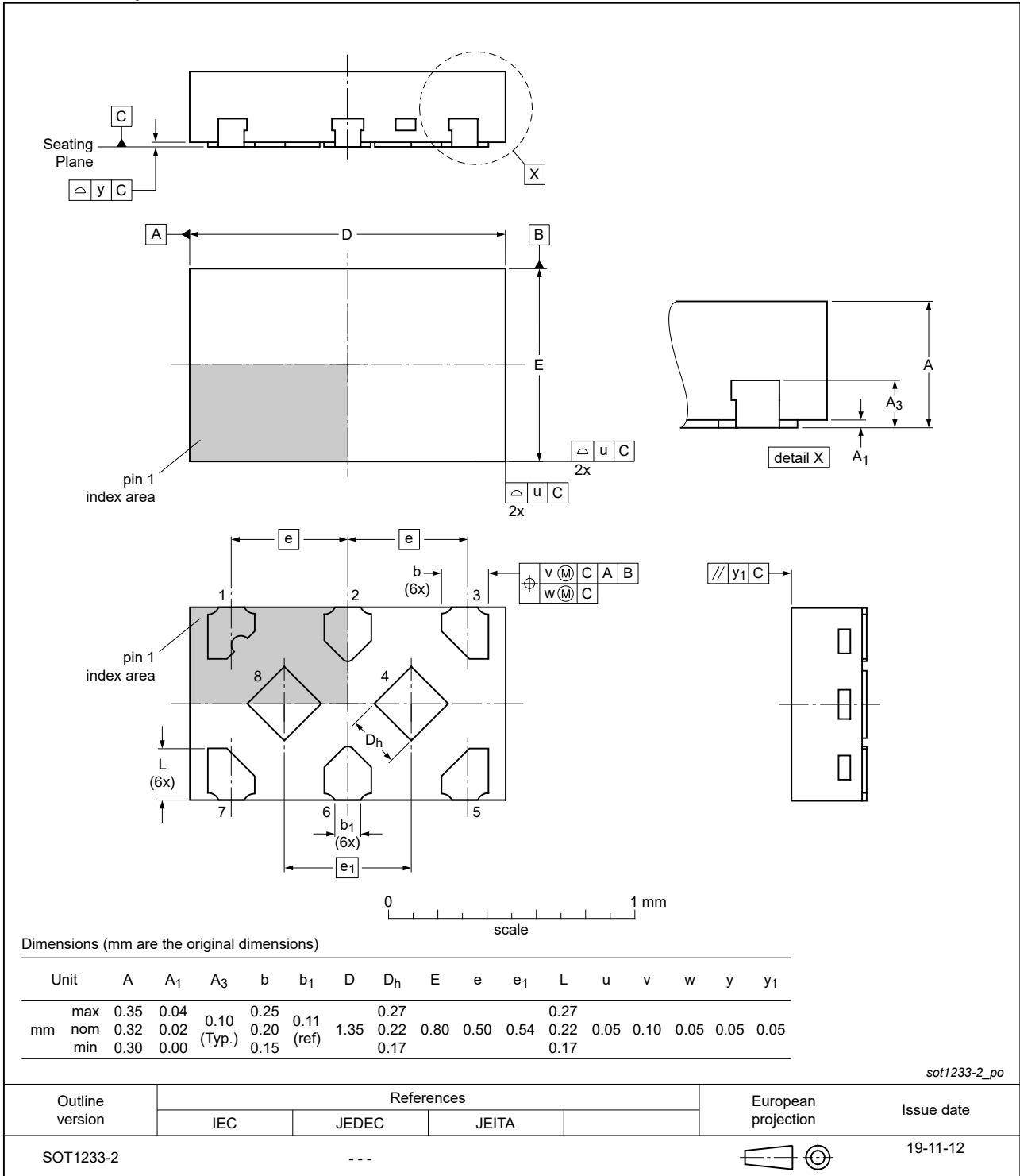


Fig. 15. Package outline SOT1233-2 (X2SON8)

## 13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

## 14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1G74 v.14	20230714	Product data sheet	-	74AUP1G74 v.13
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74AUP1G74 v.13	20230123	Product data sheet	-	74AUP1G74 v.12
Modifications:	<ul style="list-style-type: none"> <li>Type number 74AUP1G74GM (SOT902-2/XQFN8) removed.</li> </ul>			
74AUP1G74 v.12	20220620	Product data sheet	-	74AUP1G74 v.11
Modifications:	<ul style="list-style-type: none"> <li>SOT1233 (X2SON8) package changed to SOT1233-2 (X2SON8) package.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Table 6</a>: Derating values for <math>P_{tot}</math> total power dissipation have been updated.</li> </ul>			
74AUP1G74 v.11	20170703	Product data sheet	-	74AUP1G74 v.10
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Fig. 6</a> and <a href="#">Fig. 15</a> (drawings SOT1233/X2SON8) updated</li> <li>Type number 74AUP1G74GD removed.</li> </ul>			
74AUP1G74 v.10	20161028	Product data sheet	-	74AUP1G74 v.9
Modifications:	<ul style="list-style-type: none"> <li>Added type number 74AUP1G74GX (SOT1233/X2SON8)</li> </ul>			
74AUP1G74 v.9	20140106	Product data sheet	-	74AUP1G74 v.8
Modifications:	<ul style="list-style-type: none"> <li>Conditions for <math>f_{max}</math> corrected (errata).</li> </ul>			
74AUP1G74 v.8	20130123	Product data sheet	-	74AUP1G74 v.7
Modifications:	<ul style="list-style-type: none"> <li>For type number 74AUP1G74GD XSON8U has changed to XSON8.</li> </ul>			
74AUP1G74 v.7	20120522	Product data sheet	-	74AUP1G74 v.6
74AUP1G74 v.6	20111128	Product data sheet	-	74AUP1G74 v.5
74AUP1G74 v.5	20100726	Product data sheet	-	74AUP1G74 v.4
74AUP1G74 v.4	20080603	Product data sheet	-	74AUP1G74 v.3
74AUP1G74 v.3	20080207	Product data sheet	-	74AUP1G74 v.2
74AUP1G74 v.2	20070515	Product data sheet	-	74AUP1G74 v.1
74AUP1G74 v.1	20060825	Product data sheet	-	-



## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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