

**CMLDM7585****SURFACE MOUNT SILICON  
N-CHANNEL AND P-CHANNEL  
ENHANCEMENT-MODE  
COMPLEMENTARY MOSFETS****SOT-563 CASE**[www.centrasemi.com](http://www.centrasemi.com)**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CMLDM7585 consists of complementary N-Channel and P-Channel enhancement-mode silicon MOSFETs designed for high speed pulsed amplifier and driver applications. These MOSFETs offer very low  $r_{DS(ON)}$  and low threshold voltage.

**MARKING CODE: 87C****FEATURES:**

- ESD protection up to 1800V (Human Body Model)
- 350mW power dissipation
- Very low  $r_{DS(ON)}$
- Low threshold voltage
- Logic level compatible
- Small, SOT-563 surface mount package

**APPLICATIONS:**

- Load/Power switches
- Power supply converter circuits
- Battery powered portable devices

**MAXIMUM RATINGS:** ( $T_A=25^\circ\text{C}$ )

	SYMBOL	N-CH (Q1)	P-CH (Q2)	UNITS
Drain-Source Voltage	$V_{DS}$	20		V
Gate-Source Voltage	$V_{GS}$	8.0		V
Continuous Drain Current (Steady State)	$I_D$	650		mA
Maximum Pulsed Drain Current ( $t_p=10\mu\text{s}$ )	$I_{DM}$	1.3	1.0	A
Power Dissipation (Note 1)	$P_D$	350		mW
Power Dissipation (Note 2)	$P_D$	300		mW
Power Dissipation (Note 3)	$P_D$	150		mW
Operating and Storage Junction Temperature	$T_J, T_{stg}$	-65 to +150		$^\circ\text{C}$
Thermal Resistance (Note 1)	$\theta_{JA}$	357		$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS:** ( $T_A=25^\circ\text{C}$ )

SYMBOL	TEST CONDITIONS	N-CH (Q1)			P-CH (Q2)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
$I_{GSSF}, I_{GSSR}$	$V_{GS}=4.5\text{V}, V_{DS}=0$	-	-	1.0	-	-	10	$\mu\text{A}$
$I_{DSS}$	$V_{DS}=16\text{V}, V_{GS}=0$	-	-	100	-	-	100	nA
$BV_{DSS}$	$V_{GS}=0, I_D=250\mu\text{A}$	20	-	-	20	-	-	V
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.5	-	1.1	0.5	-	1.0	V
$V_{SD}$	$V_{GS}=0, I_S=200\text{mA}$	-	-	1.1	-	-	-	V
$V_{SD}$	$V_{GS}=0, I_S=250\text{mA}$	-	-	-	-	-	1.1	V
$r_{DS(ON)}$	$V_{GS}=4.5\text{V}, I_D=600\text{mA}$	-	0.14	0.23	-	-	-	$\Omega$
$r_{DS(ON)}$	$V_{GS}=4.5\text{V}, I_D=350\text{mA}$	-	-	-	-	0.25	0.36	$\Omega$
$r_{DS(ON)}$	$V_{GS}=2.5\text{V}, I_D=500\text{mA}$	-	0.2	0.275	-	-	-	$\Omega$
$r_{DS(ON)}$	$V_{GS}=2.5\text{V}, I_D=300\text{mA}$	-	-	-	-	0.37	0.5	$\Omega$
$r_{DS(ON)}$	$V_{GS}=1.8\text{V}, I_D=350\text{mA}$	-	-	0.7	-	-	-	$\Omega$
$r_{DS(ON)}$	$V_{GS}=1.8\text{V}, I_D=150\text{mA}$	-	-	-	-	-	0.8	$\Omega$

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0mm<sup>2</sup>(2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0mm<sup>2</sup>(3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4mm<sup>2</sup>

R4 (5-June 2013)

**CMLDM7585**

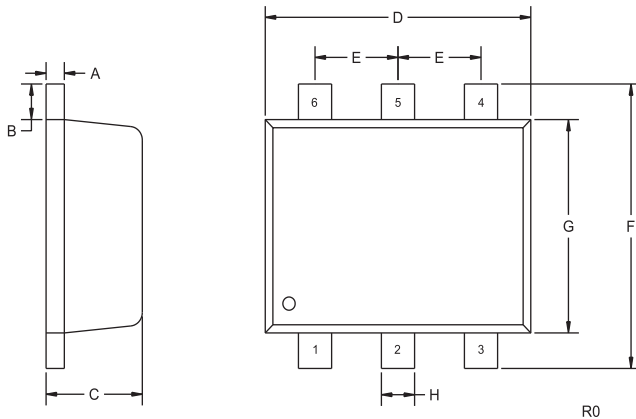
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**ELECTRICAL CHARACTERISTICS - Continued:** ( $T_A=25^\circ\text{C}$ )

SYMBOL	TEST CONDITIONS	N-CH (Q1)		P-CH (Q2)		UNITS
		MIN	TYP	MIN	TYP	
gFS	$V_{DS}=10\text{V}, I_D=400\text{mA}$	1.0	-	-	-	S
gFS	$V_{DS}=10\text{V}, I_D=200\text{mA}$	-	-	0.2	-	S
$C_{rss}$	$V_{DS}=16\text{V}, V_{GS}=0, f=1.0\text{MHz}$	-	18	-	25	pF
$C_{iss}$	$V_{DS}=16\text{V}, V_{GS}=0, f=1.0\text{MHz}$	-	100	-	100	pF
$C_{oss}$	$V_{DS}=16\text{V}, V_{GS}=0, f=1.0\text{MHz}$	-	16	-	21	pF
$Q_{g(\text{tot})}$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=500\text{mA}$	-	1.58	-	-	nC
$Q_{g(\text{tot})}$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=200\text{mA}$	-	-	-	1.2	nC
$Q_{gs}$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=500\text{mA}$	-	0.17	-	-	nC
$Q_{gs}$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=200\text{mA}$	-	-	-	0.24	nC
$Q_{gd}$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=500\text{mA}$	-	0.24	-	-	nC
$Q_{gd}$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=200\text{mA}$	-	-	-	0.36	nC
$t_{\text{on}}$	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=200\text{mA}, R_G=10\Omega$	-	10	-	38	ns
$t_{\text{off}}$	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=200\text{mA}, R_G=10\Omega$	-	25	-	48	ns

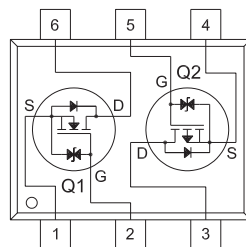
**SOT-563 CASE - MECHANICAL OUTLINE**



SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.004	0.007	0.10	0.18
B	0.008		0.20	
C	0.022	0.024	0.56	0.60
D	0.059	0.067	1.50	1.70
E	0.020		0.50	
F	0.061	0.067	1.55	1.70
G	0.047		1.20	
H	0.006	0.012	0.15	0.30

SOT-563 (REV: R0)

**PIN CONFIGURATION**



**LEAD CODE:**

- 1) Source Q1
- 2) Gate Q1
- 3) Drain Q2
- 4) Source Q2
- 5) Gate Q2
- 6) Drain Q1

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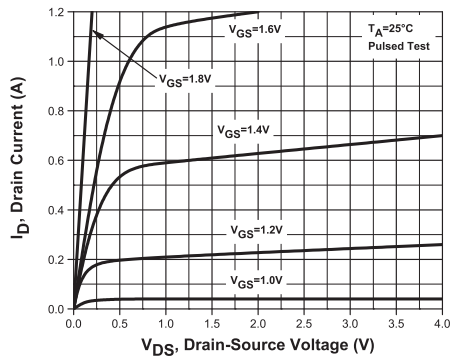
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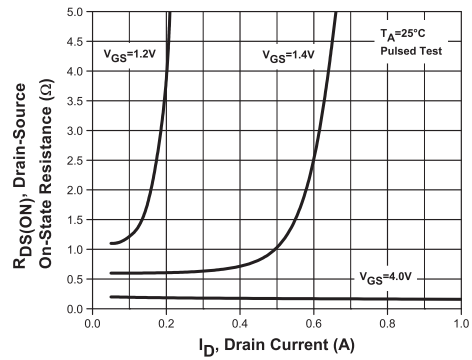


### N-CHANNEL TYPICAL ELECTRICAL CHARACTERISTICS

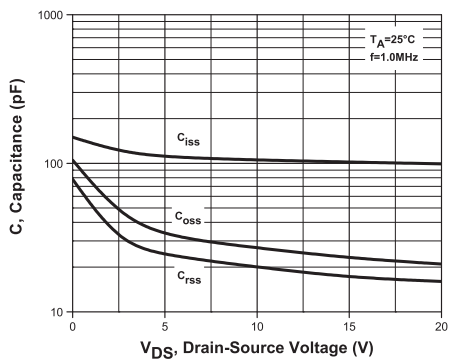
Output Characteristics



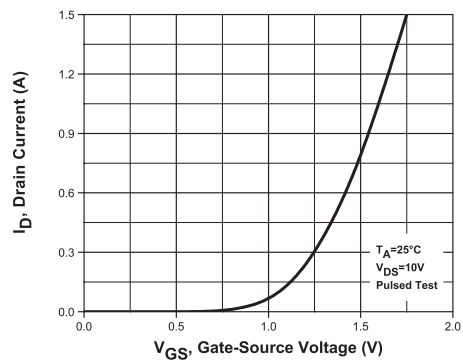
Drain Source On Resistance



Capacitance



Transfer Characteristics



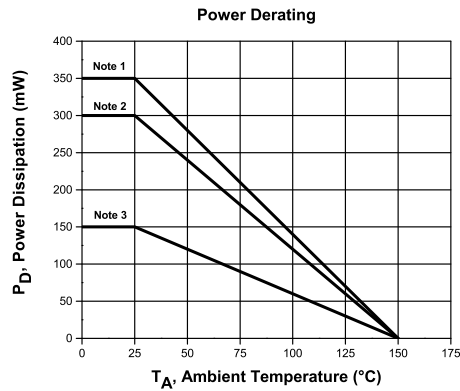
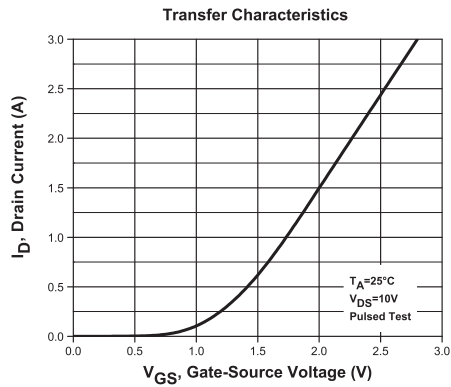
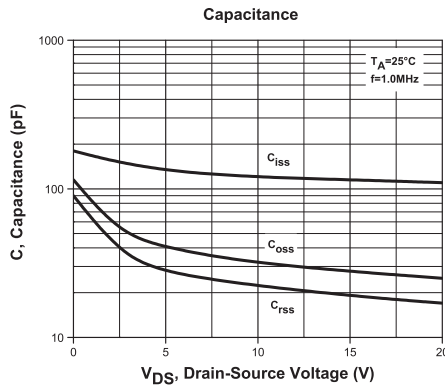
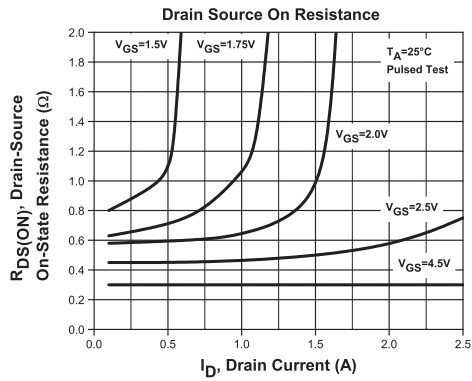
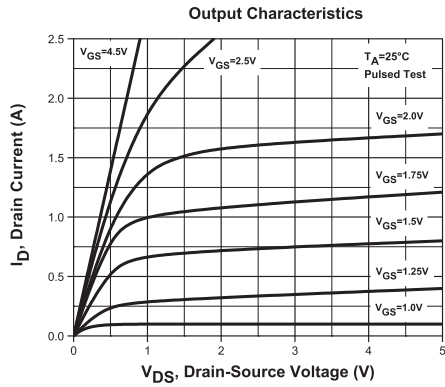
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### P-CHANNEL TYPICAL ELECTRICAL CHARACTERISTICS



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