SPI Interface, Low C_{ON} and Q_{INJ}, ±15 V/+12 V, 1.8 V Logic Control, 8:1/Dual 4:1 Mux Switches

Data Sheet **ADGS1208/ADGS1209**

FEATURES

SPI interface with error detection
Includes CRC, invalid read/write address, and SCLK count error detection
Supports burst mode and daisy-chain mode
Industry standard SPI Mode 0 and SPI Mode 3 interface compatible
Round robin mode allows switching times that are comparable with a parallel interface
Four general-purpose digital outputs that can be used to control other devices
<1 pC charge injection over full signal range
1 pF off capacitance
V_{SS} to V_{DD} analog signal range
Fully specified at ±15 V and +12 V
1.8 V logic compatibility with 2.7 V ≤ V_L ≤ 3.3 V
24-lead LFCSP package

APPLICATIONS

Audio and video routing
Automatic test equipment
Data acquisition systems
Battery-powered systems
Sample-and-hold systems
Communication systems

GENERAL DESCRIPTION

The ADGS1208/ADGS1209 are analog multiplexers comprising eight single channels and four differential channels, respectively. A serial peripheral interface (SPI) controls the switches. The SPI interface has robust error detection features, such as cyclic redundancy check (CRC) error detection, invalid read/write address detection, and SCLK count error detection.

It is possible to daisy-chain multiple ADGS1208/ADGS1209 devices together. Daisy-chain mode enables the configuration of multiple devices with a minimal amount of digital lines. The ADGS1208/ADGS1209 can also operate in burst mode to decrease the time between SPI commands.

iCMOS® construction ensures ultralow power dissipation, making the devices ideally suited for portable and battery-powered instruments.

Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

FUNCTIONAL BLOCK DIAGRAMS

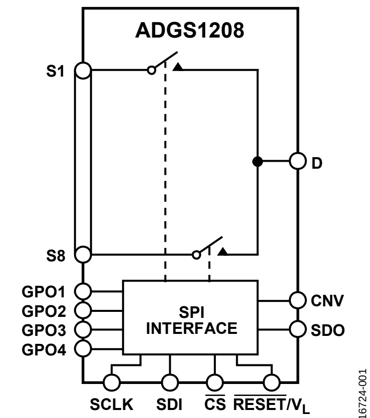

Figure 1. ADGS1208 Functional Block Diagram

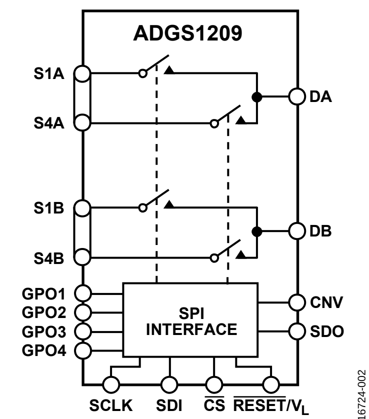

Figure 2. ADGS1209 Functional Block Diagram

The ultralow on capacitance (C_{ON}) and exceptionally low charge injection (Q_{INJ}) of these multiplexers make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required.

PRODUCT HIGHLIGHTS

1. SPI interface removes the need for parallel conversion, logic traces, and reduces GPIO channel count.
2. Daisy-chain mode removes additional logic traces when multiple devices are used.
3. CRC error detection, invalid read/write address detection, and SCLK count error detection ensure a robust digital interface.
4. CRC and error detection capabilities allow the use of the ADGS1208/ADGS1209 in safety critical systems.

Rev. 0 Document Feedback

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REVISION HISTORY

4/2018—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, V_L = 2.7 V to 5.5 V, and GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	150			Ω typ	V_S = ±10 V, I_S = −1 mA, see Figure 39
	200	240	270	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On Resistance Match Between Channels, ΔR_{ON}	3.5			Ω typ	V_S = ±10 V, I_S = −1 mA
	6	10	12	Ω max	
On Resistance Flatness, $R_{FLAT (ON)}$	35			Ω typ	V_S = ±10 V, I_S = −1 mA
	64	76	83	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.003			nA typ	V_S = ±10 V, V_D = ∓ 10 V, see Figure 36
	±0.1	±0.6	±1.0	nA max	
Drain Off Leakage, I_D (Off)	±0.003			nA typ	V_S = ±10 V, V_D = ∓ 10 V, see Figure 36
	±0.1	±0.6	±1.0	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.02			nA typ	V_S = V_D = ±10 V, see Figure 32
	±0.3	±0.6	±1.0	nA max	
DIGITAL OUTPUTS					
SDO					
Output Voltage					
Low, V_{OL}			0.4	V max	Sink current (I_{SINK}) = 5 mA
			0.2	V max	I_{SINK} = 1 mA
High Impedance Leakage Current	0.001			μA typ	Output voltage (V_{OUT}) = V_{GND} or V_L
			±0.1	μA max	
High Impedance Output Capacitance	4			pF typ	
GPOx					
Output Voltage					
High, V_{OH}			V_L − 0.2 V	V min	I_{SOURCE} = 100 μA
Low, V_{OL}			0.2	V max	I_{SINK} = 100 μA
Timing					
t_{ON}	95			ns typ	C_L = 15 pF, see Figure 44
	115	115	115	ns max	
t_{OFF}	15			ns typ	C_L = 15 pF, see Figure 44
	20	25	25	ns max	
Break-Before-Make Time Delay, t_D	50			ns typ	C_L = 15 pF, see Figure 45
			35	ns min	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DIGITAL INPUTS/OUTPUTS					
Input Voltage					
High, V_{INH}			2	V min	$3.3\ V < V_L \leq 5.5\ V$
			1.35	V min	$2.7\ V \leq V_L \leq 3.3\ V$
Low, V_{INL}			0.8	V max	$3.3\ V < V_L \leq 5.5\ V$
			0.8	V max	$2.7\ V \leq V_L \leq 3.3\ V$
Input Current, I_{INL} or I_{INH}	0.001			µA typ	Input voltage (V_{IN}) = V_{GND} or V_L
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	90			ns typ	R_L = 300 Ω, C_L = 35 pF
	145	170	195	ns max	V_S = 10 V, see Figure 41
t_{ON} (EN)	92			ns typ	R_L = 300 Ω, C_L = 35 pF
	110	140	155	ns max	V_S = 10 V, see Figure 42
t_{OFF} (EN)	120			ns typ	R_L = 300 Ω, C_L = 35 pF
	135	170	190	ns max	V_S = 10 V, see Figure 42
Break-Before-Make Time Delay, t_D	32			ns typ	R_L = 300 Ω, C_L = 35 pF
			7	ns min	V_{S1} = V_{S2} = 10 V, see Figure 40
Charge Injection, Q_{INJ}	0.4			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 43
Off Isolation	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34
Channel to Channel Crosstalk	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33
Total Harmonic Distortion Plus Noise	0.15			% typ	R_L = 110 Ω, 15 V p-p, f = 20 Hz to 20 kHz, see Figure 38
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF, see Figure 37
ADGS1208	550			MHz typ	
ADGS1209	630			MHz typ	
Insertion Loss	−6			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 37
C_S (Off)	1			pF typ	V_S = 0 V, f = 1 MHz
	1.6			pF max	V_S = 0 V, f = 1 MHz
C_D (Off)					
ADGS1208	5			pF typ	V_S = 0 V, f = 1 MHz
	5.5			pF max	V_S = 0 V, f = 1 MHz
ADGS1209	2			pF typ	V_S = 0 V, f = 1 MHz
	3.5			pF max	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)					
ADGS1208	5			pF typ	V_S = 0 V, f = 1 MHz
	6.5			pF max	V_S = 0 V, f = 1 MHz
ADGS1209	3			pF typ	V_S = 0 V, f = 1 MHz
	4.5			pF max	V_S = 0 V, f = 1 MHz

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.002			µA typ	All switches open
			1.0	µA max	
	220			µA typ	All switches closed, V_L = 5.5 V
			380	µA max	
	270			µA typ	All switches closed, V_L = 2.7 V
			440	µA max	
I_L					
Inactive	6.3			µA typ	Digital inputs = 0 V or V_L
			8.0	µA max	
Inactive, SCLK = 1 MHz	14			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 5 V
	7			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 3 V
SCLK = 50 MHz	390			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 5 V
	210			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 3 V
Inactive, SDI = 1 MHz	15			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 5 V
	7.5			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 3 V
SDI = 25 MHz	230			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 5 V
	120			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 3 V
Active at 50 MHz	1.8			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 5.5 V
			2.1	mA max	
	0.7			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 2.7 V
			1.0	mA max	
I_{SS}	0.002			µA typ	Digital inputs = 0 V or V_L
			1.0	µA max	
V_{DD}/V_{SS}			±4.5	V min	GND = 0 V
			±16.5	V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, V_L = 2.7 V to 5.5 V, and GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	380			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA, see Figure 39
	475	570	625	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On Resistance Match Between Channels, ΔR_{ON}	5			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	16	26	27	Ω max	
On Resistance Flatness, $R_{FLAT (ON)}$	200			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.003			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 36
	±0.1	±0.6	±1.0	nA max	
Drain Off Leakage, I_D (Off)	±0.003			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 36
	±0.1	±0.6	±1.0	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.02			nA typ	V_S = V_D = 1 V/10 V, see Figure 32
	±0.3	±0.6	±1.0	nA max	
DIGITAL OUTPUT					
Output Voltage					
Low, V_{OL}			0.4	V max	I_{SINK} = 5 mA
			0.2	V max	I_{SINK} = 1 mA
High Impedance Leakage Current	0.001			µA typ	V_{OUT} = V_{GND} or V_L
			±0.1	µA max	
High Impedance Output Capacitance	4			pF typ	
GPOx					
Output Voltage					
High, V_{OH}			V_L − 0.2 V	V min	I_{SOURCE} = 100 µA
Low, V_{OL}			0.2	V max	I_{SINK} = 100 µA
Timing					
t_{ON}	95			ns typ	C_L = 15 pF, see Figure 44
	115	115	115	ns max	
t_{OFF}	15			ns typ	C_L = 15 pF, see Figure 44
	20	25	25	ns max	
Break-Before-Make Time Delay, t_D	50			ns typ	C_L = 15 pF, see Figure 45
			35	ns min	
DIGITAL INPUTS					
Input Voltage					
High, V_{INH}			2	V min	3.3 V < V_L ≤ 5.5 V
			1.35	V min	2.7 V ≤ V_L ≤ 3.3 V
Low, V_{INL}			0.8	V max	3.3 V < V_L ≤ 5.5 V
			0.8	V max	2.7 V ≤ V_L ≤ 3.3 V
Input Current, I_{INL} or I_{INH}	0.001			µA typ	V_{IN} = V_{GND} or V_L
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTIC[1]					
Transition Time, $t_{TRANSITION}$	110			ns typ	R_L = 300 Ω, C_L = 35 pF
	185	220	245	ns max	V_S = 8 V, see Figure 41
t_{ON} (EN)	120			ns typ	R_L = 300 Ω, C_L = 35 pF
	140	190	210	ns max	V_S = 8 V, see Figure 42
t_{OFF} (EN)	130			ns typ	R_L = 300 Ω, C_L = 35 pF
	145	195	215	ns max	V_S = 8 V, see Figure 42
Break-Before-Make Time Delay, t_D	35			ns typ	R_L = 300 Ω, C_L = 35 pF
			15	ns min	V_{S1} = V_{S2} = 8 V, see Figure 40
Charge Injection, Q_{INJ}	−0.2			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 43
Off Isolation	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34
Channel to Channel Crosstalk	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF, see Figure 37
ADGS1208	450			MHz typ	
ADGS1209	550			MHz typ	
Insertion Loss	−12			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 37
C_S (Off)	1.2			pF typ	V_S = 0 V, f = 1 MHz
	1.8			pF max	V_S = 0 V, f = 1 MHz
C_D (Off)					
ADGS1208	6			pF typ	V_S = 0 V, f = 1 MHz
	6.5			pF max	V_S = 0 V, f = 1 MHz
ADGS1209	3.2			pF typ	V_S = 0 V, f = 1 MHz
	4			pF max	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)					
ADGS1208	6			pF typ	V_S = 0 V, f = 1 MHz
	7			pF max	V_S = 0 V, f = 1 MHz
ADGS1209	4			pF typ	V_S = 0 V, f = 1 MHz
	4.5			pF max	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.002			µA typ	All switches open
			1.0	µA max	
	220			µA typ	All switches closed, V_L = 5.5 V
			380	µA max	
	270			µA typ	All switches closed, V_L = 2.7 V
			440	µA max	
I_L					
Inactive	6.3			µA typ	Digital inputs = 0 V or V_L
			8.0	µA max	
Inactive, SCLK = 1 MHz	14			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 5 V
	7			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 3 V
SCLK = 50 MHz	390			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 5 V
	210			µA typ	$\overline{CS}$ = V_L and SDI = 0 V or V_L, V_L = 3 V
Inactive, SDI = 1 MHz	15			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 5 V
	7.5			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 3 V
SDI = 25 MHz	230			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 5 V
	120			µA typ	$\overline{CS}$ and SCLK = 0 V or V_L, V_L = 3 V
Active at 50 MHz	1.8			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 5.5 V
			2.1	mA max	
	0.7			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 2.7 V
			1.0	mA max	
V_{DD}			5	V min	GND = 0 V, V_{SS} = 0 V
			16.5	V max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx

Table 3. ADGS1208, One Channel On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR D[1]				
V_{DD} = +15 V, V_{SS} = −15 V ($θ_{JA}$ = 63.1°C/W)	29.3	21.9	14.1	mA max
V_{DD} = 12 V, V_{SS} = 0 V ($θ_{JA}$ = 63.1°C/W)	37.7	27.3	19	mA max

[1] Sx refers to the S1 to S8 pins.

Table 4. ADGS1209, Two Channels On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx[1]				
V_{DD} = +15 V, V_{SS} = −15 V ($θ_{JA}$ = 63.1°C/W)	21.8	16.1	9.9	mA max
V_{DD} = 12 V, V_{SS} = 0 V ($θ_{JA}$ = 63.1°C/W)	28.2	21.2	13.4	mA max

[1] Sx refers to the S1A to S4A and S1B to S4B pins, and Dx refers to the DA and DB pins.

TIMING CHARACTERISTICS

V_L = 2.7 V to 5.5 V, GND = 0 V, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Guaranteed by design and characterization, not production tested.

Table 5.

Parameter	Limit	Unit	Test Conditions/Comments
TIMING CHARACTERISTICS			
t_1	20	ns min	SCLK or CNV period
t_2	8	ns min	SCLK or CNV high pulse width
t_3	8	ns min	SCLK or CNV low pulse width
t_4	10	ns min	$\overline{CS}$ falling edge to SCLK or CNV active edge
t_5	6	ns min	Data setup time
t_6	8	ns min	Data hold time
t_7	10	ns min	SCLK or CNV active edge to $\overline{CS}$ rising edge
t_8	20	ns max	$\overline{CS}$ falling edge to SDO data available
t_9[1]	20	ns max	SCLK falling edge to SDO data available
t_{10}	20	ns max	$\overline{CS}$ rising edge to SDO returns to high impedance
t_{11}	20	ns min	$\overline{CS}$ high time between SPI commands
t_{12}	8	ns min	$\overline{CS}$ falling edge to SCLK or CNV edge rejection
t_{13}	8	ns min	$\overline{CS}$ rising edge to SCLK or CNV edge rejection

[1] Measured with the 1 kΩ pull-up resistor to V_L and 20 pF load. t_9 determines the maximum SCLK frequency when SDO is used.

Timing Diagrams

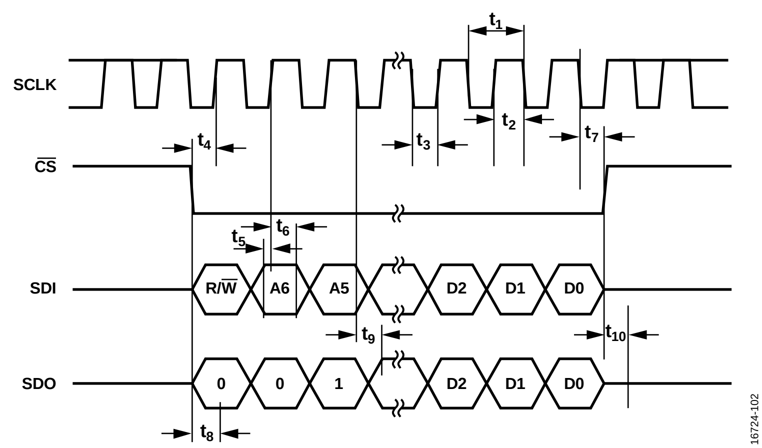


Figure 3. Address Mode Timing Diagram

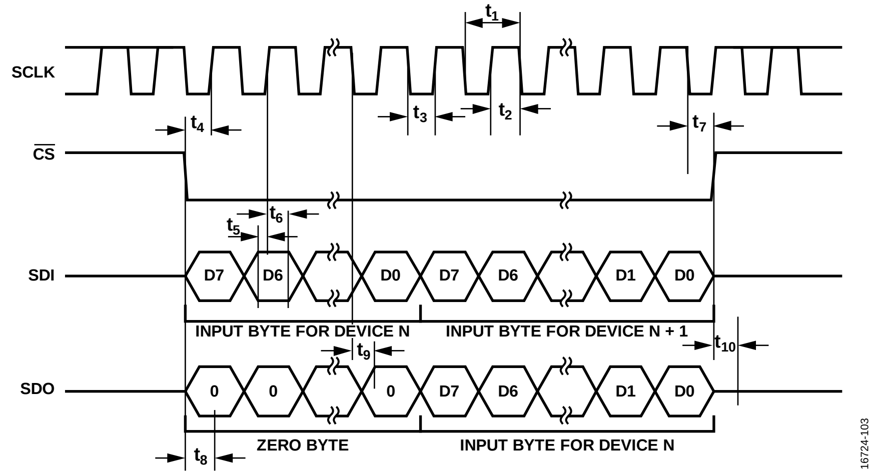


Figure 4. Daisy Chain Timing Diagram

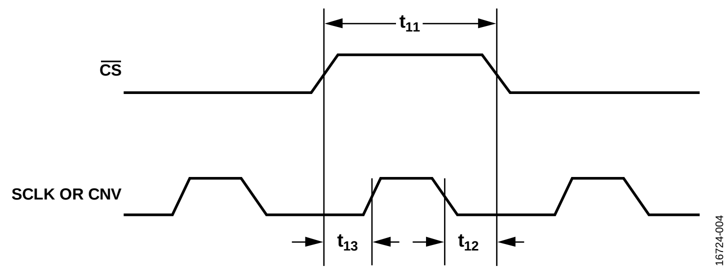


Figure 5. SCLK or CNV and CS Timing Diagram

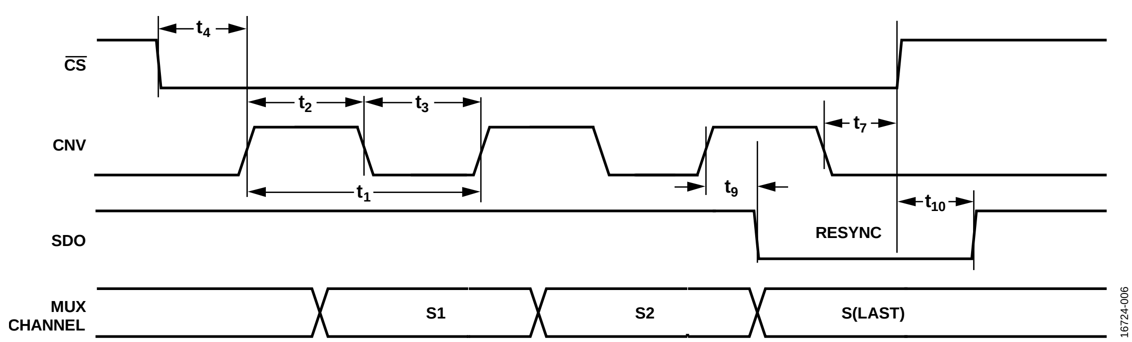


Figure 6. Round Robin Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
V_L to GND	−0.3 V to +6 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	−0.3 V to +6 V
Peak Current, Sx or Dx Pins[2]	59 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx[2, 3]	Data + 15%
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb-Free	260(+0/−5)°C

[1] Overvoltages at the digital Sx and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.
[2] Sx refers to the S1 to S4 pins, and Dx refers to the D1 to D4 pins.
[3] See Table 4 and Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

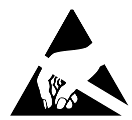
Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JCB}[1]	Unit
CP-24-15[2]	63.1	27.3	°C/W

[1] θ_{JCB} is the junction to the bottom of the case value.
[2] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD51.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

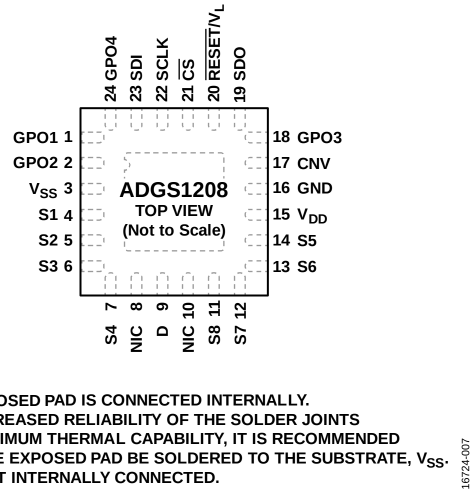


Figure 7. ADGS1208 Pin Configuration

Table 8. ADGS1208 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GPO1	General-Purpose Output 1. This pin is a digital output.
2	GPO2	General-Purpose Output 2. This pin is a digital output.
3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, tie this pin to ground.
4	S1	Source Terminal 1. This pin can be an input or output.
5	S2	Source Terminal 2. This pin can be an input or output.
6	S3	Source Terminal 3. This pin can be an input or output.
7	S4	Source Terminal 4. This pin can be an input or output.
8, 10	NIC	Not Internally Connected. These pins are not connected internally.
9	D	Drain Terminal. This pin can be an input or output.
11	S8	Source Terminal 8. This pin can be an input or output.
12	S7	Source Terminal 7. This pin can be an input or output.
13	S6	Source Terminal 6. This pin can be an input or output.
14	S5	Source Terminal 5. This pin can be an input or output.
15	V_{DD}	Most Positive Power Supply Potential.
16	GND	Ground (0 V) Reference.
17	CNV	Channel Cycle Input. When in round robin mode, the CNV pin is used to cycle through the selected channels.
18	GPO3	General-Purpose Output 3. This pin is a digital output.
19	SDO	Serial Data Output. This pin can be used for daisy chaining a number of these devices together or for reading back the data stored in a register for diagnostic purposes. The serial data is propagated on the falling edge of SCLK. Pull this open-drain output to V_L with an external resistor.
20	$\overline{RESET}/V_L$	$\overline{RESET}$/Logic Power Supply Input (V_L). Under normal operation, drive the $\overline{RESET}/V_L$ pin with a 2.7 V to 5.5 V supply. Pull the $\overline{RESET}/V_L$ pin low to complete a hardware reset. After a reset, all switches open, and the appropriate registers are set to their default values.
21	$\overline{CS}$	Active Low Control Input. $\overline{CS}$ is the frame synchronization signal for the input data.
22	SCLK	Serial Clock Input. Data is captured on the positive edge of SCLK. Data can be transferred at rates of up to 50 MHz.
23	SDI	Serial Data Input. Data is captured on the positive edge of the serial clock input.
24	GPO4	General-Purpose Output 4. This pin is a digital output.
	EPAD	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the exposed pad be soldered to the substrate, V_{SS}.

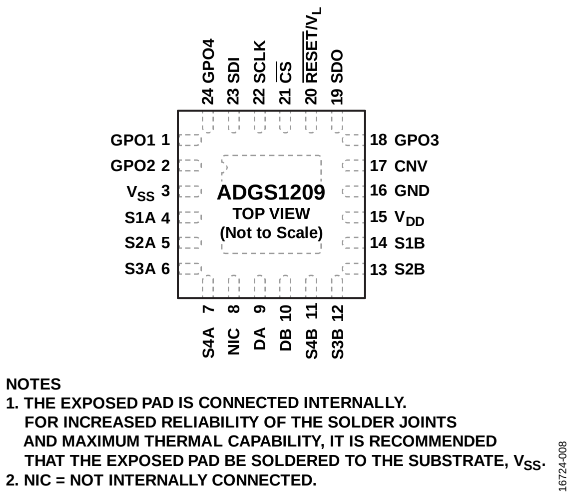


Figure 8. ADGS1209 Pin Configuration

Table 9. ADGS1209 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GPO1	General-Purpose Output 1. This pin is a digital output.
2	GPO2	General-Purpose Output 2. This pin is a digital output.
3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, tie this pin to ground.
4	S1A	Source Terminal 1A. This pin can be an input or output.
5	S2A	Source Terminal 2A. This pin can be an input or output.
6	S3A	Source Terminal 3A. This pin can be an input or output.
7	S4A	Source Terminal 4A. This pin can be an input or output.
8	NIC	Not Internally Connected. This pin is not internally connected.
9	DA	Drain Terminal A. This pin can be an input or output.
10	DB	Drain Terminal B. This pin can be an input or output.
11	S4B	Source Terminal 4B. This pin can be an input or output.
12	S3B	Source Terminal 3B. This pin can be an input or output.
13	S2B	Source Terminal 2B. This pin can be an input or output.
14	S1B	Source Terminal 1B. This pin can be an input or output.
15	V_{DD}	Most Positive Power Supply Potential.
16	GND	Ground (0 V) Reference.
17	CNV	Channel Cycle Input. When in round robin mode, the CNV pin is used to cycle through the selected channels.
18	GPO3	General-Purpose Output 3. This pin is a digital output.
19	SDO	Serial Data Output. This pin can be used for daisy chaining a number of these devices together or for reading back the data stored in a register for diagnostic purposes. The serial data is propagated on the falling edge of SCLK. Pull this open-drain output to V_L with an external resistor.
20	$\overline{RESET}/V_L$	$\overline{RESET}$/Logic Power Supply Input (V_L). Under normal operation, drive the $\overline{RESET}/V_L$ pin with a 2.7 V to 5.5 V supply. Pull the $\overline{RESET}/V_L$ pin low to complete a hardware reset. After a reset, all switches open, and the appropriate registers are set to their default values.
21	$\overline{CS}$	Active Low Control Input. $\overline{CS}$ is the frame synchronization signal for the input data.
22	SCLK	Serial Clock Input. Data is captured on the positive edge of SCLK. Data can be transferred at rates of up to 50 MHz.
23	SDI	Serial Data Input. Data is captured on the positive edge of the serial clock input.
24	GPO4	General-Purpose Output 4. This pin is a digital output.
	EPAD	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the exposed pad be soldered to the substrate, V_{SS}.

TYPICAL PERFORMANCE CHARACTERISTICS

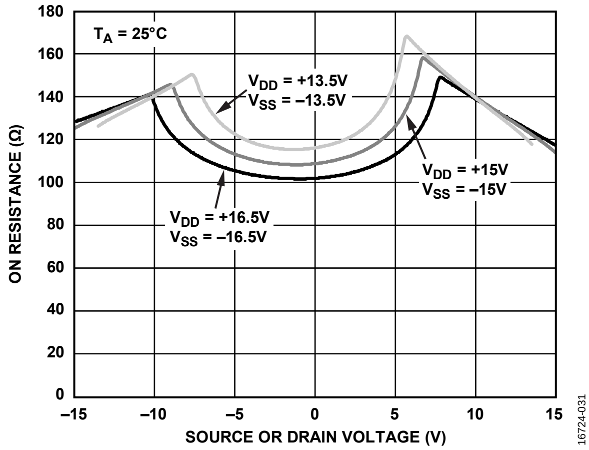


Figure 9. On Resistance vs. Source or Drain Voltage for Various Dual Supplies

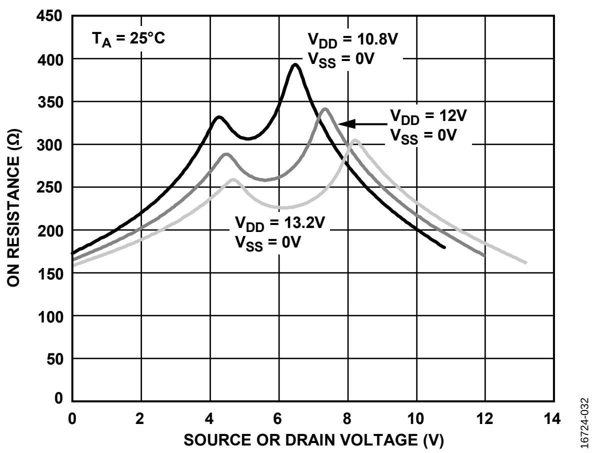


Figure 10. On Resistance vs. Source or Drain Voltage for Various Single Supplies

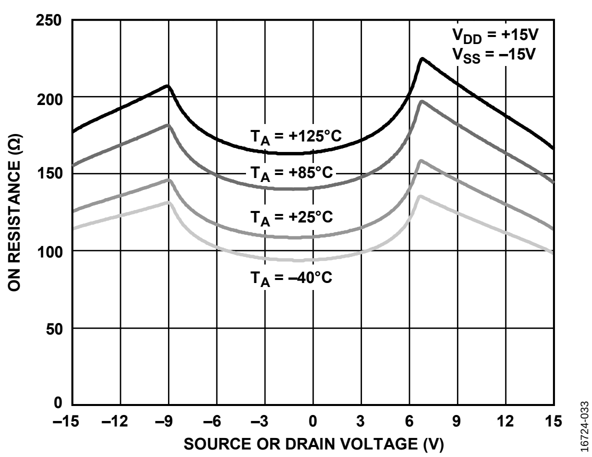


Figure 11. On Resistance vs. Source or Drain Voltage for Various Temperatures, ±15 V Dual Supply

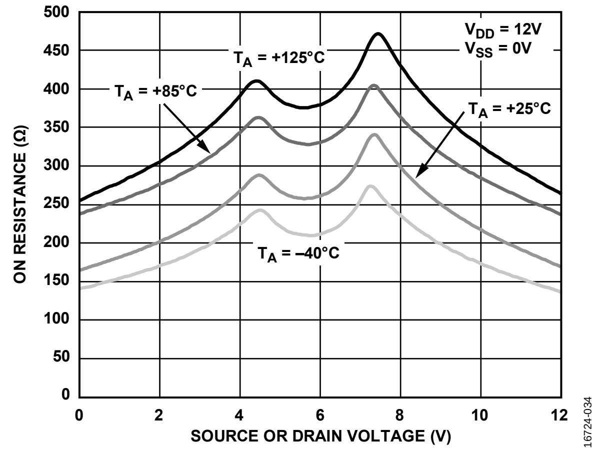


Figure 12. On Resistance vs. Source or Drain Voltage for Various Temperatures, 12 V Single Supply

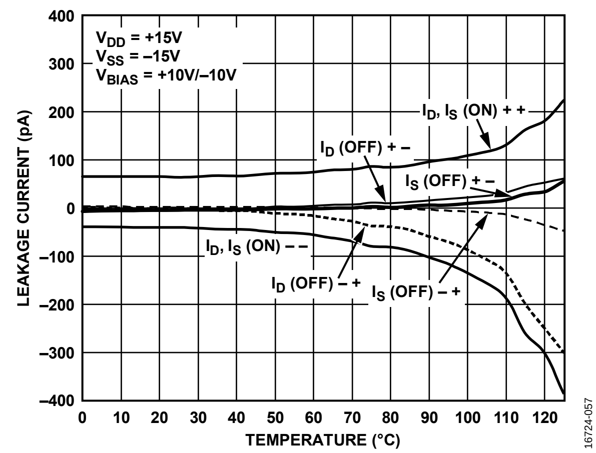


Figure 13. Leakage Current vs. Temperature, ±15 V Dual Supply

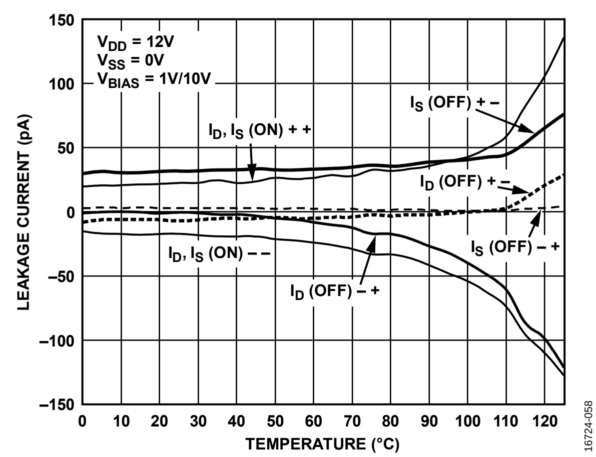


Figure 14. Leakage Current vs. Temperature, 12 V Single Supply

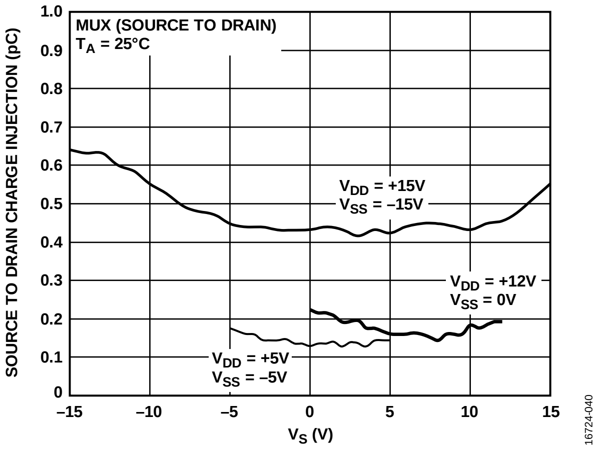


Figure 15. Source to Drain Charge Injection vs. Source Voltage (V_S)

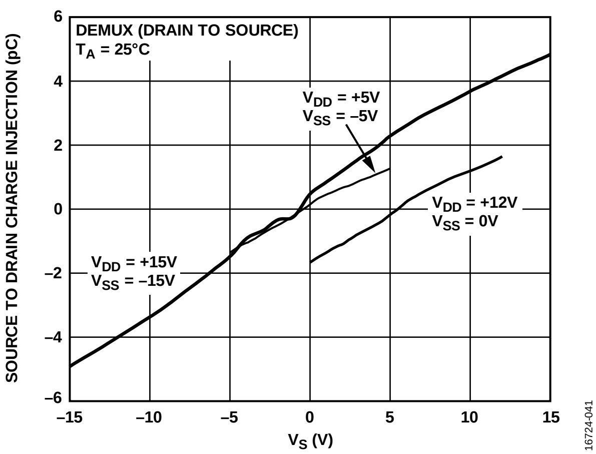


Figure 16. Drain to Source Charge Injection vs. Source Voltage (V_S)

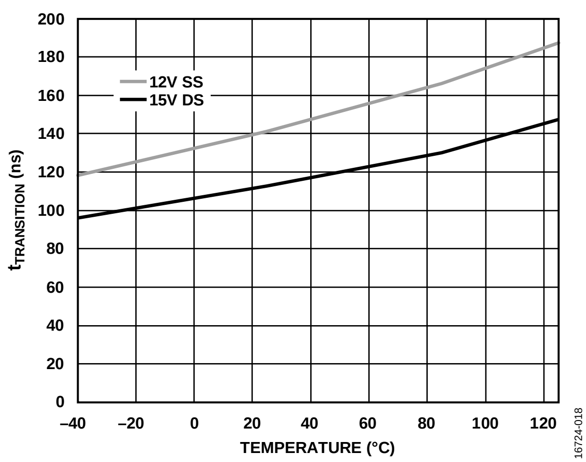


Figure 17. Transition Time ($t_{TRANSITION}$) vs. Temperature for Single Supply (SS) and Dual Supply (DS)

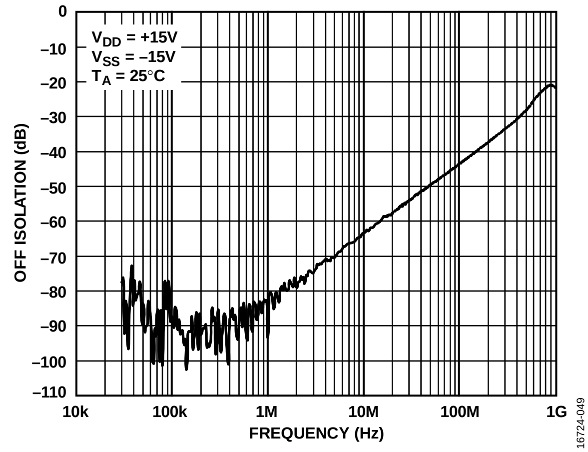


Figure 18. Off Isolation vs. Frequency, ±15 V Dual Supply

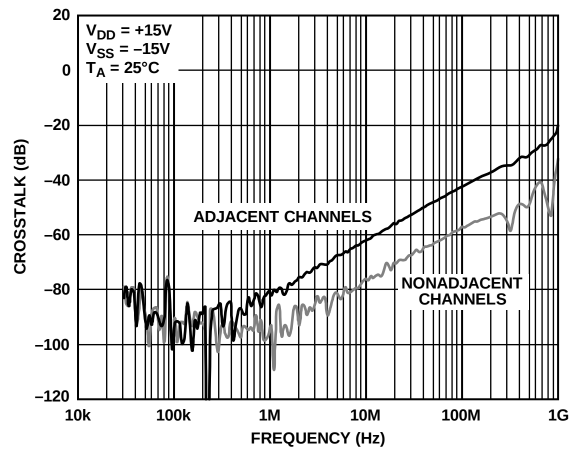


Figure 19. ADGS1208 Crosstalk vs. Frequency, ±15 V Dual Supply

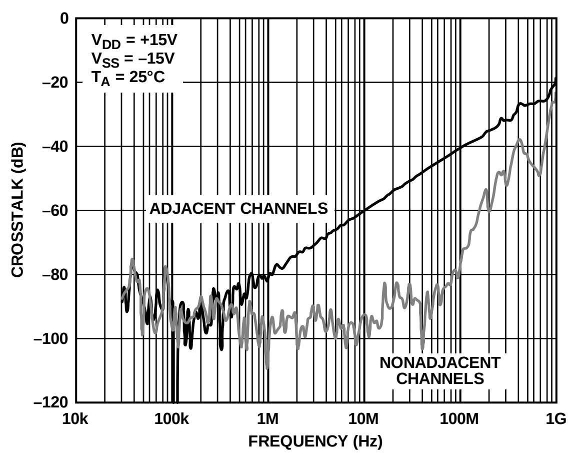


Figure 20. ADGS1209 Crosstalk vs. Frequency, ±15 V Dual Supply

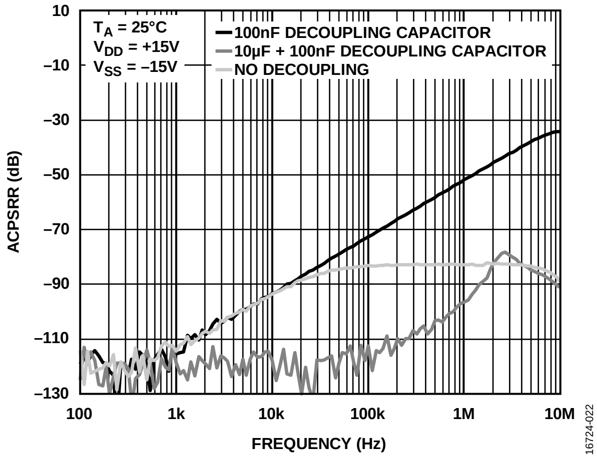


Figure 21. AC Power Supply Rejection Ratio (ACPSRR) vs. Frequency, ±15 V Dual Supply

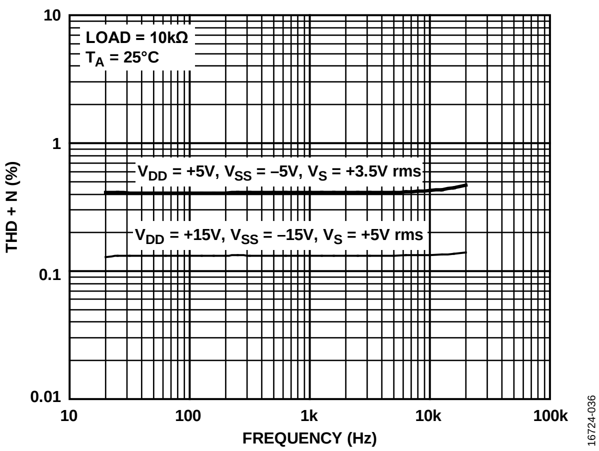


Figure 22. THD + N vs. Frequency

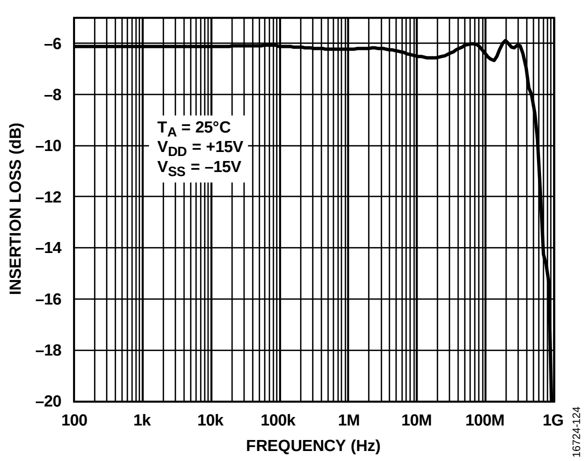


Figure 23. ADGS1208 Insertion Loss vs. Frequency, ±15 V Dual Supply

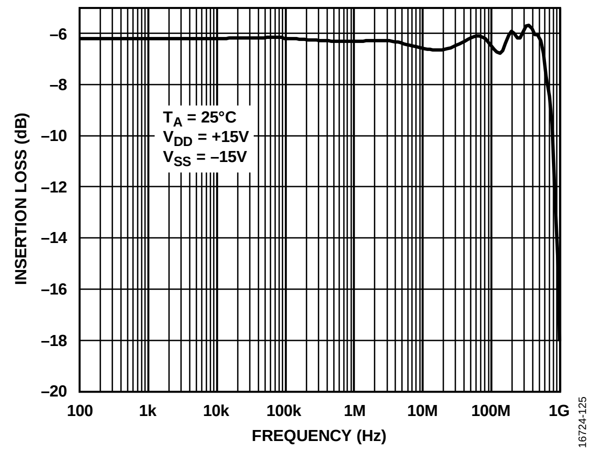


Figure 24. ADGS1209 Insertion Loss vs. Frequency, ±15 V Dual Supply

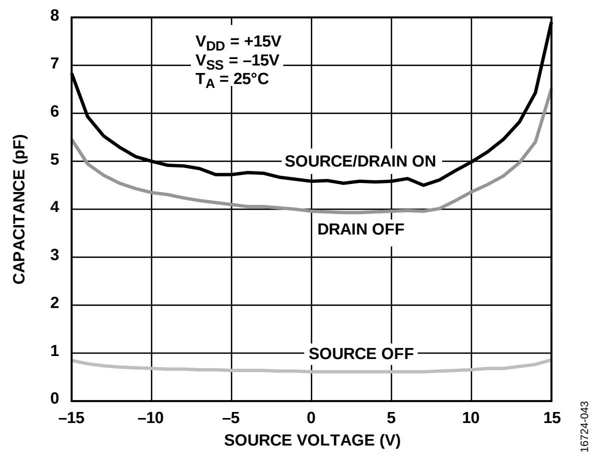


Figure 25. ADG1208 Capacitance vs. Source Voltage, ±15 V Dual Supply

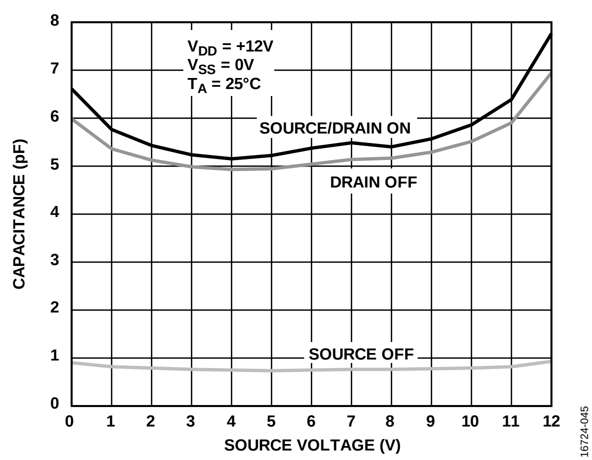


Figure 26. ADG1208 Capacitance vs. Source Voltage, 12 V Single Supply

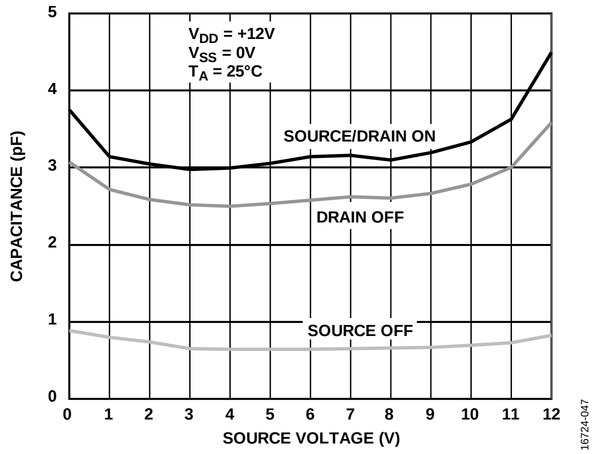


Figure 27. ADG1209 Capacitance vs. Source Voltage, 12 V Single Supply

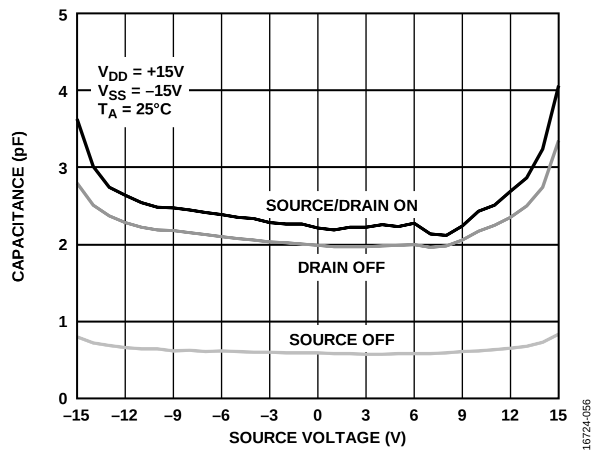


Figure 28. ADG1209 Capacitance vs. Source Voltage, ±15 V Dual Supply

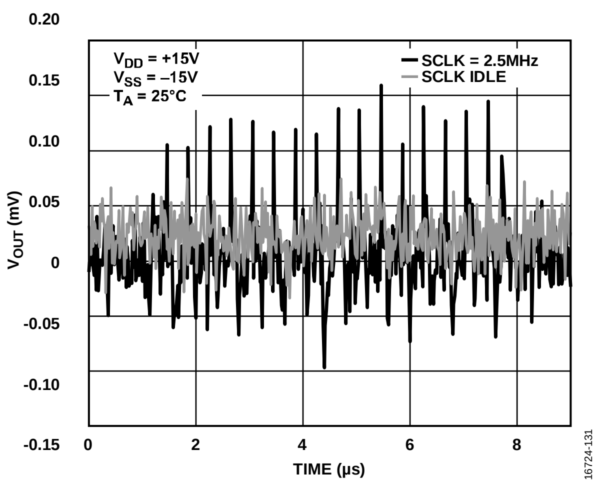


Figure 29. Digital Feedthrough

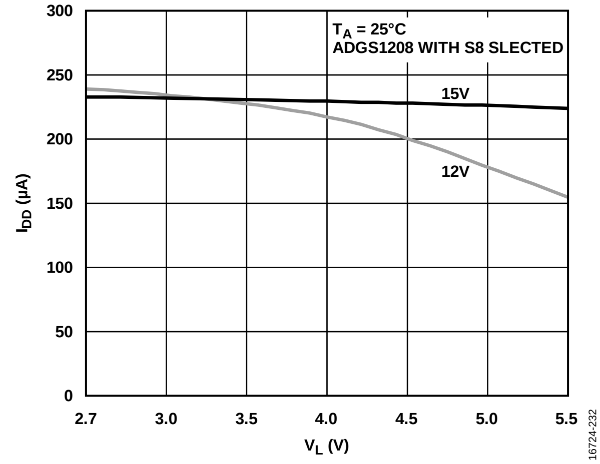


Figure 30. I_{DD} vs. V_L

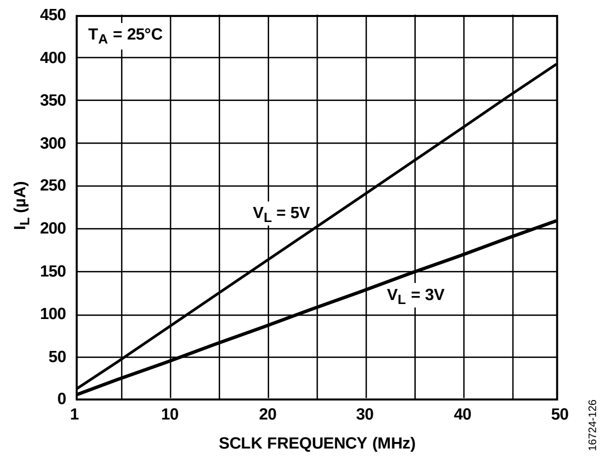


Figure 31. I_L vs. SCLK Frequency when $\overline{CS}$ is High

TEST CIRCUITS

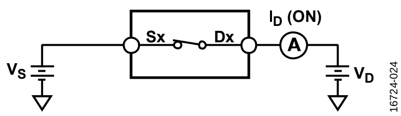


Figure 32. On Leakage

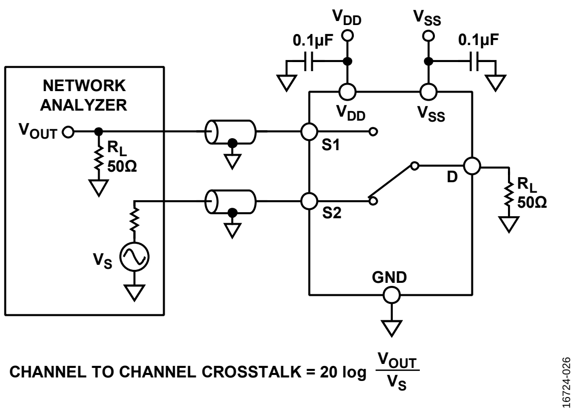


Figure 33. Channel to Channel Crosstalk

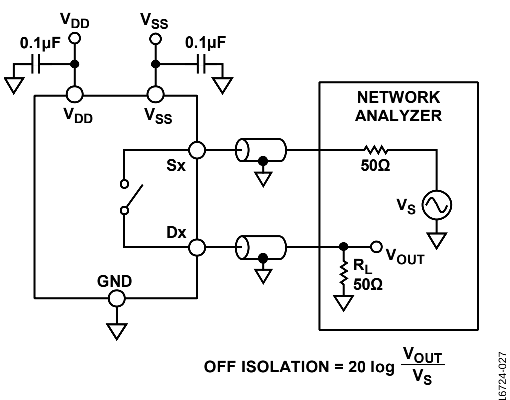
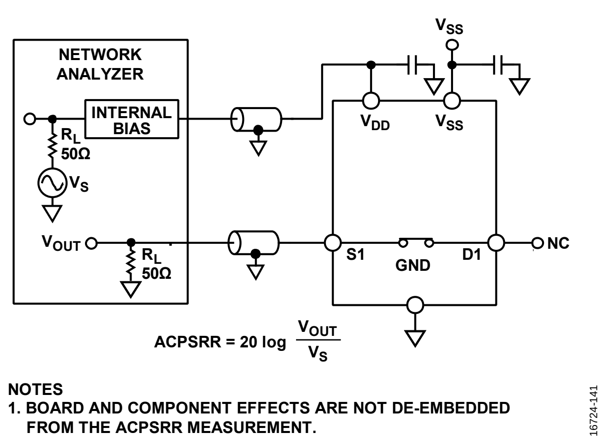


Figure 34. Off Isolation



NOTES
1. BOARD AND COMPONENT EFFECTS ARE NOT DE-EMBEDDED FROM THE ACPSRR MEASUREMENT.

Figure 35. ACPSRR

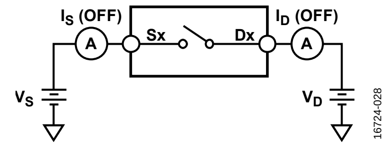


Figure 36. Off Leakage

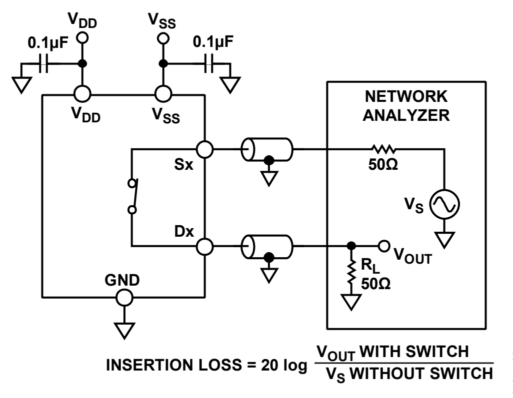


Figure 37. Insertion Loss/−3 dB Bandwidth

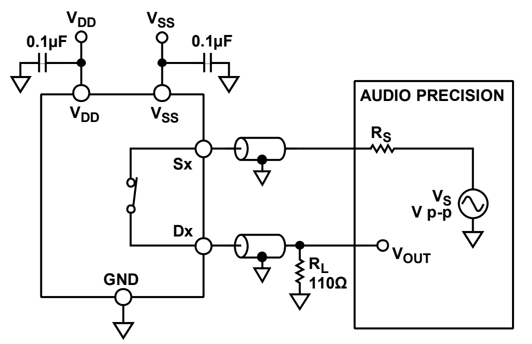


Figure 38. THD + N

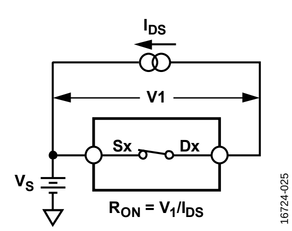


Figure 39. On Resistance

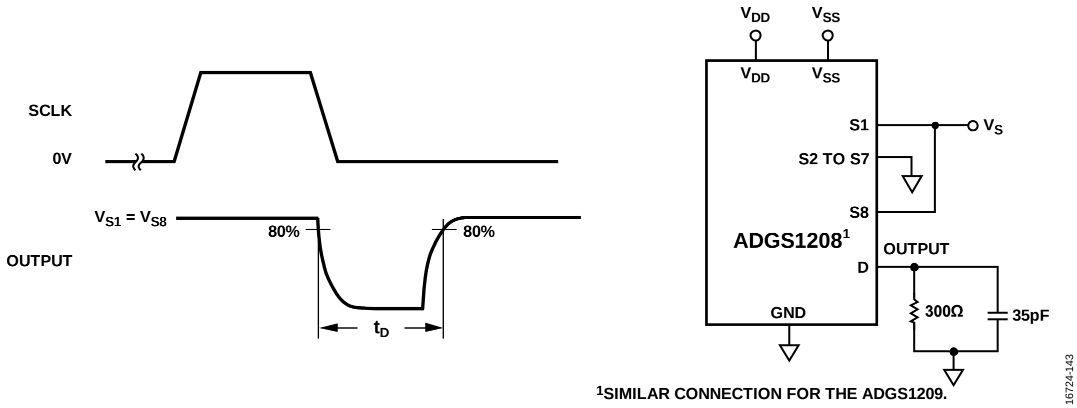


Figure 40. Break-Before-Make Time Delay, t_D

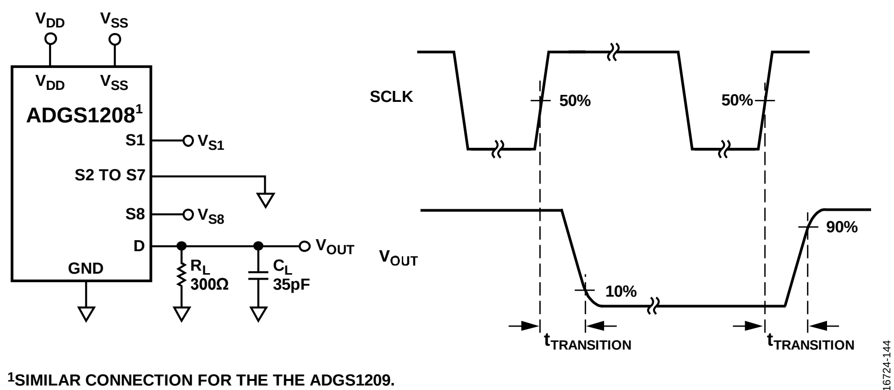


Figure 41. Transition Time, $t_{TRANSITION}$

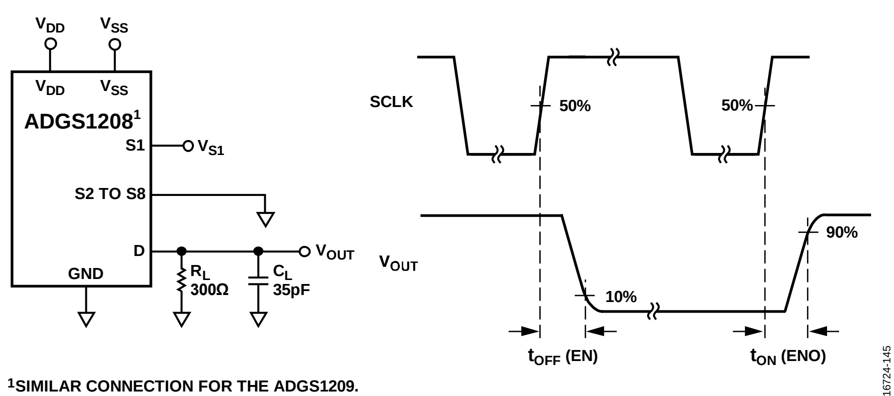


Figure 42. Switching Times, t_{ON} (EN) and t_{OFF} (EN)

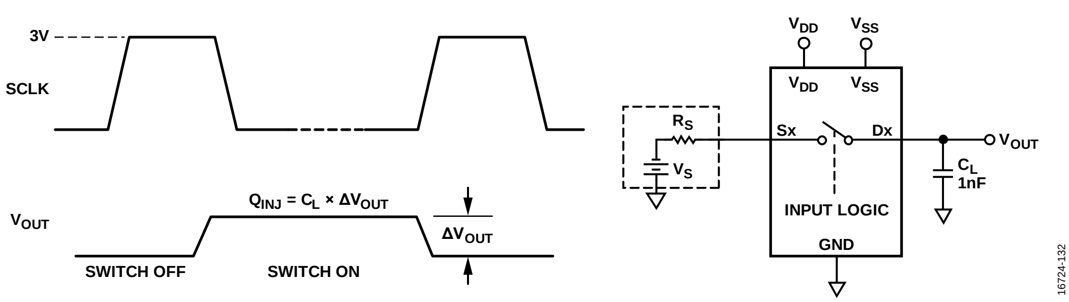


Figure 43. Charge Injection, Q_{INJ}

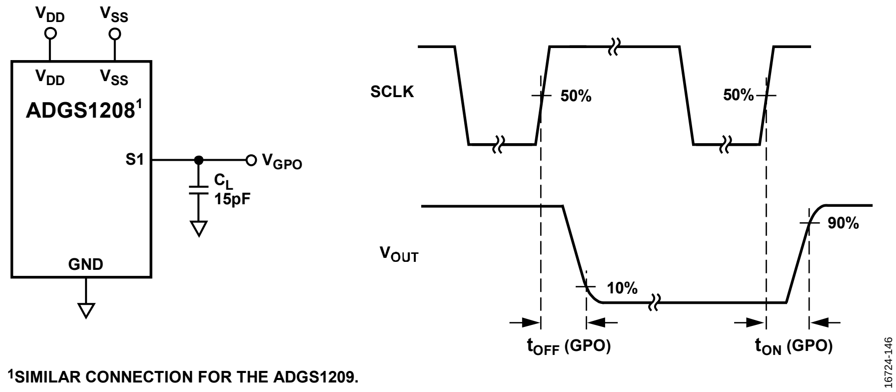


Figure 44. GPOx Timing, t_{ON} and t_{OFF}

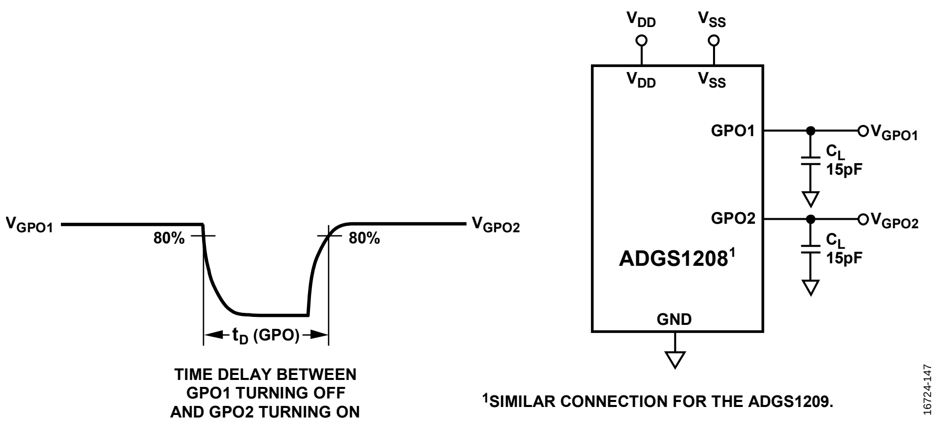


Figure 45. GPOx Break-Before-Make Time Delay, t_D

TERMINOLOGY

I_{DD}
I_{DD} is the positive supply current.

I_{SS}
I_{SS} is the negative supply current.

V_D, V_S
V_D and V_S are the analog voltage on Terminal Dx and Terminal Sx, respectively.

R_{ON}
R_{ON} is the ohmic resistance between Terminal Dx and Terminal Sx.

ΔR_{ON}
ΔR_{ON} is the difference between the R_{ON} of any two channels.

$R_{FLAT (ON)}$
$R_{FLAT (ON)}$ is flatness that is the difference between maximum and minimum on resistance values measured over the specified analog signal range.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_S (On), I_D (On)
I_S (On) and I_D (On) are the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} are the low and high input currents of the digital inputs, respectively.

C_S (Off)
C_S (Off) is the off switch source capacitance, which is measured with reference to ground.

C_D (Off)
C_D (Off) is the off switch drain capacitance, which is measured with reference to ground.

C_S (On), C_D (On)
C_S (On) and C_D (On) are the on switch capacitances, which are measured with reference the ground.

C_{IN}
C_{IN} is the digital input capacitance.

t_{ON}
t_{ON} is the delay between applying the digital control input and the output switching on.

t_{OFF}
t_{OFF} is the delay between applying the digital control input and the output switching off.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk
Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

−3 dB Bandwidth
Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response
On response is the frequency response of the on switch.

Insertion Loss
Insertion loss is the loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)
THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. ACPSRR is a measure of the ability of the devices to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

THEORY OF OPERATION

The ADGS1208/ADGS1209 are a set of serially controlled analog multiplexers comprising eight single channels and four differential channels, respectively, with error detection features. SPI Mode 0 and SPI Mode 3 can be used with the devices, and they operate with SCLK frequencies up to 50 MHz. The default mode for the ADGS1208/ADGS1209 is address mode, in which the registers of the device are accessed by a 16-bit SPI command bounded by $\overline{CS}$. The SPI command becomes 24-bit if the user enables CRC error detection. Other error detection features include SCLK count error and invalid read/write error. If any of these SPI interface errors occur, they are detectable by reading the error flags register. The ADGS1208/ADGS1209 can also operate in two other modes, namely burst mode and daisy-chain mode.

The interface pins of the ADGS1208/ADGS1209 are $\overline{CS}$, SCLK, SDI, and SDO. Hold $\overline{CS}$ low when using the SPI interface. Data is captured on SDI on the rising edge of SCLK, and data is propagated out on SDO on the falling edge of SCLK. SDO has an open-drain output; thus, connect a pull-up to this output. When not pulled low by the ADGS1208/ADGS1209, SDO is in a high impedance state.

ADDRESS MODE

Address mode is the default mode for the ADGS1208/ADGS1209 on power-up. A single SPI frame in address mode is bounded by a $\overline{CS}$ falling edge and the succeeding $\overline{CS}$ rising edge. An SPI frame is comprised of 16 SCLK cycles. The timing diagram for address mode is shown in Figure 46. The first SDI bit indicates if the SPI command is a read or write command. When the first bit is set to 0, a write command is issued, and if the first bit is set to 1, a read command is issued. The next seven bits determine the target register address. The remaining eight bits provide the data to the addressed register. The last eight bits are ignored during a read command, because during these clock cycles, SDO propagates out the data contained in the addressed register.

The target register address of an SPI command is determined on the eighth SCLK rising edge. Data from this register propagates out on SDO from the ninth to the 16th SCLK falling edge during SPI reads. A register write occurs on the 16th SCLK rising edge during SPI writes.

During any SPI command, SDO sends out eight alignment bits on the first eight SCLK falling edges. The alignment bits observed at SDO are 0x25.

ERROR DETECTION FEATURES

Protocol and communication errors on the SPI interface are detectable. The three detectable errors are incorrect SCLK error detection, invalid read and write address error detection, and CRC error detection. Each error has a corresponding enable bit in the error configuration register. In addition, there is an error flag bit for each error in the error flags register.

Cyclic Redundancy Check (CRC) Error Detection

The CRC error detection feature extends a valid SPI frame by eight SCLK cycles. These eight extra cycles are needed to send the CRC byte for that SPI frame. The CRC byte is calculated by the SPI block using the 16-bit payload: the R/$\overline{W}$ bit, Register Address Bits[6:0], and Register Data Bits[7:0]. The CRC polynomial used in the SPI block is $x^8 + x^2 + x^1 + 1$ with a seed value of 0. For a timing diagram with CRC enabled, see Figure 47. Register writes occur at the 24th SCLK rising edge with CRC error checking enabled.

During an SPI write, the microcontroller/CPU provides the CRC byte through SDI. The SPI block checks the CRC byte just before the 24th SCLK rising edge. On this same edge, the register write is prevented if an incorrect CRC byte is received by the SPI interface. In the case that an incorrect CRC byte is detected, the CRC error flag is asserted in the error flags register.

During an SPI read, the CRC byte is provided to the microcontroller through SDO.

The CRC error detection feature is disabled by default and can be configured by the user through the error configuration register.

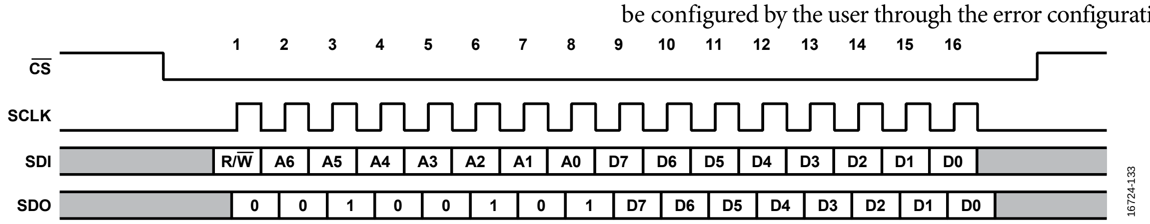


Figure 46. Address Mode Timing Diagram

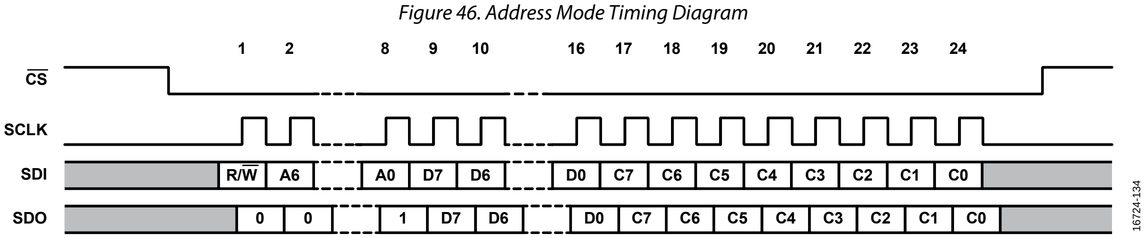


Figure 47. Timing Diagram with CRC Enabled

SCLK Count Error Detection

SCLK count error detection allows the user to detect if an incorrect number of SCLK cycles are sent by the microcontroller/CPU. When in address mode, with CRC disabled, 16 SCLK cycles are expected. If 16 SCLK cycles are not detected, the SCLK count error flag asserts in the error flags register. When less than 16 SCLK cycles are received by the device, a write to the register map never occurs. When the ADGS1208/ADGS1209 receive more than 16 SCLK cycles, a write to the memory map still occurs at the 16th SCLK rising edge, and the flag asserts in the error flags register. With CRC enabled, the expected number of SCLK cycles is 24. SCLK count error detection is enabled by default and can be configured by the user through the error configuration register.

Invalid Read/Write Address Error Detection

An invalid read/write address error detects when a nonexistent register address is a target for a read or write. In addition, this error asserts when a write to a read only register is attempted. The invalid read/write address error flag asserts in the error flags register when an invalid read/write address error occurs. The invalid read/write address error is detected on the ninth SCLK rising edge, which means a write to the register never occurs when an invalid address is targeted. Invalid read/write address error detection is enabled by default and can be disabled by the user through the error configuration register.

CLEARING THE ERROR FLAGS REGISTER

To clear the error flags register, write the special 16-bit SPI frame, 0x6CA9, to the device. This SPI command does not trigger the invalid read/write address error. When CRC is enabled, the user must also send the correct CRC byte for a successful error clear command. At the 16th or 24th SCLK rising edge, the error flags register resets to 0.

BURST MODE

The SPI interface can accept consecutive SPI commands without the need to de-assert the $\overline{CS}$ line, which is called burst mode. Burst mode is enabled through the burst enable register. This mode uses the same 16-bit command to communicate with the device. In addition, the response of the device at SDO is still aligned with the corresponding SPI command. Figure 48 shows an example of SDI and SDO during burst mode.

The invalid read/write address and CRC error checking functions operate similarly during burst mode as they do during address mode. However, SCLK count error detection operates in a slightly different manner. The total number of SCLK cycles within a given $\overline{CS}$ frame are counted, and if the total is not a multiple of 16, or a multiple of 24 when CRC is enabled, the SCLK count error flag asserts.

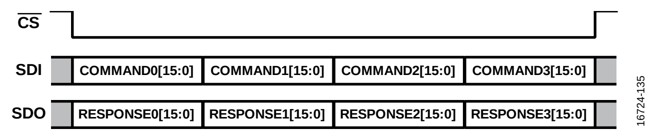


Figure 48. Burst Mode Frame

SOFTWARE RESET

When in address mode, the user can initiate a software reset. To do so, write two consecutive SPI commands, 0xA3 followed by 0x05, targeting Register 0x0B. After a software reset, all register values are set to default.

DAISY-CHAIN MODE

The connection of several ADGS1208/ADGS1209 devices in a daisy chain configuration is possible, and Figure 49 shows this setup. All devices share the same $\overline{CS}$ and SCLK line, whereas the SDO of a device forms a connection to the SDI of the next device, creating a shift register. In daisy-chain mode, SDO is an eight cycle delayed version of SDI. When in daisy-chain mode, all commands target the switch data register. Therefore, it is not possible to make configuration changes while in daisy-chain mode.

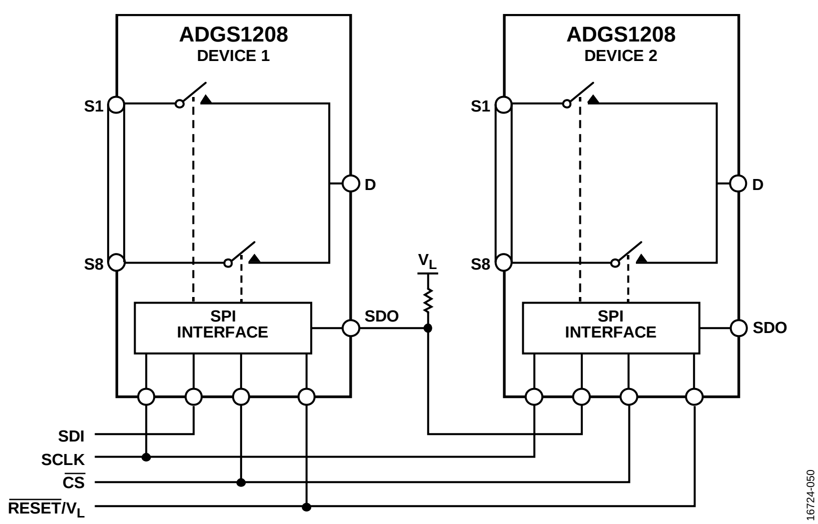


Figure 49. Two ADGS1208/ADGS1209 Devices Connected in a Daisy-Chain Configuration

The ADGS1208/ADGS1209 can only enter daisy-chain mode when in address mode by sending the 16-bit SPI command, 0x2500 (see Figure 50). When the ADGS1208/ADGS1209 receive this command, the SDO of the device sends out the same command because the alignment bits at SDO are 0x25, which allows multiple daisy-connected devices to enter daisy-chain mode in a single SPI frame. A hardware reset is required to exit daisy-chain mode.

For the timing diagram of a typical daisy-chain SPI frame, see Figure 51. When $\overline{CS}$ goes high, Device 1 writes Command 0, Bits[7:0] to its switch data register, Device 2 writes Command 1, Bits[7:0] to its switches, and so on. The SPI block uses the last eight bits it received through SDI to update the switches. After entering daisy chain mode, the first eight bits sent out by SDO on each device in the chain are 0x00. When $\overline{CS}$ goes high, the internal shift register value does not reset back to 0.

An SCLK rising edge reads in data on SDI while data is propagated out of SDO on an SCLK falling edge. The expected number of SCLK cycles must be a multiple of eight before $\overline{CS}$ goes high. When this is not the case, the SPI interface sends the last eight bits received to the switch data register.

POWER-ON RESET

The digital section of the ADGS1208/ADGS1209 goes through an initialization phase during V_L power up. This initialization also occurs after a hardware or software reset. After V_L power-up or a reset, ensure that a minimum of 120 µs from the time of power-up or reset before any SPI command is issued. Ensure that V_L does not drop out during the 120 µs initialization phase, because it may result in incorrect operation of the ADGS1208/ADGS1209.

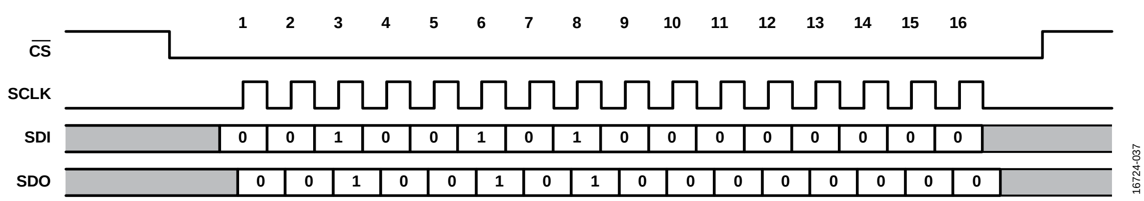


Figure 50. SPI Command to Enter Daisy-Chain Mode

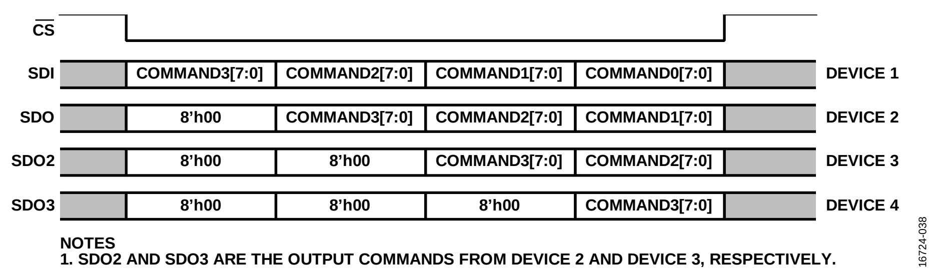


Figure 51. Example of an SPI Frame Where Four ADGS1208/ADGS1209 Devices Connect in Daisy-Chain Mode

ROUND ROBIN MODE

Round robin mode allows the ADGS1208/ADGS1209 to cycle through the channels faster by reducing the overhead needed from the digital interface to switch from one channel to the next. The round robin configuration register selects which channels are to be included in a cycle, while the CNV edge select register selects on which edge of CNV the ADGS1208/ ADGS1209 switch to the next channel in the sequence. At the end of the channel cycle, a resync pulse appears on SDO to inform the user that the current cycle ended and then it loops back to the start of the sequence of channels. Figure 52 shows an example of the round robin mode interface and Figure 53 shows the CNV signal of the analog-to-digital converter (ADC) being used in conjunction with the ADGS1208 in round robin mode.

After configuration completes, the round robin enable register allows the ADGS1208/ADGS1209 to enter round robin mode.

When in round robin mode, the SPI is no longer used to switch between channels. Instead, to switch from one channel to another, ensure that a digital signal is present on the CNV pin while $\overline{CS}$ is pulled low.

To exit round robin mode, either perform a hardware reset or send the 16-bit addressable mode SPI frames: 0xA318 followed by 0xE3B4. These are the only SPI commands recognized by the SPI interface while in round robin mode.

Round robin mode is significantly faster than addressable mode to cycle through channels because it removes the 16-bit overhead required to change input channel. In addition, round robin mode removes the need for SCLK to be running, which reduces the digital current consumption (I_L). The maximum CNV frequency is bound by the transition time of the device, along with the required settling time for the application.

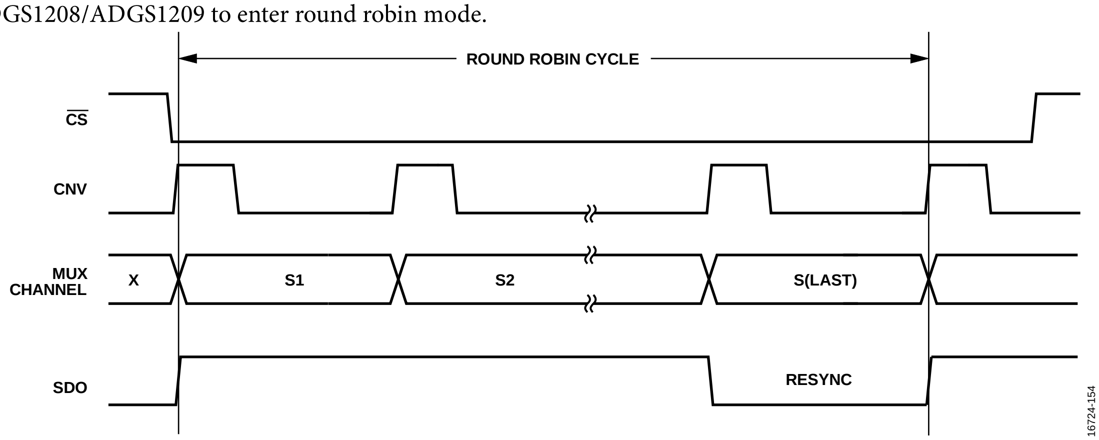


Figure 52. Round Robin Mode Interface Example

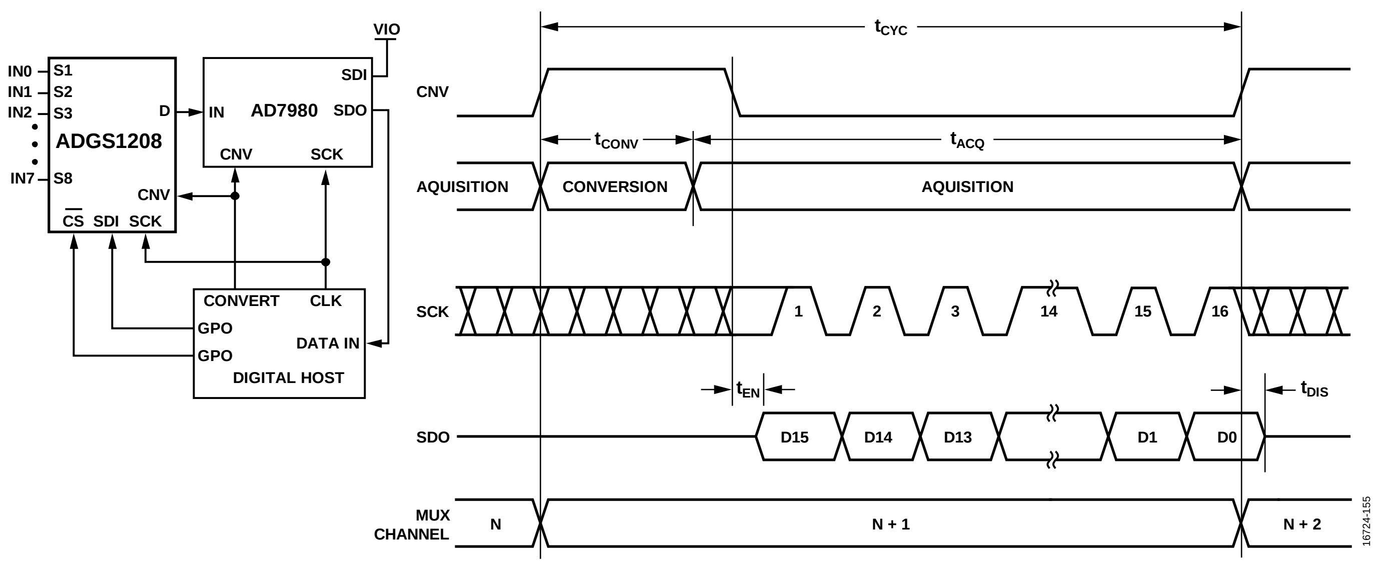


Figure 53. Example of CNV Signal of an ADC Cycling Through Channels in the ADGS1208

GENERAL-PURPOSE OUTPUTS

The ADGS1208/ADGS1209 have four general-purpose outputs (GPOs). These digital outputs allow the control of other devices using the ADGS1208/ADGS1209. The GPOs are controlled from the SW_DATA register, where they can be either set high or low. When the device is in round robin mode, the GPOs are driven low. The logic low level is GND and V_L sets the logic high level. Figure 54 shows how the ADGS1208 can be used to control another device, which in this example is the ADG758.

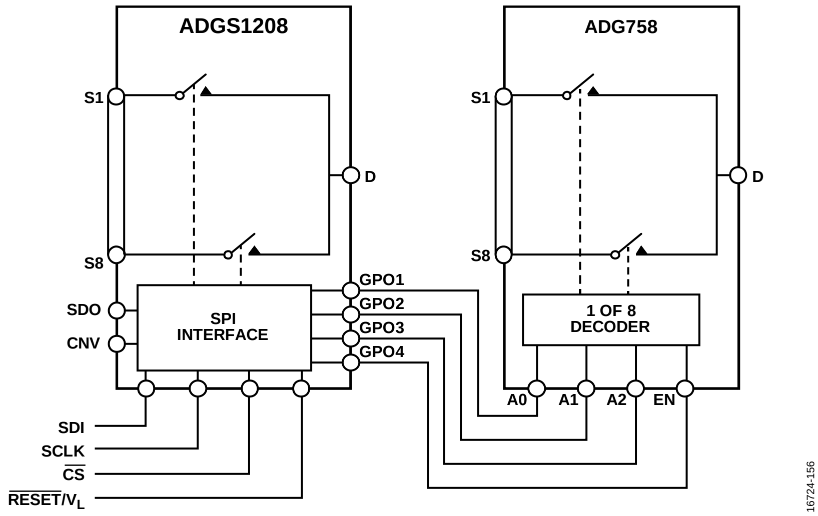


Figure 54. ADGS1208 Device Controlling the ADG758

APPLICATIONS INFORMATION

DIGITAL INPUT BUFFERS

There are input buffers present on the digital input pins ($\overline{CS}$, SCLK, and SDI). These buffers are active at all times; as result, there is current draw from the V_L supply if SCLK or SDI are toggling, regardless of whether $\overline{CS}$ is active. For typical values of this current draw, refer to the Specifications section and Figure 31.

SETTLING TIME

Disturbances are apparent on the source/drain when switching between channels, as is typical with complementary metal-oxide semiconductor (CMOS) switches and multiplexers. A sufficient wait time is necessary for these disturbances to settle before taking a measurement to ensure an accurate reading. The settling time for a data acquisition system is dependent on the load on the output of the multiplexer.

POWER SUPPLY RAILS

To guarantee correct operation of the ADGS1208/ADGS1209, 0.1 µF decoupling capacitors are required.

The ADGS1208/ADGS1209 can operate with bipolar supplies between ±4.5 V and ±16.5 V. The supplies on V_{DD} and V_{SS} do not need to be symmetrical. However, the V_{DD} to V_{SS} range must not exceed 33 V. The ADGS1208/ADGS1209 can also operate with single supplies between 5 V and 20 V with V_{SS} connected to GND.

The voltage range that can be supplied to V_L is from 2.7 V to 5.5 V.

The device is fully specified at ±15 V and +12 V analog supply voltage ranges.

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a bipolar power solution is shown in Figure 55. The ADP5070 dual switching regulator generates a positive and negative supply rail for the ADGS1208/ADGS1209, amplifier, and/or a precision converter in a typical signal chain. Also shown in Figure 55 are two optional low dropout (LDO) regulators, ADP7118 and ADP7182 (positive and negative, respectively), that can be used to reduce the output ripple of the ADP5070 in ultralow noise sensitive applications.

The ADM7160 can be used to generate the V_L voltage required to power digital circuitry within the ADGS1208/ADGS1209.

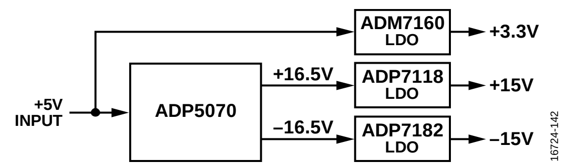


Figure 55. Bipolar Power Solution

Table 10. Recommended Power Management Devices

Product	Description
ADP5070	1 A/0.6 A, dc-to-dc switching regulator with independent positive and negative outputs
ADM7160	5.5 V, 200 mA, ultralow noise LDO linear regulator
ADP7118	20 V, 200 mA, low noise CMOS LDO linear regulator
ADP7182	−28 V, −200 mA, low noise LDO linear regulator

REGISTER SUMMARIES

Table 11. ADGS1208 Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	RW
0x01	SW_DATA	GPO4	GPO3	GPO2	GPO1	A2	A1	A0	EN	0x00	R/W
0x02	ERR_CONFIG	Reserved					RW_ERR_EN	SCLK_ERR_EN	CRC_ERR_EN	0x06	R/W
0x03	ERR_FLAGS	Reserved					RW_ERR_FLAG	SCLK_ERR_FLAG	CRC_ERR_FLAG	0x00	R
0x05	BURST_EN	Reserved							BURST_MODE_EN	0x00	R/W
0x06	ROUND_ROBIN_EN	Reserved							ROUND_ROBIN_EN	0x00	R/W
0x07	RROBIN_CHANNEL_CONFIG	S8_EN	S7_EN	S6_EN	S5_EN	S4_EN	S3_EN	S2_EN	S1_EN	0xFF	R/W
0x09	CNV_EDGE_SEL	RESERVED							CNV_EDGE_SEL	0x00	R/W
0x0B	SOFT_RESETB	SOFT_RESETB								0x00	R/W

Table 12. ADGS1209 Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	RW
0x01	SW_DATA	GPO4	GPO3	GPO2	GPO1	Reserved	A1	A0	EN	0x00	R/W
0x02	ERR_CONFIG	Reserved					RW_ERR_EN	SCLK_ERR_EN	CRC_ERR_EN	0x06	R/W
0x03	ERR_FLAGS	Reserved					RW_ERR_FLAG	SCLK_ERR_FLAG	CRC_ERR_FLAG	0x00	R
0x05	BURST_EN	Reserved							BURST_MODE_EN	0x00	R/W
0x06	ROUND_ROBIN_EN	Reserved							ROUND_ROBIN_EN	0x00	R/W
0x07	RROBIN_CHANNEL_CONFIG	Reserved				S4_EN	S3_EN	S2_EN	S1_EN	0x0F	R/W
0x09	CNV_EDGE_SEL	Reserved							CNV_EDGE_SEL	0x00	R/W
0x0B	SOFT_RESETB	SOFT_RESETB								0x00	R/W

REGISTER DETAILS

SWITCH DATA REGISTER

Address: 0x01, Reset: 0x00, Name: SW_DATA

The switch data register controls the status of the eight switches of the ADGS1208/ADGS1209 as well as the general-purpose digital outputs. Use the ADGS1208/ADGS1209 truth tables in conjunction with the bit descriptions.

Table 13. Bit Descriptions for SW_DATA in the ADGS1208

Bits	Bit Name	Settings	Description	Default	Access
7	GPO4		Enable bit for GPO4.	0x0	R/W
6	GPO3		Enable bit for GPO3.	0x0	R/W
5	GPO2		Enable bit for GPO2.	0x0	R/W
4	GPO1		Enable bit for GPO1.	0x0	R/W
3	A2		Enable bit for A2.	0x0	R/W
2	A1		Enable bit for A1.	0x0	R/W
1	A0		Enable bit for A0.	0x0	R/W
0	EN		Enable bit for the ADGS1208.	0x0	R/W
		0	ADGS1208 disabled.		
		1	ADGS1208 enabled.		

Table 14. Bit Descriptions for SW_DATA ADGS1209

Bits	Bit Name	Settings	Description	Default	Access
7	GPO4		Enable bit for GPO4.	0x0	R/W
6	GPO3		Enable bit for GPO3.	0x0	R/W
5	GPO2		Enable bit for GPO2.	0x0	R/W
4	GPO1		Enable bit for GPO1.	0x0	R/W
3	Reserved		This bit is reserved. Set this bit to 0.	0x0	R
2	A1		Enable bit for A1.	0x0	R/W
1	A0		Enable bit for A0.	0x0	R/W
0	EN		Enable bit for ADGS1209.	0x0	R/W
		0	ADGS1209 disabled.		
		1	ADGS1209 enabled.		

Table 15. ADGS1208 Truth Table

A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	S1
0	0	1	1	S2
0	1	0	1	S3
0	1	1	1	S4
1	0	0	1	S5
1	0	1	1	S6
1	1	0	1	S7
1	1	1	1	S8

Table 16. ADGS1209 Truth Table

A1	A0	EN	On Switch Pair
X	X	0	None
0	0	1	S1
0	1	1	S2
1	0	1	S3
1	1	1	S4

ERROR CONFIGURATION REGISTER

Address: 0x02, Reset: 0x06, Name: ERR_CONFIG

The error configuration register allows the user to enable and disable the relevant error features as required.

Table 17. Bit Descriptions for ERR_CONFIG

Bits	Bit Name	Settings	Description	Default	Access
[7:3]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
2	RW_ERR_EN		Enable bit for detecting an invalid read/write address.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
1	SCLK_ERR_EN		Enable bit for detecting the correct number of SCLK cycles in an SPI frame. 16 SCLK cycles are expected when CRC is disabled and burst mode is disabled. 24 SCLK cycles are expected when CRC is enabled and burst mode is disabled. A multiple of 16 SCLK cycles is expected when CRC is disabled and burst mode is enabled. A multiple of 24 SCLK cycles is expected when CRC is enabled and burst mode is enabled.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
0	CRC_ERR_EN		Enable bit for CRC error detection. SPI frames are 24 bits wide when enabled.	0x0	R/W
		0	Disabled.		
		1	Enabled.		

ERROR FLAGS REGISTER

Address: 0x03, Reset: 0x00, Name: ERR_FLAGS

The error flags register allows the user to determine if an error occurred. To clear the error flags register, write the special 16-bit SPI command, 0x6CA9, to the device. This SPI command does not trigger the invalid R/W address error. When CRC is enabled, the user must include the correct CRC byte during the SPI write for the clear error flags register command to succeed.

Table 18. Bit Descriptions for ERR_FLAGS

Bits	Bit Name	Settings	Description	Default	Access
[7:3]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
2	RW_ERR_FLAG		Error flag for invalid read/write address. The error flag asserts during an SPI read if the target address does not exist. The error flag also asserts when the target address of an SPI write does not exist or is read only.	0x0	R
		0	No error.		
		1	Error.		
1	SCLK_ERR_FLAG		Error flag for the detection of the correct number of SCLK cycles in an SPI frame.	0x0	R
		0	No error.		
		1	Error.		
0	CRC_ERR_FLAG		Error flag that determines if a CRC error occurred during a register write.	0x0	R
		0	No error.		
		1	Error.		

BURST ENABLE REGISTER

Address: 0x05, Reset: 0x00, Name: BURST_EN

The burst enable register allows the user to enable or disable burst mode. When enabled, the user can send multiple consecutive SPI commands without deasserting $\overline{CS}$.

Table 19. Bit Descriptions for BURST_EN

Bits	Bit Name	Settings	Description	Default	Access
[7:1]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
0	BURST_MODE_EN		Burst mode enable bit.	0x0	R/W
		0	Disabled.		
		1	Enabled.		

ROUND ROBIN ENABLE REGISTER

Address: 0x06, Reset: 0x00, Name: ROUND_ROBIN_EN

The round robin register allows the user to enable or disable round robin mode. When enabled, the user can cycle through the channels enabled in the round robin configuration register by presenting the relevant edge on the CNV pin.

Table 20. Bit Descriptions for ROUND_ROBIN_EN

Bits	Bit Name	Settings	Description	Default	Access
[7:1]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
0	ROUND_ROBIN_EN		Round robin mode enable bit.	0x0	R/W
		0	Disabled.		
		1	Enabled.		

ROUND ROBIN CHANNEL CONFIGURATION REGISTER

Address: 0x07, Reset: 0xFF (ADGS1208), 0x0F (ADGS1209), Name: RROBIN_CHANNEL_CONFIG

The round robin channel configuration register controls which channels are included a cycle during round robin mode. During round robin mode, the channels are cycled through in ascending order.

Table 21. Bit Descriptions for RROBIN_CHANNEL_CONFIG (ADGS1208)

Bits	Bit Name	Settings	Description	Default	Access
7	S8_EN		Enable bit for S8.	0x1	R/W
		0	S8 disabled during round robin mode.		
		1	S8 enabled during round robin mode.		
6	S7_EN		Enable bit for S7.	0x1	R/W
		0	S7 disabled during round robin mode.		
		1	S7 enabled during round robin mode.		
5	S6_EN		Enable bit for S6.	0x1	R/W
		0	S6 disabled during round robin mode.		
		1	S6 enabled during round robin mode.		
4	S5_EN		Enable bit for S5.	0x1	R/W
		0	S5 disabled during round robin mode.		
		1	S5 enabled during round robin mode.		
3	S4_EN		Enable bit for S4.	0x1	R/W
		0	S4 disabled during round robin mode.		
		1	S4 enabled during round robin mode.		
2	S3_EN		Enable bit for S3.	0x1	R/W
		0	S3 disabled during round robin mode.		
		1	S3 enabled during round robin mode.		

Bits	Bit Name	Settings	Description	Default	Access
1	S2_EN		Enable bit for S2.	0x1	R/W
		0	S2 disabled during round robin mode.		
		1	S2 enabled during round robin mode.		
0	S1_EN		Enable bit for S1.	0x1	R/W
		0	S1 disabled during round robin mode.		
		1	S1 enabled during round robin mode.		

Table 22. Bit Descriptions for RROBIN_CHANNEL_CONFIG (ADGS1209)

Bits	Bit Name	Settings	Description	Default	Access
[7:4]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
3	S4_EN		Enable bit for S4.	0x1	R/W
		0	S4 disabled during round robin mode.		
		1	S4 enabled during round robin mode.		
2	S3_EN		Enable bit for S3.	0x1	R/W
		0	S3 disabled during round robin mode.		
		1	S3 enabled during round robin mode.		
1	S2_EN		Enable bit for S2.	0x1	R/W
		0	S2 disabled during round robin mode.		
		1	S2 enabled during round robin mode.		
0	S1_EN		Enable bit for S1.	0x1	R/W
		0	S1 disabled during round robin mode.		
		1	S1 enabled during round robin mode.		

CNV EDGE SELECT REGISTER

Address: 0x09, Reset: 0x00, Name: CNV_EDGE_SEL

The CNV edge select register allows the user to select the active edge of the CNV pin when the device is in round robin mode.

Table 23. Bit Descriptions for CNV_EDGE_SEL

Bits	Bit Name	Settings	Description	Default	Access
[7:1]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
0	CNV_EDGE_SEL		CNV active edge select bit.	0x0	R/W
		0	Falling edge of CNV is the active edge.		
		1	Rising edge of CNV is the active edge.		

SOFTWARE RESET REGISTER

Address: 0x0B, Reset: 0x00, Name: SOFT_RESETB

Use the software reset register to perform a software reset. Consecutively, write 0xA3 followed by 0x05 to this register, and the registers of the device reset to their default state.

Table 24. Bit Descriptions for SOFT_RESETB

Bits	Bit Name	Settings	Description	Default	Access
[7:0]	SOFT_RESETB		To perform a software reset, consecutively write 0xA3 followed by 0x05 to this register.	0x0	R

OUTLINE DIMENSIONS

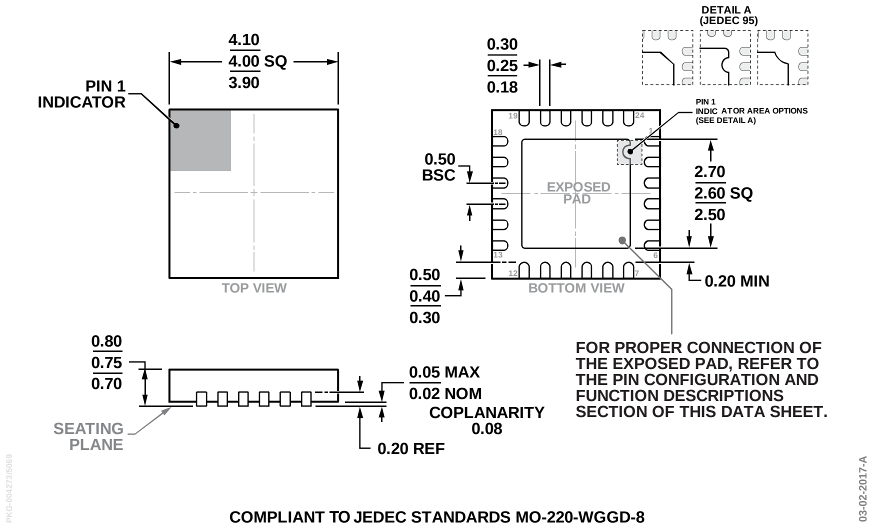


Figure 56. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADGS1208BCPZ	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-15
ADGS1208BCPZ-RL7	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-15
ADGS1209BCPZ	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-15
ADGS1209BCPZ-RL7	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-15
EVAL-ADGS1208SDZ		ADGS1208 Evaluation Board	
EVAL-ADGS1209SDZ		ADGS1209 Evaluation Board	

[1] Z = RoHS Compliant Part.