

# Clock Divider/Sine Wave 50Ω to CMOS Level Converter

## DESCRIPTION

Demonstration circuit 1075B is a divide by 2/4/8 clock divider for use with high speed ADCs. Each assembly includes a clock divider followed by a re-timing stage used to produce sharp clock edges. Functionally, the DC1075B receives a high frequency sine wave which is attenuated and routed into the clock divider. The output of the clock divider is then routed to a D flip flop re-timing stage. This D flip flop is clocked by the original high frequency sine wave. This is critical to ensure signal integrity. The output

of this re-timing stage is a CMOS signal suitable to be a clock source for high speed ADCs.

This circuit also is a model for designs involving FPGAs which serve as clock dividers. Whenever this is done, a D flip flop re-timing stage is required to ensure a low jitter clock signal.

[Design files for this circuit board are available.](#)

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## BOARD PHOTO

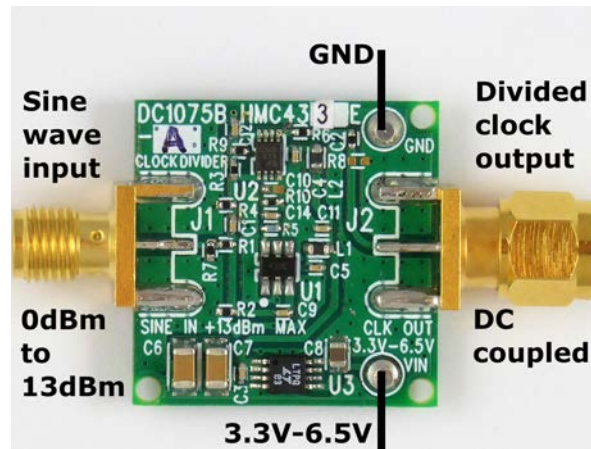


Figure 1. DC1075B Connection Diagram

# DEMO MANUAL DC1075B

## QUICK START PROCEDURE

### Setup

The DC1075B requires an external sine wave input source and an external power supply above 3.3V. The input voltage should not exceed 6.5V. Connect the female SMA connector to the sine wave generator. The input signal level should not exceed 13.0dBm. The DC1075B uses a male SMA output connector that can be connected directly to the clock input of ADC demo boards without additional adaptors.

For best results put a bandpass filter between the sine wave input source and the DC1075B to reduce the jitter

of the input signal and terminate the divided clock output signal with 50Ω.

**Table 1. DC1075B Assembly Options**

	U1	DIVIDE BY	MAX INPUT FREQ (MHz)
DC1075B-A	HMC433E	4	1100*
DC1075B-B	HMC432E	2	500
DC1075B-C	HMC434E	8	1300

\*Input frequencies for the DC1075B-A from 540MHz to 700MHz are not recommended.



#### ESD Caution

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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