16-Bit, 1 MSPS, PulSAR ADC in MSOP/LFCSP

Data Sheet **AD7980**

FEATURES

- **High performance**
  - **Pseudo differential analog input range**
    - **0 V to V_{REF} with V_{REF} between 2.5 V to 5 V**
  - **Throughput: 1 MSPS**
    - **Zero latency architecture**
  - **16-bit resolution with no missing codes**
  - **INL: ±0.6 LSB typical, ±1.25 LSB maximum**
  - **Dynamic range: 92 dB, V_{REF} = 5 V**
  - **SNR: 91.5 dB at f_{IN} = 10 kHz, V_{REF} = 5 V**
  - **THD: −114 dB at f_{IN} = 10 kHz, V_{REF} = 5 V**
  - **SINAD: 91 dB at f_{IN} = 10 kHz, V_{REF} = 5 V**
- **Low power dissipation**
  - **Single-supply 2.5 V operation with 1.8 V/2.5 V/3 V/5 V logic interface**
  - **4 mW at 1 MSPS (VDD only)**
  - **7 mW at 1 MSPS (total)**
  - **70 µW at 10 kSPS**
- **Proprietary serial interface**
  - **SPI/QSPI/MICROWIRE™/DSP compatible**
- **Daisy-chain multiple ADCs and busy indicator**
- **10-lead MSOP, 10-lead, 3 mm × 3 mm LFCSP**
- **Wide operating temperature range: −40°C to +125°C**

APPLICATIONS

- **Automated test equipment**
- **Data acquisition systems**
- **Medical instruments**
- **Machine automation**

TYPICAL APPLICATION CIRCUIT

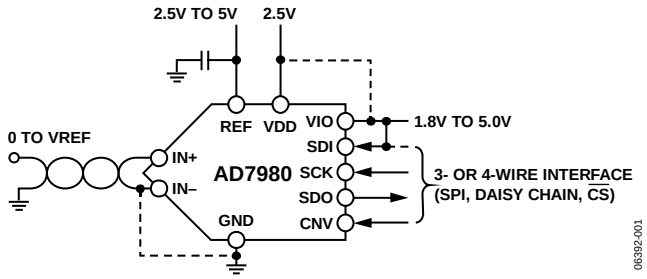

Figure 1.

GENERAL DESCRIPTION

The AD7980[1] is a 16-bit, successive approximation, analog-to-digital converter (ADC) that operates from a single power supply, VDD. It contains a low power, high speed, 16-bit sampling ADC and a versatile serial interface port. On the CNV rising edge, it samples an analog input, IN+, between 0 V to REF with respect to a ground sense, IN−. The reference voltage, REF, is applied externally and can be set independent of the supply voltage, VDD. Its power scales linearly with throughput.

The SPI-compatible serial interface also features the ability, using the SDI input, to daisy-chain several ADCs on a single, 3-wire bus and provides an optional busy indicator. It is compatible with 1.8 V, 2.5 V, 3 V, or 5 V logic, using the separate supply VIO.

The AD7980 is housed in a 10-lead MSOP or a 10-lead LFCSP with operation specified from −40°C to +125°C.

[1] Protected by U.S. Patent 6,703,961.

Table 1. MSOP, LFCSP 16-/18-/20-Bit Precision SAR ADCs and SAR ADC-Based µModule Data Acquisition Solutions

Type	≤100 kSPS	≤250 kSPS	≤500 kSPS	≤1000 kSPS	≤2000 kSPS	µModule Data Acquisition Solutions
Differential						
20-Bit			AD4022[1]	AD4021[1]	AD4020[1]	
18-Bit	AD7989-1[1]	AD7691[1]	AD4011[1]	AD4007[1]	AD4003[1]	
			AD7690[1]	AD7982[1]		
			AD7989-5[1]	AD7984[1]		
16-Bit	AD7684	AD7687[1]	AD7688[1]	AD4005[1]	AD4001[1]	
			AD7693[1]	AD7915[1]		
			AD7916[1]			
Pseudo Differential						
18-Bit			AD4010[1]	AD4006[1]	AD4002[1]	
16-Bit	AD7988-1[1]	AD7685[1]	AD4008[1]	AD4004[1]	AD4000[1]	ADAQ7980
	AD7680	AD7694	AD7988-5[1]	AD7980[1]		ADAQ7988
	AD7683		AD7686[1]	AD7983[1]		

[1] Pin for pin compatible.

Rev. G **Document Feedback**

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SPECIFICATIONS

VDD = 2.5 V, VIO = 1.71 V to 5.5 V, V_{REF} = 5 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	A Grade			B Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
RESOLUTION		16			16			Bits
ANALOG INPUT								
Voltage Range	IN+ − IN−	0		V_{REF}	0		V_{REF}	V
Absolute Input Voltage	IN+	−0.1		V_{REF} + 0.1	−0.1		V_{REF} + 0.1	V
	IN−	−0.1		+0.1	−0.1		+0.1	V
Analog Input CMRR	f_{IN} = 100 kHz		60			60		dB
Leakage Current at 25°C	Acquisition phase		1			1		nA
Input Impedance			See the Analog Input section			See the Analog Input section		
ACCURACY								
No Missing Codes		16			16			Bits
Differential Linearity Error	REF = 5 V	−1.0	±0.5	+2.0	−0.9	±0.4	+0.9	LSB[1]
	REF = 2.5 V		±0.7			±0.55		LSB[1]
Integral Linearity Error	REF = 5 V	−2.5	±1.5	+2.5	−1.25	±0.6	+1.25	LSB[1]
	REF = 2.5 V		±1.65			±0.65		LSB[1]
Transition Noise	REF = 5 V		0.75			0.6		LSB[1]
	REF = 2.5 V		1.2			1.0		LSB[1]
Gain Error, T_{MIN} to T_{MAX}[2]			±2			±2		LSB[1]
Gain Error Temperature Drift			±0.35			±0.35		ppm/°C
Zero Error, T_{MIN} to T_{MAX}[2]		−1.0	±0.08	+1.0	−0.5	±0.08	+0.5	mV
Zero Temperature Drift			0.54			0.54		ppm/°C
Power Supply Sensitivity	VDD = 2.5 V ± 5%		±0.1			±0.1		LSB[1]
THROUGHPUT								
Conversion Rate	VIO ≥ 3.3 V	0		1	0		1	MSPS
	VIO < 3.3 V, 85°C to 125°C			833			833	kSPS
	VIO > 2.3 V, up to 85°C			1			1	MSPS
	VIO ≤ 2.3 V			833			833	kSPS
Transient Response	Full-scale step			290			290	ns
AC ACCURACY								
Dynamic Range	V_{REF} = 5 V		91			92		dB[3]
	V_{REF} = 2.5 V		86			87		dB[3]
Oversampled Dynamic Range	f_O = 10 kSPS		110			111		dB[3]
Signal-to-Noise Ratio, SNR	f_{IN} = 10 kHz, V_{REF} = 5 V		90.5		90	91.5		dB[3]
	f_{IN} = 10 kHz, V_{REF} = 2.5 V		86.0			87.0		dB[3]
Spurious-Free Dynamic Range, SFDR	f_{IN} = 10 kHz		−103.5			−110		dB[3]
Total Harmonic Distortion, THD	f_{IN} = 10 kHz		−101			−114		dB[3]
Signal-to-Noise-and-Distortion Ratio, SINAD	f_{IN} = 10 kHz, V_{REF} = 5 V		90			91		dB[3]
	f_{IN} = 10 kHz, V_{REF} = 2.5 V		85.5			86.5		dB[3]

[1] LSB means least significant bit. With the 5 V input range, 1 LSB is 76.3 µV.
[2] See the Terminology section. These specifications include full temperature range variation, but not the error contribution from the external reference.
[3] All specifications in dB are referred to a full-scale range (FSR). Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.

VDD = 2.5 V, VIO = 1.71 V to 5.5 V, V_{REF} = 5 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		2.4		5.1	V
Load Current	1 MSPS, REF = 5 V		330		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			10		MHz
Aperture Delay	VDD = 2.5 V		2.0		ns
DIGITAL INPUTS					
Logic Levels					
V_{IL}	VIO > 3V	−0.3		0.3 × VIO	V
V_{IH}	VIO > 3V	0.7 × VIO		VIO + 0.3	V
V_{IL}	VIO ≤ 3V	−0.3		0.1 × VIO	
V_{IH}	VIO ≤ 3V	0.9 × VIO		VIO + 0.3	µA
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format		Serial 16 bits straight binary			
Pipeline Delay		Conversion results available immediately after completed conversion			
V_{OL}	I_{SINK} = 500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD		2.375	2.5	2.625	V
VIO		1.71		5.5	V
Standby Current[1, 2]	VDD and VIO = 2.5 V, 25°C		0.35		µA
Power Dissipation	VDD = 2.625 V, V_{REF} = 5 V, VIO = 3 V				
Total	10 kSPS throughput		70		µW
	1 MSPS throughput, B grade		7.0	9.0	mW
	1 MSPS throughput, A grade		7.0	10	mW
VDD Only			4		mW
REF Only			1.7		mW
VIO Only			1.3		mW
Energy per Conversion			7.0		nJ/sample
TEMPERATURE RANGE[3]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+125	°C

[1] With all digital inputs forced to VIO or GND as required.
[2] During the acquisition phase.
[3] Contact sales for extended temperature range.

TIMING SPECIFICATIONS

VDD = 2.37 V to 2.63 V, VIO = 2.3 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise stated. See Figure 2 for load conditions.

Table 4.

Parameter[1]	Symbol	Min	Typ	Max	Unit
Throughput Rate					
VIO Above 3.3 V				1	MSPS
VIO Above 2.3 V, T_A = -40°C to 85°C				1	MSPS
VIO Above 2.3 V, T_A > 85°C				833	kSPS
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}				
VIO Above 3.3 V		500		710	ns
VIO Above 2.3 V, T_A = -40°C to 85°C		500		710	ns
VIO Above 2.3 V, T_A > 85°C		500		800	ns
Acquisition Time	t_{ACQ}	290			ns
Time Between Conversions	t_{CYC}				
VIO Above 3.3 V		1000			ns
VIO Above 2.3 V, T_A = -40°C to 85°C		1000			ns
VIO Above 2.3 V, T_A > 85°C		1.2			µs
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}				ns
VIO Above 4.5 V		10.5			ns
VIO Above 3 V		12			ns
VIO Above 2.7 V		13			ns
VIO Above 2.3 V		15			ns
SCK Period (Chain Mode)	t_{SCK}				ns
VIO Above 4.5 V		11.5			ns
VIO Above 3 V		13			ns
VIO Above 2.7 V		14			ns
VIO Above 2.3 V		16			ns
SCK Low Time	t_{SCKL}	4.5			ns
SCK High Time	t_{SCKH}	4.5			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	3			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 4.5 V				9.5	ns
VIO Above 3 V				11	ns
VIO Above 2.7 V				12	ns
VIO Above 2.3 V				14	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO Above 3 V				10	ns
VIO Above 2.3 V				15	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			20	ns
SDI Valid Setup Time from CNV Rising Edge	$t_{SSDICNV}$	5			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	2			ns
SDI Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	5			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	2			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	3			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	$t_{DSDOSDI}$			15	ns

[1] Timing parameters measured with respect to a falling edge are defined as triggered at x% VIO. Timing parameters measured with respect to a rising edge are defined as triggered at y% VIO. For VIO ≤ 3 V, x = 90 and y = 10. For VIO > 3 V, x = 70 and y = 30. The minimum V_{IH} and maximum V_{IL} are used. See the Digital Inputs Specifications in Table 2.

VDD = 2.37 V to 2.63 V, VIO = 1.71 V to 2.3 V, T_A = −40°C to +125°C, unless otherwise stated. See Figure 2 for load conditions.

Table 5.

Parameter[1]	Symbol	Min	Typ	Max	Unit
Throughput Rate				833	kSPS
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	500		800	ns
Acquisition Time	t_{ACQ}	290			ns
Time Between Conversions[2]	t_{CYC}	1.2			µs
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}	22			ns
SCK Period (Chain Mode)	t_{SCK}	23			ns
SCK Low Time	t_{SCKL}	6			ns
SCK High Time	t_{SCKH}	6			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	3			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}		14	21	ns
CNV or SDI Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}		18	40	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			20	ns
SDI Valid Setup Time from CNV Rising Edge	$t_{SSDICNV}$	5			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	10			ns
SDI Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	5			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	2			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	3			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	$t_{DSDOSDI}$			22	ns

[1] Timing parameters measured with respect to a falling edge are defined as triggered at x% VIO. Timing parameters measured with respect to a rising edge are defined as triggered at y% VIO. For VIO ≤ 3 V, x = 90 and y = 10. For VIO > 3 V, x = 70 and y = 30. The minimum V_{IH} and maximum V_{IL} are used. See the Digital Inputs Specifications in Table 2.

[2] The time required to clock out N bits of data, t_{READ}, may be greater than t_{ACQ}, depending on the magnitude of VIO. If t_{READ} is greater than t_{ACQ}, the throughput must be limited to ensure that all N bits are read back from the device.

Timing Diagrams

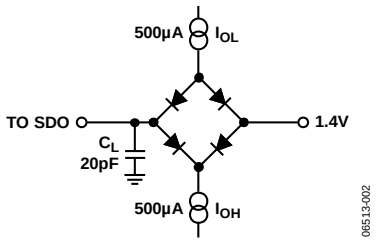

Figure 2. Load Circuit for Digital Interface Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog Inputs	
IN+,[1] IN−[1] to GND	−0.3 V to V_{REF} + 0.3 V or ±130 mA
Supply Voltage	
REF, VIO to GND	−0.3 V to +6 V
VDD to GND	−0.3 V to +3 V
VDD to VIO	+3 V to −6 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] See the Analog Input section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 7. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
RM-10	200	44	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on use of a 2S2P JEDEC PCB. See the Ordering Guide.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

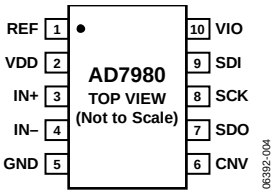

Figure 3. 10-Lead MSOP Pin Configuration

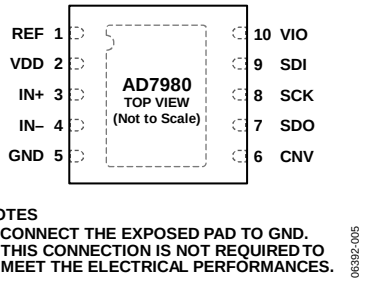

Figure 4. 10-Lead LFCSP Pin Configuration

Table 8. Pin Function Descriptions

Pin No.				
MSOP	**LFCSP**	**Mnemonic**	**Type[1]**	**Description**
1	1	REF	AI	Reference Input Voltage. The REF range is from 2.4 V to 5.1 V. It is referred to the GND pin. This pin should be decoupled closely to the pin with a 10 µF capacitor.
2	2	VDD	P	Power Supply.
3	3	IN+	AI	Analog Input. It is referred to IN–. The voltage range, for example, the difference between IN+ and IN–, is 0 V to V_{REF}.
4	4	IN–	AI	Analog Input Ground Sense. To be connected to the analog ground plane or to a remote sense ground.
5	5	GND	P	Power Supply Ground.
6	6	CNV	DI	Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the device, chain, or $\overline{CS}$ mode. In $\overline{CS}$ mode, it enables the SDO pin when low. In chain mode, the data should be read when CNV is high.
7	7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	8	SCK	DI	Serial Data Clock Input. When the device is selected, the conversion result is shifted out by this clock.
9	9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows. Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low; if SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.
10	10	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
Not applicable	0	EPAD	Not applicable	Exposed Pad. Connect the exposed pad to GND. This connection is not required to meet the electrical performances.

[1]AI = analog input, DI = digital input, DO = digital output, and P = power.

TERMINOLOGY

Integral Nonlinearity Error (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 25).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error
The first transition should occur at a level ½ LSB above analog ground (38.1 µV for the 0 V to 5 V range). The offset error is the deviation of the actual transition from that point.

Gain Error
The last transition (from 111 … 10 to 111 … 11) should occur for an analog voltage 1½ LSB below the nominal full scale (4.999886 V for the 0 V to 5 V range). The gain error is the deviation of the actual level of the last transition from the ideal level after the offset is adjusted out.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is expressed in bits and related to SINAD by the following formula:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

Noise-Free Code Resolution
Noise-free code resolution is the number of bits beyond which it is impossible to distinctly resolve individual codes. It is calculated as

$$\textit{Noise-Free Code Resolution} = \log_2(2^N/\textit{Peak-to-Peak Noise})$$

and is expressed in bits.

Effective Resolution
Effective resolution is calculated as

$$\textit{Effective Resolution} = \log_2(2^N/\textit{RMS Input Noise})$$

and is expressed in bits.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in dB.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in dB. It is measured with a signal at −60 dBFS to include all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in dB.

Signal-to-Noise-and-Distortion Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in dB.

Aperture Delay
Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 2.5 V, V_{REF} = 5.0 V, VIO = 3.3 V, unless otherwise noted.

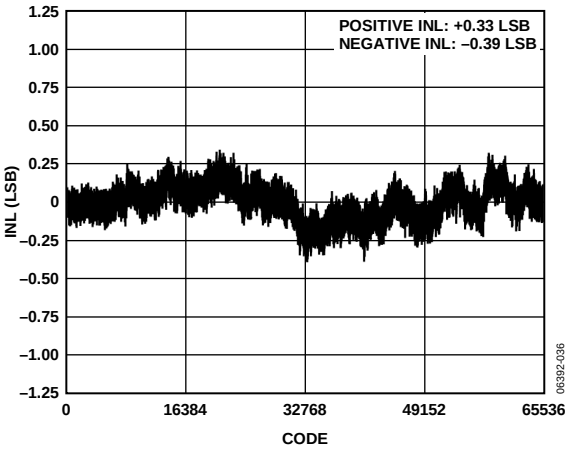

Figure 5. Integral Nonlinearity vs. Code, REF = 5 V

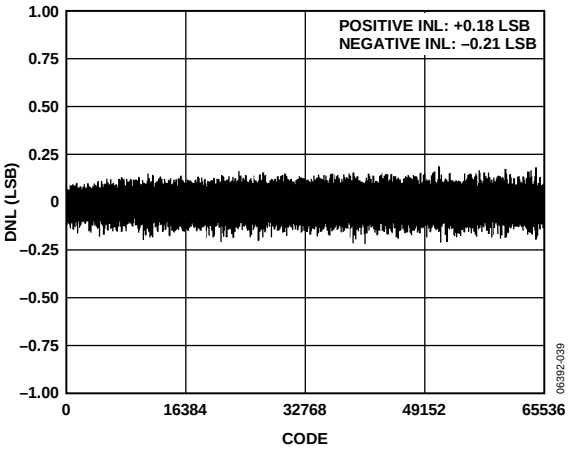

Figure 8. Differential Nonlinearity vs. Code, REF = 5 V

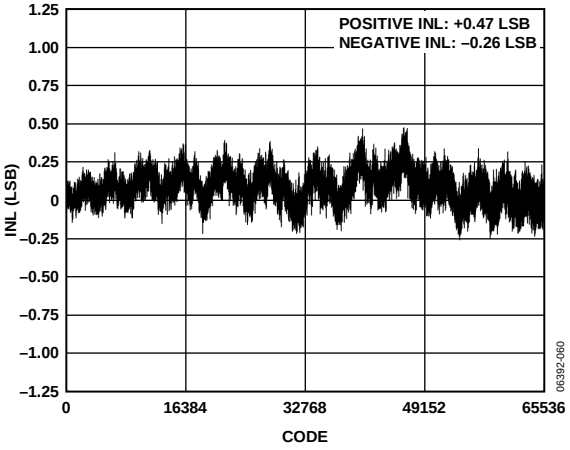

Figure 6. Integral Nonlinearity vs. Code, REF = 2.5 V

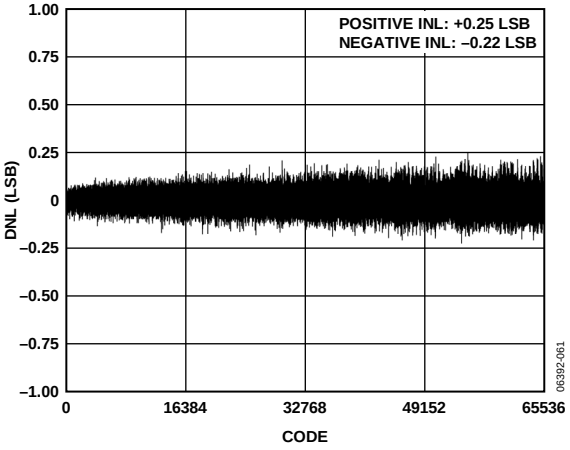

Figure 9. Differential Nonlinearity vs. Code, REF = 2.5 V

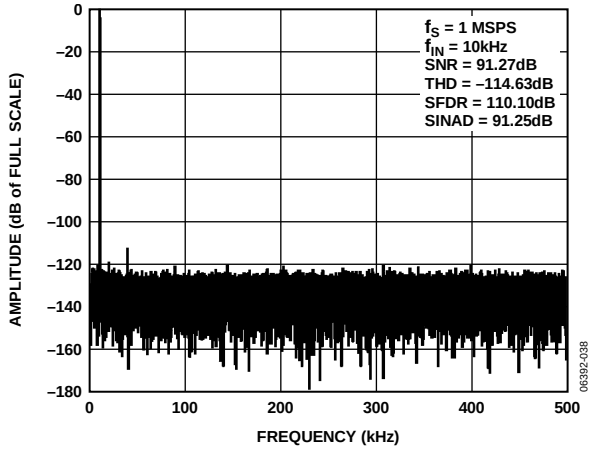

Figure 7. FFT Plot, REF = 5 V

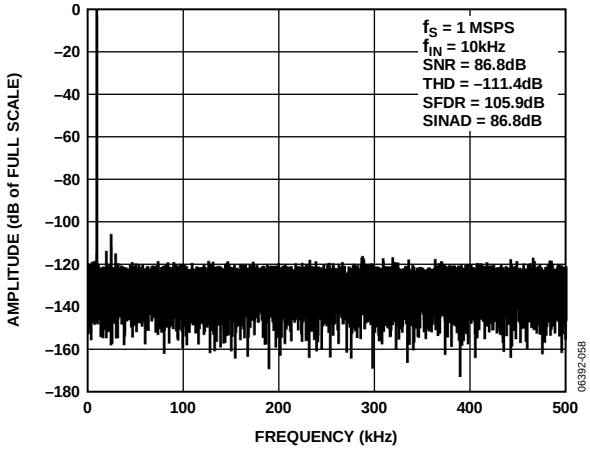

Figure 10. FFT Plot, REF = 2.5 V

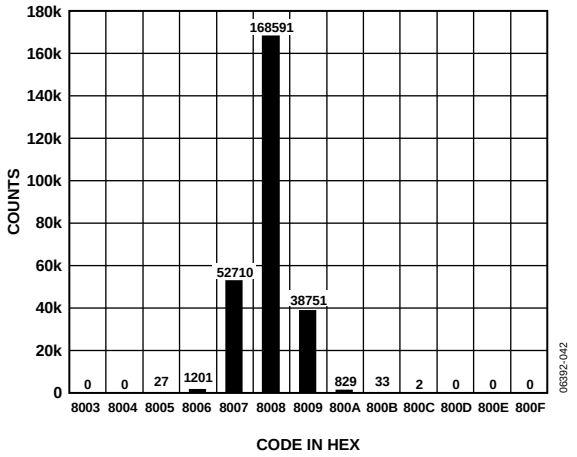

Figure 11. Histogram of a DC Input at the Code Center, REF = 5 V

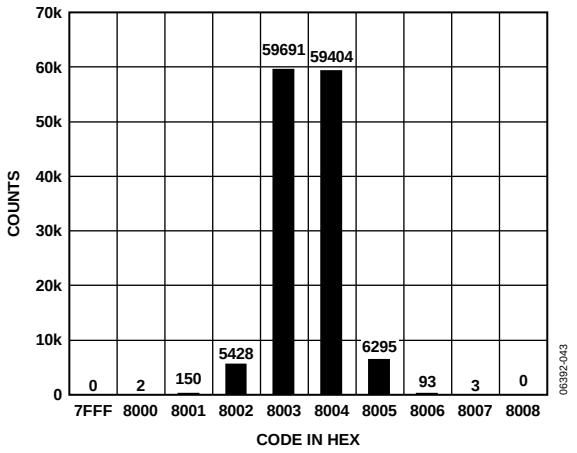

Figure 12. Histogram of a DC Input at the Code Transition, REF = 5 V

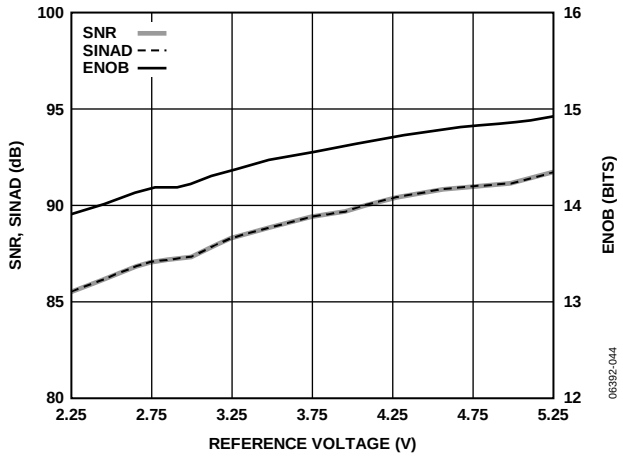

Figure 13. SNR, SINAD, and ENOB vs. Reference Voltage

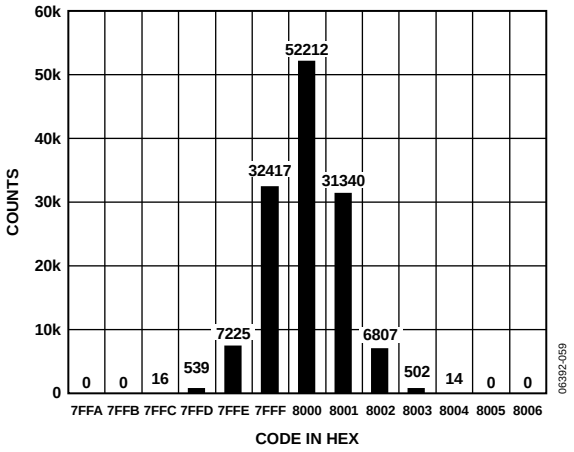

Figure 14. Histogram of a DC Input at the Code Center, REF = 2.5 V

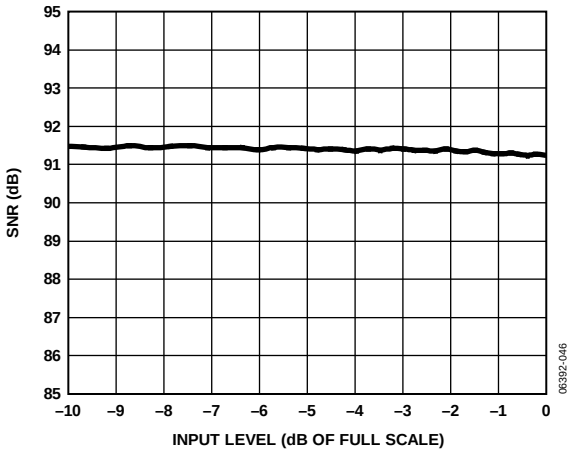

Figure 15. SNR vs. Input Level

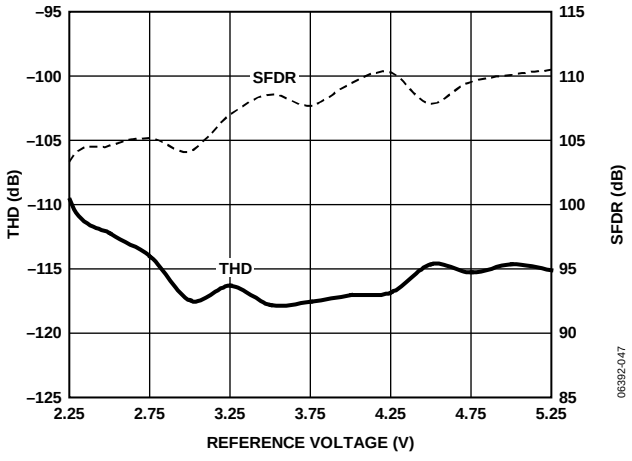

Figure 16. THD, SFDR vs. Reference Voltage

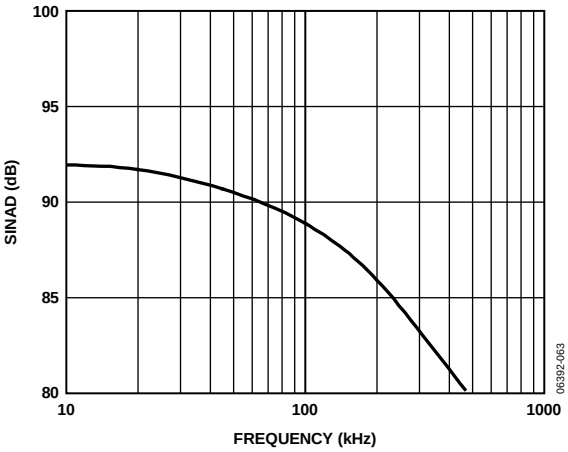

Figure 17. SINAD vs. Frequency

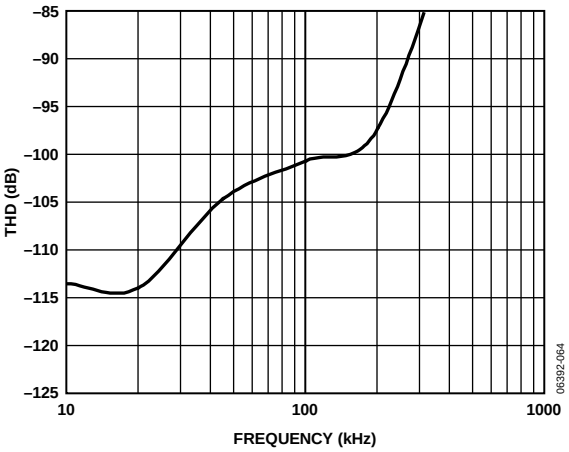

Figure 20. THD vs. Frequency

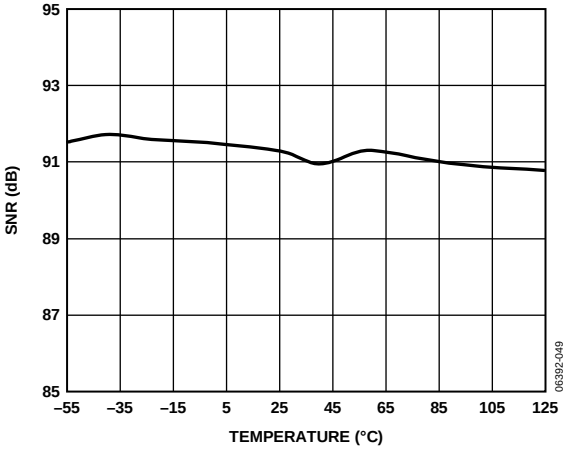

Figure 18. SNR vs. Temperature

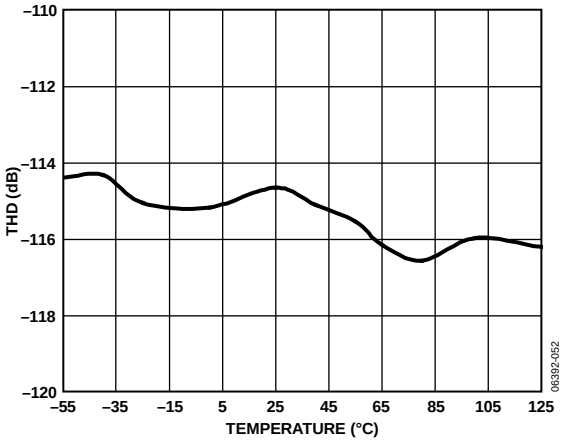

Figure 21. THD vs. Temperature

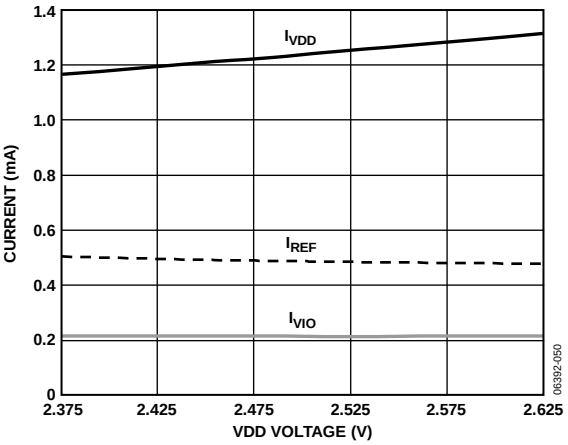

Figure 19. Operating Currents vs. Supply

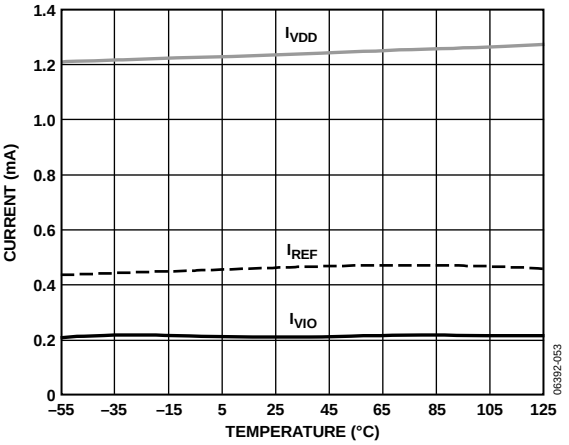

Figure 22. Operating Currents vs. Temperature

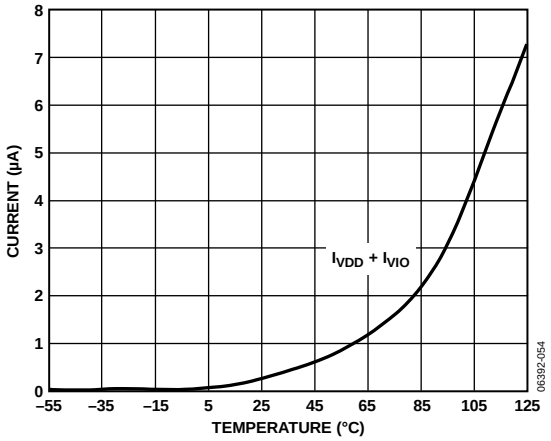

Figure 23. Power-Down Currents vs. Temperature

THEORY OF OPERATION

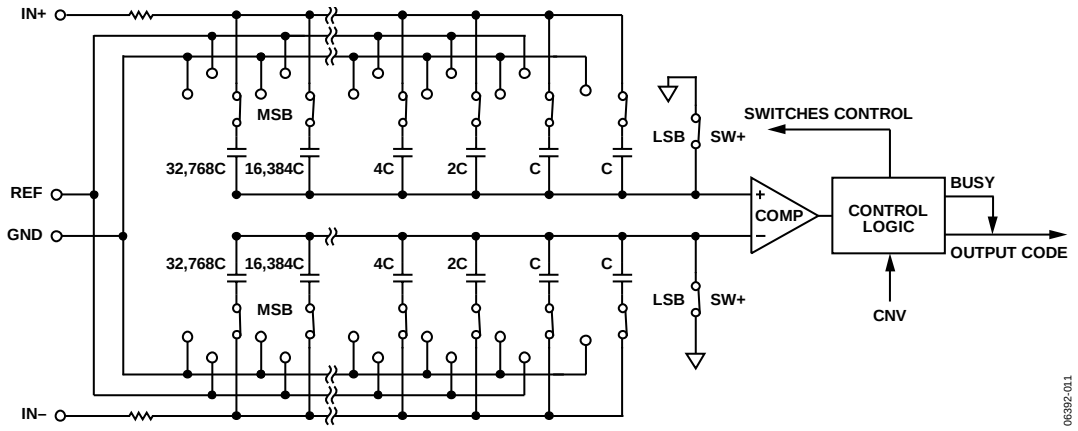

Figure 24. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7980 is a fast, low power, single-supply, precise 16-bit ADC that uses a successive approximation architecture.

The AD7980 is capable of converting 1,000,000 samples per second (1 MSPS) and powers down between conversions. When operating at 10 kSPS, for example, it consumes 70 µW typically, ideal for battery-powered applications.

The AD7980 provides the user with on-chip track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple multiplexed channel applications.

The AD7980 can be interfaced to any 1.8 V to 5 V digital logic family. It is housed in a 10-lead MSOP or a tiny 10-lead LFCSP that combines space savings and allows flexible configurations.

It is pin-for-pin compatible with the 18-bit AD7982.

CONVERTER OPERATION

The AD7980 is a successive approximation ADC based on a charge redistribution DAC. Figure 24 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the input of the comparator are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. When the acquisition phase is completed and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs IN+ and IN− captured at the end of the acquisition phase are applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ … $V_{REF}/65{,}536$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the device returns to the acquisition phase and the control logic generates the ADC output code and a busy signal indicator.

Because the AD7980 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

Transfer Functions

The ideal transfer characteristic for the AD7980 is shown in Figure 25 and Table 9.

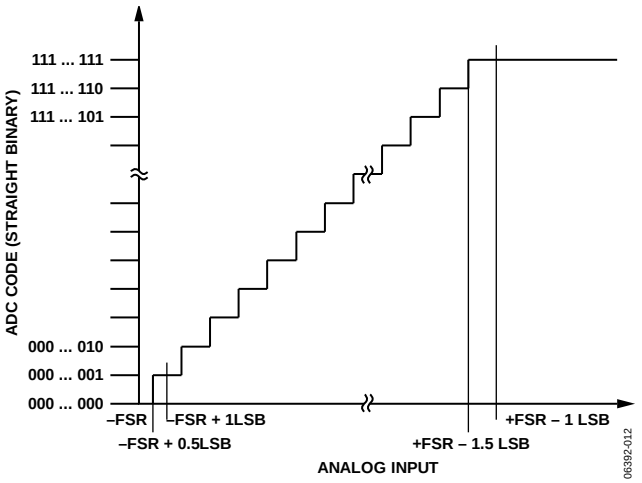

Figure 25. ADC Ideal Transfer Function

Table 9. Output Codes and Ideal Input Voltages

	Analog Input	
Description	**V_{REF} = 5 V**	**Digital Output Code (Hex)**
FSR – 1 LSB	4.999924 V	FFFF[1]
Midscale + 1 LSB	2.500076 V	8001
Midscale	2.5 V	8000
Midscale – 1 LSB	2.499924 V	7FFF
–FSR + 1 LSB	76.3 µV	0001
–FSR	0 V	0000[2]

[1] This is also the code for an overranged analog input (V_{IN+} – V_{IN-} above V_{REF} – V_{GND}).
[2] This is also the code for an underranged analog input (V_{IN+} – V_{IN-} below V_{GND}).

TYPICAL APPLICATION CIRCUIT WITH MULTIPLE SUPPLIES

Figure 26 shows an example of a typical application circuit for the AD7980 when multiple supplies are available.

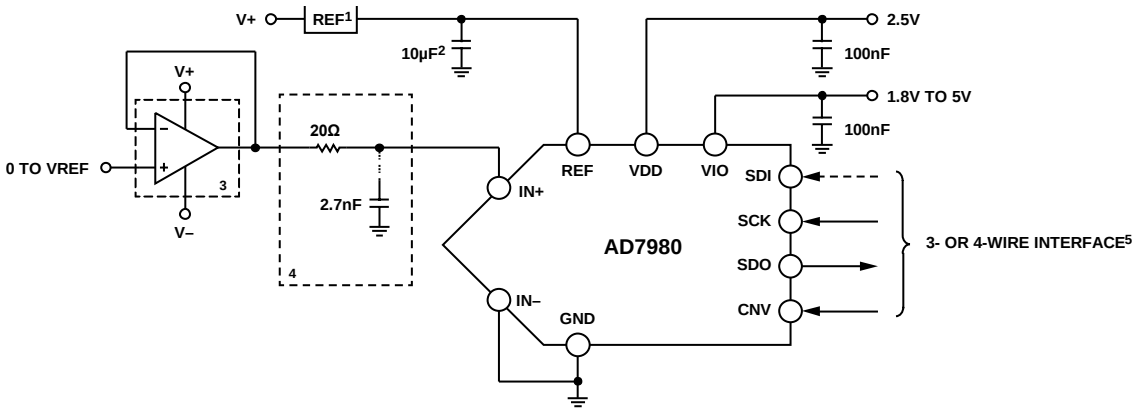

Figure 26. Typical Application Circuit with Multiple Supplies

ANALOG INPUT

Figure 27 shows an equivalent circuit of the input structure of the AD7980.

The two diodes, D1 and D2, provide ESD protection for the analog inputs, IN+ and IN−. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V, because this causes these diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. For instance, these conditions could eventually occur when the supplies of the input buffer (U1) are different from VDD. In such a case (for example, an input buffer with a short circuit), the current limitation can be used to protect the device.

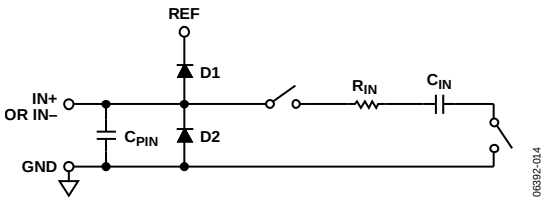

Figure 27. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. By using these differential inputs, signals common to both inputs are rejected.

During the acquisition phase, the impedance of the analog inputs (IN+ and IN−) can be modeled as a parallel combination of capacitor, C_{PIN}, and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 400 Ω and is a lumped component made up of some serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor. During the conversion phase, where the switches are opened, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a 1-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise.

When the source impedance of the driving circuit is low, the AD7980 can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

DRIVER AMPLIFIER CHOICE

Although the AD7980 is easy to drive, the driver amplifier needs to meet the following requirements:

- The noise generated by the driver amplifier needs to be kept as low as possible to preserve the SNR and transition noise performance of the AD7980. The noise coming from the driver is filtered by the 1-pole, low-pass filter of the AD7980 analog input circuit made by R_{IN} and C_{IN} or by the external filter, if one is used. Because the typical noise of the AD7980 is 47.3 μV rms, the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20 \log \left(\frac{47.3}{\sqrt{47.3^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}} \right)$$

  where:
  f_{-3dB} is the input bandwidth in MHz of the AD7980 (10 MHz) or the cutoff frequency of the input filter, if one is used.
  N is the noise gain of the amplifier (for example, 1 in buffer configuration).
  e_N is the equivalent input noise voltage of the op amp, in nV/√Hz.

- For ac applications, the driver should have a THD performance commensurate with the AD7980.
- For multichannel multiplexed applications, the driver amplifier and the AD7980 analog input circuit must settle for a full-scale step onto the capacitor array at a 16-bit level (0.0015%, 15 ppm). In the amplifier data sheet, settling at 0.1% to 0.01% is more commonly specified. This can differ significantly from the settling time at a 16-bit level and should be verified prior to driver selection.

The Precision ADC Driver Tool can be used to model the settling behavior and to estimate the ac performance of the AD7980 with a selected driver and RC filter.

Table 10. Recommended Driver Amplifiers[1]

Amplifier	Typical Application
ADA4805-1	Low noise, small size, and low power
ADA4807-1	Very low noise and high frequency
ADA4627-1	Precision, low noise, and low input bias current
ADA4522-1	Precision, zero drift, and EMI enhanced
ADA4841-1	Low noise, low distortion, and low power

[1] For the latest recommended drivers, see the product recommendations listed on the product webpage.

VOLTAGE REFERENCE INPUT

The AD7980 voltage reference input, REF, has a dynamic input impedance and should therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins, as explained in the Layout section.

When REF is driven by a very low impedance source, for example, a reference buffer using the AD8031, the ADA4805-1, or the ADA4807-1, a ceramic chip capacitor is appropriate for optimum performance.

If an unbuffered reference voltage is used, the decoupling value depends on the reference used. For instance, a 22 µF (X5R, 1206 size) ceramic chip capacitor is appropriate for optimum performance using a low temperature drift reference, such as the ADR435, ADR445, LTC6655, or ADR4550.

If desired, a reference-decoupling capacitor value as small as 2.2 µF can be used with a minimal impact on performance, especially DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and GND pins.

POWER SUPPLY

The AD7980 uses two power supply pins: a core supply, VDD, and a digital input/output interface supply, VIO. VIO allows direct interface with any logic between 1.8 V and 5.0 V. To reduce the number of supplies needed, VIO and VDD can be tied together. When VIO is greater than or equal to VDD, the AD7980 is insensitive to power supply sequencing. In normal operation, if the magnitude of VIO is less than the magnitude of VDD, VIO must be applied before VDD. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 28.

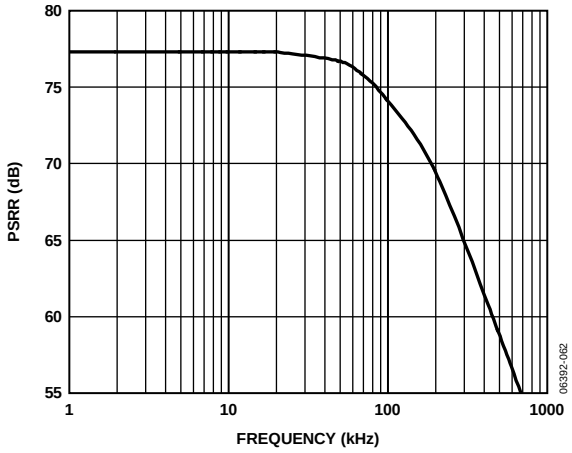

Figure 28. PSRR vs. Frequency

The AD7980 powers down automatically at the end of each conversion phase and, therefore, the power scales linearly with the sampling rate. This makes the device ideal for low sampling rate (even of a few Hz) and low battery-powered applications.

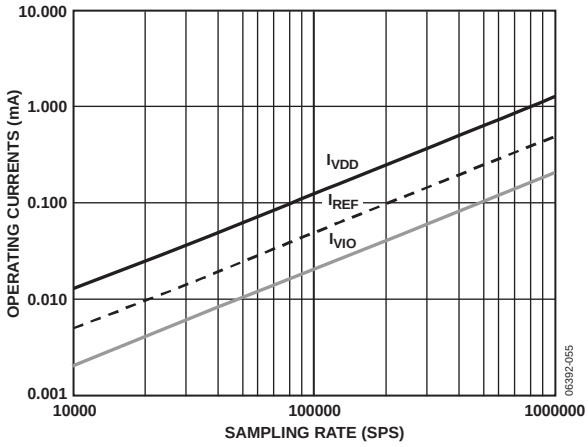

Figure 29. Operating Currents vs. Sampling Rate

DIGITAL INTERFACE

Though the AD7980 has a reduced number of pins, it offers flexibility in its serial interface modes.

The AD7980, when in $\overline{CS}$ mode, is compatible with SPI, QSPI™, and digital hosts. This interface can use either a 3-wire or 4-wire interface. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). This is useful in low jitter sampling or simultaneous sampling applications.

The AD7980, when in chain mode, provides a daisy-chain feature using the SDI input for cascading multiple ADCs on a single data line similar to a shift register.

The mode in which the device operates depends on the SDI level when the CNV rising edge occurs. The $\overline{CS}$ mode is selected if SDI is high, and the chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected together, the chain mode is selected.

In either mode, the AD7980 offers the flexibility to optionally force a start bit in front of the data bits. This start bit can be used as a busy signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a busy indicator, the user must time out the maximum conversion time prior to readback.

The busy indicator feature is enabled in the $\overline{CS}$ mode if CNV or SDI is low when the ADC conversion ends (see Figure 33 and Figure 37). The busy indicator feature is enabled in the chain mode if SCK is high during the CNV rising edge (see Figure 41).

3-WIRE $\overline{CS}$ MODE WITHOUT BUSY INDICATOR

This mode is usually used when a single AD7980 is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 30, and the corresponding timing is given in Figure 31.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. Once a conversion is initiated, it continues until completion irrespective of the state of CNV. This can be useful, for instance, to bring CNV low to select other SPI devices, such as analog multiplexers; however, CNV must be returned high before the minimum conversion time elapses and then held high for the maximum conversion time to avoid the generation of the busy signal indicator. When the conversion is complete, the AD7980 enters the acquisition phase and powers down.

When CNV goes low, the MSB is output onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate provided that it has an acceptable hold time. After the 16th SCK falling edge or when CNV goes high, whichever is earlier, SDO returns to high impedance.

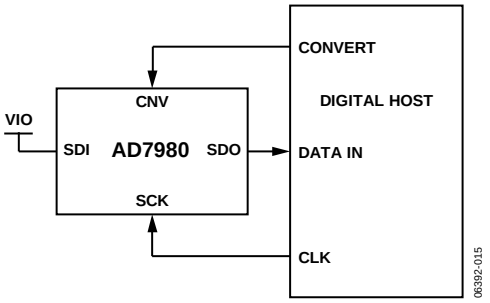

Figure 30. 3-Wire $\overline{CS}$ Mode Without Busy Indicator Connection Diagram (SDI High)

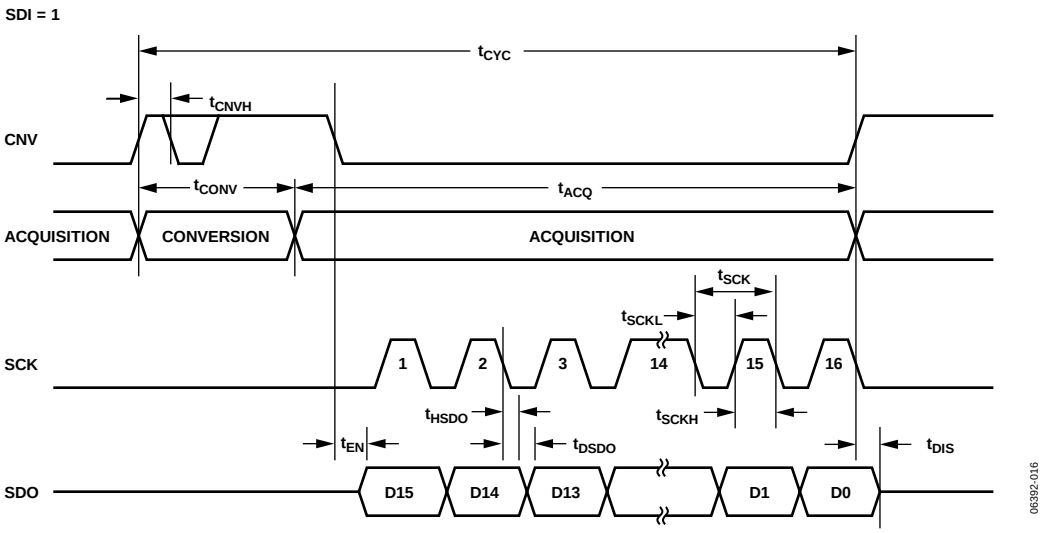

Figure 31. 3-Wire $\overline{CS}$ Mode Without Busy Indicator Serial Interface Timing (SDI High)

3-WIRE $\overline{CS}$ MODE WITH BUSY INDICATOR

This mode is usually used when a single AD7980 is connected to an SPI-compatible digital host having an interrupt input.

The connection diagram is shown in Figure 32, and the corresponding timing is given in Figure 33.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion irrespective of the state of CNV. Prior to the minimum conversion time, CNV can be used to select other SPI devices, such as analog multiplexers, but CNV must be returned low before the minimum conversion time elapses and then held low for the maximum conversion time to guarantee the generation of the busy signal indicator. When the conversion is complete, SDO goes from high impedance to low. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The AD7980 then enters the acquisition phase and powers down. The data bits are clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate provided it has an acceptable hold time. After the optional 17th SCK falling edge or when CNV goes high, whichever is earlier, SDO returns to high impedance.

If multiple AD7980 devices are selected at the same time, the SDO output pin handles this contention without damage or induced latch-up. Meanwhile, it is recommended to keep this contention as short as possible to limit extra power dissipation.

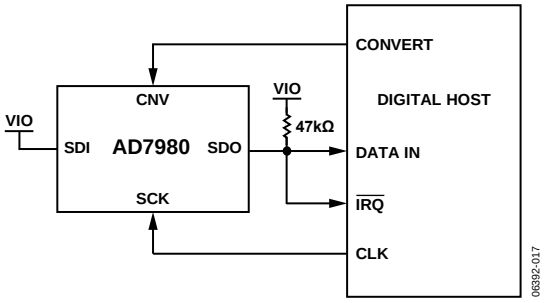

Figure 32. 3-Wire $\overline{CS}$ Mode with Busy Indicator Connection Diagram (SDI High)

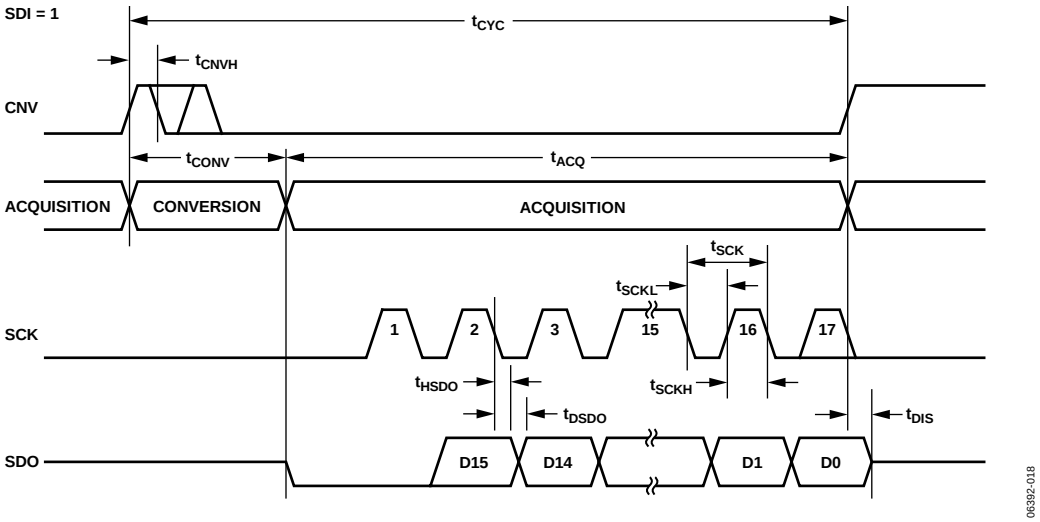

Figure 33. 3-Wire $\overline{CS}$ Mode with Busy Indicator Serial Interface Timing (SDI High)

4-WIRE $\overline{CS}$ MODE WITHOUT BUSY INDICATOR

This mode is usually used when multiple AD7980 devices are connected to an SPI-compatible digital host.

A connection diagram example using two AD7980 devices is shown in Figure 34, and the corresponding timing is given in Figure 35.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI can be used to select other SPI devices, such as analog multiplexers, but SDI must be returned high before the minimum conversion time elapses and then held high for the maximum conversion time to avoid the generation of the busy signal indicator.

When the conversion is complete, the AD7980 enters the acquisition phase and powers down. Each ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate provided it has an acceptable hold time. After the 16th SCK falling edge or when SDI goes high, whichever is earlier, SDO returns to high impedance and another AD7980 can be read.

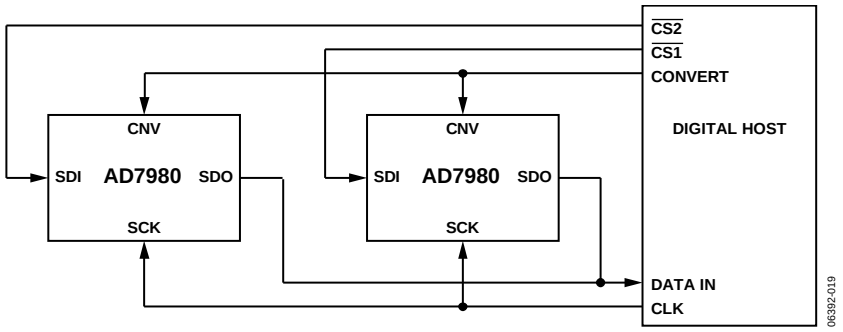

Figure 34. 4-Wire $\overline{CS}$ Mode Without Busy Indicator Connection Diagram

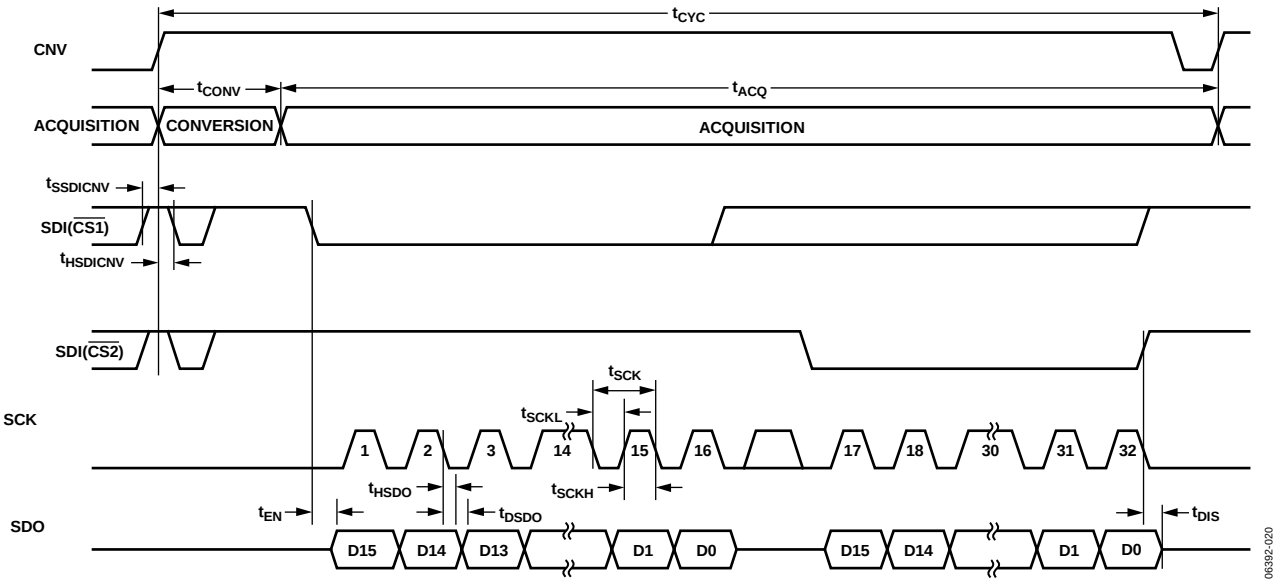

Figure 35. 4-Wire $\overline{CS}$ Mode Without Busy Indicator Serial Interface Timing

4-WIRE $\overline{CS}$ MODE WITH BUSY INDICATOR

This mode is usually used when a single AD7980 is connected to an SPI-compatible digital host that has an interrupt input, and it is desired to keep CNV, which is used to sample the analog input, independent of the signal used to select the data reading. This requirement is particularly important in applications where low jitter on CNV is desired.

The connection diagram is shown in Figure 36, and the corresponding timing is given in Figure 37.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI can be used to select other SPI devices, such as analog multiplexers, but SDI must be returned low before the minimum conversion time elapses and then held low for the maximum conversion time to guarantee the generation of the busy signal indicator. When the conversion is complete, SDO goes from high impedance to low.

With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The AD7980 then enters the acquisition phase and powers down. The data bits are clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate provided it has an acceptable hold time. After the optional 17th SCK falling edge or SDI going high, whichever is earlier, the SDO returns to high impedance.

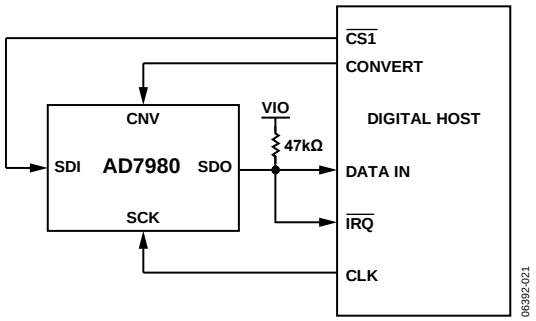

Figure 36. 4-Wire $\overline{CS}$ Mode with Busy Indicator Connection Diagram

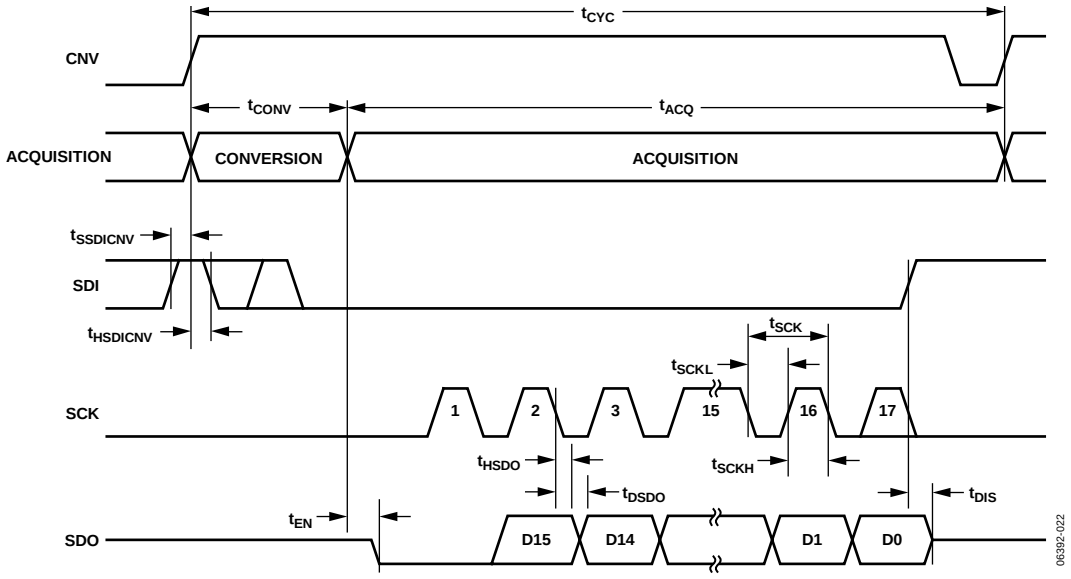

Figure 37. 4-Wire $\overline{CS}$ Mode with Busy Indicator Serial Interface Timing

CHAIN MODE WITHOUT BUSY INDICATOR

This mode can be used to daisy-chain multiple AD7980 devices on a 3-wire serial interface. This feature is useful for reducing component count and wiring connections, for example, in isolated multi-converter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using two AD7980s is shown in Figure 38, and the corresponding timing is given in Figure 39.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, selects the chain mode, and disables the busy indicator. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO and the AD7980 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are clocked by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 16 × N clocks are required to readback the N ADCs. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate and, consequently, more AD7980 devices in the chain, provided the digital host has an acceptable hold time. The maximum conversion rate may be reduced due to the total readback time.

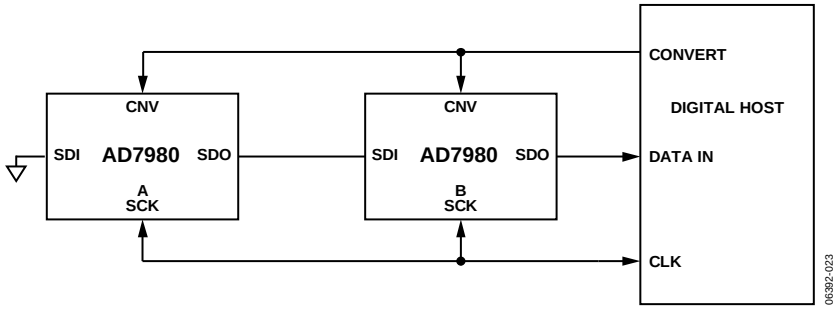

Figure 38. Chain Mode Without Busy Indicator Connection Diagram

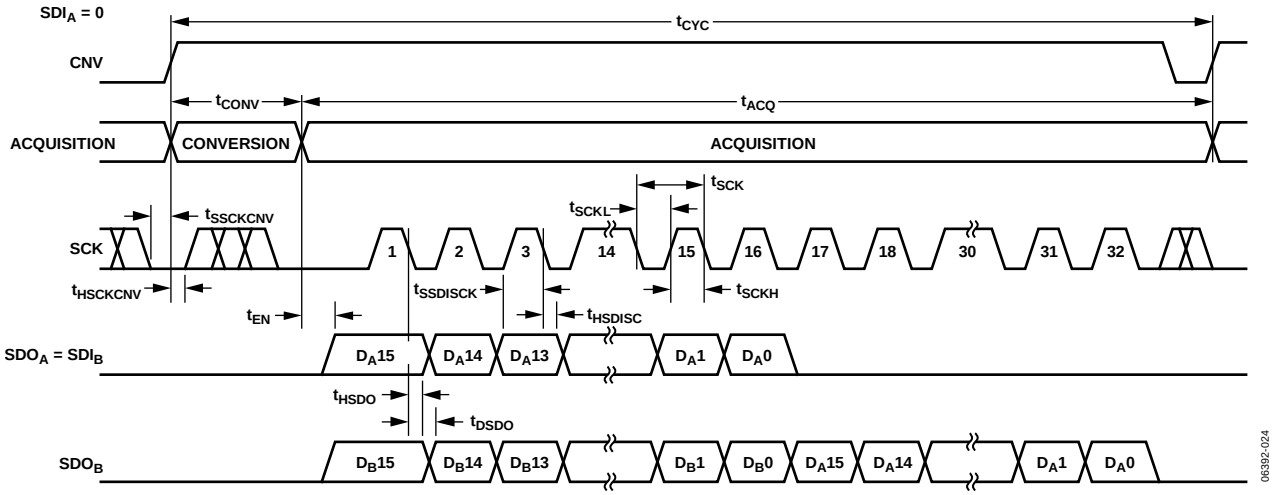

Figure 39. Chain Mode Without Busy Indicator Serial Interface Timing

CHAIN MODE WITH BUSY INDICATOR

This mode can also be used to daisy-chain multiple AD7980 devices on a 3-wire serial interface while providing a busy indicator. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using three AD7980 devices is shown in Figure 40, and the corresponding timing is given in Figure 41.

When SDI and CNV are low, SDO is driven low. With SCK high, a rising edge on CNV initiates a conversion, selects the chain mode, and enables the busy indicator feature. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When all ADCs in the chain have completed their conversions, the SDO pin of the ADC closest to the digital host (see the AD7980 ADC labeled C in Figure 40) is driven high. This transition on SDO can be used as a busy indicator to trigger the data readback controlled by the digital host. The AD7980 then enters the acquisition phase and powers down. The data bits stored in the internal shift register are clocked out, MSB first, by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 16 × N + 1 clocks are required to readback the N ADCs. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate and, consequently, more AD7980 devices in the chain, provided the digital host has an acceptable hold time.

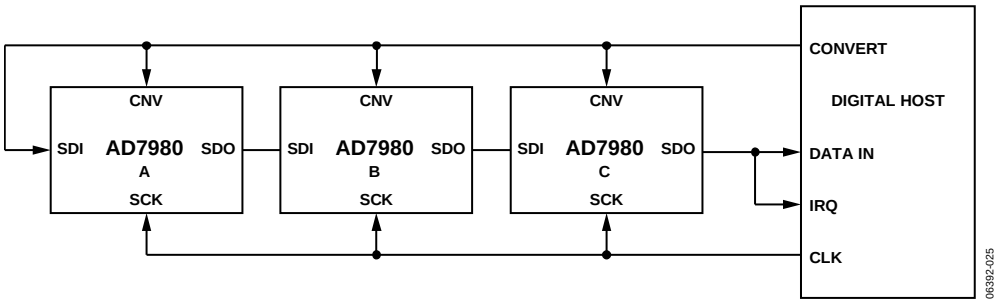

Figure 40. Chain Mode with Busy Indicator Connection Diagram

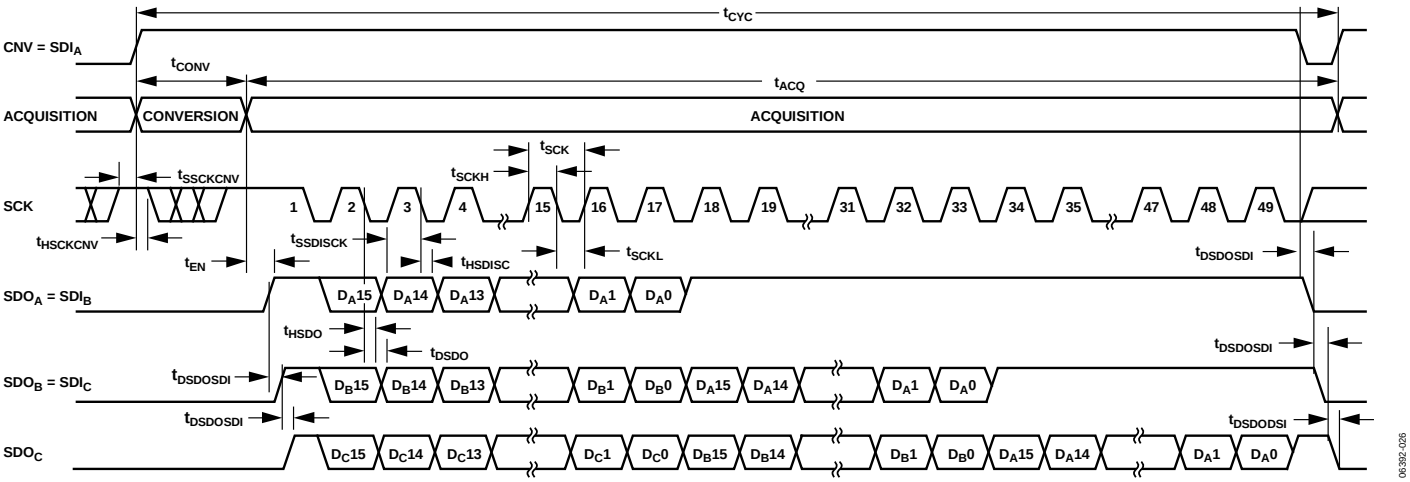

Figure 41. Chain Mode with Busy Indicator Serial Interface Timing

APPLICATIONS INFORMATION

LAYOUT

The printed circuit board (PCB) that houses the AD7980 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7980, with all its analog signals on the left side and all its digital signals on the right side, eases this task.

Avoid running digital lines under the device because these couple noise onto the die, unless a ground plane under the AD7980 is used as a shield. Fast switching signals, such as CNV or clocks, should never run near analog signal paths. Crossover of digital and analog signals should be avoided.

At least one ground plane should be used. The ground plane can be common or split between the digital and analog section. In the latter case, the planes should be joined underneath the AD7980 devices.

The AD7980 voltage reference input REF has a dynamic input impedance and should be decoupled with minimal parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, ideally right up against, the REF and GND pins and connecting them with wide, low impedance traces.

Finally, the power supplies VDD and VIO of the AD7980 should be decoupled with ceramic capacitors, typically 100 nF, placed close to the AD7980 and connected using short and wide traces to provide low impedance paths and reduce the effect of glitches on the power supply lines.

An example of a layout following these rules is shown in Figure 42 and Figure 43.

EVALUATING THE PERFORMANCE OF THE AD7980

Other recommended layouts for the AD7980 are outlined in the documentation of the evaluation board for the AD7980 (EVAL-AD7980SDZ). The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-SDP-CB1Z.

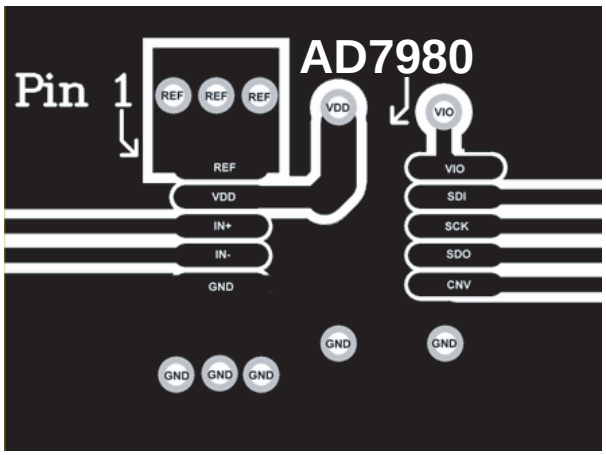

Figure 42. Example Layout of the AD7980 (Top Layer)

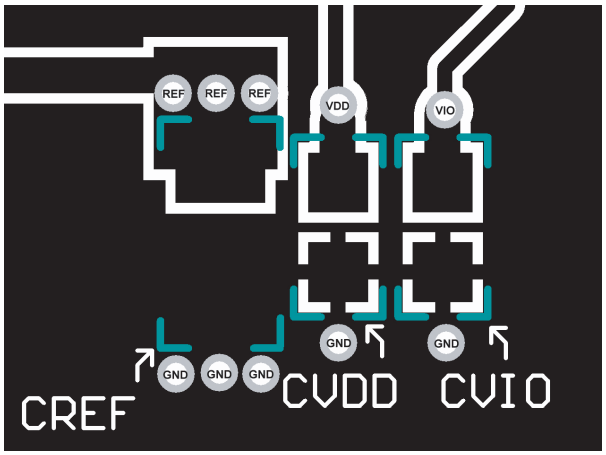

Figure 43. Example Layout of the AD7980 (Bottom Layer)

OUTLINE DIMENSIONS

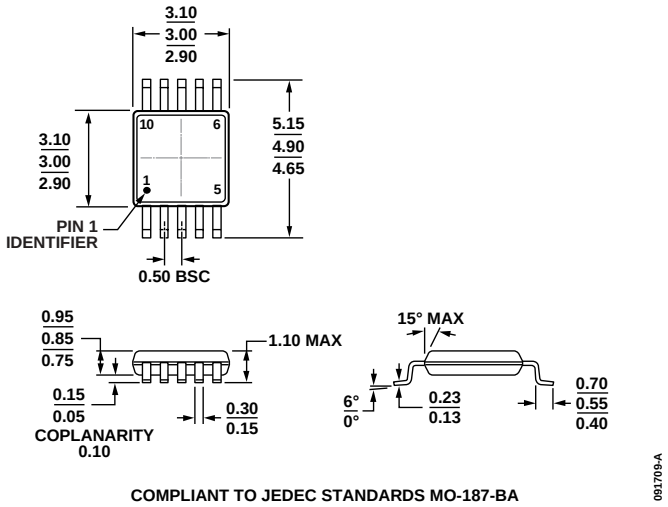

Figure 44.10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

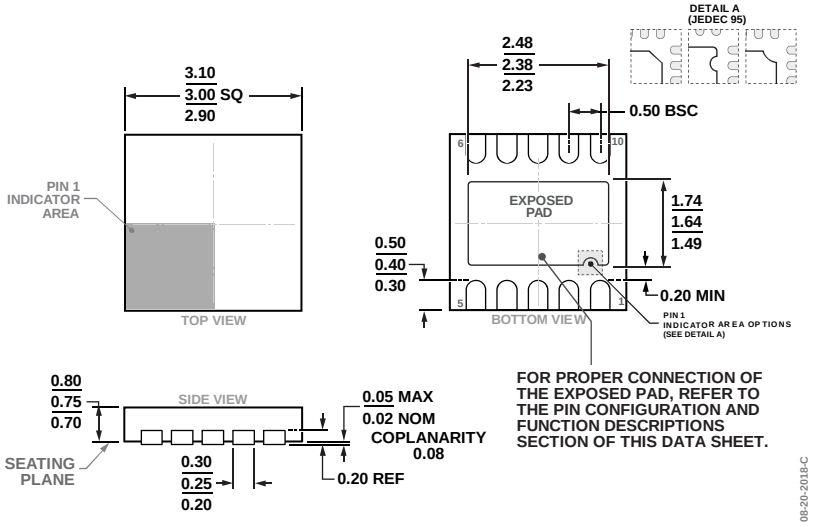

Figure 45. 10-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-10-9)
Dimensions shown in millimeters

Contact sales for the non-RoHS compliant version of the device.

ORDERING GUIDE

Model[1, 2, 3]	Integral Nonlinearity	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
AD7980ARMZ	±2.5 LSB max	−40°C to +125°C	10-Lead MSOP	RM-10	C5X	Tube, 50
AD7980ARMZRL7	±2.5 LSB max	−40°C to +125°C	10-Lead MSOP	RM-10	C5X	Reel, 1,000
AD7980BRMZ	±1.25 LSB max	−40°C to +125°C	10-Lead MSOP	RM-10	C5D	Tube, 50
AD7980BRMZRL7	±1.25 LSB max	−40°C to +125°C	10-Lead MSOP	RM-10	C5D	Reel, 1,000
AD7980ACPZ-RL	±2.5 LSB max	−40°C to +125°C	10-Lead LFCSP	CP-10-9	C5X	Reel, 5,000
AD7980ACPZ-RL7	±2.5 LSB max	−40°C to +125°C	10-Lead LFCSP	CP-10-9	C5X	Reel, 1,000
AD7980BCPZ-RL	±1.25 LSB max	−40°C to +125°C	10-Lead LFCSP	CP-10-9	C5D	Reel, 5,000
AD7980BCPZ-RL7	±1.25 LSB max	−40°C to +125°C	10-Lead LFCSP	CP-10-9	C5D	Reel, 1,000
AD7980BCPZ-R2	±1.25 LSB max	−40°C to +125°C	10-Lead LFCSP	CP-10-9	C5D	Reel, 1,000
EVAL-AD7980SDZ			Evaluation Board			
EVAL-SDP-CB1Z			Controller Board			

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD7980SDZ can be used as a standalone evaluation board or in conjunction with the EVAL-SDP-CB1Z for evaluation/demonstration purposes.
[3] The EVAL-SDP-CB1Z allows a PC to control and communicate with all Analog Devices evaluation boards ending in the SD designator.

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D06392-1/21(G)

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Analog Devices Inc.:

AD7980BRMZ AD7980ARMZ AD7980BRMZRL7 AD7980BCPZ-RL7 AD7980BCPZ-RL AD7980ACPZ-RL7 AD7980SRMZ-EP-RL7 AD7980ARMZRL7 EVAL-AD7980SDZ AD7980SRMZ-EP