How to parallel CoolGaN™ 600 V HEMT in half-bridge configurations for higher-power applications

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About this document

Scope and purpose

This document presents design considerations, the setup and results from the half-bridge evaluation board when paralleling CoolGAN™ 600 V HEMTs. The board features four 70 mΩ GaN power transistors, a pair of 1EDI EiceDRIVER™ compact gate drivers, along with input logic that provides adjustable dead-time. Using an external inductor, the board can be configured for buck or boost mode, double-pulse testing or continuous pulse-width modulation (PWM) operation, hard- or soft-switching at power levels to several kW and frequencies up to 1 MHz.

Intended audience

This document is intended for power electronic engineers and designers who want to understand how to parallel CoolGaN™ HEMTs in order to increase the current and power capability of half-bridge configurations in both hard- and soft-switching applications.

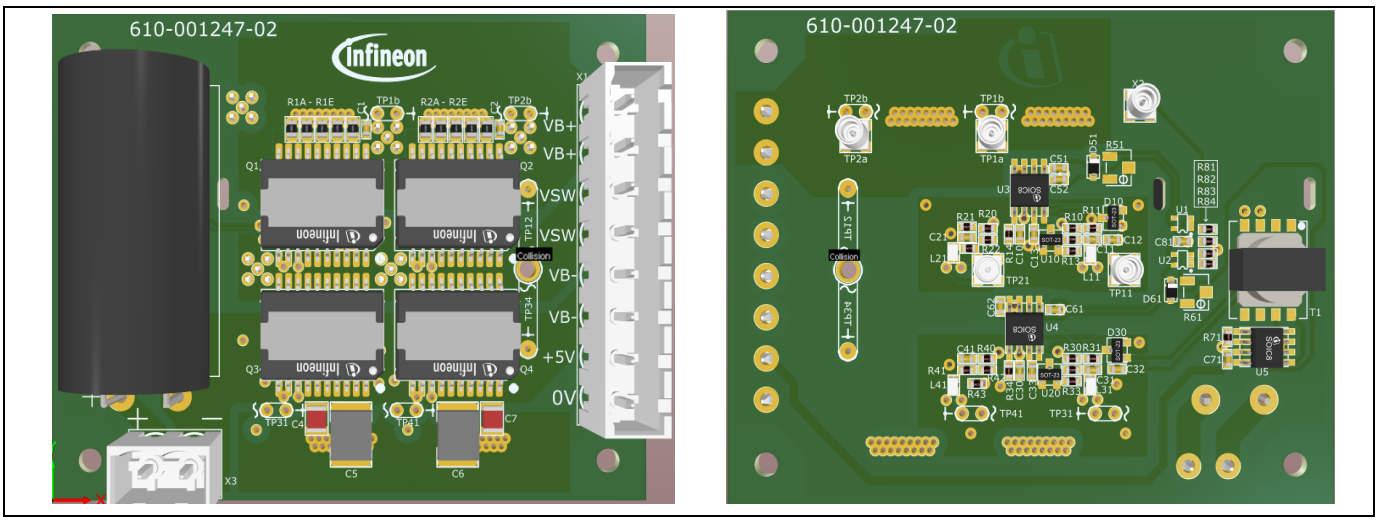

Figure 1 Front and back view of the paralleling CoolGAN™ in half-bridge configuration evaluation platform

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1 Summary of the paralleling CoolGaN™ in half-bridge configurations

This engineering report provides a detailed description of the design of paralleling Infineon Technologies GaN HEMT transistors in half-bridge configurations along with the appropriate gate-driving circuitry. Furthermore, the report explains step by step how to operate the board under double-pulse test or hard-switching conditions as well as under soft-switching conditions.

Below is a summary of the key features offered by this demo board when used as a reference for increasing the current and thereby the power capabilities of half-bridge configurations:

- Flexible usage and reliable performance at several tens of amps of the board for:
    - Double-pulse testing in hard-switching conditions as shown in **Figure 2**. Further details can be found in section **5.7.1**.
    - Inverted double-pulse testing in soft-switching conditions as shown in **Figure 3**. Further details can be found in section **5.7.2**.
    - Testing buck and boost converter configurations as shown in **Figure 10** and **Figure 11**.
- Serveral test points, as explained in **Table 2**, are provided for measuring:
    - Drain current sharing between the high-side parallel GaN transistors
    - Gate-to-source voltage waveforms on each parallel GaN transistor
    - Drain-to-source voltage waveforms on each high and/or low-side pair
- Thermal design considerations when the board is intended to be used in continuous operation, for example as an open-loop buck or boost converter, described in section **5.2.4**.
- The undesirable effects when the Common Mode (CM) inductors are not being used when paralleling GaN transitors are shown in **Figure 18** and **Figure 21**.
- Performance of paralleled corner GaN transistors with extreme parameter specifications, i.e. asymmetries in gate threshold voltages and $R_{DS\,(on)}$ between GaN devices as well as in PCB layout, is comprehensively explained in section **5.8**.

Below is a summary of the practical results by testing the demo board as well as SIMetrix simulations that lead to recommendations when paralleling GaN transistors.

- This demo board confirms that GaN transistors can be parallel in half-bridge configurations for both hard- and soft-switching applications.
- There is always a risk of destructive high-frequency oscillations due to slight imbalance in gate thresholds or circuit parasitics when GaN transistors are operated in parallel. Asymmetry due to $R_{DS\,(on)}$ is only a reason for static unbalance in current sharing.
- The introduction of CM inductors in each of the gate to Kelvin source circuit loops eliminates the risk of destructive sustained oscillations and allows proper and reliable control of parallel devices. However, for acceptable dynamic current sharing, perfectly symmetrical circuit layout and matched gate thresholds are essential. For static current sharing, matched $R_{DS\,(on)}$ values help.
- All good layout practices are also important for parallel operated GaN transistors. Power loops and gate-drive loops must be as small as possible with parallel GaN layouts too. Additionally, they must be as symmetrical as possible.
- SIMetrix simulations demonstrate that reliable performance is possible even when using corner devices in parallel, say extreme gate threshold voltages and $R_{DS\,(on)}$ values, thanks to the usage of the CM inductor in the gate to Kelvin source loop of each GaN transistor, which considerably mitigates destructive oscillations during both turn-on and turn-off events.

2 Introduction

This half-bridge evaluation board enables easy, rapid setup and test of paralleling 600 V CoolGaN™ transistors along with the isolated gate driver IC. The generic topology is configurable for boost or buck operation with limited pulse testing, or in continuous full-power operation. Test points provide easy access to connect signals to an oscilloscope for measuring the switching performance of CoolGaN™ transistors in parallel, and the gate driver. This board saves time for users designing power circuits to evaluate GaN power transistors functioning in parallel configuration.

The half-bridge circuit board has a single PWM input intended for connection to a 50 Ω pulse or signal generator. Board power comes from a single 5 V supply input, which powers everything including the isolated gate driver power supplies. Dead-time between the high- and low-side is pre-set to 100 ns, but is adjustable via trim potentiometers. An external inductor connects to the supplied pluggable terminal-block connector. The output and bus voltage can range up to 450 V, limited by the capacitor rating. This half-bridge can switch continuous currents of 28 A, and peak currents of 70 A during hard- or soft-switching. Operating frequency can be up to 1 MHz, depending on transistor dissipation (limited to about 13 W per device with appropriate heatsink, thermal interface material and airflow).

2.1 Evaluation board specifications

Table 1 Evaluation board specifications

Parameter	Values			Unit	Note
	Min.	Typ.	Max.		
V_{CC} input voltage	4.8	5.0	5.2	V	
V_{CC} input current	50	100	250	mA	Highest current at maximum frequency
PWM logic input levels	0		5	V	Standard 5 V TTL levels, 50 Ω terminated
VB+ to VB-	0	390	450	V	Limited by capacitor voltage ratings
V_{SW} to V_{in-}	0		450	V	(There may be ±50 V spikes appearing on V_{out})
Transistor pair current, DC			28	A	Keep case temp. below 125°C
Transistor pair current, pulse			70 120	A A	When case temp. is 125°C When case temp. is 25°C
Transistor pair power dissipation			26	W	With heatsink and airflow so as to keep T_{case} less than 125°C
Operating frequency	(DC)		1	MHz	Within dissipation, temperature limits
PWM pulse width	130		∞	ns	With 100 ns dead-time setting
V_{SW} transition time		7		ns	40 A load, 10 to 90 percent rise, fall times
Gate-drive voltage levels	-6		3.6	V	These are not limits, typical – and + values
Dead-time adjustment range	0		180	ns	Default setting is 100 ns. If longer dead-time is necessary, R51 and R61 can be changed accordingly.

3 Functional description

A typical block diagram is shown in **Figure 2** for a double-pulse test application setup. A 5 V power supply provides the circuit power and a 0 to 400 V power supply provides the DC bus voltage. The input PWM signal is provided by a lab pulse generator. A test inductor is then connected from the DC bus to the switch-node output. An oscilloscope can then be used to measure the inductor current (with a current probe) as well as each of the GaN power transistors at the corresponding test points (TP1a/b and TP2a/b), switch-node voltage or any other signal on the board. Available test points are described in **Table 2**.

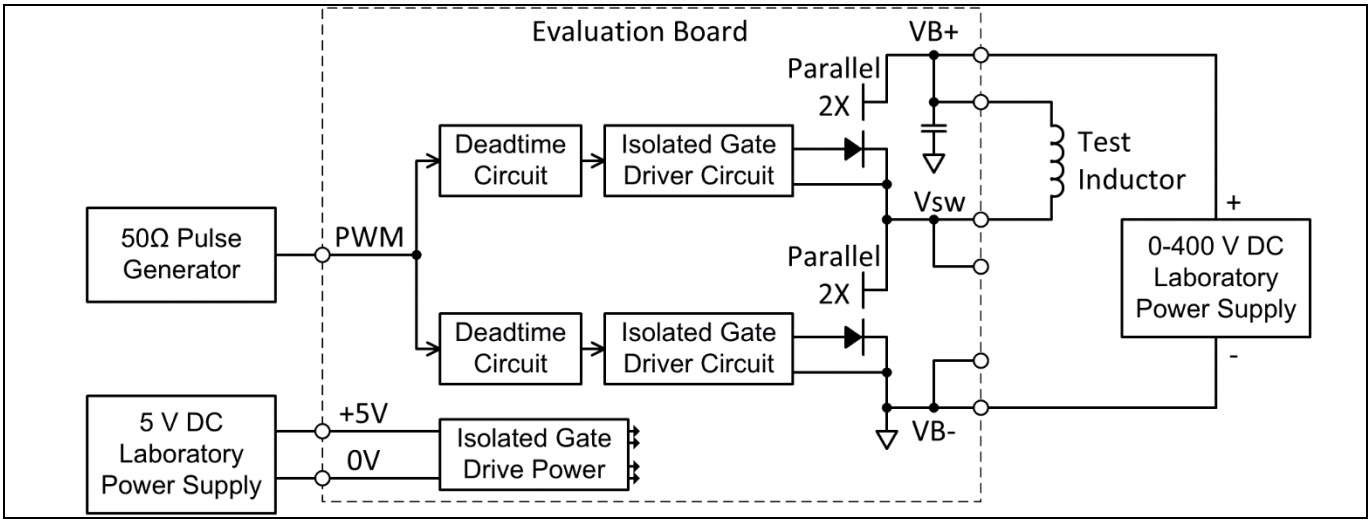


Figure 2 Evaluation board application example (double-pulse test)

Note that the inductor can be connected to either the positive DC bus as shown in **Figure 2**, or the negative bus (VB-) for inverted double-pulse where the high-side is the active switch, and the low-side is the freewheeling synchronous rectifier (**Figure 3**).

The evaluation board can also be easily configured as a buck or boost topology. See sections **5.2.2** and **5.2.3** for further details.

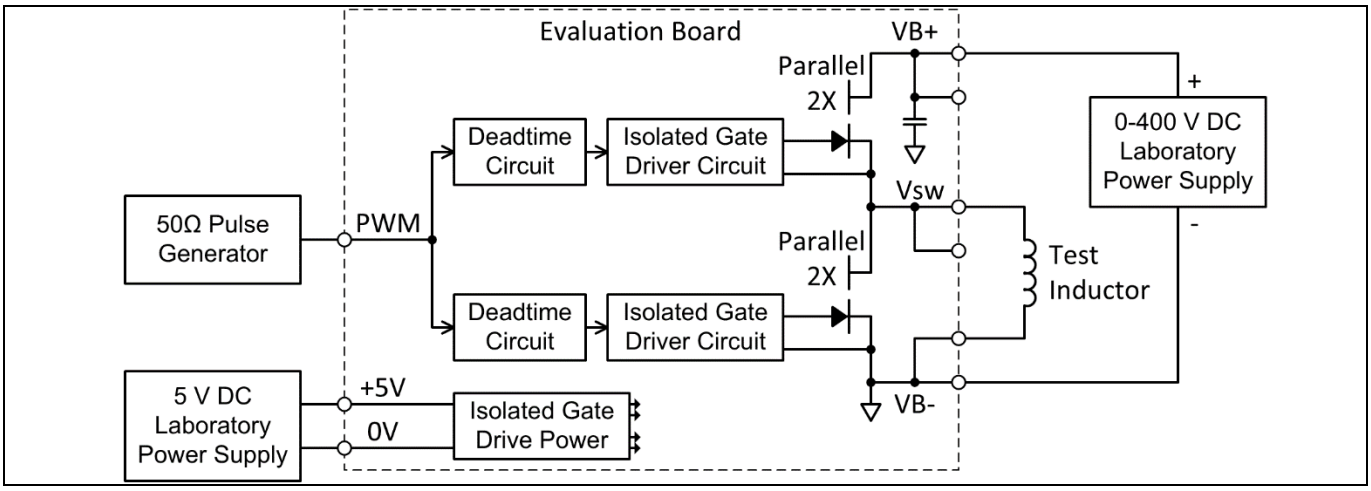


Figure 3 Evaluation board connected for inverted double-pulse test

4 Circuit description

The following sections explain each portion of the circuit in detail.

4.1 Input logic

Logic-level PWM input connects to X2 (MMCX connector) which is terminated by 50 Ω (the parallel combination of R81 to 84). The input is buffered by non-inverting buffer U1 for the high-side, and inverting buffer U2 for the low-side. These buffers are expecting standard logic-level input voltage from the PWM source, low less than or equal to 0.8 V and high 2 to 5 V. When the PWM input is low, the switch-node V_{SW} is low (the low-side GaN transistor turns on). Conversely, when the PWM input is high, the V_{SW} node is driven high as the high-side GaN transistor turns on.

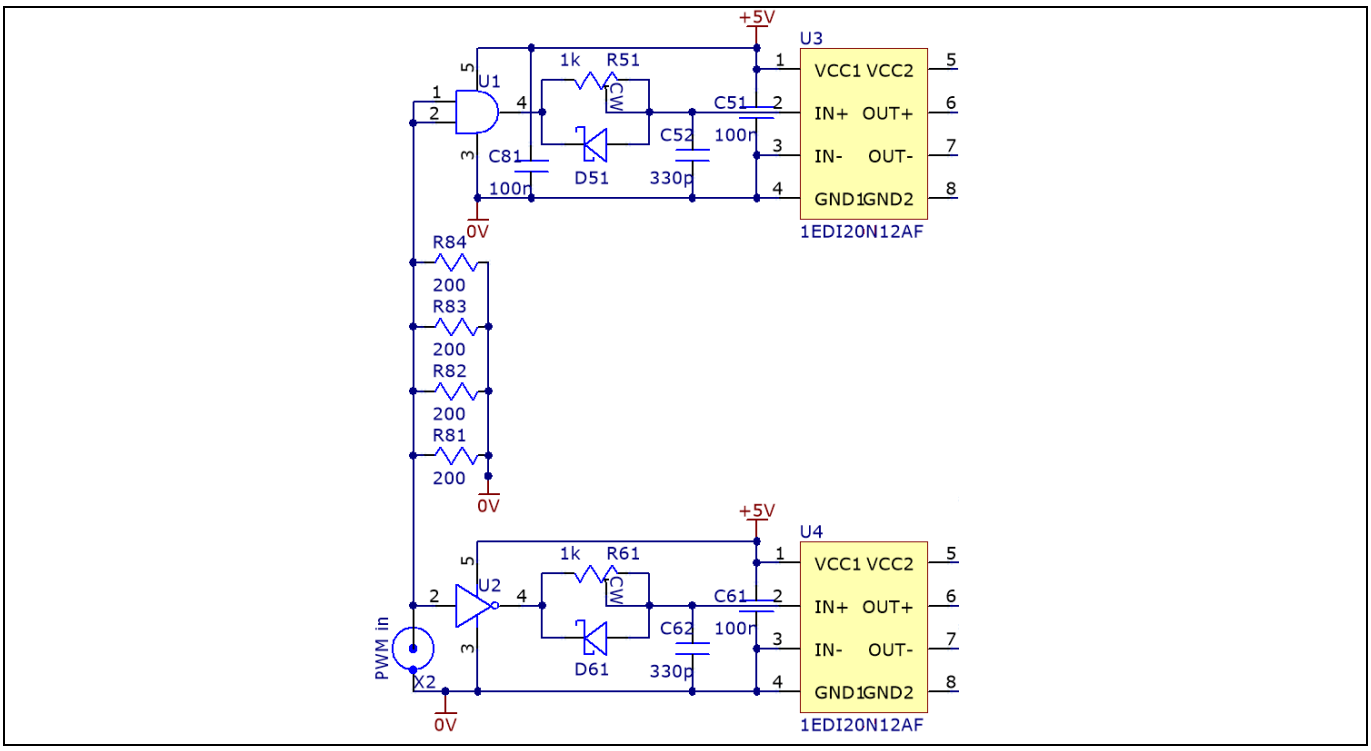


Figure 4 Input logic and dead-time generator

The purpose of the dead-time circuit is to make sure that the high- and low-side GaN transistors are never on simultaneously. The dead-time should be set long enough that the high-side always fully turns off before the low-side turns on (with some margin), and vice versa. A simple adjustable RCD delay circuit generates the dead-time. Whenever U1 or U2 outputs a positive (turn-on) edge, the Rx1-Cx2 low-pass filter delays the signal by the RC time constant to the Schmitt-trigger PWM input of the respective gate driver IC. But the turn-off edge is not delayed because the Schottky diodes Dx1 bypass the resistor. Thus, each driver IC input has a delayed turn-on edge, and a non-delayed turn-off edge.

The practical minimum output pulse width at V_{SW} is about 30 ns. This would occur with an input PWM pulse width of 130 ns (minus the 100 ns dead-time as described above). Any input pulse width shorter than this is not recommended, as the resulting output pulse is so small it is really no longer effective. For extremely short output pulse widths, contact your local Infineon applications support team to discuss gate-drive circuit optimization for the specific requirement.The 5 V input power (VCC1) to the two gate driver ICs is bypassed with a 100 nF high-frequency bypass capacitor (Cx1).

4.2 Isolated gate driver power supply

Power for the gate drivers is provided by a simple isolated DC-DC converter, shown in **Figure 5**. It takes the +5 V input and provides two isolated 12 V outputs (VCC2-GND2). A small transformer T1 provides low-capacitance isolation and voltage scaling. The primary of T1 is driven by U5, a MAX256 isolated power supply driver. It provides 50 percent duty-cycle PWM, current-limited, balanced voltage to the transformer at about 500 kHz. The secondary sides are both voltage doublers consisting of Cx2, BAT54S Dx0 and C1x/C3x. The voltage doublers are used instead of straight rectifiers because this reduces the transformer turns ratio, thus providing lower leakage inductance for better load regulation. Proper regulation at all times is achieved by the additional circuit consisting of Rx4 and the shunt regulator UX0.

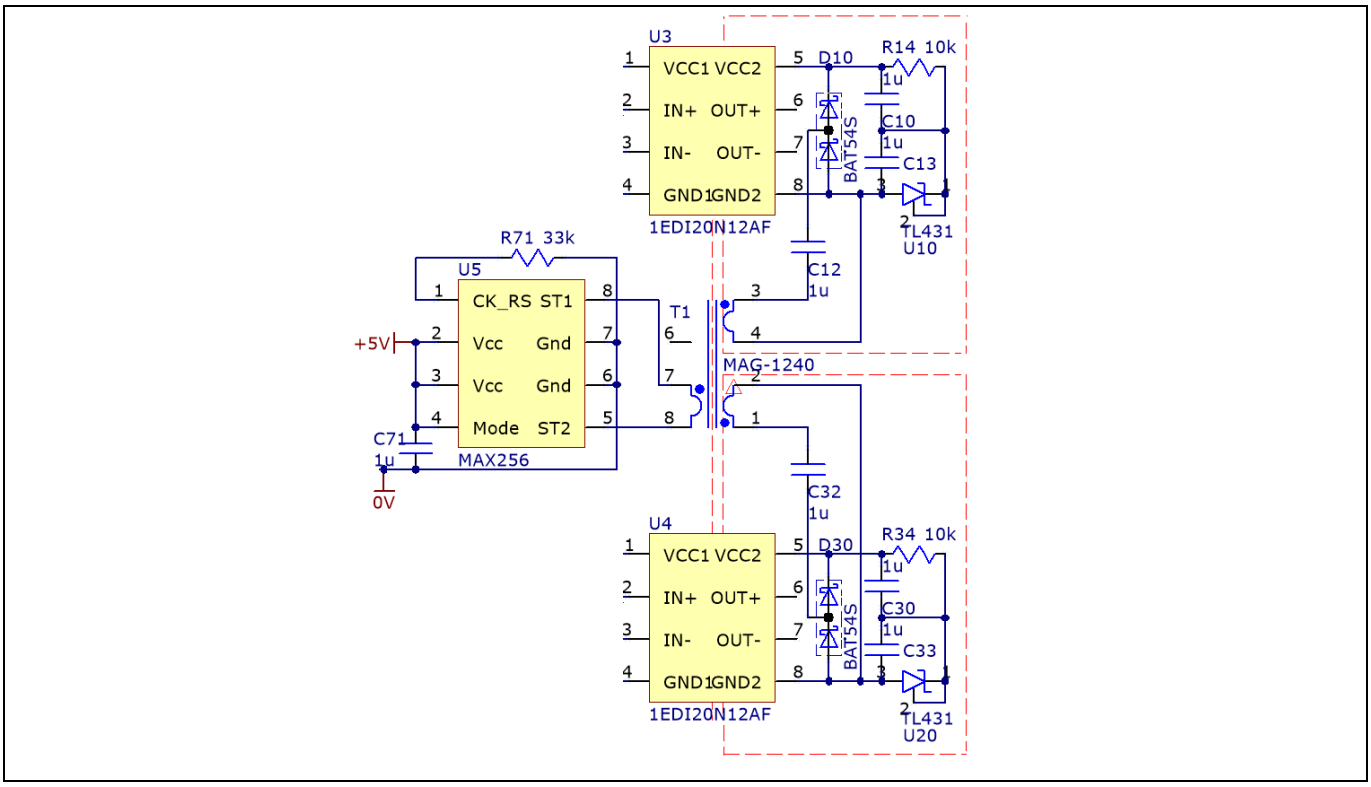


Figure 5 Isolated gate driver power supply

4.2.1 Gate driver power supply transformer

The transformer used in the gate driver power supply is specifically designed to operate with the driver IC U5 (in **Figure 5**) at 500 kHz, with the appropriate turns ratio to provide the twin isolated 12 V outputs along with the doubler circuit. Moreover, the winding arrangement balances low inter-winding capacitance with good coupling (low leakage inductance) and more than 1000 V isolation. The low capacitance is important for minimizing CM current injection due to fast-switching transients, and the low leakage helps with open-loop output voltage regulation.

The transformer is based on a Ferroxcube **ER9.5/2.5/5-3C94-S** or TDK **B65523J0000R087** ungapped core set. The matching single-section bobbin part number is Ferroxcube **CPVS-ER9.5-1S-8P-Z** or TDK **B65527B1008T001**. All three windings are made using 40 AWG magnet wire. The two secondary windings are 12 turns each, and the primary is 10 turns. For full construction detail, contact your local Infineon applications support team.

4.3 Gate drive circuit

The output side of the gate driver circuit is shown in **Figure 6**. As can be seen, the paralleling of each high- and low-side pair is done with a single gate drive and with each GaN transistor having its own Rx0, Rx1, Rx2-Cx1 driving network. It is worth noticing how the **1EDI20N12AF** driver's separate source (OUT+) and sink (OUT-) outputs are connected for turn-on and turn-off of the devices, respectively.

The actual driving of the GaN transitors is realized by splitting the +12 V into a positive and a negative. Negative driver voltage is regulated at -2.5 V to ensure that the gate threshold voltages are not exceeded during transients and also to minimize the reverse conduction losses. The advantage of this solution is that the gate voltage of the GaN device is well defined with respect to the negative driver voltage. Even at small duty-cycle values (with dominant off-times) the voltage on the gate will not move toward 0 V and thus guarantee robustness against the C dv/dt that is induced by gate turn-on.

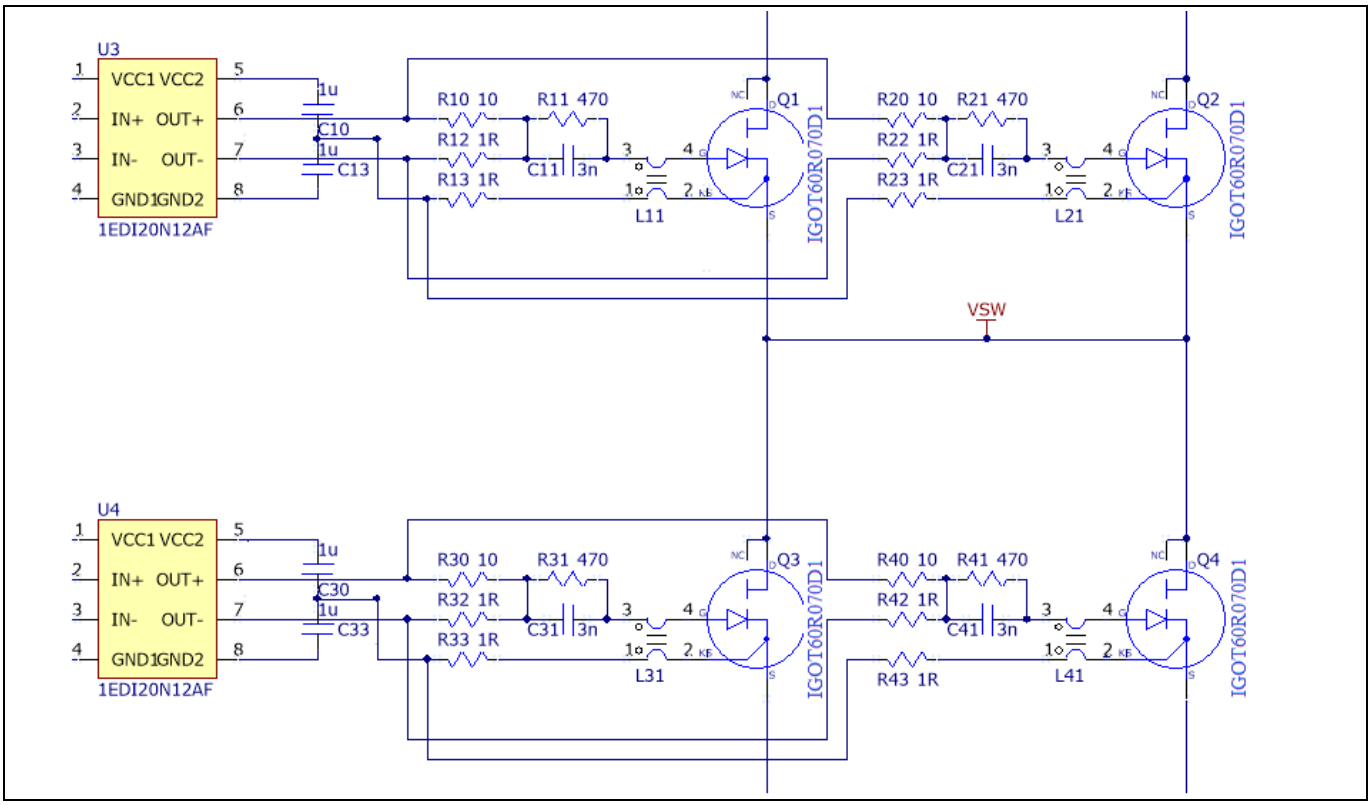


Figure 6 Gate driver output section

If two GaN devices are directly paralleled, even with separate RC networks on each gate, there is still a shared current path that will interfere with the gate driver loops. The main intended current path for the source current is through the source terminals and their connection on the PCB, as seen in **Figure 7** in green. But through the Kelvin source connection, there is another parallel path shown in red. Ideally all of the source current would flow only in the intended primary path, and no current would flow in the alternate path. But of course there will be some finite current flowing in the parallel alternate path, and if the impedance and routing of all the connections are not identical, then the gate loops for each CoolGaN™ HEMT transistor can have different impedances, and therefore differential V_{GS} voltage can result. A few hundred mV difference between Kelvin source pins due to the different main path source currents would result in several amps of undesirable Kelvin source currents. Furthermore, undesirable main current effects would be immediately detected as unbalanced current sharing as well as severe oscillatons between the two GaN transistors during the switching events. Please refer to section **5.7.3** for further understanding of this severe issue.

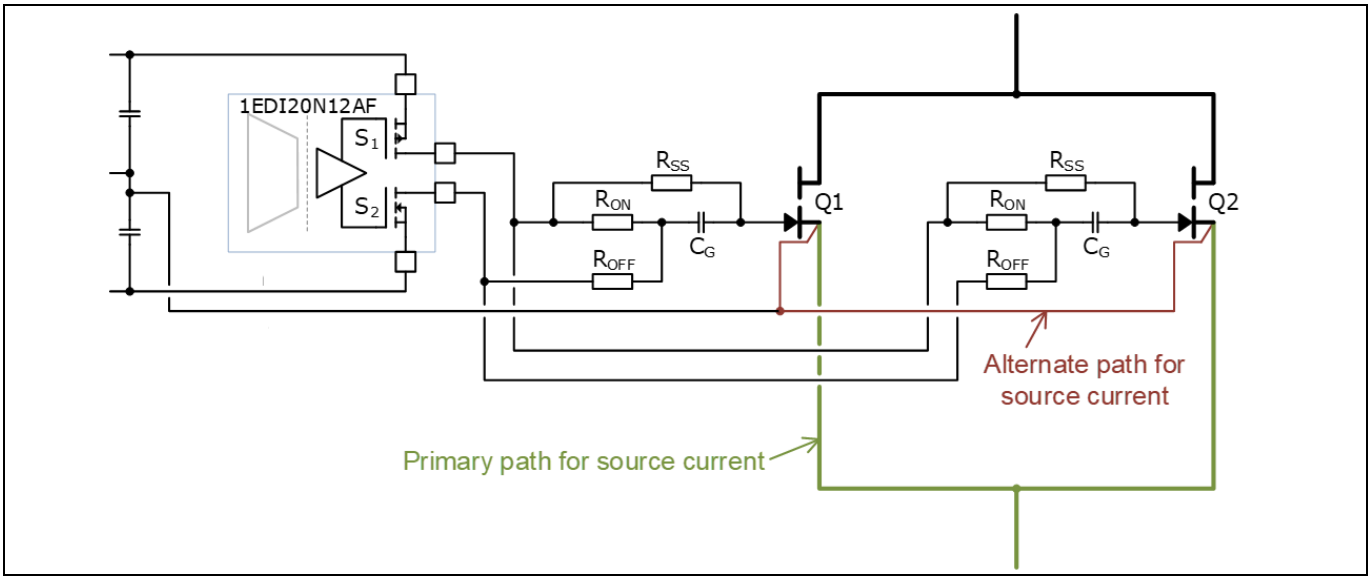


Figure 7 Directly paralleled GaN HEMT devices

Reliable operation of GaN transistors working in parallel is possible by just adding a very high CM path impedance – in the range of hundreds of Ω – but still a very low DCR between them to ensure proper gate driving due to unbalanced circuit impedances. This is achieved by placing CM inductors, like Bourns SRF2012-361YA, between the gates and the corresponding Kelvin source driver return path along with 1 Ω resistors. The gate-drive loop sees only a small leakage inductance, but the shared current path between the Kelvin source connections sees the full differential (CM) inductance of both CM inductors, as indicated in **Figure 8**. At the end, as previously stated, proper selection of the CM inductor value should be made without compromising the capability of the gate driver.

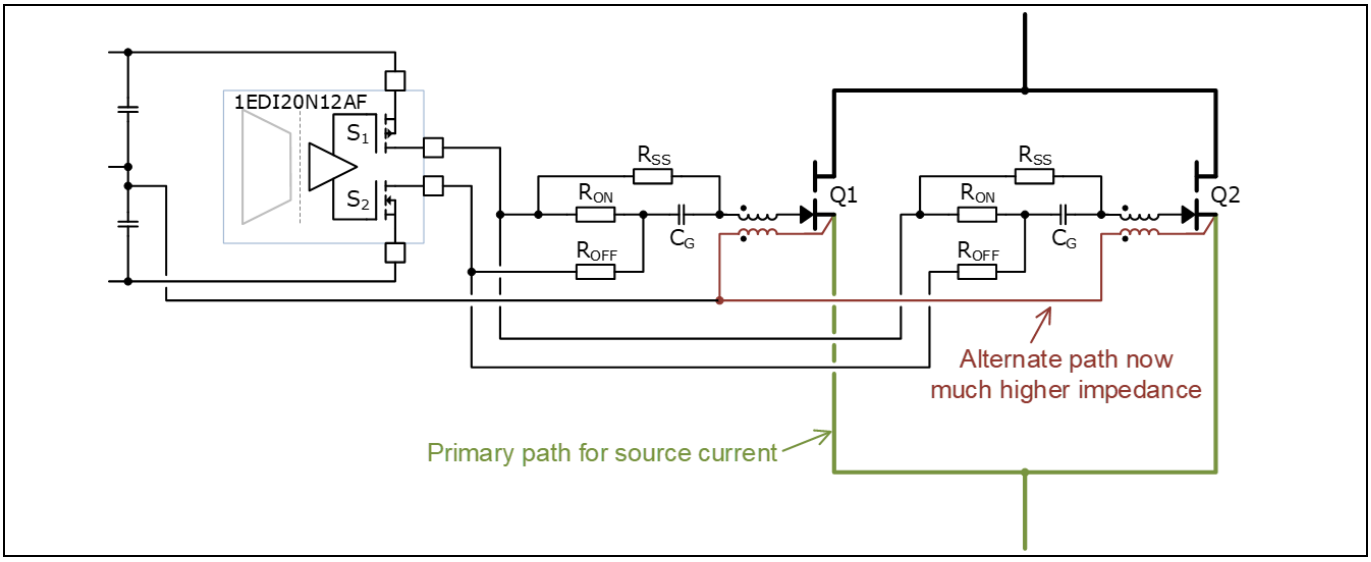


Figure 8 Paralleled GaN HEMT devices with CM inductors in gate to Kelvin source paths

4.4 Half-bridge circuit

GaN transistors Q1 and Q2 form the high-side and Q3 and Q4 form the low-side transistors of the half-bridge, as shown in **Figure 9**. The drains of Q1 and Q2 are connected to their corresponding Current Sense (CS) shunt resistor array, RxA-RxE. This arrangement allows the monitoring of each of the transistor drain currents, on TPxa/b, as well as the ability to obtain cleaner and more reliable measurements. This also avoids any spurious gate-source loop signals if the current shunt resistors are placed on the bottom-side devices. Hence, the sources of Q3 and Q4 are directly connected to the to DC bus (VB-).

Capacitors C4 to C7 are high-frequency bypass capacitors for keeping the half-bridge input (when configured as buck converter) or output (when configured as boost converter) loop smaller. The bulk electrolytic bus capacitor C3 has a value of 100 µF. This capacitive network along with a low-inductance power-loop layout provides an extremely low-impedance bus with very little overshoot or ringing, as evidenced by the waveforms in **Figure 13** and **Figure 15**, where you can see 76 A commutating to the bus in a few ns, with less than 100 V overshoot. For any specific test/evaluation requirements, further capacitance can be added by attaching external capacitors to the X3 connector.

Attention: ***Normally the bus capacitor is discharged when the lab power supply is switched off. But if the power connector is removed while the capacitor is charged (not recommended!), the bus capacitor can store high voltage and this takes several minutes to dissipate. Be sure to wait until the capacitor voltage is at a safe level before handling the board.***

The half-bridge point labeled “VSW” should be used as the point for connecting the test inductor for either hard-switching or soft-switching applications through pins 3 and 4 of the X1 connector, as shown in **Figure 9**. Test circuit diagram examples and the associated topologies are provided in section **5.2**.

Attention: ***On one hand, the drain-source voltage waveform of the top-side pair can be monitored at TP12 by having the reference of the oscilloscope attached at VB+. On the other hand, the drain-source voltage waveform of the bottom-side pair can be monitored at TP34 by having the reference of the oscilloscope attached at VB-.***

Gate signals of each side’s GaN transistors can be monitored at each of the corresponding TPx1 test points either by MMCX connectors on the high-side components or at PCB points in the low-side ones.

Attention: ***Due to the actual configuration of the board, one sole gate signal can be monitored at a time using a standard passive probe with the oscilloscope electrically isolated and measuring no other signal. If one top-side and one bottom-side GaN transistor gate signal is required to be monitored or a gate signal needs to be compared to any other voltage/current signal, it is highly recommended to use an electro-optical isolated probe, e.g., Tektronix TIVM1, for doing measurements on a top-side GaN transitor. Ordinary active differential probes are not recommended as these have insufficient CM range for making such high-frequency high dv/dt measurements. However, 1 GHz bandwidth active diffential probes could be used.***

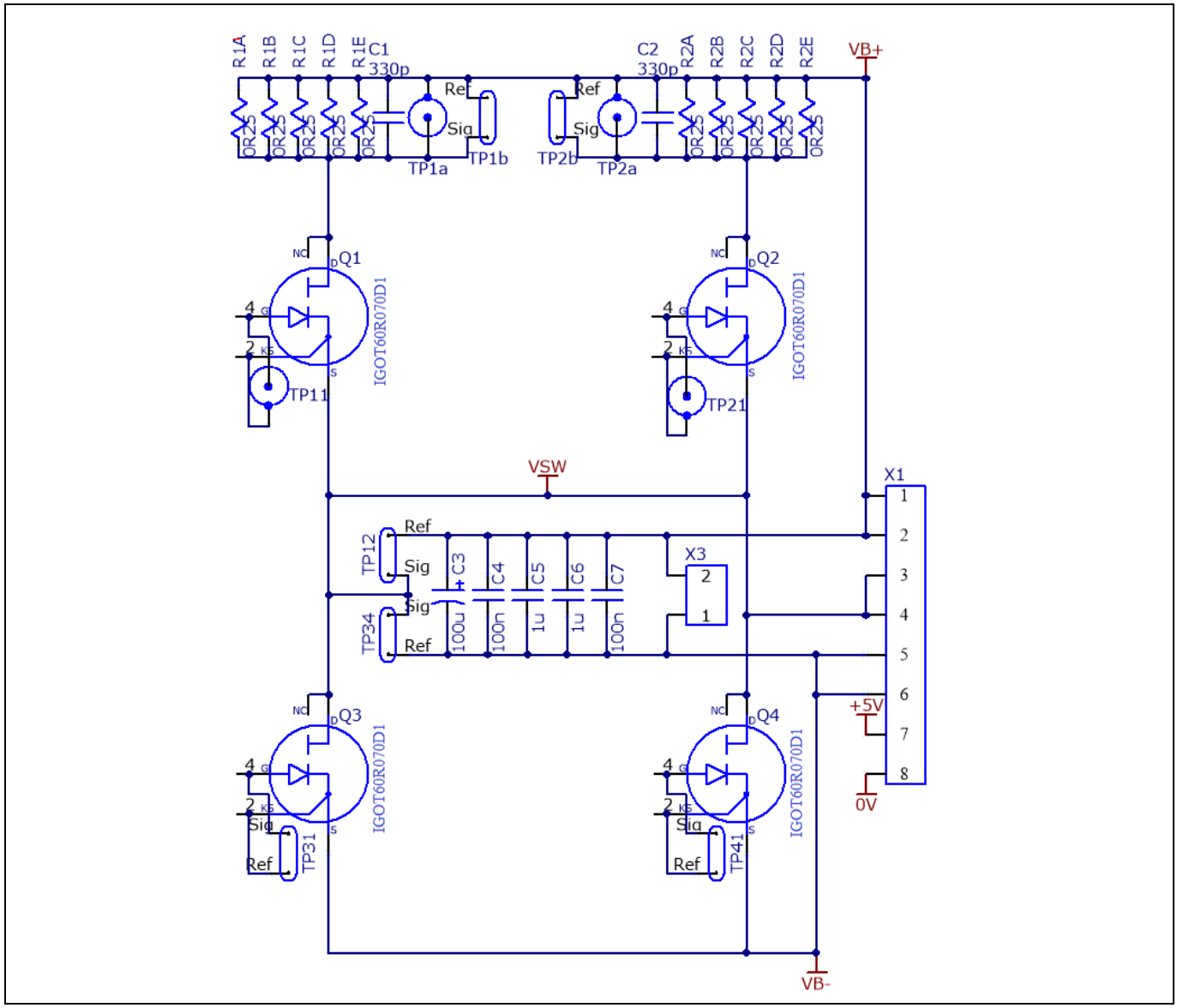


Figure 9 Half-bridge circuit

5 Setup and use

Attention: ***This evaluation board has exposed high-voltage contacts. Use appropriate protective measures to avoid shock. The evaluation board has no over-current shutdown, so it is possible to drive the GaN transistors to currents far beyond their rating, which may result in their destruction. Use appropriate protective covers to prevent any possible injury from exploding components. Observe the maximum rating of the DC bus capacitor, and keep the bus voltage below 450 V. Exceeding this value risks the capacitor venting violently. Always set appropriate current limit values on the external lab power supplies to minimize catastrophic damage to the board in the event of a fault. It is up to you to set the PWM input signal appropriately to avoid damage.***

5.1 Test equipment needed

- 5 V power supply capable of 0.5 A output current to supply V_{CC}.
- Bus voltage supply up to 450 V DC with sufficient current to supply the power needed for the test of interest. For short pulse testing even to maximum current, the current drawn from the bus voltage supply is very small, as the DC bus bulk storage capacitor provides the instantaneous energy.
- Signal generator to provide the necessary PWM drive command for the half-bridge. The generator must be capable of driving standard 5 V logic levels into a 50 Ω terminated load. Rise and fall time should be in the 5 ns range for best timing accuracy/repeatability.
- 1.2 mm slotted screwdriver for adjusting the dead-time trim potentiometers R51 and R61.
- Interconnect cable for PWM input: The PWM input connector is a 50 Ω terminated MMCX coaxial connector. Assuming the signal source is a conventional BNC connector, you will need a BNC male to MMCX plug cable (Fairview Microwave FMC0809315) or a BNC to MMCX adapter.
- Oscilloscope for measurement. Due to the fast transient voltage and current possible with GaN transistors, an oscilloscope with a bandwidth of more than 500 MHz is recommended.
- For measuring high-side gate voltages, a 1 GHz isolated probe such as the Tektronix TIVM1 is recommended. MMCX connectors are provided for this purpose (TP11 and T21 on the back side of the board). We are not aware of any other isolated probe with sufficient CM transient immunity to accurately measure the high-side gate voltage.
- A standard (more than 500 MHz) passive probe with the short ground pin can be used to measure either Q3 or Q4 low-side gate voltage on TP31 or TP41, respectively. But the test point reference on the Kelvin source of Q3 or Q4 may have ground bounce compared to the V_{SW} measurement reference due to L di/dt ground bounce. A hinged snap-on ferrite core on each passive probe cable can help minimize any measurement artifacts due to CM cable shield currents. Another effective solution is to use a 1 GHz active differential probe such as the Tektronix TDP1000. This can further minimize measurement errors/artifacts due to CM ground currents, but can be sensitive to coupled dv/dt from the TIVM1 probe snout.
- Make sure the voltage probe used on TP12 and/or T34 to measure the switch-node voltage is rated appropriately for voltage and bandwidth. We recommend either Tektronix TPP0850 50x high-voltage probe with 800 MHz bandwidth, Tektronix P5100A 100x high-voltage probe with 500 MHz bandwidth or PMK 1000 100x high-voltage probe with 400 MHz.

5.2 Connections to terminal block

With the exception of the coaxial PWM connection to X2, all other I/O and power connections to the evaluation board are made to the pluggable terminal block X1. The pluggable terminal block makes it more convenient to

remove the board from the test bench for any component value changes during testing, without having to disconnect and reconnect everything each time a change is made.

5.2.1 Connections for double-pulse testing

Referring back to **Figure 2** for the proper setup and connections for double-pulse testing. Note the configuration of all power connections. The inductor also connects to the terminal block. No load is required for pulse testing – the inductor energy is dissipated in the freewheeling transistor.

5.2.2 Connections for buck topology

When the external inductor is connected between V_{SW} and the DC load, the circuit is configured as a buck converter. If a PWM signal is applied to the PWM input, the output voltage will be proportional to the input voltage times the PWM duty cycle. With the appropriate inductor, PWM frequency can be set low (tens of kHz), or up to 1 MHz. The circuit can be operated continuously in this mode, **provided that the temperature of the transistors is kept to a safe level**. The circuit is entirely open-loop since there is no feedback control, so the output will not be load regulated. When operating at high frequencies, ensure that the inductor ripple current always changes polarity each half-cycle, so that the circuit operates in ZVS mode. Otherwise, hard-switching at high frequency will result in large power dissipation due to the switching loss.

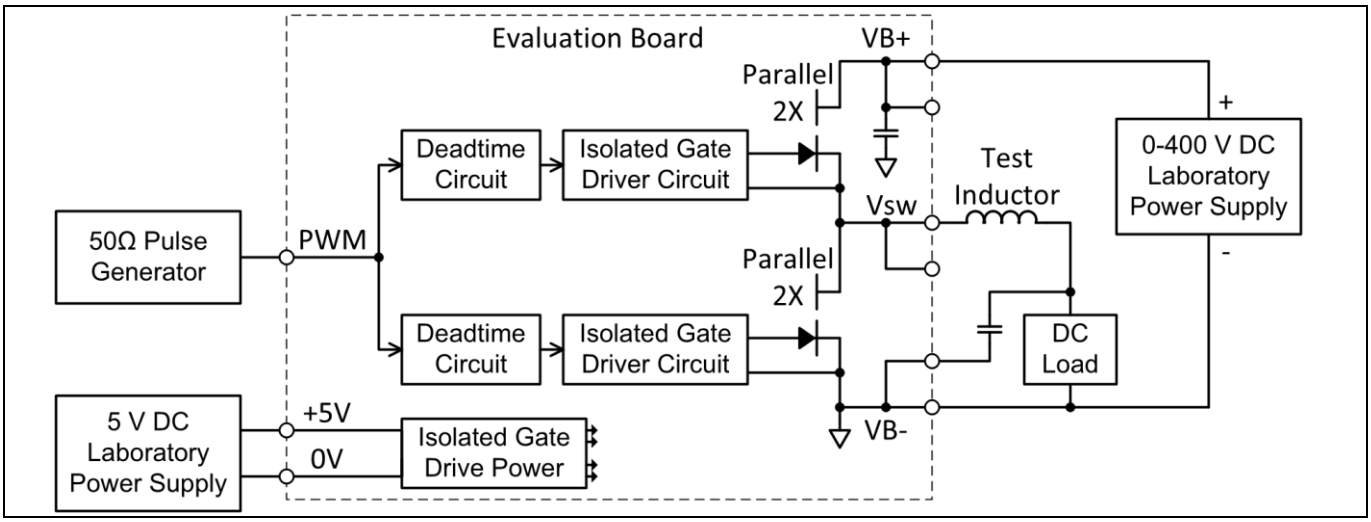


Figure 10 Connecting the evaluation board in the buck configuration

5.2.3 Connections for boost topology

When operated in boost mode, the roles of V_{SW} and VB+ are reversed. **Figure 11** shows how the inductor is connected between the input power supply and the switch node. When the low-side transistor is on, inductor current is ramped up, then it is commutated to the “output” (the VB+ bus) through the high-side transistor, which acts as a synchronous rectifier. An appropriate load must be connected to the VB+ terminal.

Attention: ***When operated in boost mode, it is possible to rapidly charge the VB+ bus to voltages beyond its rating, which may result in catastrophic failure of the bus capacitors and other components. Always make sure that the input voltage, PWM signals and output load are coordinated to achieve the desired output voltage in this mode, as there is no closed-loop voltage control or limit.***

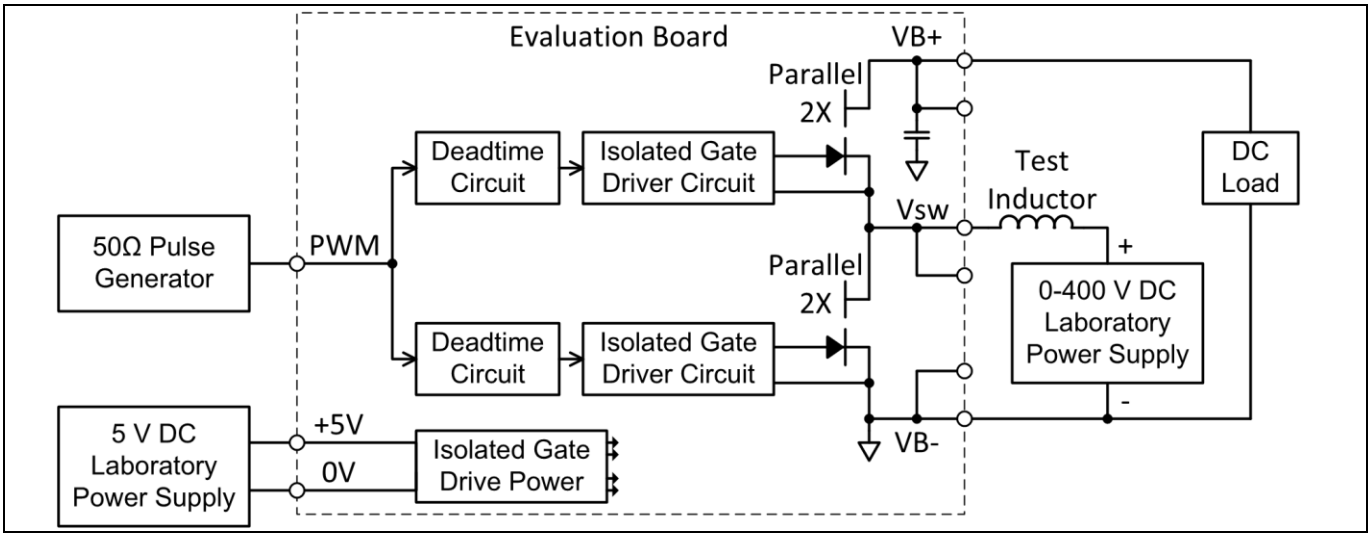


Figure 11 Connecting the evaluation board in the boost configuration

5.2.4 Continuous operation

Continuous operation of the board in buck or boost mode is possible if a suitable heatsink is attached to the DSO devices, along with a Thermal Interface Material (TIM) and the appropriate forced-air cooling system. The precise thermal management must be carefully calculated and managed by the user. The following cooling options are possible:

- Single heatsink that could be directly soldered to the exposed pad of each GaN HEMT device from Fischer Elektronik: ICK SMD A 13 MI.
- Heatsink plus fan from Fischer Elektronik: LA ICK 15 x 15 F 05 or F12.
- Heatsink from Adafruit Industries LLC at Digikey distributor: 1528-1693-ND. As this heatsink cannot be symmetrically placed on the top of the device due to the proximity to the heatsink of the next device, a flame-retardant polyimide high-grade masking tape might be needed to cover those components (resistors, capacitors) that lie beneath the heatsink, just as a measure of extra protection.

5.3 Input generator connections and settings

The PWM input is the logic command to the half-bridge output: when the PWM input is high, the half-bridge output V_{SW} is at its high state (connected to the VB+ bus). Conversely, when the PWM input command is at logic low, the half-bridge output V_{SW} is at 0 (VB-). The input is an MMCX coaxial connector terminated in 50 Ω. Recommended signal/pulse generator settings are fastest rise/fall time, low level of 0 V and high level of 3.5 V. The pulse generator can be set to pulse or burst mode for double-pulse testing, or continuous operation for buck or boost modes, within the constraints of the warnings given in sections **5** and **5.2.3**.

5.4 Measurement points

The evaluation board has 10 test points for connecting an oscilloscope to look at various signals. The test points are either a through-hole pad-pair, or an MMCX connector. The pad-pairs have a letterscreen symbol that identifies which pads are signal and reference (common): the signal pad is designated by the ~ symbol, and the reference pad is designated by the ⊥ symbol.

Table 2 Test point label descriptions

Test point label	Description
TP1a/TP2a	Shunt voltage drop due to the current through the high-side Q1/Q2 GaN HEMT. Please note that the shunt value is 50 mΩ. This test point is an MMCX connector and is designed to be directly connected either to the input of a Tektronix TIVM1 isolated probe or to the oscilloscope through an MMCX to BNC adapter/cable assembly. In case the second option is used, note that the reference point (the barrel of TP1a/TP2a MMCX connector) is essentially at a high voltage, i.e. VB+. **Do not use another non-isolated probe to measure any other signal on a different test point or damage will occur**. (Except any other TP having the same reference at TP1a/TP2a.)
TP1b/TP2b	This is the test point to observe the shunt voltage drop due to the current through the high-side Q1/Q2 GaN HEMT. Note that the reference pad is essentially at a high voltage, i.e. VB+. **Do not use another non-isolated probe to measure any other signal on a different test point or damage will occur**. (Except any other TP having the same reference at TP1b/TP2b.)
TP11/TP21	High-side gate voltage: signal is the gate of Q1/Q2, reference is the Kelvin source of Q1/Q2. This test point is an MMCX connector and is designed to be directly connected to the input of a Tektronix TIVM1 isolated probe. Note that the reference point (the barrel of TP1 MMCX connector) is essentially the output switch node of the half-bridge so the CM voltage is a fast high-voltage signal – **do not use a non-isolated probe on TP11/TP21 or damage will occur**. The CM voltage is 0-VB+, and the differential-mode measured signal at this point is typically in the range of -8 V to +4 V.
TP31/TP41	Low-side gate voltage: signal is the gate of Q3/Q4, reference is the Kelvin source of Q3/Q4. Since the reference is the Kelvin-source, there is some CM voltage bounce between this test point reference and “ground” (VB-, the reference point for TP34). See recommendations in section **5.1**.
TP12	This is the test point to observe the half-bridge switch-node output respect to VB+. In other words, helps to monitor the drain-to-source voltage of the high-side GaN transistors. Since the bus voltage is typically in the range of 350 to 400 V, be sure to use a voltage probe with appropriate voltage rating.
TP34	This is the test point to observe the half-bridge switch-node output with respect to VB-. In other words, helps to monitor the drain-to-source voltage of the low-side GaN transistors. Since the bus voltage is typically in the range of 350 to 400 V, be sure to use a voltage probe with appropriate voltage rating.

5.5 Power-up and power-down sequencing

The gate drivers are designed to keep V_{GS} below the turn-on threshold even if they are unpowered. Regardless, it is good practice to make sure the 5 V power (and thus the gate drivers) is always applied before powering up the high-voltage bus. Conversely, power-down the high-voltage bus before powering-down the 5 V supply. Recommended current limit on the 5 V lab supply is 300 mA, and on the high-voltage supply, it depends on the expected load power. For basic double-pulse testing, even to 100 A peak, the HV supply can be limited to 1 A because the on-board bus capacitors will provide the peak current.

5.6 Verifying and adjusting dead-time

The evaluation board has two independent dead-time adjustments. When the PWM input goes high, the low-side gate driver turns off and then the high-side gate driver turns on after the rising-edge dead-time. This dead-time is adjusted with the trim potentiometer R51. On the falling edge of PWM input, the high-side gate driver turns off, then the low-side gate driver turns on after the falling-edge dead-time. This is adjusted with the trim potentiometer R61. A small (1.2 mm) slotted (flat-blade) screwdriver will be needed to adjust the trim potentiometers.

To verify and adjust dead-time, connect a 5 V DC supply to the 5 V input on the evaluation board, and connect a pulse generator to the PWM input X2 (refer to section **5.3**). Set the generator for a square-wave (50 percent duty cycle) at 100 kHz and apply the 5 V power to the board. Connect a probe to TP31 (low-side gate), and an isolated probe (TIVM1, mentioned earlier) to a high-side gate test connector, say TP11. Be sure to follow the scope instructions for adjusting the scope channel timing-offset “de-skew” values to compensate for the group delay of each probe. Isolated probes can have significant delay times on the order of 30 ns, so that could result in a large error if the de-skew is not properly calibrated on the scope.

Note: If an isolated probe is not available, standard passive probes can be used to measure the high-side gate signal for setting dead-time, as long as the high-voltage bus is at 0 V. Just be sure to disconnect the passive probe from TP11 or TP21 before applying any bus voltage.

Apply power to the board, monitor the PWM signal on X2 and trigger on the rising edge. Adjust R51 (trim potentiometer) to achieve the desired dead-time (factory preset is 100 ns). Adjust trim potentiometer R61 to dial-in the dead-time to the desired value on the falling edge of PWM. Normally the rising and falling edge dead-times are set to the same value. Turning the trim potentiometers clockwise increases the dead-time.

5.7 Starting measurements

5.7.1 Performance under hard-switching with double-pulse test

Assuming the board is already set up per sections **5.5** and **5.6**, the next step is to add an external inductor and bring up the DC bus to operate at the desired test condition. This example shows how to set up the board for double-pulse testing. In such testing, first a GaN transistor pair turns on and ramps up the inductor current to a test value. Then this GaN transistor pair turns off, and the current freewheels through the other GaN transistor, which acts as a synchronous rectifier. The second pulse shows hard-switched turn-on performance on the leading edge (at the test current) and then continues the ramp to a higher current level. GaN devices perform particularly well on these tests because the freewheeling diode has zero reverse-recovery characteristic. Double-pulse testing is typically done one burst at a time (not continuously) in order to keep power dissipation low, even when testing to the voltage and current limits of the device.

Connect an external inductor and HV power supply as shown in **Figure 2**. Set the pulse generator for double-pulse operation with the desired on-times and off-times between them. Choose the inductor value and the test voltage to give the desired current ramp for the test.

Note: When the low-side GaN transistor pair is operated in the double-pulse test, the default state of the half-bridge is that the high-side synchronous rectifier is normally-on. Thus, the logic input should be inverted – normally high with two pulses going low. Make sure to power-off the HV supply before shutting off the output of the pulse generator: if the pulse generator is powered off first, it will turn-on the low-side and ramp the current to uncontrolled value, unless the bus is at zero volts. ***The HV supply should always be the last thing to turn-on, and the first thing to turn-off when measurement is completed.***

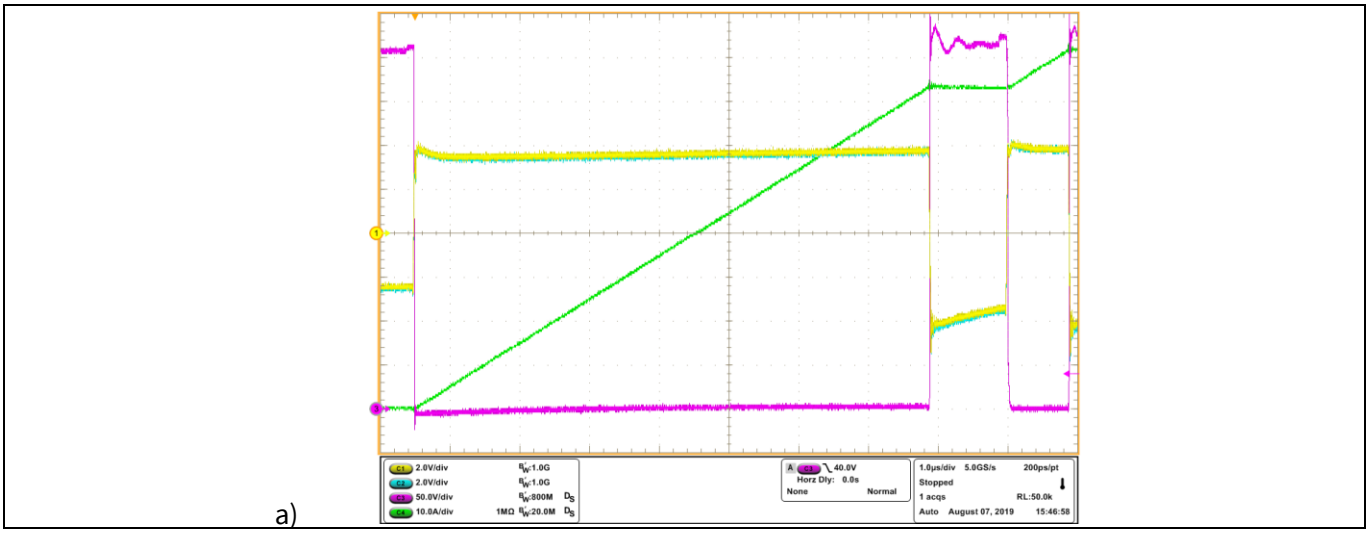
For the inductor(s) under test a low-permeability toroidal core, say μ_i = 10, and physically big enough so that a single-layer winding with minimal interwinding capacitance is recommended. The number of turns and the wire gauge must be chosen according to the current to be tested. A good reference is the Micrometals T200-2B powder toroidal core. For example at 400 V DC bus voltage with a pulse width of 5 µs, if the desired peak current at the end of the pulse is 40 A then a 50 µH inductor would be required.

Start with a low voltage on the DC bus, say 25 V, just to make sure that everything is connected properly, and that the current is ramping up as expected, the current probe polarity is correct, etc. If everything looks good, then continue to increase the bus voltage while checking test pulses to ensure the waveforms are as expected. This will also help to ensure that the inductor is not saturating and the current is within bounds. The typical test condition is to set the bus voltage to 400 V, and keep the current peak to 100 A or lower. Adjust the pulse on-time to increase or decrease the current at the end of each pulse.

Key to the following figure:

Table 3 Oscilloscope channels description

CH 1 (yellow)	Q3 low-side GaN gate singal, 2 V/div
CH 2 (blue)	Q4 low-side GaN gate signal, 2 V/div
CH 3 (purple)	V_{SW}, switch-node voltage, 50 V/div
Ch 4 (green)	Total switch-node current, 40 A/div



a)

Figure 12 Double-pulse test waveform example by monitoring the low-side GaN transistor pair

Refer to **Figure 12** for the following timing sequence description: at the beginning of the waveform, the high-side has been on for a long time, and the low-side has been off. First, the high-side gate turns-off, followed by the low-side gate turning on. When the low-side transistor turns on, the current in the inductor ramps up at a rate determined by $I_L = V_{BUS}t_{ON}/L$. Then the low-side switches turn-off, and the inductor current (e.g., 74 A) immediately commutates to the high-side transistor operating in third-quadrant conduction mode. It can be appreciated that the switch-node voltage rises several volts above the bus during dead-time (or transition time), i.e. up to 500 V. Then the high-side transistor gate turns on. The inductor current freewheels for about 1.1 µs, then the low-side turns on again for the second pulse. The cycle repeats as the inductor current ramps to a higher value, in this case 82 A (this could be lower if the second pulse is shortened). The “body diode” voltage-drop effect of the low-side GaN transistor can be appreciated as a voltage bump of around 10 V during 100 ns (dead-time) prior to the second pulse.

Key to the following figures:

Table 4 Oscilloscope channels description

CH 1 (yellow)	Q3 low-side GaN gate waveform, 2 V/div
CH 2 (blue)	Q4 low-side GaN gate waveform, 2 V/div
CH 3 (purple)	V_{SW}, switch-node voltage, 50 V/div
Ch 4 (green)	Total switch-node current, 40 A/div

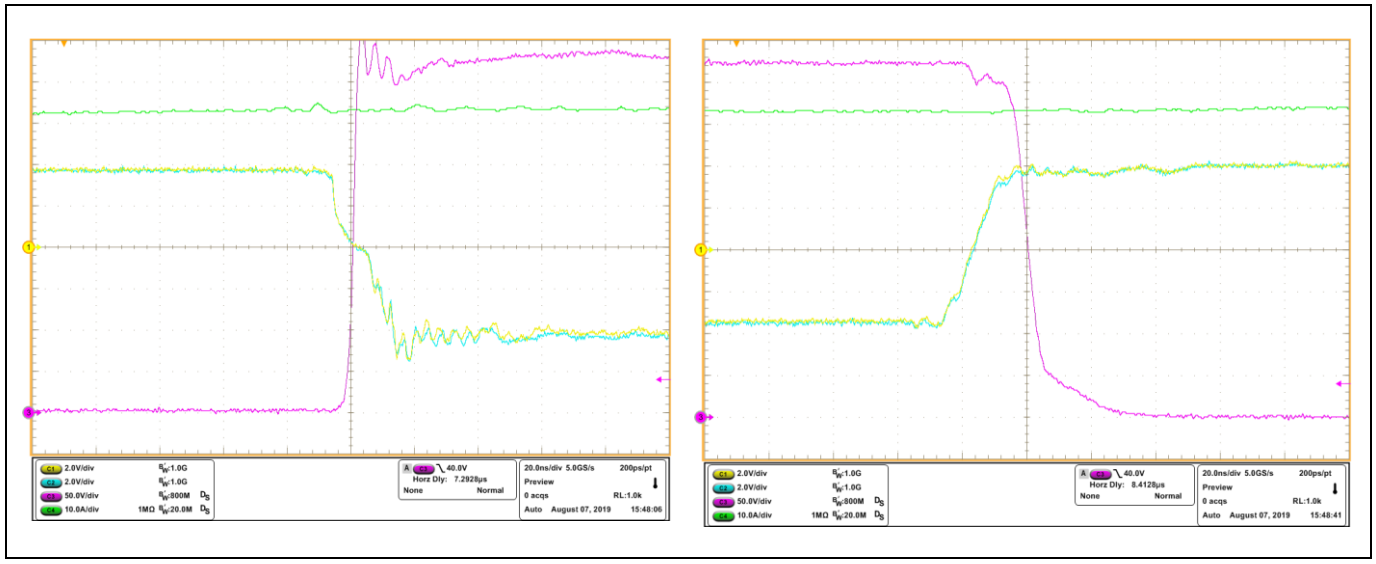


Figure 13 Zoom-in captures of the turn-off and turn-on events at 74 A in the low-side GaN transistors, i.e. at the end of the first pulse and at the beginning of the second pulse

Note that both the gate and drain voltage are well behaved, with minimal ringing or overshoot, despite the extremely fast switching performance. This is the performance that GaN can deliver to help reduce switching loss, while also decreasing conducted and radiated emissions at the same time.

By setting up the board as described in **Figure 3**, as inverted double-pulse testing, it is possible to monitor the drain current sharing between the parallel devices.

Key to the following figures:

Table 5 Oscilloscope channels description

CH 1 (yellow)	Q1 high-side GaN drain current, 20 A/div
CH 2 (blue)	Q2 high-side GaN drain current, 20 A/div
CH 3 (purple)	V_{SW}, switch-node voltage, 50 V/div
Ch 4 (green)	Total switch-node current, 40 A/div

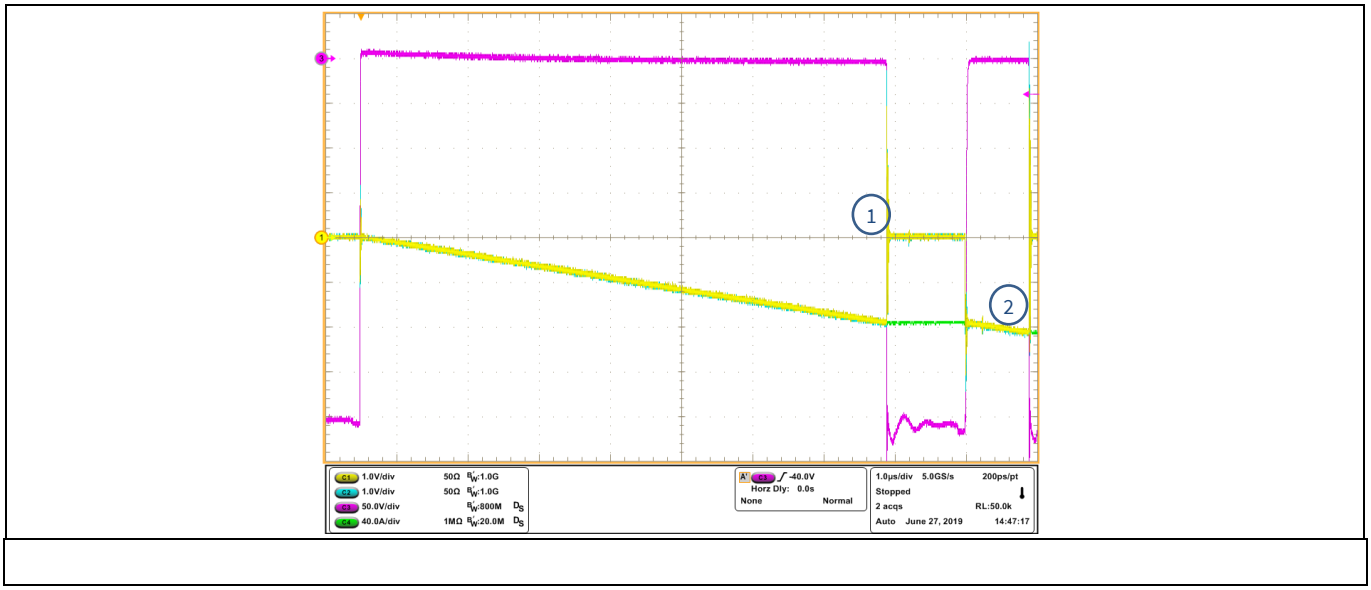


Figure 14 Inverted double-pulse testing at 76 A

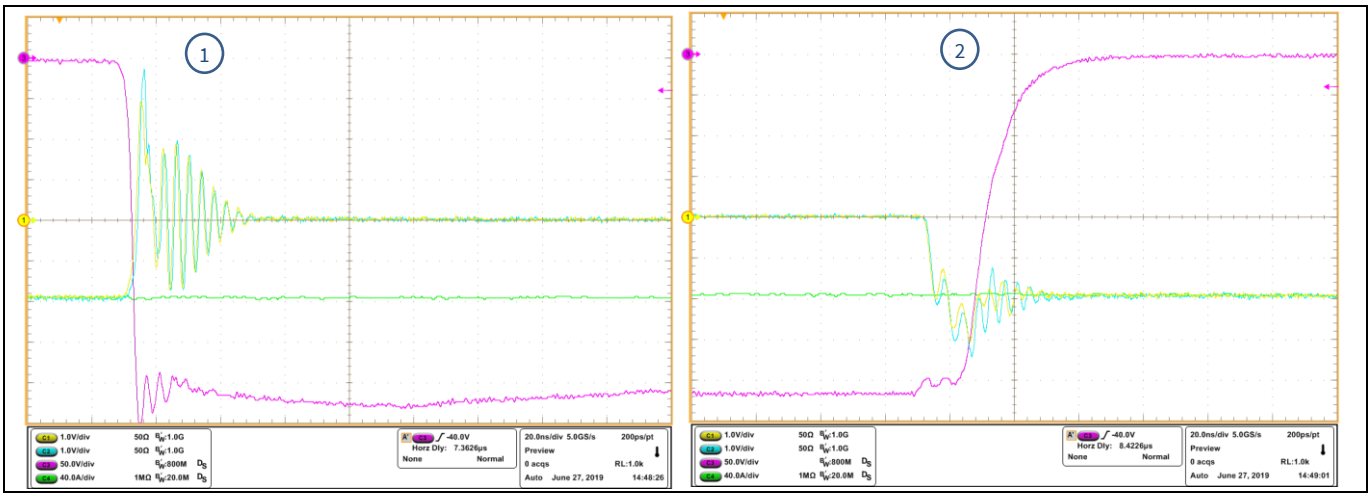


Figure 15 Zoom-in captures of the (1) turn-off and (2) turn-on events at 76 A in the high-side GaN transistors during inverted double-pulse test

5.7.2 Performance under soft-switching conditions

Again, assuming the board is already set up per sections **5.5** and **5.6**, the next step is to add an external inductor and bring the HV power supply to operate at the desired test condition. The board can be set up as depicted in **Figure 3** or **Figure 11** **but without connecting the DC load**. The peak-to-peak inductor must be larger than twice the average inductor current. In this test, the high-side GaN transistor pair will charge the inductor until a certain current is reached. Then this GaN transistor pair turns off, and the current freewheels through the low-side GaN transistor. The soft-switching test is done by applying a 1 MHz PWM signal with 50 percent duty cycle. The test runs just for a couple of seconds (not continuously, in order to keep power dissipation low) until the waveforms become stable.

Key to the following figures:

Table 6 Oscilloscope channels description

CH 1 (yellow)	Q1 high-side GaN drain current, 10 A/div
Ch 2 (blue)	Q2 high-side GaN drain current, 10 A/div
CH 3 (purple)	V_{SW}, switch-node voltage, 50 V/div
CH 4 (green)	Total switch-node current, 20 A/div

Bear in mind that the current on each GaN transistor is measured at the corresponding test points, TP1a and TP2a, respectively, the V_{SW} is measured at TP12 and the inductor current is measured with a current probe.

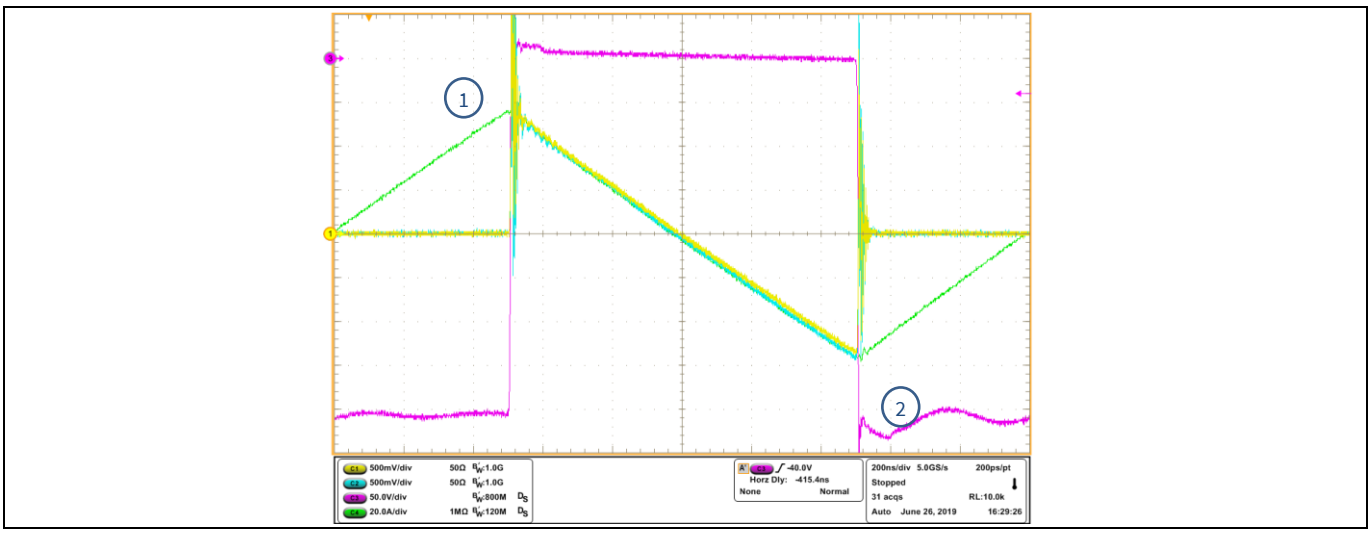


Figure 16 Soft-switching performance at an inductor current of 56 A

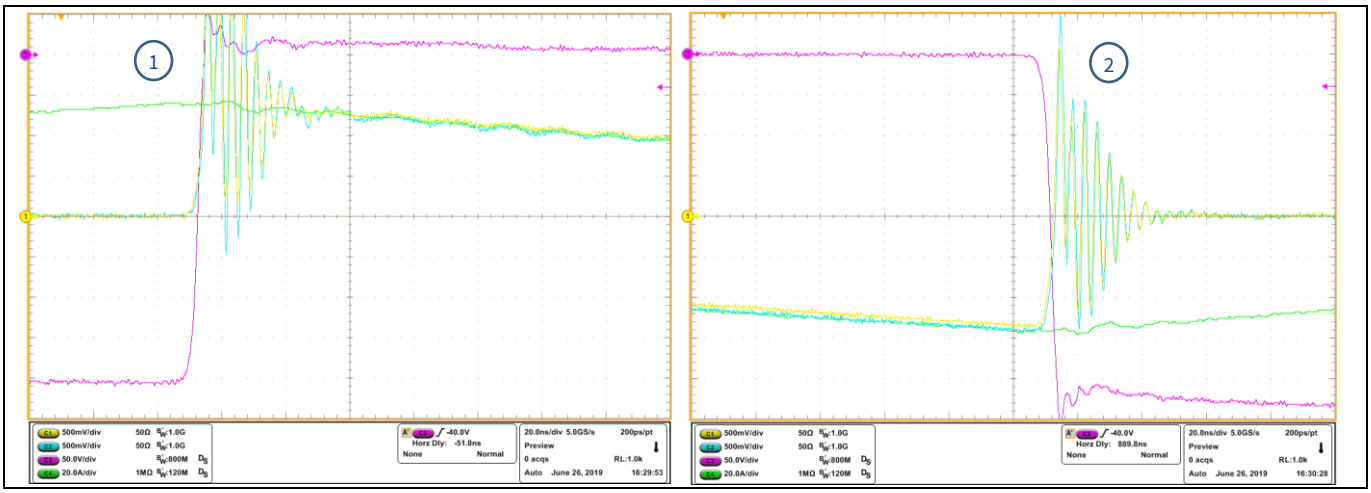


Figure 17 Zoom-in details at turn-on of high-side GaN transistors during soft-switching at 56 A

The benefit of using the CM inductor from gate to Kelvin source on each parallel device can be seen on the ringing waveforms as they are in phase and rapidly mitigated in than 30 ns.

5.7.3 Problems when CM inductor is not used

Key to the following figures:

Table 7 Oscilloscope channels description

CH 1 (yellow)	Q1 high-side GaN drain current, 5 A/div
CH 2 (blue)	Q2 high-side GaN drain current, 5 A/div
CH 3 (purple)	V_{SW}, switch-node voltage, 50 V/div
CH 4 (green)	Total switch-node current, 10 A/div

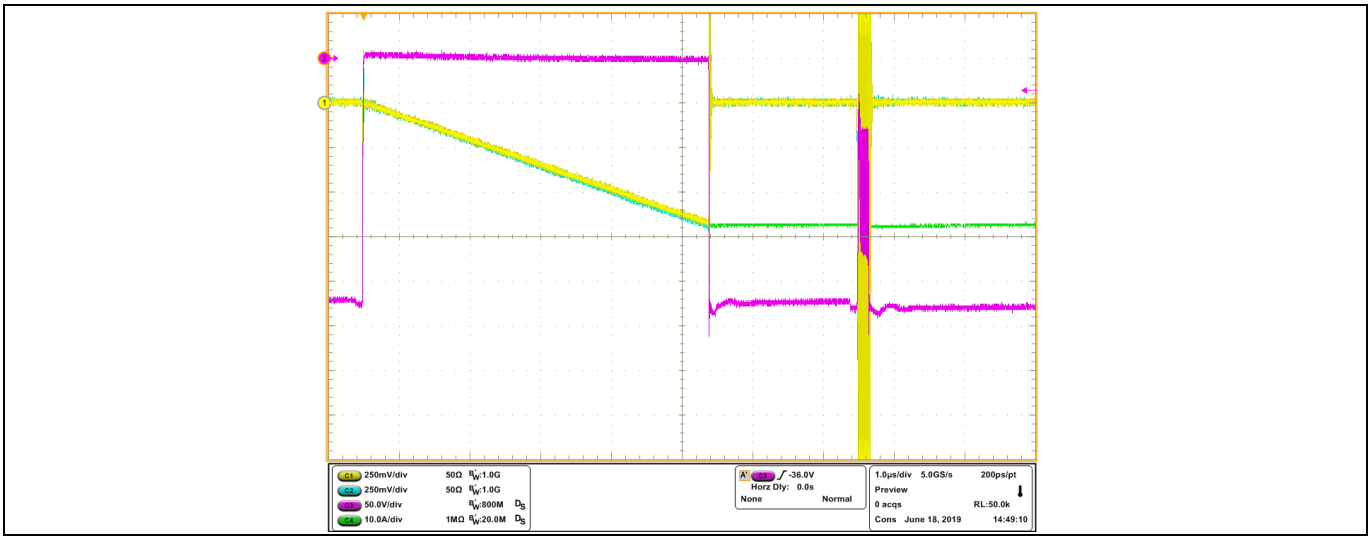


Figure 18 Hard-switching waveforms without CM choke from gate to Kelvin source at 28 A

Figure 18 shows that oscillations can happen without CM inductors which may lead to failures. Oscillations can be in the order of hundreds of MHz and over 100 A peak-to-peak.

5.8 Current sharing between parallel GaN transistors with extreme parameter or corner devices

When two switches are connected in parallel, it is expected, theoretically, that both devices share equally the load operating current. This condition is expected to happen in both static and dynamic conditions. In reality, however, this hardly happens. Unequal sharing happens due to asymmetries at different physical points. The most common ones are investigated in this analysis and listed below:

- Asymmetry due to stray inductances and capacitances in PCB layouts, traces, layer arrangements as well as in used components.
- Different gate threshold voltages or different $R_{DS(on)}$ values.

Different pairs of devices used during the real evaluation of the paralleling operation presented a deviation of less than 2 percent in $R_{DS(ON)}$ and less than 1 percent in threshold voltages. During both hard- and soft-switching conditions, a certain amount of unequal current sharing is visible but still acceptable and non-destructive. However, some concerning and valid questions may arise, like:

1. How big would the current imbalance be when two GaN transistors with extreme threshold voltages are paralleled?

2. How big would the current imbalance be during turn-on and turn-off when two GaN transistors with extreme $R_{DS(on)}$ values are paralleled?
3. How would the parasitics of the PCB layout influence the paralleling operation?

In order to address such concerns, it would be necessary to screen several thousand samples in order to find those devices with extreme parameter values. As this activity is quite tedious, different simulations have been done in SIMetrix in order to investigate the potential issues. The following SIMetrix models of the IGOT60R070D1 have been created for this analysis:

Table 8 Extreme parameter or corner device models used in simulations

Device modeling	$R_{DS(on)}$	Threshold voltage
M1	55 mΩ	0.9 V
M2	55 mΩ	1.6 V
M3	55 mΩ	1.2 V
M4	70 mΩ	1.2 V
M5	70 mΩ	1.6 V

Two different half-bridge configuration circuits have been simulated in order to analyze the impact of using extreme parameter value devices as well as the benfits of implementing the CM inductors in the gate to Kelvin source loop.

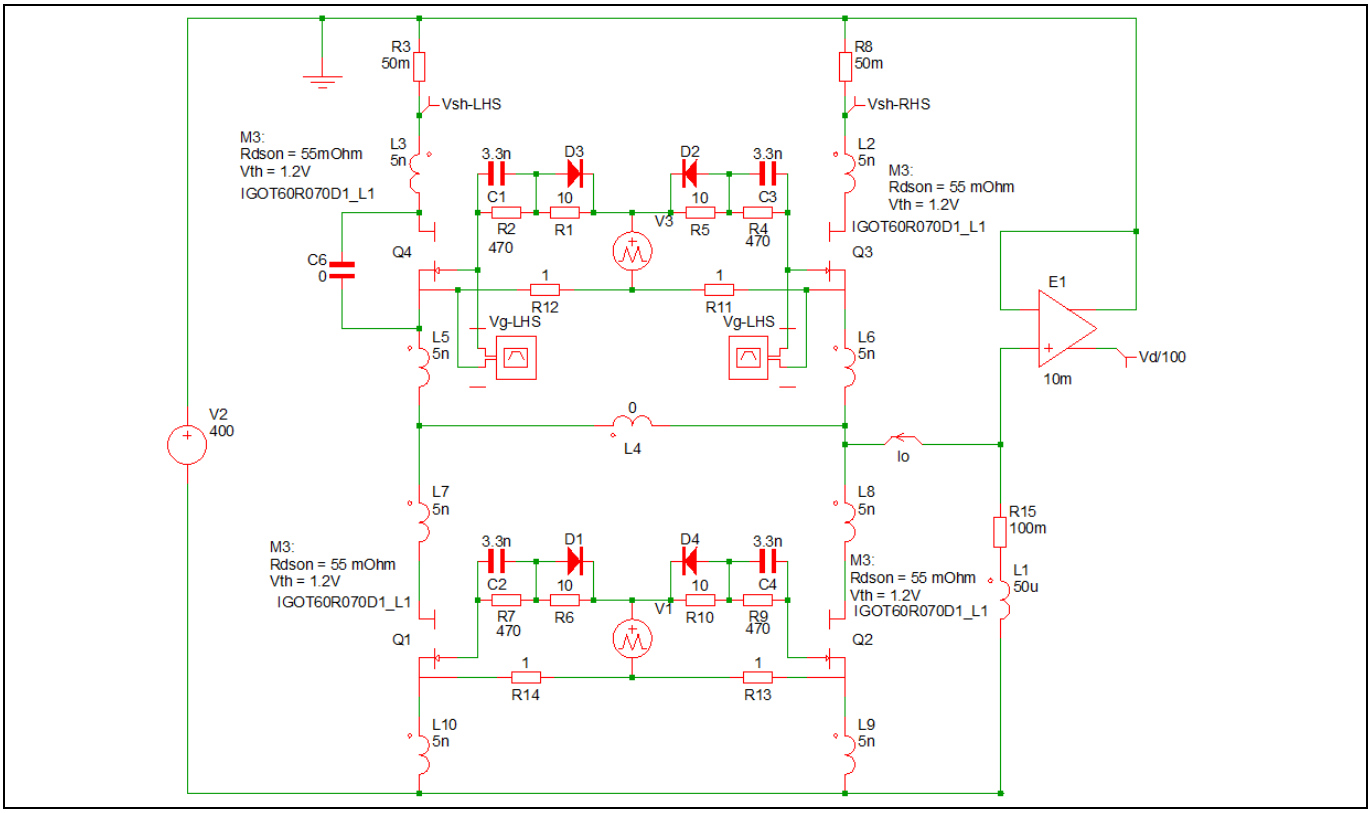


Figure 19 Example of paralleling CoolGaN™ 600 V HEMT in half-bridge without CM inductors in the gate to Kelvin source loop

The circuit in **Figure 19** shows the parallel GaN devices with the parasitic circuit components. The circuit operates as a double-pulse test circuit and reference is the "+" of 400 V. Asymmetry due to parasitic components in the PCB layouts, like trace inductances and layer capacitances, are investigated by varying L4 and C6.

Asymmetry due to device gate thresholds and device $R_{DS\,(on)}$ values are investigated by using extreme device models for the high-side devices. Low-side devices are kept as M3, typical devices.

With this circuit it was possible to start high-frequency oscillations at the turn-on edge at 40 A total current with the following asymmetry conditions:

- Asymmetry due to parasitics with all M3 GaN transistors. For C6 more than 160 pF → sustained high-frequency oscillations.
- Asymmetry due to extreme gate thresholds with C6 = 0 and M3 low-side devices. M1 + M2 or M2 + M1 high-side devices → sustained high-frequency oscillations.
- Asymmetry due to extreme $R_{DS\,(on)}$ values with C6 = 0 and M3 low-side devices. M3 + M4 or M4 + M3 high-side devices → no sustained oscillations, only proportional static current imbalance is observed.

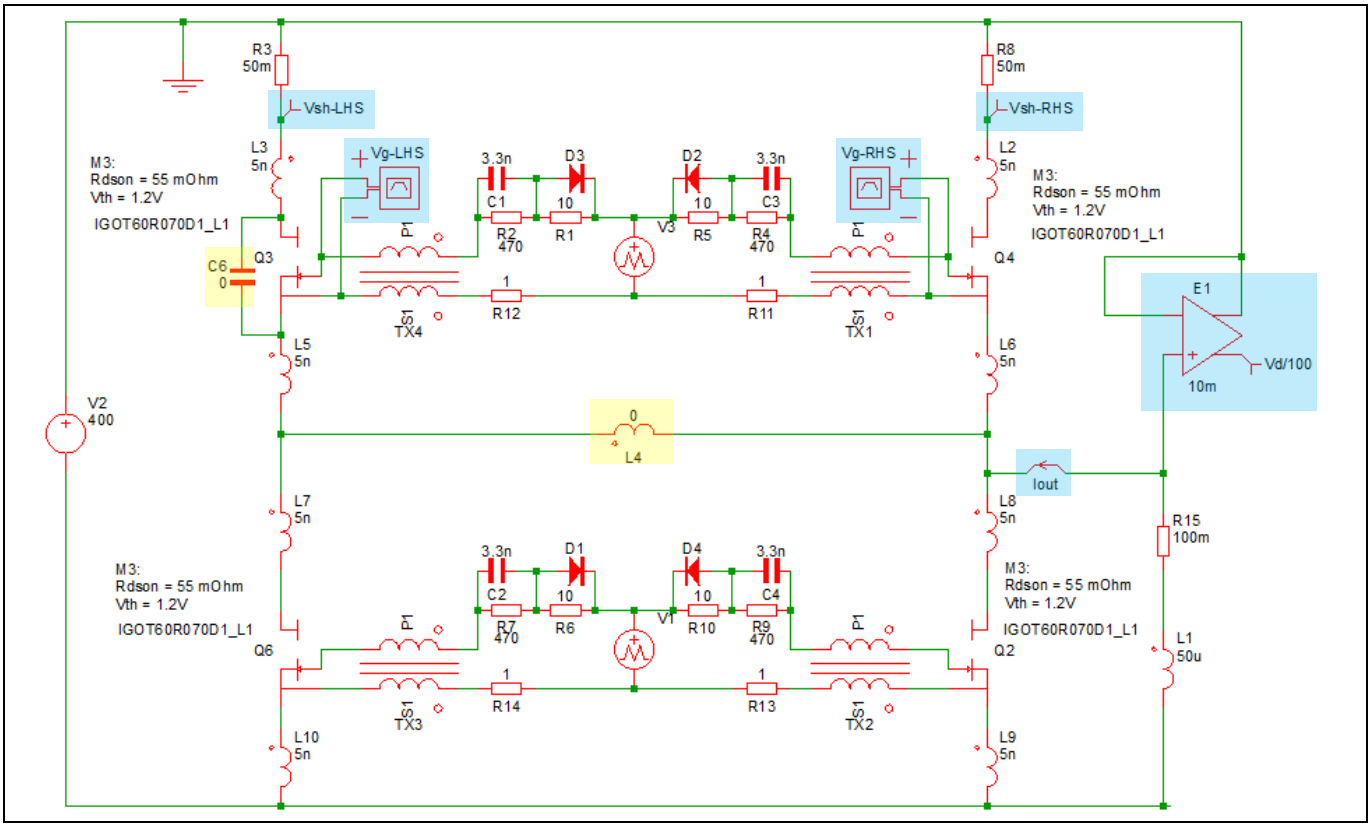


Figure 20 Paralleling CoolGaN™ 600 V HEMT in half-bridge with CM inductors in the gate to Kelvin source loop.

As mentioned in section **4.3**, in order to resolve the oscillations issue, CM inductors were introduced in the gates of each GaN transistor, as shown in **Figure 20**. The "SRF2012-361YA" is selected for its bifilar structure to give maximum CM impedance with minimal leakage. No model is available for this device. Therefore, the SIMetrix model for "Ideal Transformer" with 500 nH primary inductance was used to satisfy the datasheet parameters 360 Ω at 100 MHz.

With the circuit shown in **Figure 20**, it was possible to considerably mitigate sustained high-frequency oscillations with the following asymmetry conditions:

- Asymmetry due to parasitics with all M3 GaN transistors. Tested up to C6 =1000 pF → no high-frequency oscillations.
- Asymmetry due to extreme gate thresholds with C6 = 0 and M3 low-side devices. M1 + M2 or M2 + M1 high-side devices → no high-frequency oscillations.
- Asymmetry due to extreme $R_{DS\ (on)}$ values with C6 = 0 and M3 low-side devices. M3 + M4 or M4 + M3 high-side devices → no high-frequency oscillations.
- Double asymmetry with C6 = 1000 pF, M3 low-side devices. M1 + M2 or M2 + M1 high-side devices → no high-frequency oscillations.
- Double asymmetry due to extreme $R_{DS\ (on)}$ values with C6 = 1000 pF and M3 low-side devices: M3 + M4 or M4 + M3 high-side device → TBA.
- Triple asymmetry with C6 = 1000 pF and M3 low-side devices. M1 + M5 or M5 + M1 high-side devices → no high-frequency oscillations.

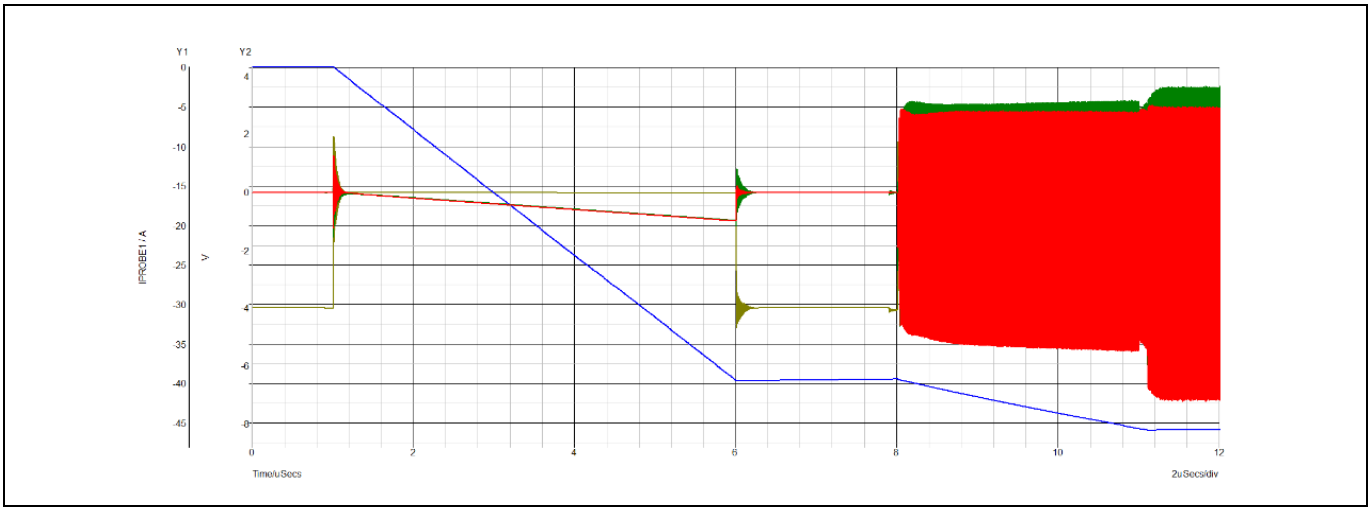


Figure 21 Typical output from the circuit without the CM inductors showing the start of sustained oscillations at turn-on at 40 A total current

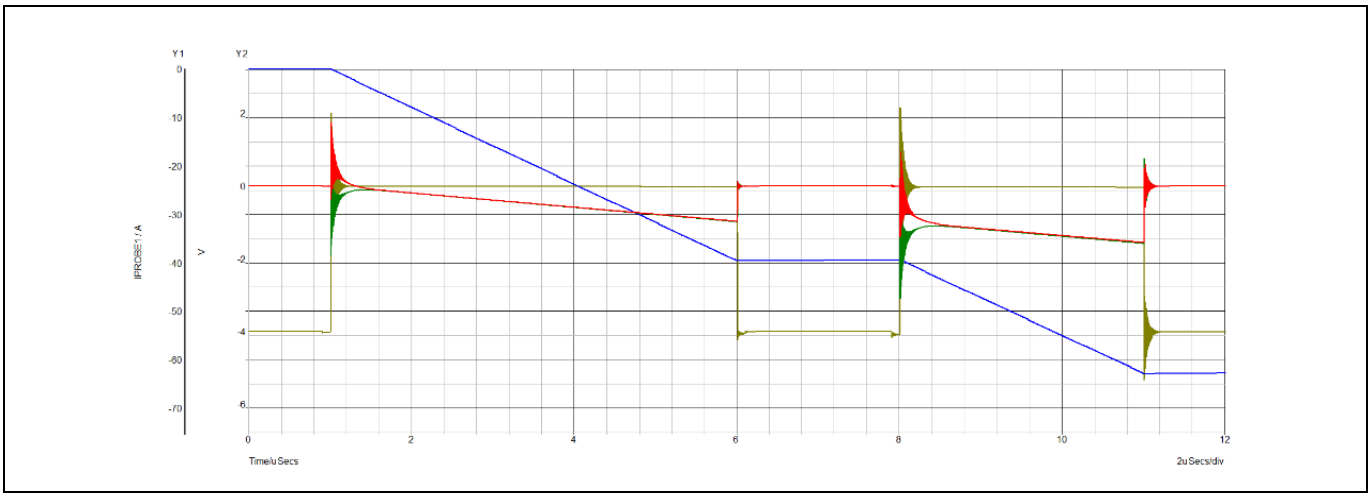


Figure 22 Typical output from the circuit with the CM inductors showing only damped oscillations, which is normal

Based on the waveforms shown in **Figure 21** and **Figure 22**, the importance of using of the CM inductor in the gate to Kelvin source loop can be realized. As a result, the rest of the analysis explained below is based on the circuit from **Figure 20**.

Please notice in **Figure 20** that the components highlighted in yellow represent the parasitics of the PCB and the elements highlighted in blue are the measuring probes for the different signals under analysis. The waveforms shown in the following figures as based on these probes.

Key to the following figures:

Table 9	**Waveforms description**
Vg-LHS	Gate voltage of Q3 (left high-side transistor according to **Figure 20**)
Vg-RHS	Gate voltage of Q4 (right high-side transistor according to **Figure 20**)
Vsh-LHS	Voltage across the shunt resistor R3 (drain current of Q3 according to **Figure 20**)
Vsh-RHS	Voltage across the shunt resistor R8 (drain current of Q4 according to **Figure 20**)
Vd/100	Drain-to-source voltage of the high-side parallel pair (Q3 and Q4 according to **Figure 20**)
I_{out}	Load current

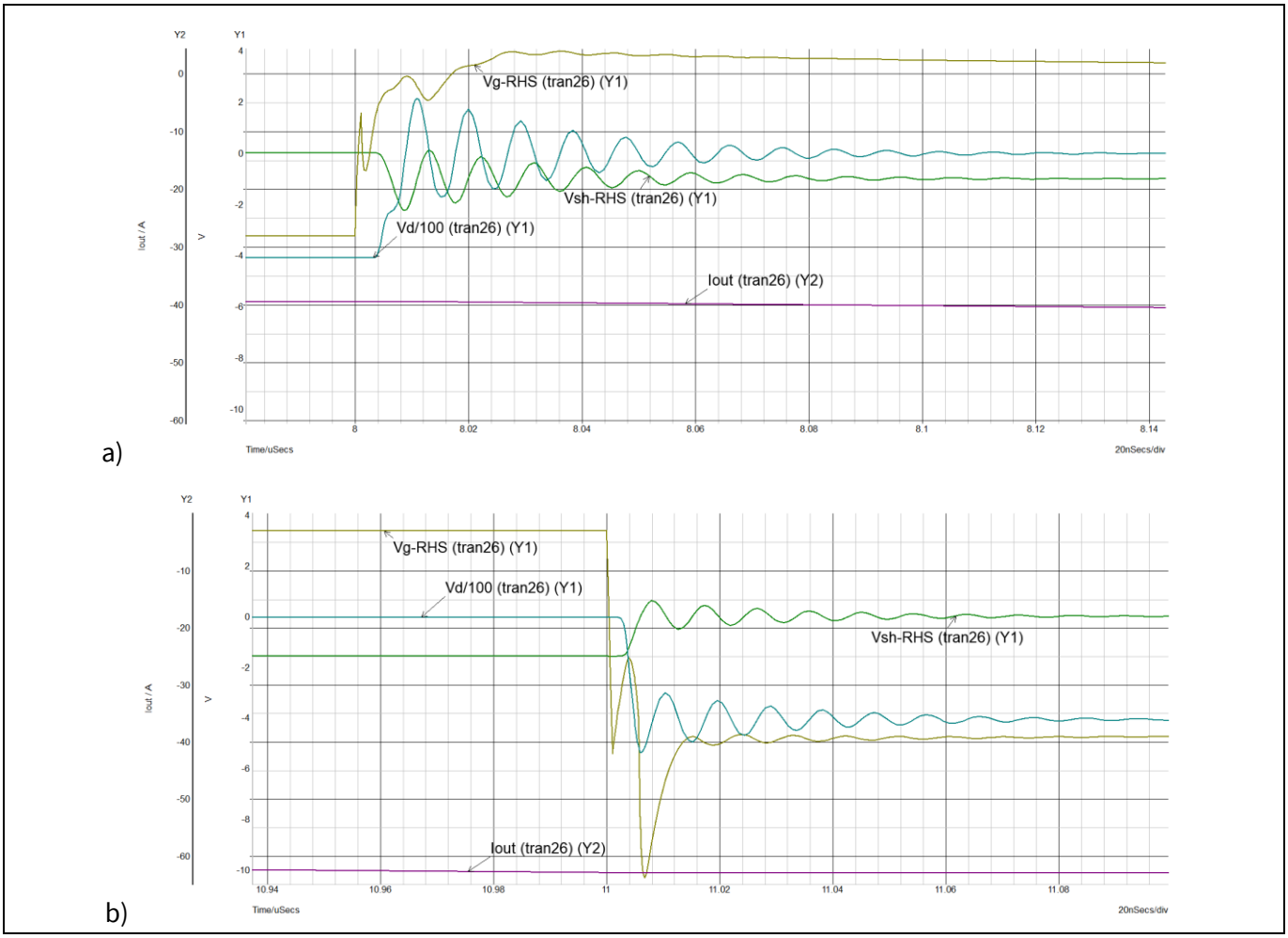


Figure 23 **Waveforms for the case when all GaN transistors are symmetrical, i.e. M3 models: a) turn-on at 20 + 20 A, b) turn-off at 30 + 30 A**

Waveforms shown in **Figure 23** are obtained from simulations where all GaN transistors are based on M3 models, C6 = 0 and L4 = 0 representing full symmetry. As expected, the gate and shunt voltages match perfectly. The ringing on V_{DS} and shunt voltages is due to large drain-loop inductances, which will be minimized in real life.

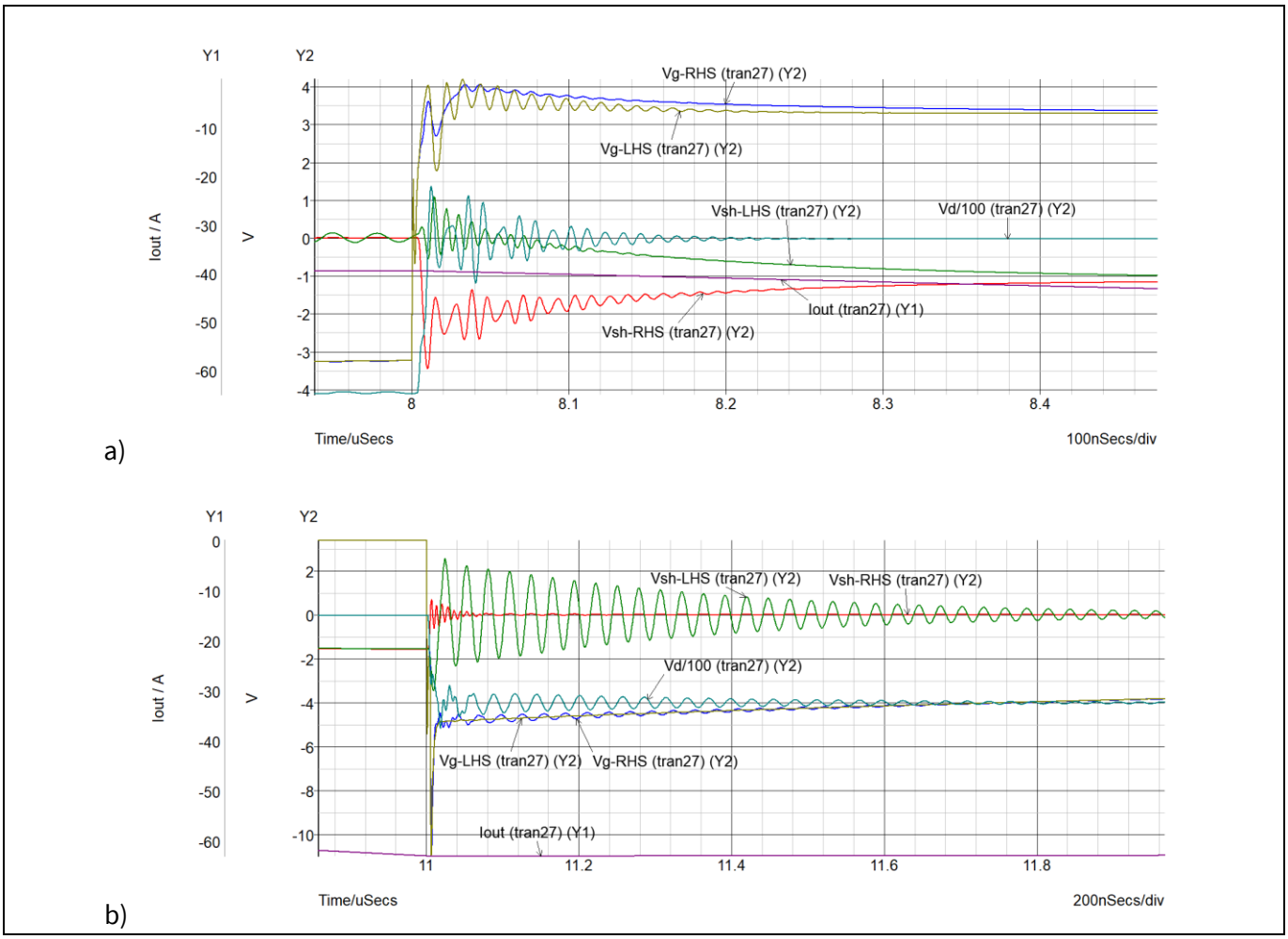


Figure 24 Waveforms for the case when the asymmetry is due to parasitic component on the PCB: a) turn-on at 20 + 20 A, b) turn-off at 30 + 30 A

Waveforms shown in **Figure 24** are obtained from the simulation where all GaN transistors are M3 models, C6 = 1000 pF and L4 = 10 nH, representing an extreme case for parasitic values. No sustained oscillations were observed. However, gate and shunt voltage waveforms deviate considerably from each other. Especially at turn-on at 20 + 20 A, the right high-side (Vsh-RHS) shunt starts with full output current while the other shunt, left high-side (Vsh-LHS) starts with no current. They eventually approach each other and share the load equally after about 500 ns until the end of the on-cycle.

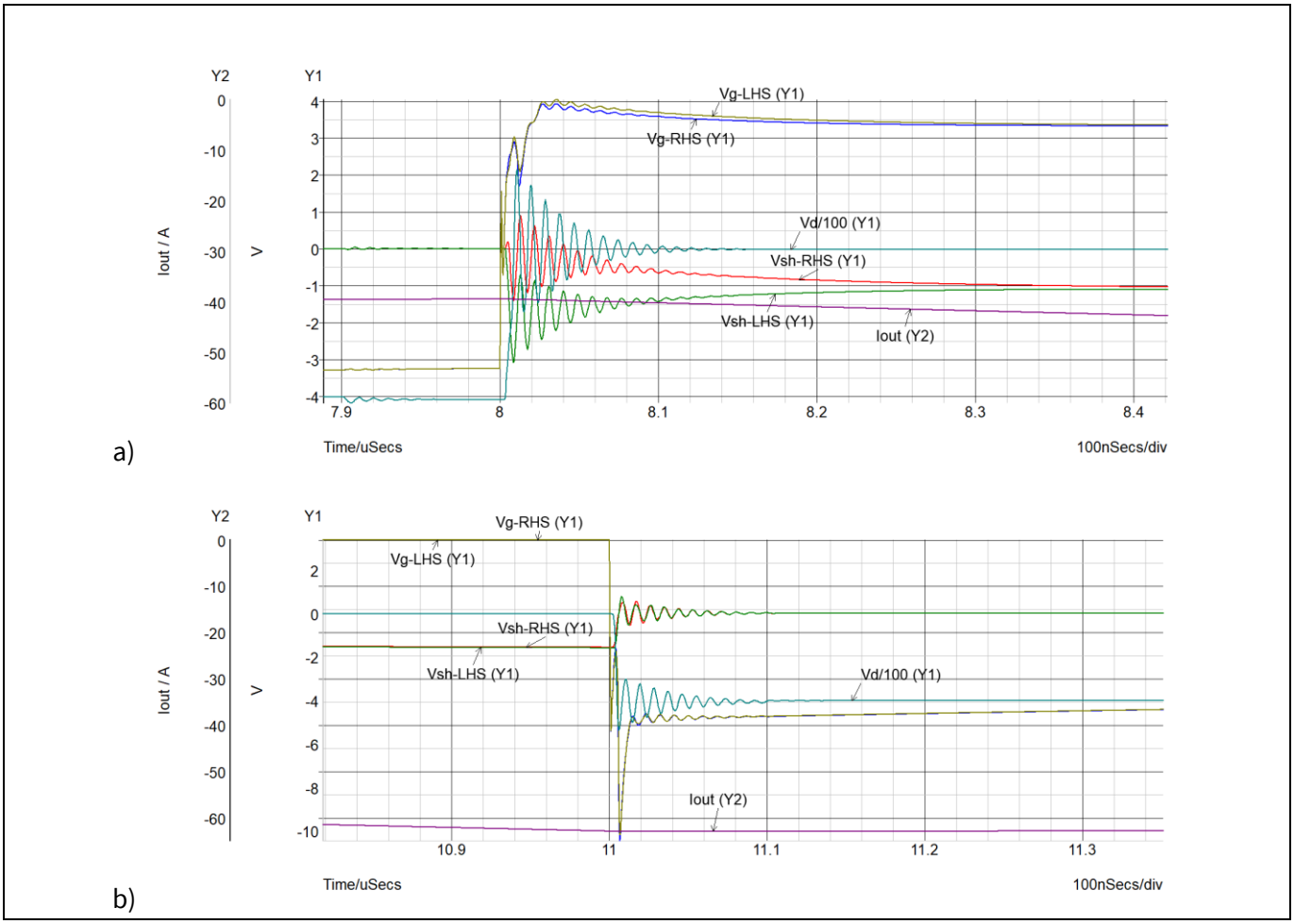


Figure 25 Waveforms for the case when high-side GaN transistors are M1 and M2, i.e. asymmetry in gate threshold voltages: a) turn-on at 20 + 20 A, b) turn-off at 30 + 30 A

Waveforms shown in **Figure 25** are from simulations where M1 + M2 models are used as high-side devices, with C6 = 0 pF and L4 = 0 nH representing extreme cases for gate threshold values. Low-side devices have been kept as M3 + M3 for the rest of the simulations. No sustained oscillations are observed. However, similar to the case with extreme parasitics, gate and shunt voltage waveforms deviate from each other.

As expected, at turn-on at 20 + 20 A, the left high-side (Vsh-LHS) shunt takes most of the current because of the lower gate threshold of the connected device at left high-side. The shunt voltages eventually approach each other and share the load equally after about 500 ns until the end of the on-cycle.

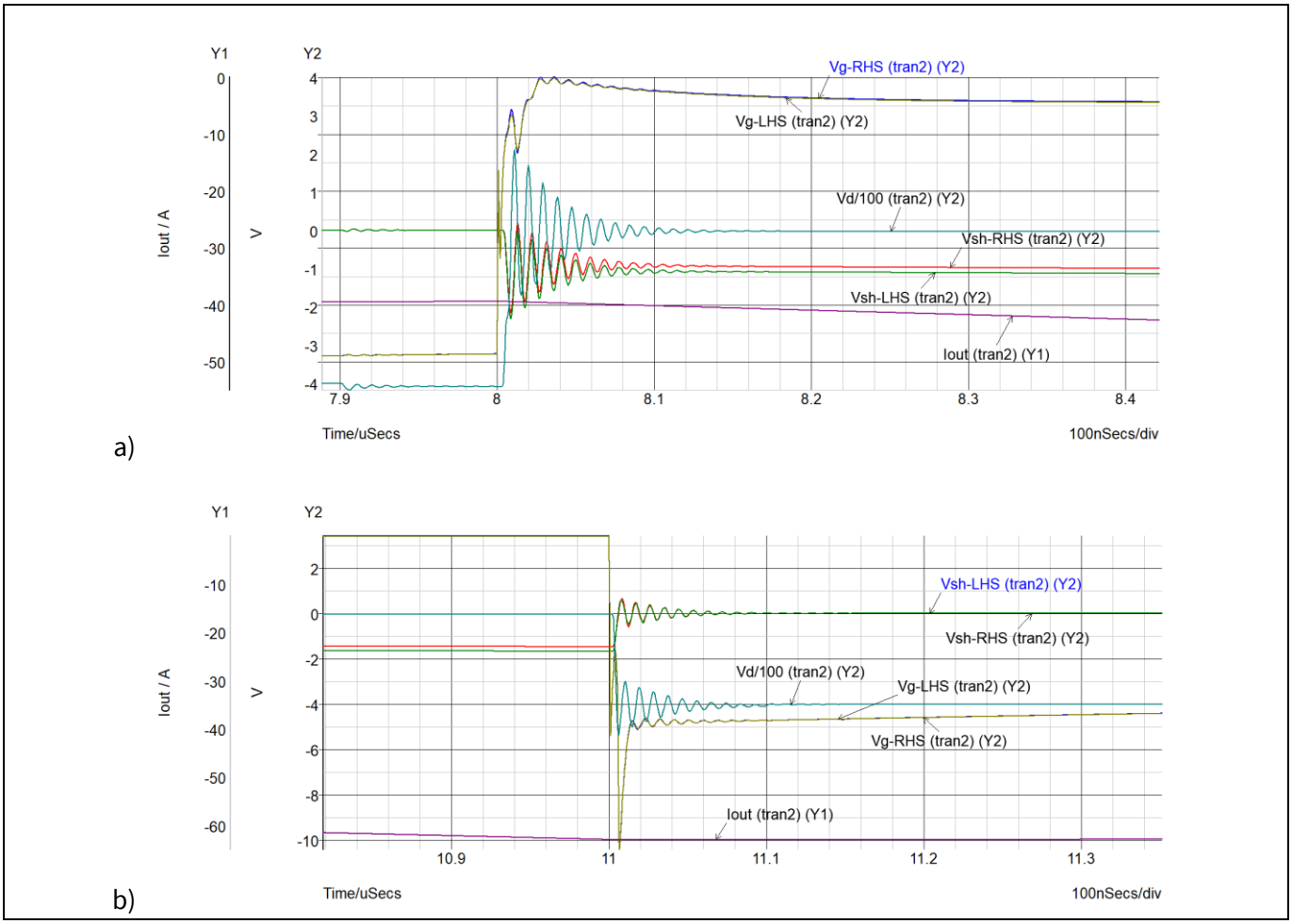


Figure 26 Waveforms for the case when high-side GaN transistors are M3 and M4, i.e. asymmetry in $R_{DS\,(on)}$ values: a) turn-on at 20 + 20 A, b) turn-off at 30 + 30 A

Waveforms from **Figure 26** are from simulations run with M3 + M4 models used as high-side devices, C6 = 0 pF and L4 = 0 nH representing extreme cases for $R_{DS\,(on)}$ values. As expected, only some imbalance shows in static current sharing. The left high-side device takes more current due to its lower $R_{DS\,(on)}$ and it goes on for the duration of on-time. No sustained oscillations are observed.

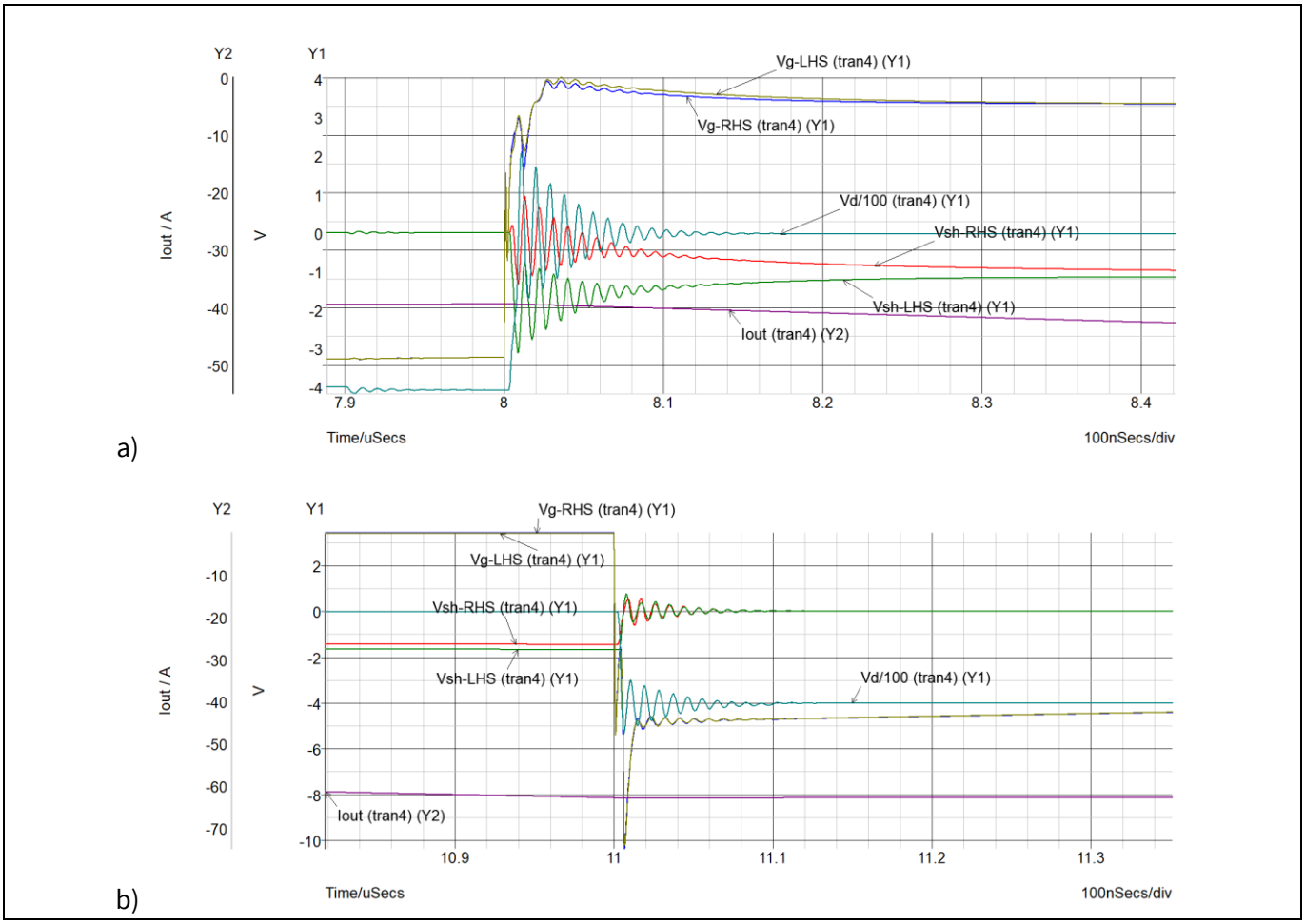


Figure 27 Waveforms for the case when high-side GaN transistors are M1 and M5, i.e. asymmetries in gate threshold voltage and $R_{DS(on)}$ value: a) turn-on at 20 + 20 A, b) turn-off at 30 + 30 A

Waveforms shown in **Figure 27** are obtained from simulations run with M1 + M5 models used as high-side devices, C6 = 0 pF and L4 = 0 nH representing extreme case for $R_{DS\,(on)}$ and gate threshold values together. Some dynamic imbalance in shunt voltages is observed at the start due to gate threshold voltage difference and some static imbalance at the end due to $R_{DS\,(on)}$ difference. No sustained oscillations are observed.

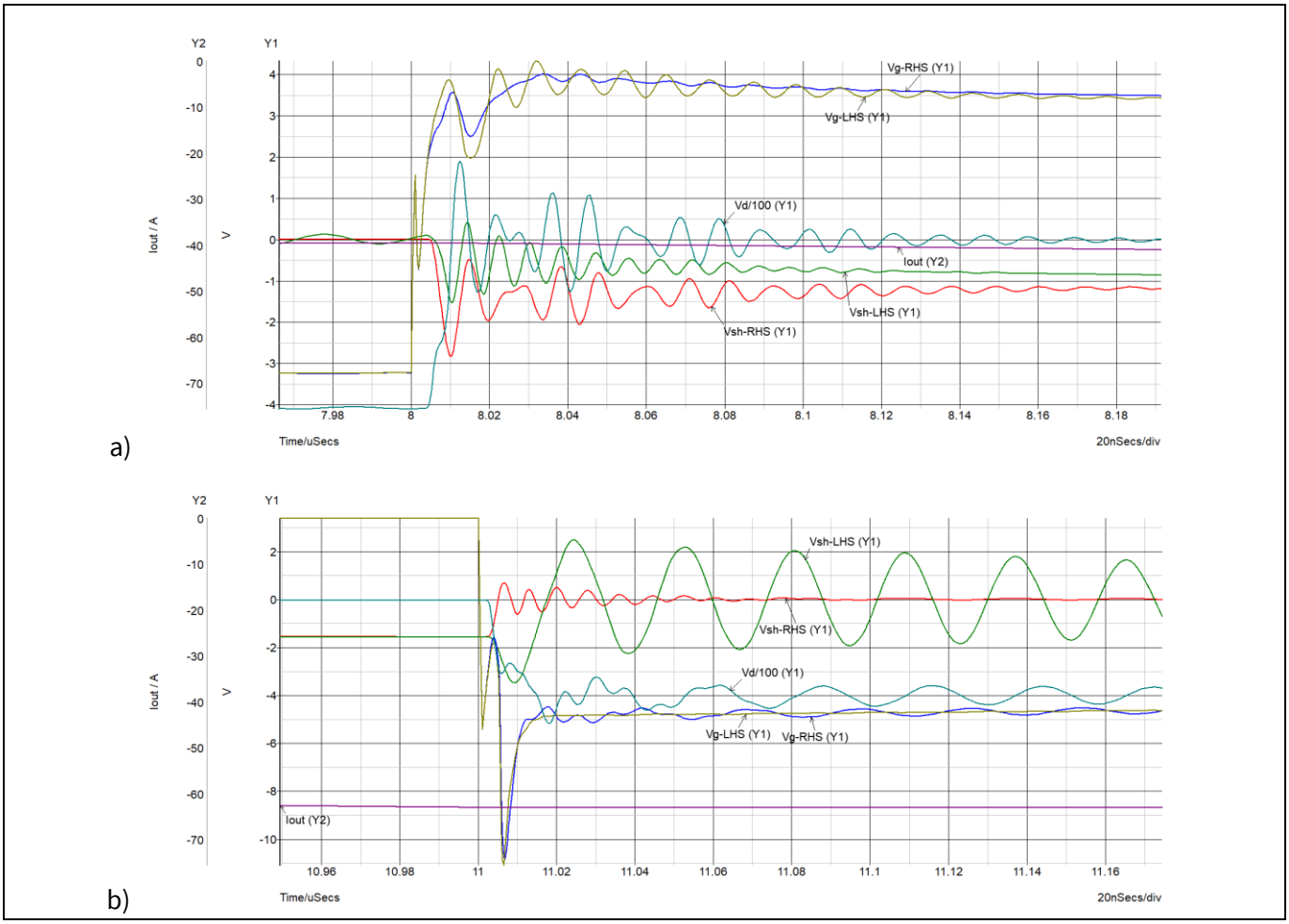


Figure 28 Waveforms for the case when high-side GaN transistors are M1 and M2 as well as circuit parasitics: a) turn-on at 20 + 20 A, b) turn-off at 30 + 30 A

Waveforms shown in **Figure 28** are obtained from simulations run with M1 + M2 models used as high-side devices, C6 = 1000 pF and L4 = 10 nH representing extreme case for gate threshold and parasitic C and L values together. The left high-side current takes about a microsecond to damp but this is not a sustained situation.

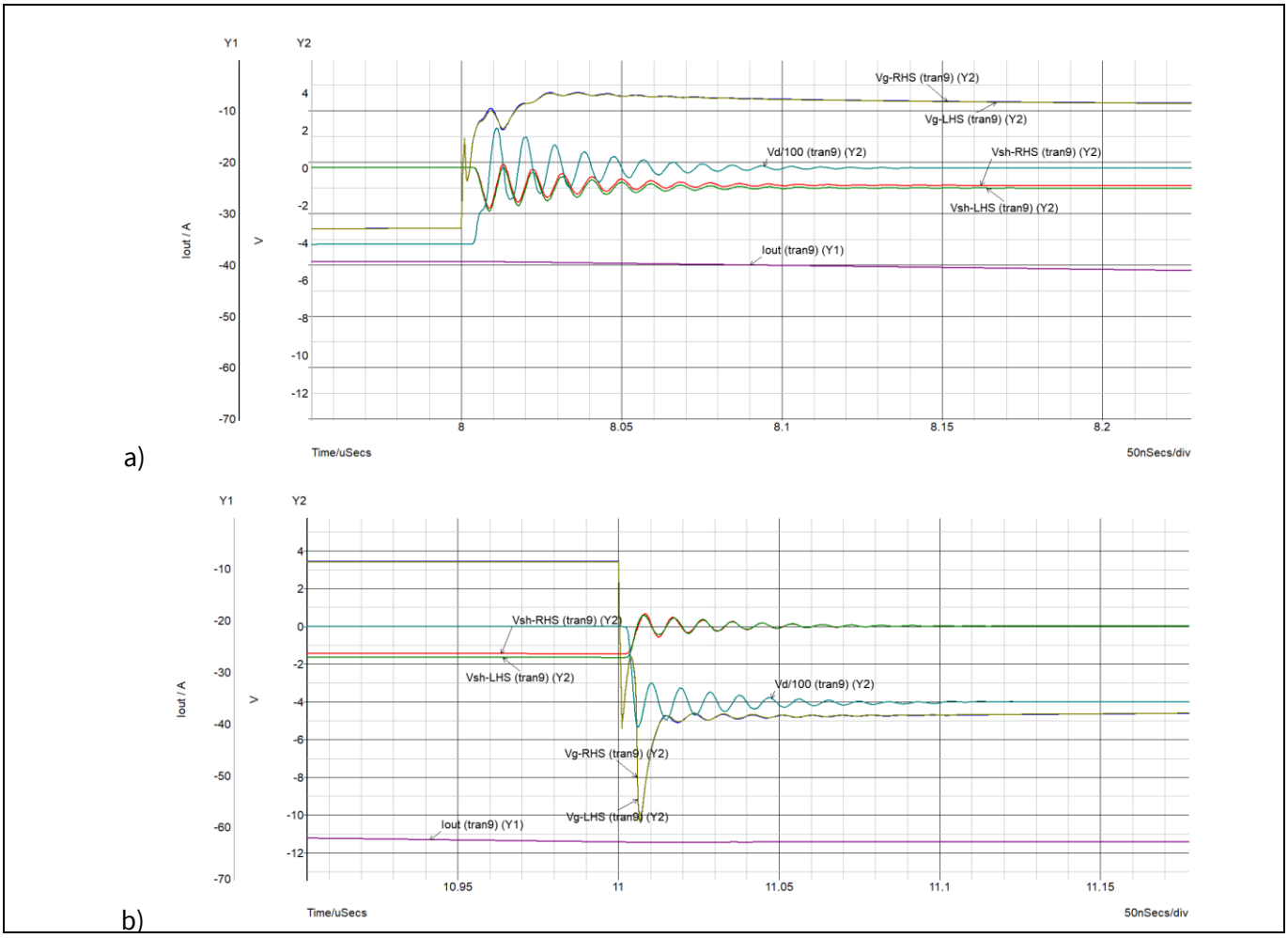


Figure 29 Waveforms for the case when high-side GaN transistors are M3 and M4 as well as circuit parasitics: a) turn-on at 20 + 20 A, b) turn-off at 30 + 30 A

Waveforms from **Figure 29** are obtained from the simulations where M3 + M4 models are used as high-side devices, C6 = 1000 pF and L4 = 10 nH, representing extreme case for $R_{DS\,(on)}$ values and parasitic C and L values together. No new issues are observed.

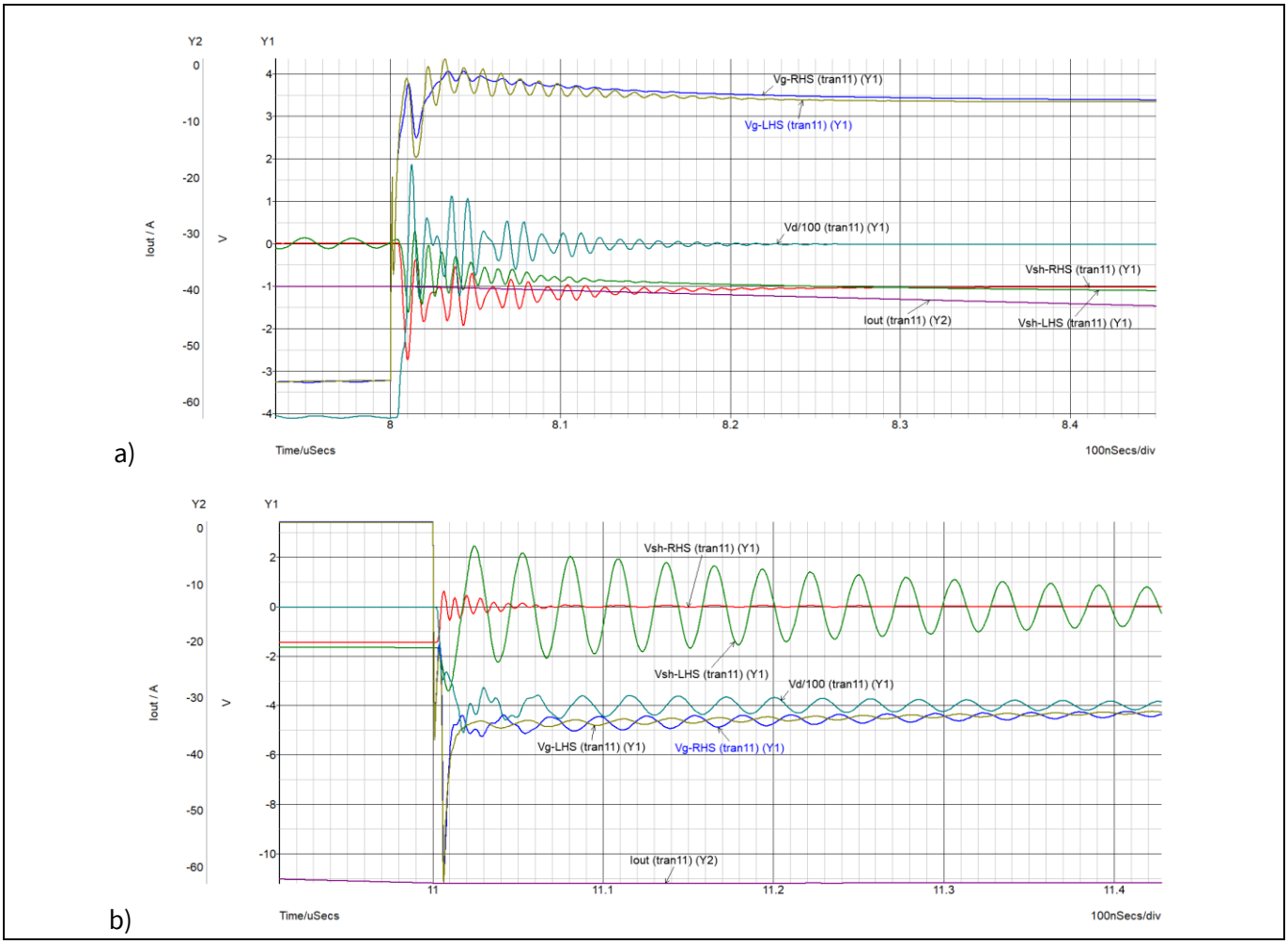


Figure 30 Waveforms for the case when high-side GaN transistors are M1 and M5 as well as circuit parasitics: a) turn-on at 20 + 20 A, b) turn-off at 30 + 30 A

Waveforms from **Figure 30** are obtained from the simulation where M1 + M5 models are used as high-side devices, C6 = 1000 pF and L4 = 10 nH, representing extreme cases for $R_{DS\,(on)}$ values, gate thresholds and parasitic C and L values together. No new issues are observed.

Summarizing:

- Effects of extreme parameter or corner cases in parallel GaN applications can be analyzed by way of simulation considering extreme gate threshold voltages, $R_{DS\,(on)}$ values and PCB parasitics.
- There is always a risk of destructive high-frequency oscillations due to slight imbalance in gate thresholds or circuit parasitics when GaN transistors are operated in parallel. Asymmetry due to $R_{DS\,(on)}$ is only a reason for static imbalance in current sharing.
- The introduction of CM inductors in the gate to Kelvin source circuit loops eliminates the risk of destructive sustained oscillations. However, for acceptable dynamic current sharing, perfectly symmetrical circuit layout and matched gate thresholds are essential. For static current sharing, matched $R_{DS\,(on)}$ values help.
- All good layout practices are also important for parallel operated GaN transistors. Power loops and gate-drive loops must be as small as possible with parallel GaN layouts too. Additionally, they must be as symmetrical as possible. The switch-node parasitic capacitance must be kept as low as possible.

6 Schematics

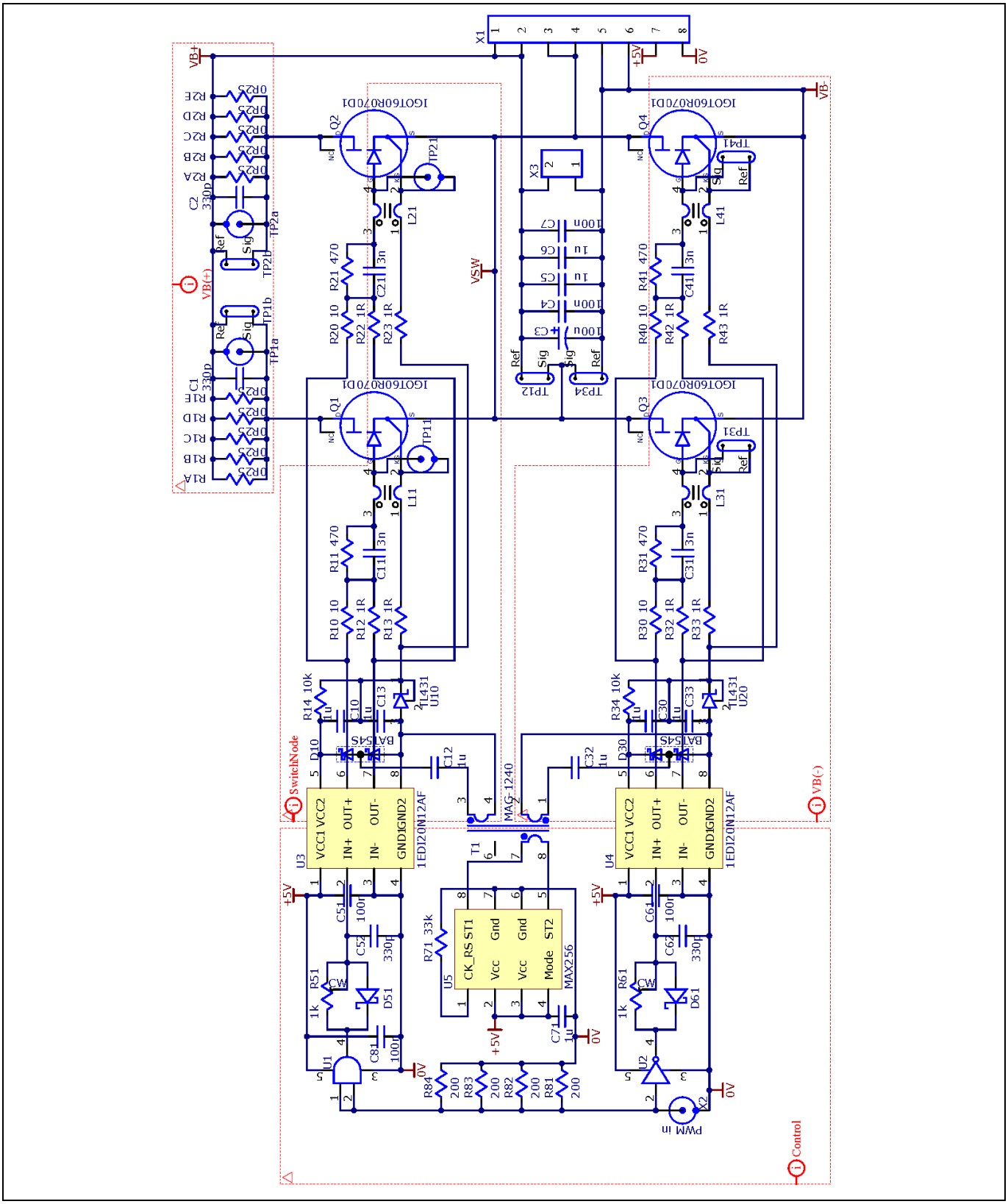


Figure 31 Schematics of the paralleling CoolGaN™ in the half-bridge configuration evaluation board

7 PCB layout

The evaluation board consists of four layers. The layer stack-up is shown below.

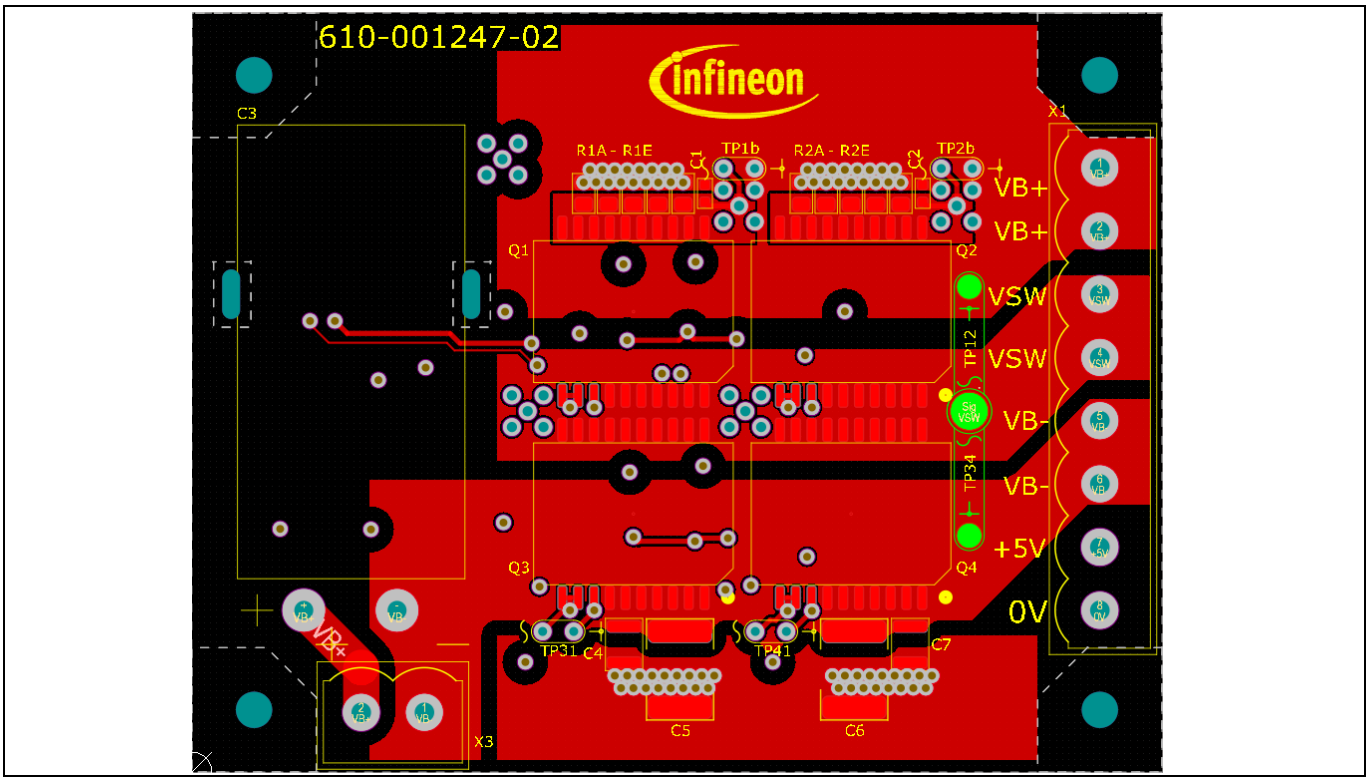


Figure 32 Top layer with component silkscreen

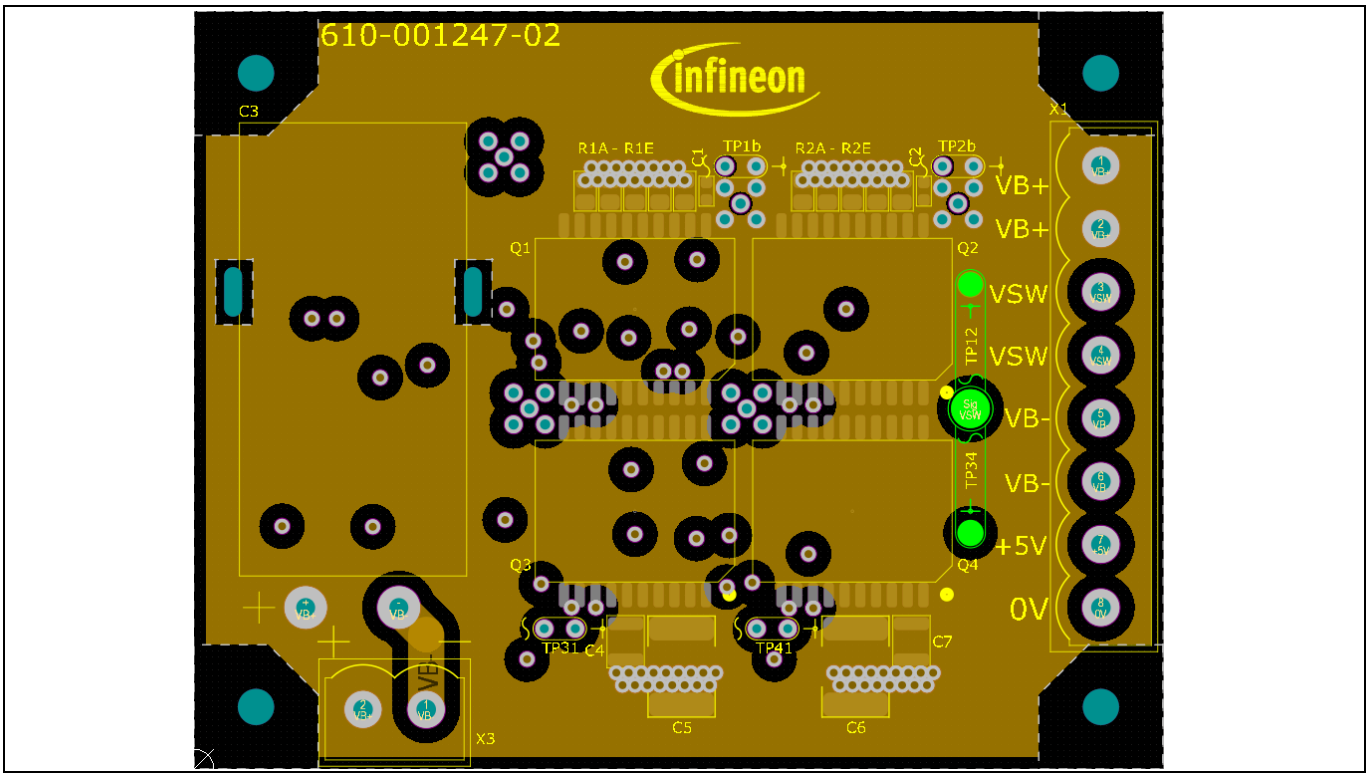


Figure 33 First inner layer with top and bottom component silkscreen

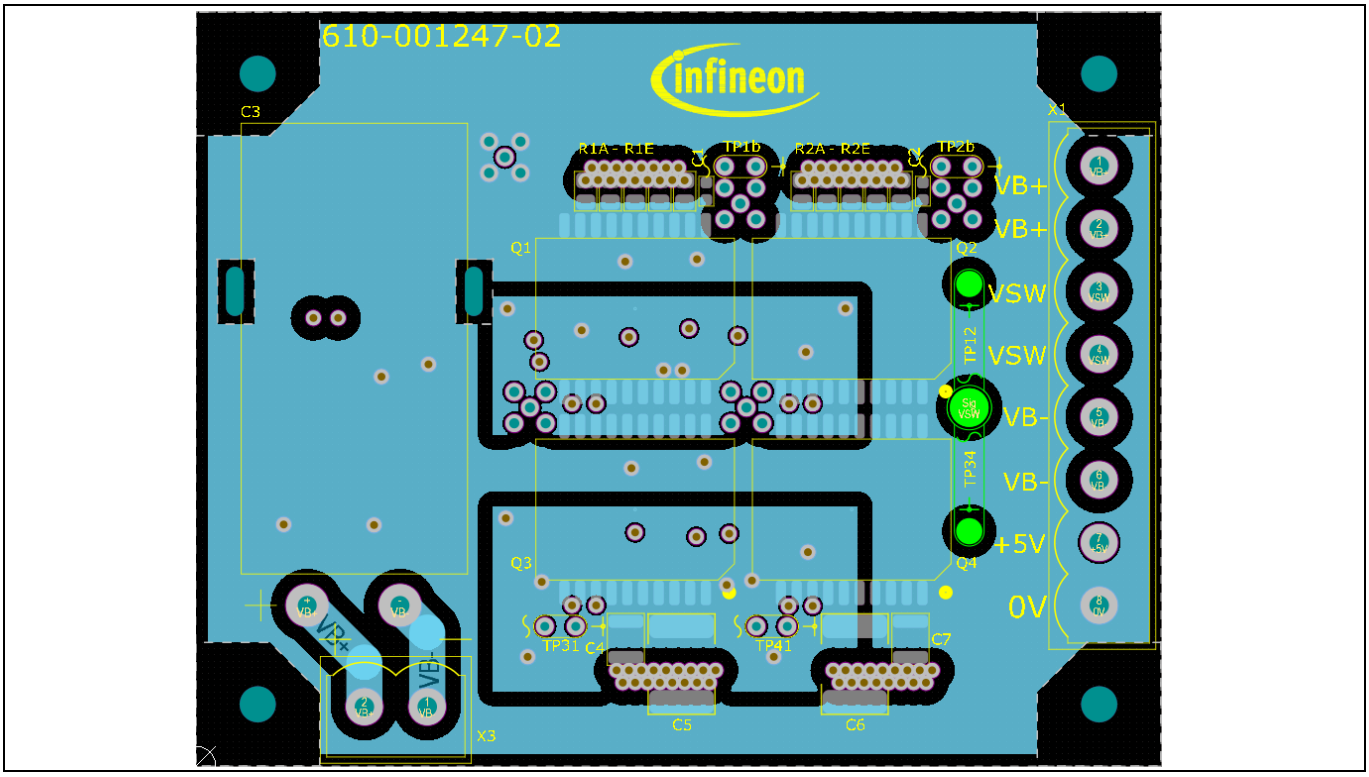


Figure 34 **Second inner layer with top and bottom component silkscreen**

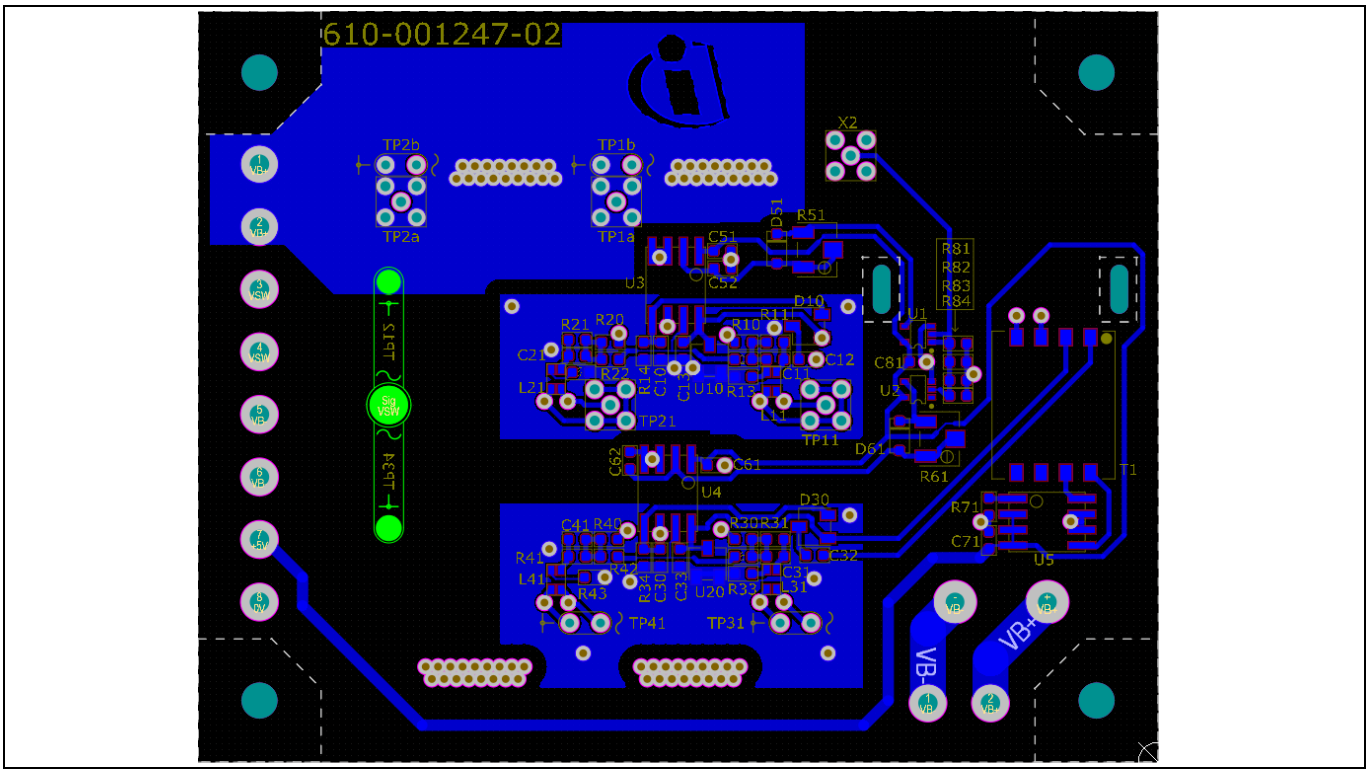


Figure 35 **Bottom layer with bottom component silkscreen**

8 Bill of Materials (BOM)

The following table lists all the components on the PCB.

Table 10 Bill of Materials

Quantity	Designator	Value	Description	Footprint
4	C1, C2, C52, C62	330 pF	Ceramic capacitor 330 pF 50 V C0G/NP0 0603	0603C
1	C3	100 µF	Aluminum capacitor 100 µF 20 percent 450 V 18D 35L 7.5P	C-POL 7.5P18D38H - horizontal
2	C4, C7	100 nF	Ceramic capacitor 0.1 µF 630 V X7R 1210	1210C
2	C5, C6	1 µF	Capacitor 1 µF 450 V X7T 2220	2220
7	C10, C12, C13, C30, C32, C33, C71	1 µF	Ceramic capacitor 1 µF 25 V X7R 0603	0603C
4	C11, C21, C31, C41	3 nF	Ceramic capacitor 3000 pF 50 V C0G/NP0 0603	0603C
3	C51, C61, C81	100 nF	Ceramic capacitor 0.1 µF 25 V X7R 0603	0603C
2	D10, D30	BAT54S	Dual Schottky diode – voltage doubler	SOT23
2	D51, D61	D-Sch	Schottky diode 30 V 200 MA SOD323	SOD323
4	L11, L21, L31, L41	360 R at 100 MHz	CM chip inductor – Bourns SRF2012-361YA	Inductor SRF2012-361YA
1	PCB1	610-001247-02		Infineon logo
1	PCB2	610-001247-01		Infineon logo Polygon cutout
4	Q1, Q2, Q3, Q4	IGOT60R070D1	70 mΩ 600 V DSO-TSC GaN HEMT	DSO20 – TSC-GaN
20	R1A, R1B, R1C, R1D, R1E, R2A, R2B, R2C, R2D, R2E	0R50 ‖ 0R50 = 0R25	Resistor 500 mΩ 1 percent 1/3 W 0805 (two per position used for 0R25)	0805R
4	R10, R20, R30, R40	10 R	Resistor SMD 10 Ω 1 percent 1/10 W 0603	0603R
4	R11, R21, R31, R41	470 R	Resistor SMD 470 Ω 1 percent 1/10 W 0603	0603R
8	R12, R13, R22, R23, R32, R33, R42, R43	1 R	Resistor SMD 1 Ω 1 percent 1/10 W 0603	0603R
2	R14, R34	10 k	Resistor SMD 10 kΩ 1 percent 1/10 W 0603	0603R
2	R51, R61	1 k	Trimmer 1 kΩ 0.125 W SMD	POTEN3223W
1	R71	33 k	Resistor SMD 33 kΩ 1 percent 1/10 W 0603	0603R
4	R81, R82, R83, R84	200 R	Resistor SMD 200 Ω 1 percent 1/8 W 0805	0603R
1	T1	MAG-1240	GaN drive transformer 5 V to 12 V	Core: ER9.5/5 Bobbin: 8-pin SM
4	TP1a, TP2a, TP11, TP21	TP	Connector MMCX jack STR 50 Ω through-hole	MMCX_VERTICAL – through-hole
4	TP1b, TP2b, TP31, TP41	TP pair		TP pair small
2	TP12, TP34	TP pair		TP pair large

Bill of Materials (BOM)

Quantity	Designator	Value	Description	Footprint
1	U1	74AHCT1G08	IC gate and 1CH 2-INP SOT-353	SOT353-5
1	U2	74AHCT1G04	IC single inverter gate SOT353	SOT353-5
2	U3, U4	1EDI20N12AF	Single isolated driver 4 A 1200 V	SO8
1	U5	MAX256	IC DVR half-bridge 3 W 8-SOIC	SO8
2	U10, U20	TL431	TL431 adjustable precision shunt regulator	SOT23
1	X1	CN8	Terminal block HDR eight-position vertical 5.08 mm -MOLEX 0395311008 Terminal block plug eight-position 5.08 mm MOLEX 0395333008	CN8
1	X2	PWM in	Connector MMCX jack STR 50 Ω through-hole	MMCX_VERTICAL – through-hole
1	X3	CN2	Terminal block HDR two-position vertical 5.08 mm MOLEX 0395311002 Terminal block plug two-position 5.08 mm MOLEX 0395333002	CN2

9 References

[1] AN_201702_PL52_012 Driving 600 V CoolGaN™ high electron mobility transistors. Zojer, Bernhard.

[2] AN_18100_PL52_1811_234307 600 V CoolGaN™ half-bridge evaluation platform featuring GaN EiceDRIVER™. Persson, Eric and Haksoz, Yalcin.

10 Revision history

Document version	Date of release	Description of changes
V 1.0	2020-03-23	First release

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Edition 2020-03-23

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

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Document reference
ER_1908_PL52_1910_100139

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