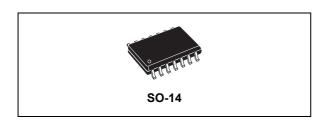


High voltage high and low-side driver

Datasheet - production data



Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/nsec in full temperature range
- Driver current capability
 - 400 mA source
 - 650 mA sink
- Switching times 50/30 nsec rise/fall with 1 nF load
- CMOS/TTL Schmitt trigger inputs with hysteresis and pull-down
- Undervoltage lockout on lower and upper driving section
- · Integrated bootstrap diode
- · Outputs in phase with inputs

Applications

- · Home appliances
- Induction heating
- · Industrial applications and drives
- Motor drivers
 - SR motors,
 - DC, AC, PMDC and PMAC motors
- · Asymmetrical half-bridge topologies
- HVAC
- · Lighting applications
- · Factory automation
- Power supply systems

Description

The L6386AD is a high voltage gate driver, manufactured with the BCD™ "offline" technology, and able to drive simultaneously one high and one low-side power MOS or IGBT device. The high-side (floating) section is enabled to work with voltage rail up to 600 V. Both device outputs can independently sink and source 650 mA and 400 mA respectively and can be simultaneously driven high.

The L6386AD device provides two input pins, two output pins and an enable pin (SD), and guarantees the outputs switch in phase with inputs. The logic inputs are CMOS/TTL compatible to ease the interfacing with controlling devices.

The L6386AD integrates a comparator (inverting input internally referenced to 0.5 V) that can be used to protect the device against fault events, like overcurrent. The DIAG output is a diagnostic pin, driven by the comparator, and used to signal a fault event occurrence to the controlling device.

The bootstrap diode is integrated in the driver allowing a more compact and reliable solution.

The L6386AD device features the UVLO protection on both supply voltages (V_{CC} and V_{boot}) ensuring greater protection against voltage drops on the supply lines.

The device is available in a SO-14 package, in tube, and tape and reel packaging.

Table 1. Device summary

Order codes	Package	Packaging
L6386AD	SO-14	Tube
L6386AD013TR	SO-14	Tape and reel

Contents L6386AD

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L6386AD **Block diagram**

Block diagram 1

Figure 1. Block diagram BOOTSTRAP DRIVER Vboot 14 C_{BOOT} UV DETECTION UV DETECTION HVG R DRIVER R 13 LEVEL HIN OUT SHIFTER TO LOAD 12 LOGIC LVG SD 9 LVG DRIVER PGND LIN DIAG VREF 5 SGND 6 CIN D97IN520D

Electrical data L6386AD

2 Electrical data

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{out}	Output voltage	-3 to V _{boot} - 18	V
V _{cc}	Supply voltage	- 0.3 to +18	V
V _{boot}	Floating supply voltage	-1 to 618	V
V _{hvg}	High-side gate output voltage	- 1 to V _{boot}	V
V _{Ivg}	Low-side gate output voltage	-0.3 to V _{cc} +0.3	V
Vi	Logic input voltage	-0.3 to V _{cc} +0.3	V
V _{diag}	Open drain forced voltage	-0.3 to V _{cc} +0.3	V
V _{cin}	Comparator input voltage	-0.3 to 10 V	V
dV _{out} /dt	Allowed output slew rate	50	V/ns
P _{tot}	Total power dissipation (T _J = 85 °C)	750	mW
T _j	Junction temperature	150	°C
T _{stg}	Storage temperature	-50 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	SO-14	Unit
R _{th(JA)}	Thermal resistance junction to ambient	165	°C/W

2.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min.	Тур.	Max.	Unit
V _{out}	12	Output voltage		(1)		580	V
V _{BS} ⁽²⁾	14	Floating supply voltage		(1)		17	V
f _{sw}		Switching frequency	HVG, LVG load C _L = 1 nF			400	kHz
V _{cc}	4	Supply voltage				17	V
T _J		Junction temperature		-45		125	°C

^{1.} If the condition $\rm V_{boot}$ - $\rm V_{out}$ < 18 V is guaranteed, $\rm V_{out}$ can range from -3 to 580 V.



^{2.} $V_{BS} = V_{boot} - V_{out}$

L6386AD Electrical data

2.4 Pin connection

Figure 2. Pin connection (top view)

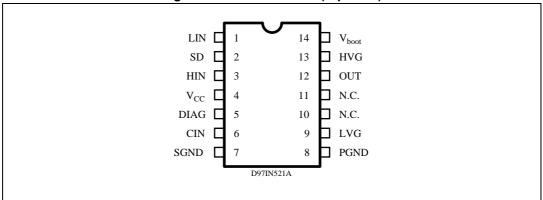


Table 5. Pin description

No.	Pin	Туре	Function
1	LIN	I	Low-side driver logic input
2	SD ⁽¹⁾	I	Shutdown logic input
3	HIN	I	High-side driver logic input
4	V _{CC}	Р	Low voltage supply
5	DIAG	0	Open drain diagnostic output
6	CIN	I	Comparator input
7	SGND	Р	Ground
8	PGND	Р	Power ground
9	LVG ⁽¹⁾	0	Low-side driver output
10, 11	N.C.		Not connected
12	OUT	Р	High-side driver floating driver
13	HVG ⁽¹⁾	0	High-side driver output
14	V _{boot}	Р	Bootstrapped supply voltage

The circuit guarantees 0.3 V maximum on the pin (at Isink = 10 mA), with V_{CC} > 3 V. This allows to omit the
"bleeder" resistor connected between the gate and the source of the external MOSFET normally used to
hold the pin low; the gate driver assures low impedance also in SD condition.

Electrical characteristics L6386AD

3 Electrical characteristics

3.1 AC operation

Table 6. AC operation electrical characteristics (V $_{CC}$ = 15 V; T $_{J}$ = 25 °C)

Symbol	Pin	Parameter	Test condition	Min.	Тур.	Max.	Unit
t _{on}	1, 3 vs. 9, 13	High/low-side driver turn-on propagation delay			110	150	ns
t _{off}	1, 3 vs. 9, 13	High/low-side driver turn-off propagation delay	V _{out} = 0 V		110	150	ns
t _{sd}	2 vs. 9,13	Shutdown to high/low-side propagation delay			105	150	
t _r	9, 13	Rise time	C _L = 1000 pF		50		ns
t _f	9, 13	Fall time	C _L = 1000 pF		30		ns

3.2 DC operation

Table 7. DC operation electrical characteristics (V_{CC} = 15 V; T_J = 25 °C)

	Parameter	Test condition	Min.	Тур.	Max.	Unit
ply voltage s	ection				•	
	V _{cc} UV turn-on threshold		9.1	9.6	10.1	V
	V _{cc} UV turn-off threshold		7.9	8.3	8.8	V
4	V _{cc} UV hysteresis			1.3		V
·	Undervoltage quiescent supply current	V _{cc} ≤ 9 V		200		μА
	Quiescent current	V _{cc} = 15 V		250	320	μΑ
pped supply	section					
	V _{boot} UV turn-on threshold		8.5	9.5	10.5	V
	V _{boot} UV turn-off threshold		7.2	8.2	9.2	V
14	V _{boot} UV hysteresis			1.3		V
	V _{boot} quiescent current	HVG ON			200	μΑ
	High voltage leakage current	$V_{\text{hvg}} = V_{\text{out}} = V_{\text{boot}} = 600 \text{ V}$			10	μА
	Bootstrap driver on-resistance ⁽¹⁾	$V_{cc} \ge 12.5 \text{ V V}_{IN} = 0 \text{ V}$		125		Ω
uffers section	n					
9, 13	High/low-side source short-circuit current	$V_{IN} = V_{ih} (t_p < 10 \ \mu s)$	300	400		mA
9, 13	High/low-side sink short-circuit current	$V_{IN} = V_{il} (t_p < 10 \ \mu s)$	500	650		mA
	pped supply 14 ouffers section 9, 13	4 V _{cc} UV turn-off threshold V _{cc} UV hysteresis Undervoltage quiescent supply current Quiescent current Pped supply section V _{boot} UV turn-on threshold V _{boot} UV turn-off threshold V _{boot} UV hysteresis V _{boot} quiescent current High voltage leakage current Bootstrap driver on-resistance ⁽¹⁾ Puffers section 9, 13 High/low-side source short-circuit Guirent High/low-side sink short-circuit	$V_{cc} \ UV \ turn-on \ threshold$ $V_{cc} \ UV \ turn-off \ threshold$ $V_{cc} \ UV \ tyrn-off \ threshold$ $V_{cc} \ UV \ tyrn-off \ threshold$ $V_{cc} \le 9 \ V$ $V_{cc} \le 9 \ V$ $V_{cc} = 15 \ V$ $V_{boot} \ UV \ turn-on \ threshold$ $V_{boot} \ UV \ turn-off \ threshold$ $V_{boot} \ UV \ turn-off \ threshold$ $V_{boot} \ UV \ tyrn-off \ threshold$ $V_{boot} \ V_{boot} \ V_{boot$	$V_{cc} \text{ UV turn-on threshold} \qquad 9.1$ $V_{cc} \text{ UV turn-off threshold} \qquad 7.9$ $V_{cc} \text{ UV hysteresis} \qquad V_{cc} \leq 9 \text{ V}$ $Quiescent current \qquad V_{cc} = 15 \text{ V}$ $V_{cc} = 15 \text{ V}$ $V_{boot} \text{ UV turn-on threshold} \qquad 8.5$ $V_{boot} \text{ UV turn-off threshold} \qquad 7.2$ $V_{boot} \text{ UV hysteresis} \qquad V_{boot} \text{ UV hysteresis} \qquad V_{boot} \text{ Quiescent current} \qquad HVG \text{ ON}$ $High voltage leakage current \qquad V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{boot} \text{ UV hysteresis} \qquad V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{boot} \text{ UV hysteresis} \qquad V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{boot} \text{ UV hysteresis} \qquad V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = V_{out} = V_{boot} = 0.00 \text{ V}$ $V_{hvg} = 0.00 \text{ V}$ V_{hv	$V_{cc} \ UV \ turn-on \ threshold \qquad \qquad 9.1 \qquad 9.6$ $V_{cc} \ UV \ turn-off \ threshold \qquad \qquad 7.9 \qquad 8.3$ $V_{cc} \ UV \ hysteresis \qquad \qquad \qquad 1.3$ $Undervoltage \ quiescent \ supply \ current \qquad \qquad V_{cc} \le 9 \ V \qquad \qquad 200$ $Quiescent \ current \qquad \qquad V_{cc} = 15 \ V \qquad \qquad 250$ $Pped \ supply \ section \qquad \qquad$	

Symbol	Pin	Parameter Test condition		Min	Тур	Max	Unit
Logic inp	outs						
V _{il}		Low level logic voltage				1.5	V
V_{ih}	1, 2, 3	High level logic voltage		3.6			V
I _{ih}	1, 2, 3	High level logic input current	V _{IN} = 15 V		50	70	μА
I _{il}		Low level logic input current	$V_{IN} = 0 V$			1	μА
Sense co	mparator						
V _{io}		Input offset voltage		-10		10	mV
I _{io}	6	Input bias current	V _{cin} ≥ 0.5		0.2		μΑ
V _{ol}	2	Open drain low level output voltage	I _{od} = -2.5 mA			0.8	V
V _{ref}		Comparator reference voltage		0.46	0.50	0.54	V

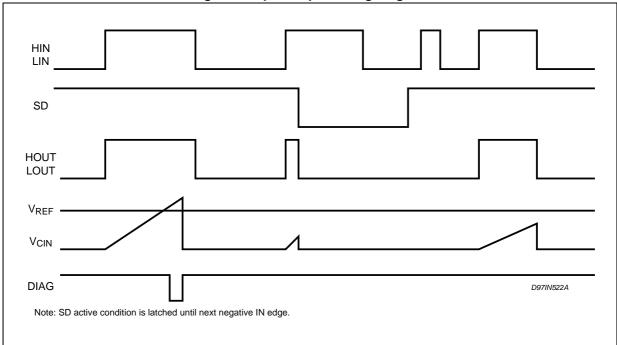
Table 7. DC operation electrical characteristics (continued) (V_{CC} = 15 V; T_J = 25 $^{\circ}C$)

$$\mathsf{R}_{\mathsf{DSON}} = \frac{(\mathsf{V}_{\mathsf{CC}} \! - \! \mathsf{V}_{\mathsf{CBOOT1}}) \! - \! (\mathsf{V}_{\mathsf{CC}} \! - \! \mathsf{V}_{\mathsf{CBOOT2}})}{\mathsf{I}_{1}(\mathsf{V}_{\mathsf{CC}}, \! \mathsf{V}_{\mathsf{CBOOT1}}) \! - \! \mathsf{I}_{2}(\mathsf{V}_{\mathsf{CC}}, \! \mathsf{V}_{\mathsf{CBOOT2}})}$$

where I_1 is the pin 14 current when $V_{CBOOT} = V_{CBOOT1}$, I_2 when $V_{CBOOT} = V_{CBOOT2}$.

3.3 Timing diagram





^{1.} $R_{DS(on)}$ is tested in the following way:

Bootstrap driver L6386AD

4 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 4* a). In the L6386AD device a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in *Figure 4* b. An internal charge pump (*Figure 4* b) provides the DMOS driving voltage. The diode connected in series to the DMOS has been added to avoid undesirable turn-on.

CBOOT selection and charging

To choose the proper C_{BOOT} value, the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

E.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage losses.

E.g.: HVG steady state consumption is lower than 200 μ A, so if HVG T_{ON} is 5 ms, C_{BOOT} has to supply 1 μ C to C_{EXT}. This charge on a 1 μ F capacitor means a voltage drop of 1 V.

The internal bootstrap driver gives great advantages: the external fast recovery diode can be avoided (it usually has a great leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS $R_{DS(on)}$ (typical value: 125 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken into account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 2

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$$V_{drop} = I_{charge}R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}}R_{dson}$$

where Qgate is the gate charge of the external power MOS, R_{dson} is the on-resistance of the bootstrap DMOS, and T_{charge} is the charging time of the bootstrap capacitor.

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L6386AD Bootstrap driver

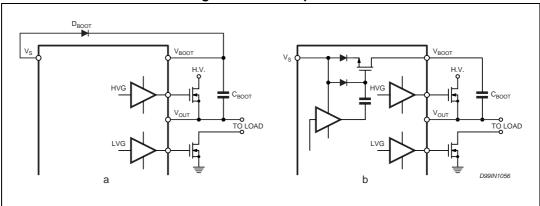
For example: using a power MOS with a total gate charge of 30 nC, the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 ms. In fact:

Equation 3

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 125\Omega \sim 0.8V$$

 V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 4. Bootstrap driver



Typical characteristic L6386AD

5 Typical characteristic

Figure 5. Typical rise and fall times vs. load capacitance

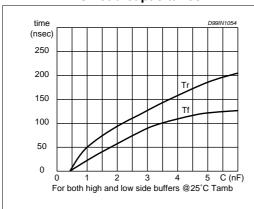


Figure 6. Quiescent current vs. supply voltage

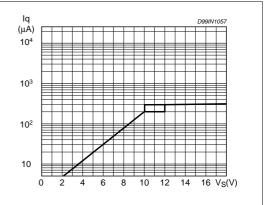
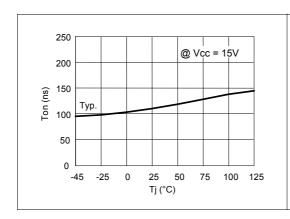


Figure 7. Turn-on time vs. temperature

Figure 8. V_{BOOT} UV turn-on threshold vs. temperature



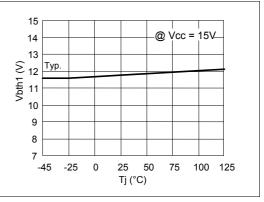
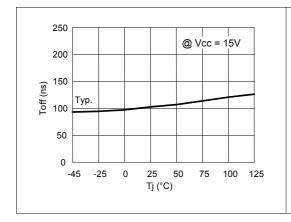
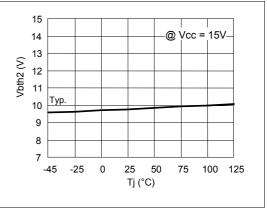


Figure 9. Turn-off time vs. temperature

Figure 10. V_{BOOT} UV turn-off threshold vs. temperature





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Figure 11. Shutdown time vs. temperature

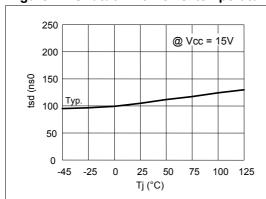


Figure 12. V_{BOOT} UV hysteresis

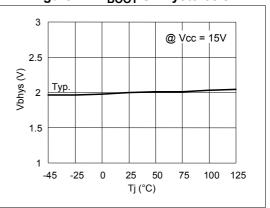


Figure 13. V_{CC} UV turn-on threshold vs. temperature

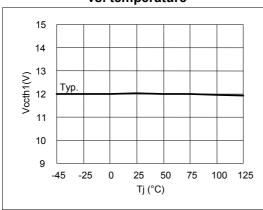


Figure 14. Output source current vs. temperature

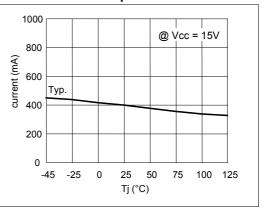


Figure 15. V_{CC} UV turn-off threshold vs. temperature

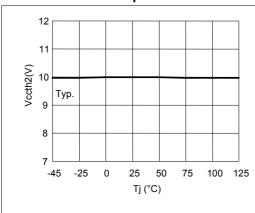
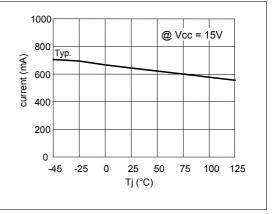
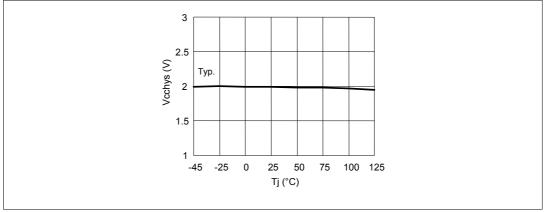


Figure 16. Output sink current vs. temperature



Typical characteristic L6386AD

Figure 17. V_{CC} UV hysteresis vs. temperature



L6386AD Package information

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at:www.st.com. ECOPACK is an ST trademark.

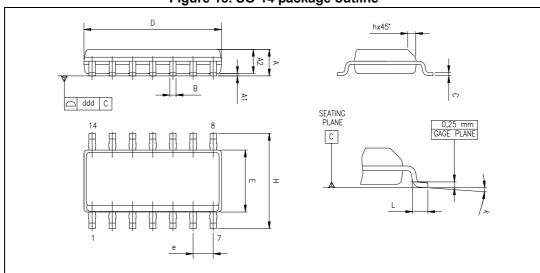


Figure 18. SO-14 package outline

Table 8. SO-14 package mechanical data

0 1 1	Dimensions (mm)			Dimensions (inch)			
Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	
Α	1.35		1.75	0.053		0.069	
A1	0.10		0.30	0.004		0.012	
A2	1.10		1.65	0.043		0.065	
В	0.33		0.51	0.013		0.020	
С	0.19		0.25	0.007		0.01	
D ⁽¹⁾	8.55		8.75	0.337		0.344	
E	3.80		4.0	0.150		0.157	
е		1.27			0.050		
Н	5.8		6.20	0.228		0.244	
h	0.25		0.50	0.01		0.02	
L	0.40		1.27	0.016		0.050	
k		1	0° (min.), 8	s° (max.)	1	ı	
ddd			0.10			0.004	

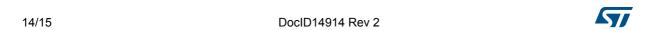
 [&]quot;D" dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

Revision history L6386AD

7 Revision history

Table 9. Document revision history

Date	Revision	Changes
14-Jul-2008	1	First release
20-Jun-2014	2	Added Section: Applications on page 1. Updated Section: Description on page 1 (replaced by new description). Updated Table 1: Device summary on page 1 (moved "Table 9 Order codes" from page 15 to page 1, renamed title of Table 1). Updated Figure 1: Block diagram on page 3 (moved to page 3, added Section 1: Block diagram on page 3). Updated Section 2.1: Absolute maximum ratings on page 4 (removed note below Table 2: Absolute maximum ratings). Updated Table 5: Pin description on page 5 (updated "Type" of several pins). Numbered Equation 1 on page 8, Equation 2 on page 8 and Equation 3 on page 9. Updated Section 6: Package information on page 13 (updated ECOPACK text, updated/added titles, reversed order of Figure 18 and Table 8 (numbered Table 8), removed 3D package figure, minor modifications]. Minor modifications throughout document.



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