

## PROTECTION PRODUCTS

### Description

RailClamps are surge rated diode arrays designed to protect high speed data interfaces. The SR series has been specifically designed to protect sensitive components which are connected to data and transmission lines from overvoltage caused by electrostatic discharge (ESD), electrical fast transients (EFT), and lightning.

The unique design of the SRDA series devices incorporates surge rated, low capacitance steering diodes and a TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. The internal TVS diode prevents overvoltage on the power line, protecting any downstream components.

The low capacitance array configuration allows the user to protect six high-speed data or transmission lines. The low inductance construction minimizes voltage overshoot during high current surges.

### Features

- Transient protection for high-speed data lines to
  - ♦ IEC 61000-4-2 (ESD)  $\pm 15\text{kV}$  (air),  $\pm 8\text{kV}$  (contact)
  - ♦ IEC 61000-4-4 (EFT) 40A (5/50ns)
  - ♦ IEC 61000-4-5 (Lightning) 25A (8/20 $\mu\text{s}$ )
- Array of surge rated diodes with internal TVS diode
- Protects six I/O lines and power supply line
- Low capacitance (<15pF)
- Low operating voltage: 3.3V
- Low clamping voltage
- Solid-state technology

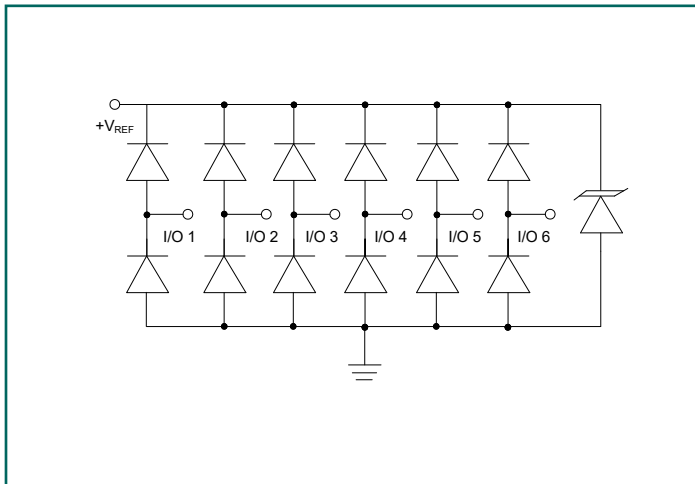
### Mechanical Characteristics

- JEDEC SO-8 Package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Molding compound flammability rating: UL 94V-0
- Marking : Part number, date code, logo
- Packaging : Tape and Reel

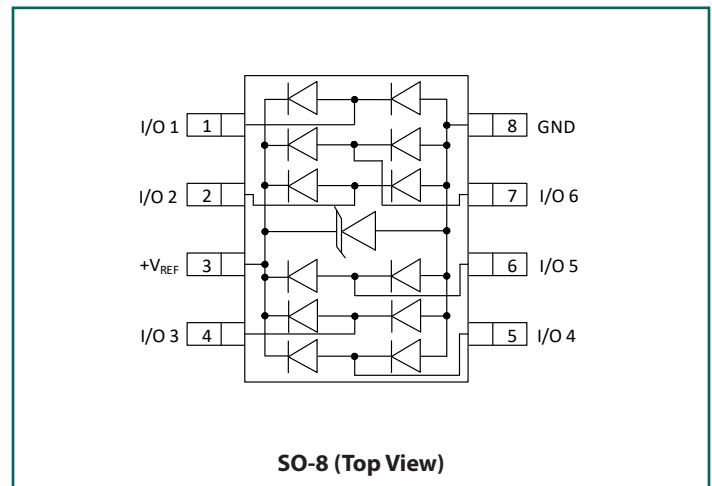
### Applications

- USB Power & Data Line Protection
- T1/E1 secondary IC Side Protection
- Token Ring
- HDSL, SDSL secondary IC Side Protection
- Video Line Protection
- Microcontroller Input Protection
- Base stations
- I<sup>2</sup>C Bus Protection

### Circuit Diagram



### Schematic and Pin Configuration



## Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Power ( $t_p = 8/20\mu s$ )	$P_{PK}$	500	W
Peak Pulse Current	$I_{PP}$	25	A
Peak Pulse Current ( $I_F = 1A, t_p = 8/20\mu s$ )	$V_{FP}$	1.5	V
Operating Temperature	$T_{OP}$	-55 to +125	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C

## Electrical Characteristics (T=25°C unless otherwise specified)

SRDA3.3-6							
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	
Reverse Stand-Off Voltage	$V_{RWM}$				3.3	V	
Punch-Through Voltage	$V_{PT}$	$I_{PT} = 2\mu A$	3.5			V	
Snap-Back Voltage	$V_{SB}$	$I_{SB} = 50mA$	2.8			V	
Reverse Leakage Current	$I_R$	$V_{RWM} = 3.3V$			1	$\mu A$	
Clamping Voltage	$V_C$	$tp = 8/20\mu s$	$I_{PP} = 1A$		5.3	V	
			$I_{PP} = 10A$		10		
			$I_{PP} = 25A$		15		
Junction Capacitance	$C_J$	$V_R = 0V, f = 1MHz$	I/O to GND		8	15	pF
			I/O to I/O		4		

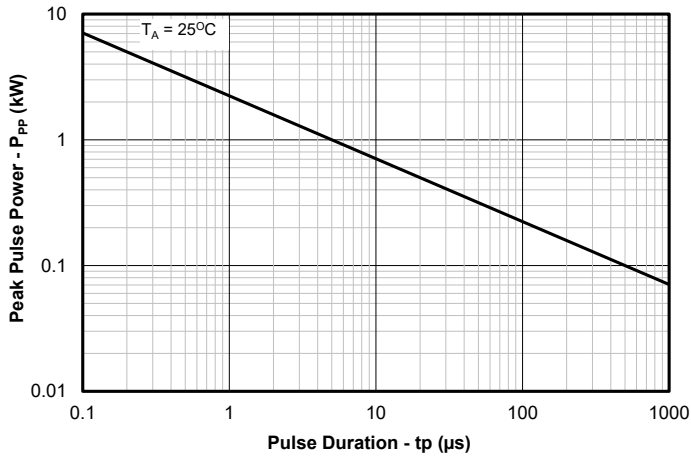
SRDA05-6							
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	
Reverse Stand-Off Voltage	$V_{RWM}$				5	V	
Reverse Breakdown Voltage	$V_{BR}$	$I_t = 1mA$	6			V	
Reverse Leakage Current	$I_R$	$V_{RWM} = 5V$			10	$\mu A$	
Clamping Voltage	$V_C$	$tp = 8/20\mu s$	$I_{PP} = 1A$		9.8	V	
			$I_{PP} = 10A$		12		
			$I_{PP} = 25A$		20		
Junction Capacitance	$C_J$	$V_R = 0V, f = 1MHz$	I/O to GND		8	15	pF
			I/O to I/O		4		

Note:

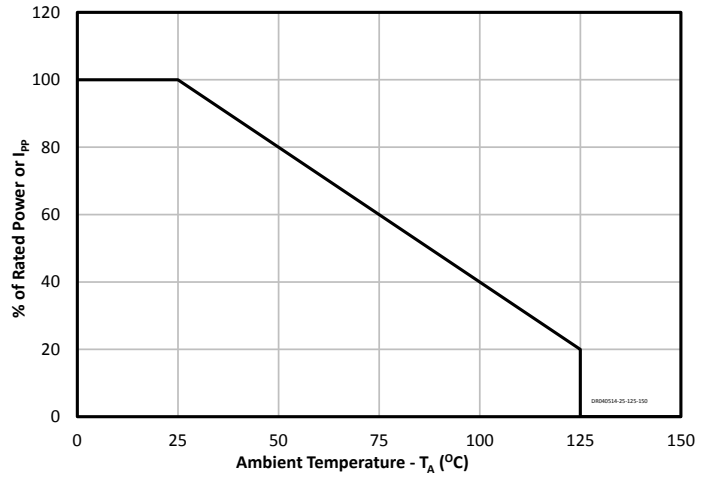
(1) The SRDA3.3-6 is constructed using Semtech's proprietary EPD process technology. See applications section for more information.

# Typical Characteristics

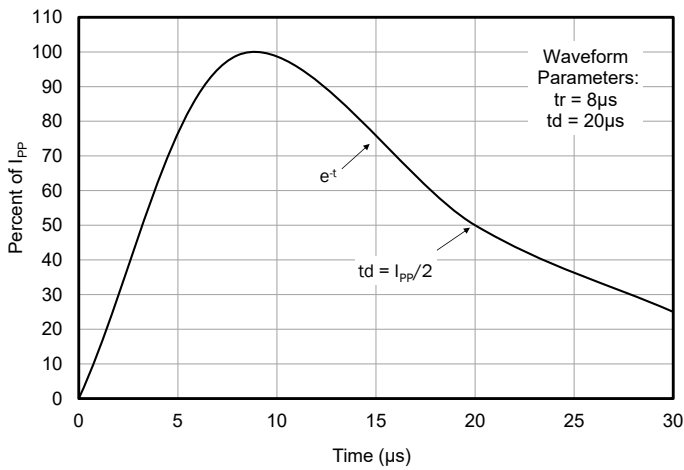
### Non-Repetitive Peak Pulse Power vs. Pulse Time



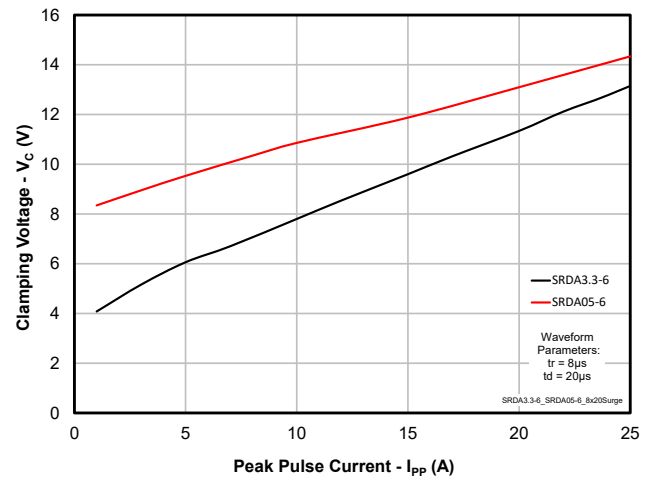
### Power Derating Curve



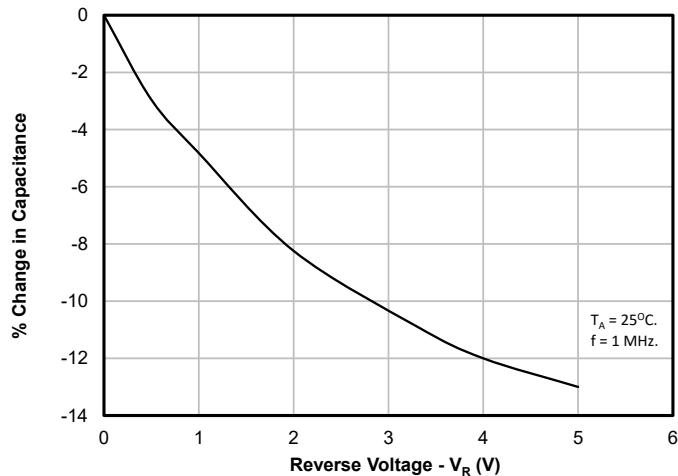
### Pulse Waveform



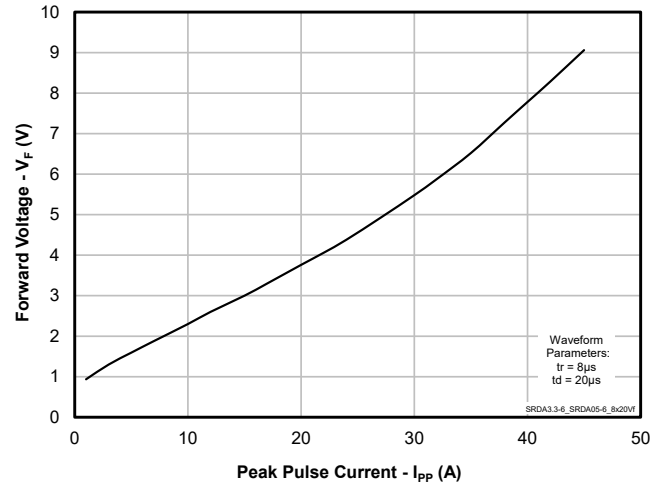
### Clamping Voltage vs. Peak Pulse Current



### Capacitance vs. Reverse Voltage



### Forward Voltage vs. Forward Current



# Application Information

## Device Connection Options for Protection of Six High-Speed Lines

The SRDA TVS is designed to protect four data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode VF) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 2, 4, 5, 6 and 7. The negative reference is connected at pin 8. These pins should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance. The positive reference is connected at pin 3.

In the case of the SRDA3.3-6, pin 3 is connected internally to the cathode of the low voltage TVS. It is not recommended that these pins be directly connected to a DC source greater than the snap-back voltage (VSB) as the device can latch on as described below.

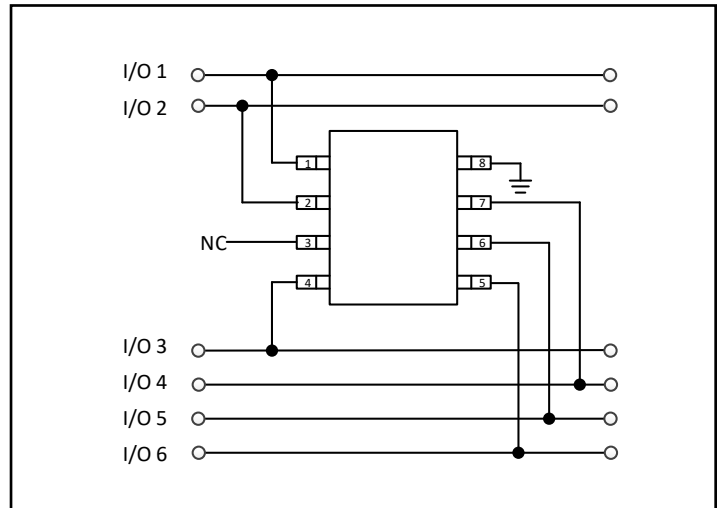
### EPD TVS Characteristics

These devices are constructed using Semtech's proprietary EPD technology. By utilizing the EPD technology, the SRDA3.3-6 can effectively operate at 3.3V while maintaining excellent electrical characteristics.

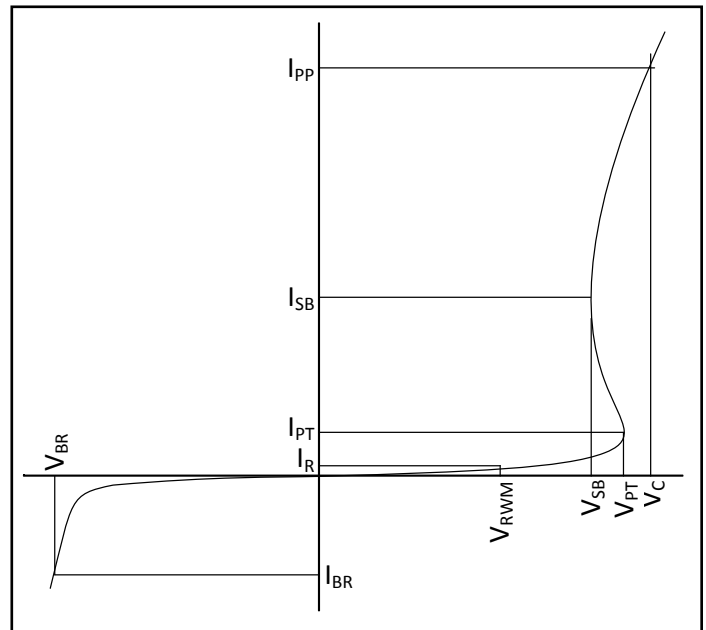
The EPD TVS employs a complex npnp structure in contrast to the pn structure normally found in traditional silicon-avalanche TVS diodes. Since the EPD TVS devices use a 4-layer structure, they exhibit a slightly different IV characteristic curve when compared to conventional devices. During normal operation, the device represents a high-impedance to the circuit up to the device working voltage (VRWM). During an ESD event, the device will begin to conduct and will enter a low impedance state when the punch through voltage (VPT) is exceeded. Unlike a conventional device, the low voltage TVS will exhibit a slight negative resistance characteristic as it conducts current. This characteristic aids in lowering the clamping voltage of the device, but must be considered in applications where DC voltages are present.

When the TVS is conducting current, it will exhibit a slight "snap-back" or negative resistance characteristics due to its structure. This point is defined on the curve by the snap-back voltage (VSB) and snap-back current (ISB).

## Data Line Protection Using Internal TVS Diode as Reference



### EPD TVS IV Characteristic Curve



To return to a non-conducting state, the current through the device must fall below the ISB (approximately <math><50\text{mA}</math>) and the voltage must fall below the VSB (normally 2.8 volts for a 3.3V device). If a 3.3V TVS is connected to 3.3V DC source, it will never fall below the snap-back voltage of 2.8V and will therefore stay in a conducting state.

## Application Information (continued)

The clamping voltage due to the characteristics of the protection diodes is given by:

$$V_C = V_{CC} + V_F \quad (\text{for positive duration pulses})$$

$$V_C = -V_F \quad (\text{for negative duration pulses})$$

However, for fast rise time transient events, the effects of parasitic inductance must also be considered as shown in Figure 2. Therefore, the actual clamping voltage seen by the protected circuit will be:

$$V_C = V_{CC} + V_F + L_P di_{ESD} / dt \quad (\text{for positive duration pulses})$$

$$V_C = -V_F - L_G di_{ESD} / dt \quad (\text{for negative duration pulses})$$

ESD current reaches a peak amplitude of 30A in 1ns for a level 4 ESD contact discharge per IEC 1000-4-2. Therefore, the voltage overshoot due to 1nH of series inductance is:

$$V = L_P di_{ESD} / dt = 1 \times 10^{-9} (30 / 1 \times 10^{-9}) = 30V$$

Example:

Consider a  $V_{CC} = 5V$ , a typical  $V_F$  of 30V (at 30A) for the steering diode and a series trace inductance of 10nH. The clamping voltage seen by the protected IC for a positive 8kV (30A) ESD pulse will be:

$$V_C = 5V + 30V + (10nH \times 30V/nH) = 335V$$

This does not take into account that the ESD current is directed into the supply rail, potentially damaging any components that are attached to that rail. Also note the high  $V_F$  of the discrete diode. It is not uncommon for the  $V_F$  of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. It is also possible that the power dissipation capability of the discrete diode will be exceeded, thus destroying the device.

The RailClamp is designed to overcome the inherent disadvantages of using discrete signal diodes for ESD suppression. The RailClamp's integrated TVS diode helps to mitigate the effects of parasitic inductance in the power supply connection. During an ESD event, the current will be directed through the integrated TVS diode to ground.

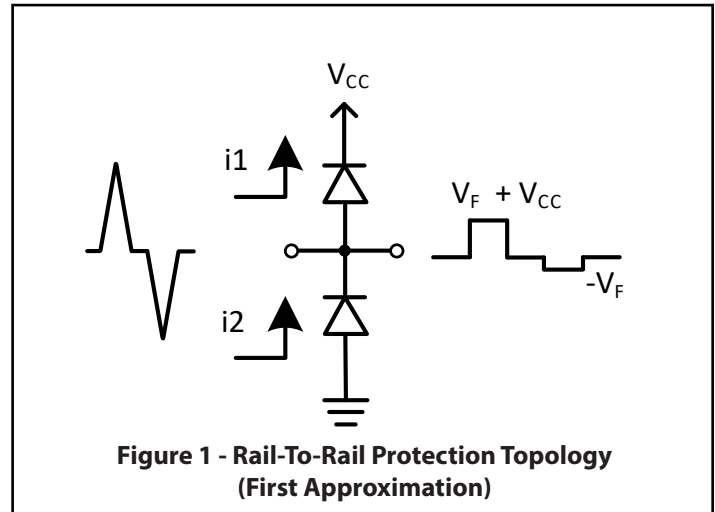


Figure 1 - Rail-To-Rail Protection Topology (First Approximation)

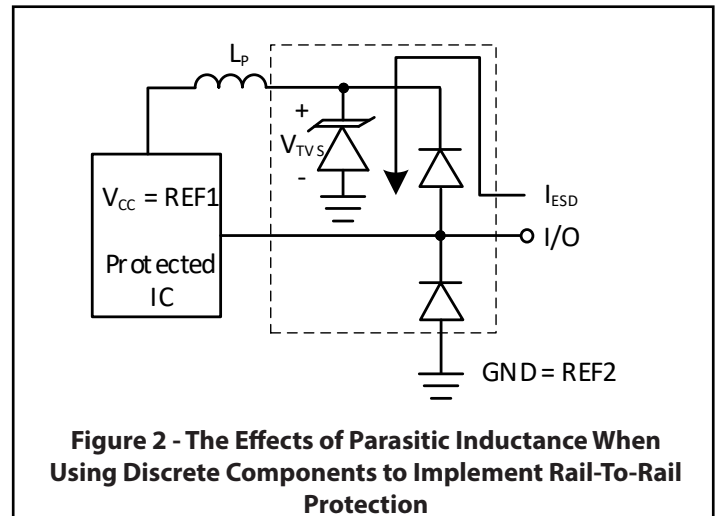


Figure 2 - The Effects of Parasitic Inductance When Using Discrete Components to Implement Rail-To-Rail Protection

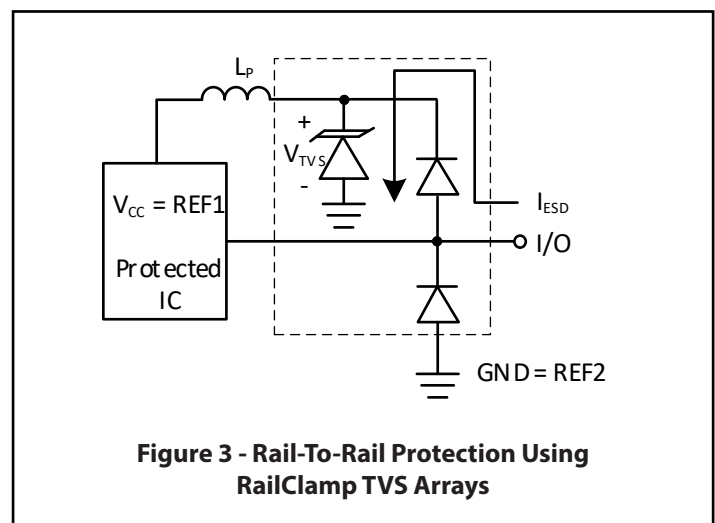


Figure 3 - Rail-To-Rail Protection Using RailClamp TVS Arrays

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## Application Information (continued)

The total clamping voltage seen by the protected IC due to this path will be:

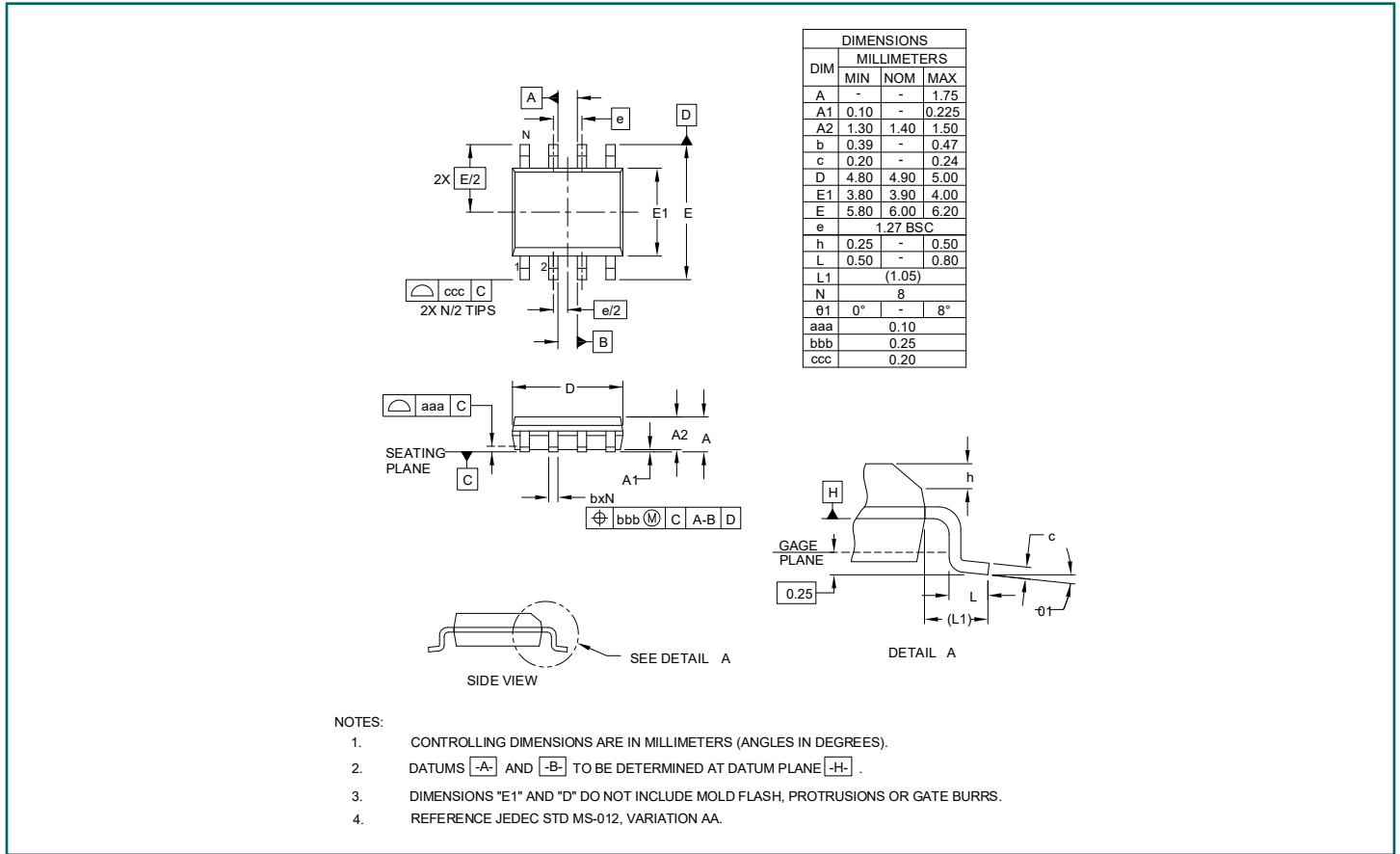
$$V_C = V_{F(\text{RailClamp})} + V_{\text{TVS}}$$

This is given in the data sheet as the rated clamping voltage of the device. For an SRDA05-6 the typical clamping voltage is <16V at  $I_{pp} = 30\text{A}$ . The diodes internal to the RailClamp are low capacitance, fast switching devices that are rated to handle high transient currents and maintain excellent forward voltage characteristics.

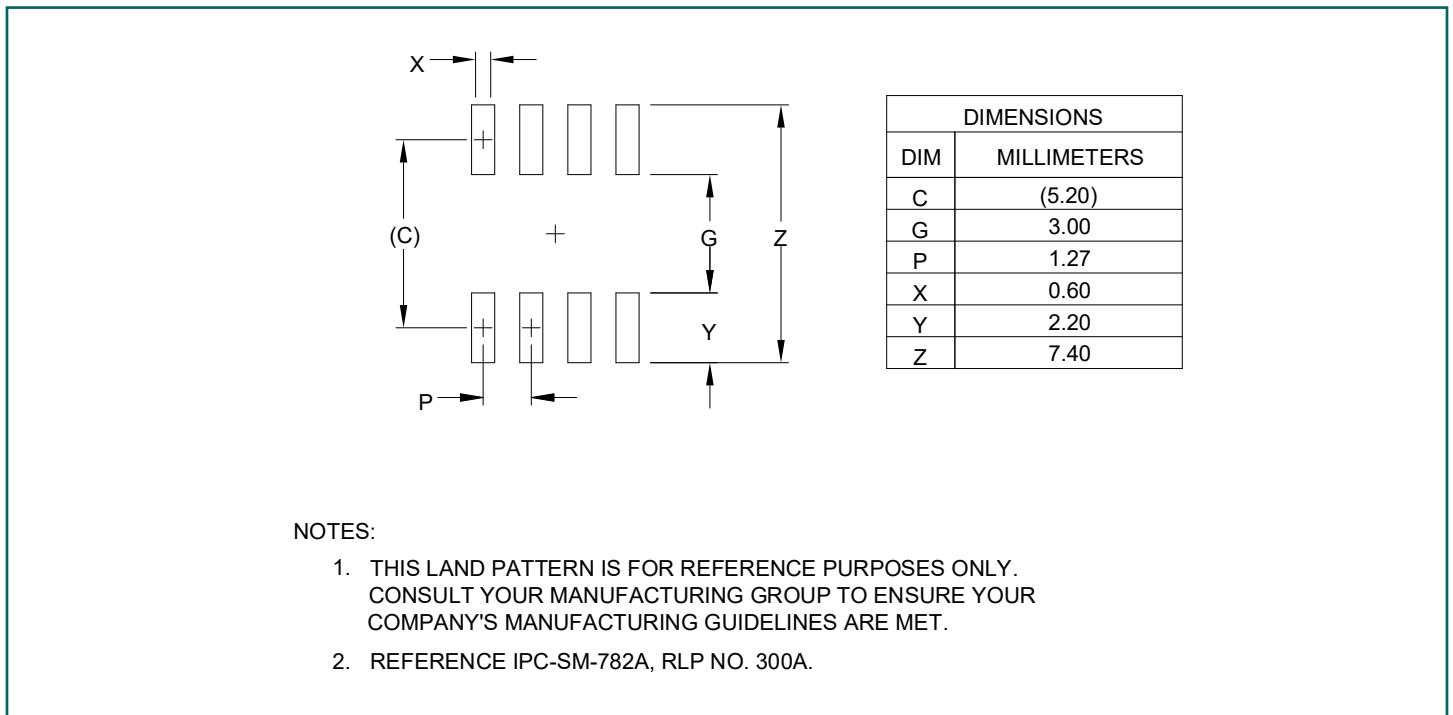
Using the RailClamp does not negate the need for good board layout. All other inductive paths must be considered. The connection between the positive supply and the SRDA and from the ground plane to the SRDA must be kept as short as possible. The path between the

SRDA and the protected line must also be minimized. The protected lines should be routed directly to the SRDA. Placement of the SRDA on the PC board is also critical for effective ESD protection. The device should be placed as close as possible to the input connector. The reason for this is twofold. First, inductance resists change in current flow. If a significant inductance exists between the connector and the TVS, the ESD current will be directed elsewhere (lower resistance path) in the system. Second, the effects of radiated emissions and transient coupling can cause upset to other areas of the board even if there is no direct path to the connector. By placing the TVS close to the connector it will divert the ESD current immediately and absorb the ESD energy before it can be coupled into nearby traces.

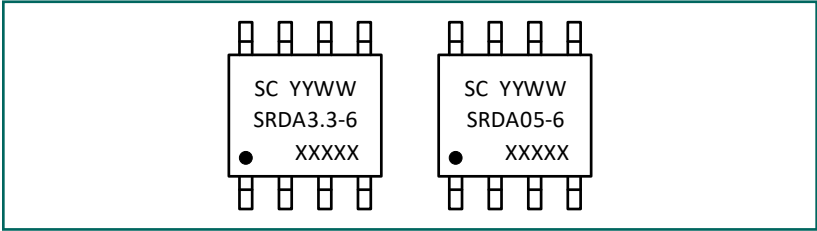
# Outline Drawing - SO-8



# Land Pattern - SO-8

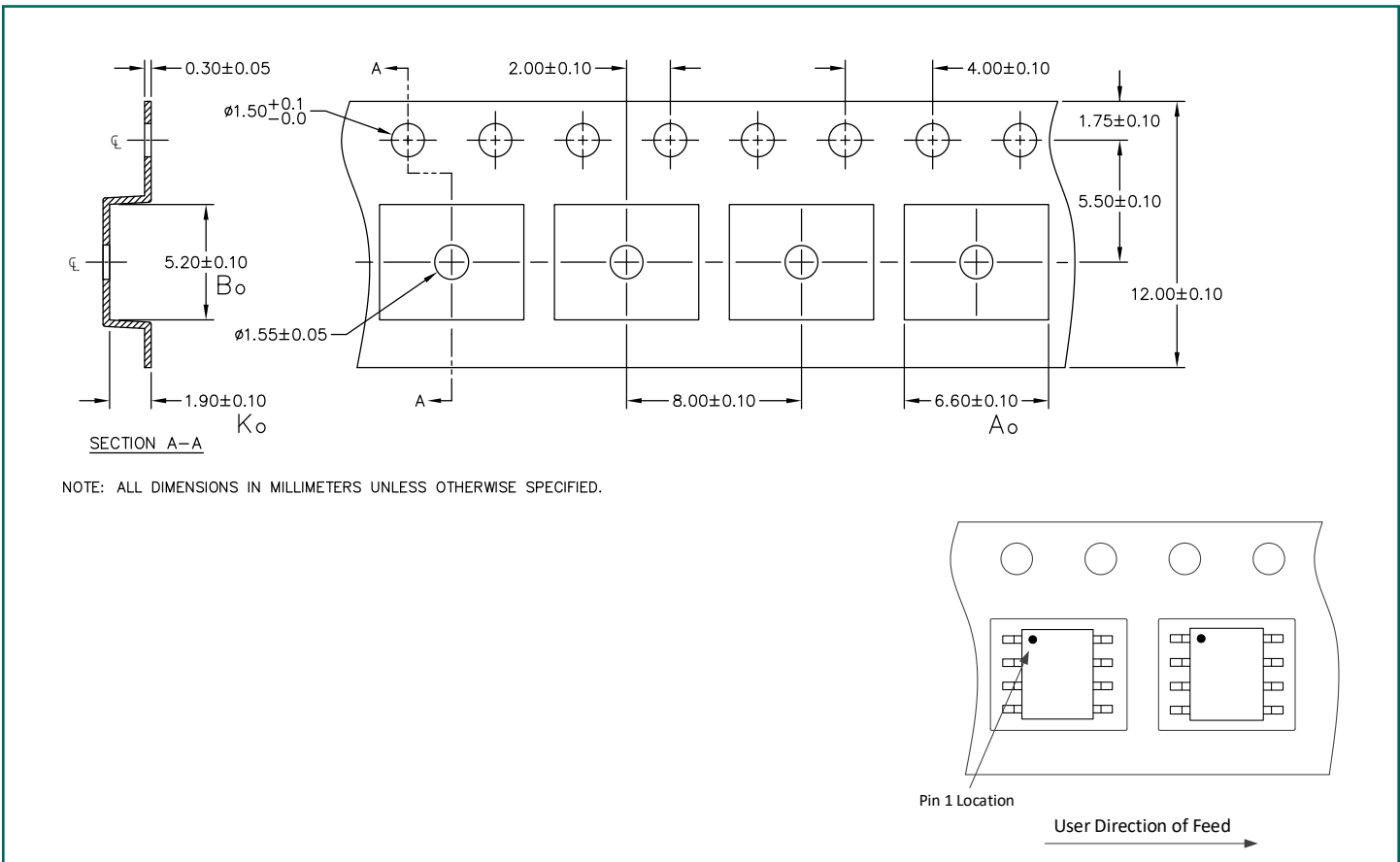


# Marking Code



Notes:  
 YYWW = Date Code  
 XXXXX = Country of Assembly

# Tape and Reel Specification



# Ordering Information

Part Number	Working Voltage	Qty per Reel	Reel Size
SRDA3.3-6.TBT	3.3V	500	7 Inch
SRDA05-6.TBT	5V	500	7 Inch





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