EiceDRIVER ™

2EDN752x / 2EDN852x

Dual Channel 5A, High-Speed, Low-Side Gate Driver With High Negative Input Voltage Capability and Advanced Revers Current Robustness

EiceDRIVER™

Fast Dual Channel Low-Side Gate Driver

Data Sheet

Revision 2.0, 2015-07-22

Power Management and Multimarket

Revision History , Revision 2.0, 2015-07-22			
Page/ Item	**Subjects (major changes since previous revision)**	**Responsible**	**Date**
	updated from version 1.1		
all	Complete revision	Tobias Gerber	2015/07/22

Table of Contents

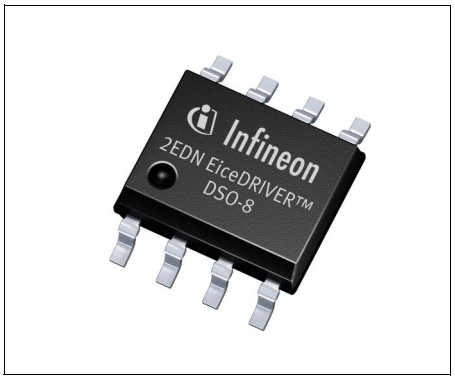
Fast Dual Channel 5 A Low-Side Gate Driver

Main Features

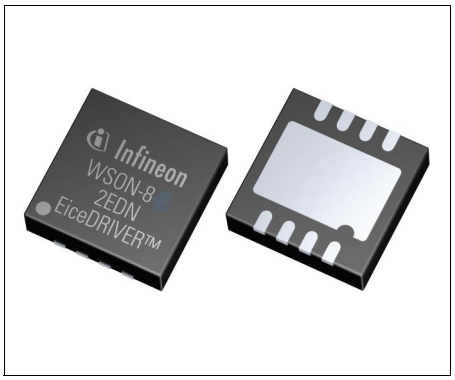
- Industry-Standard Pinout
- Two Independent Low-Side Gate Drivers
- 5 A Peak Sink/Source Output Driver at VDD = 12 V
- -10 Vdc Negative Input Capability against GND-Bouncing
- Enhanced operating robustness due to High Reverse Current Capability (5 A Peak)
- True Low-Impedance Rail-To-Rail Output (0.7 Ω and 0.55 Ω)
- Very Low Propagation Delay (19 ns)
- Typ. 1 ns Channel to Channel Delay Matching
- Wide Input and Output Voltage Range up to 20 V
- Active Low Output Driver even on Low Power or Disabled Driver
- High Flexibility through Different Logic Input Configurations (LVTTL and CMOS 3.3 V)
- PG-DSO-8, PG-WSON-8 and PG-TSSOP-8 Package
- Extended Operation from -40 °C to 150 °C (Junction Temperature)
- Particularly Well-Suited for Driving Standard, Superjunction MOSFETs, IGBTs and GaN Power Devices

Typical Applications

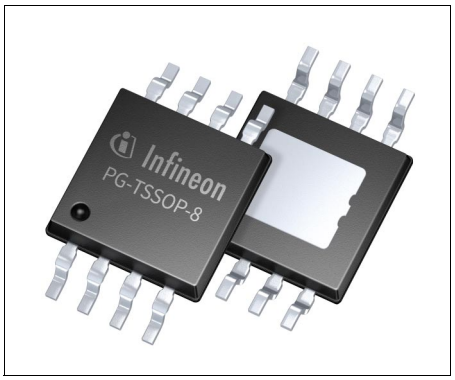
- SMPS
- Single / interleave PFC
- Synchronous rectification
- Isolated gate driving via pulse transformer's
- Local direct gate drive for high performanc SMPS
- DC-to-DC Converters
- Bricks
- Power Tools
- Industrial Applications



PG-DSO-8



PG-WSON-8



PG-TSSOP-8

Description

The Fast Dual Channel 5A Low-Side Gate Driver is an advanced dual-channel driver optimized for driving both Standard MOSFETs and Superjunction MOSFETs (OptiMOS™, CoolMOS™), as well as GaN Power devices, in all applications in which they are commonly used. The input signals are LVTTL compatible (CMOS 3.3V) with an input voltage range from 3V to +20V. The ability to operate with -10V_{DC} at the input pins protects the device against ground bounce conditions. Each of the two outputs is able to sink and source a 5 A current utilizing a true rail-to-rail stage, that ensures very low impedances of 0.7 Ω up to the positive and 0.55 Ω down to the negative rail respectively. Very low channel to channel delay matching, typ. 1 ns, enables the double source and sink capability of 10 A, by paralleling both channels. Advanced Reverse Current Robustness, demonstrated with over 5 A feedback current, sourced by MOSFET ringing or inductive feedbacks, gives more safety margin and robustness in application. Different logic input/output configurations guarantee high flexibility in all applications; e.g. with two paralleled switches in a boost configuration (see Figure below). The gate driver is available in the three package options: A standard PG-DSO-8, a thin PG-WSON-8 and PG-TSSOP-8 (small size DSO 8 package).

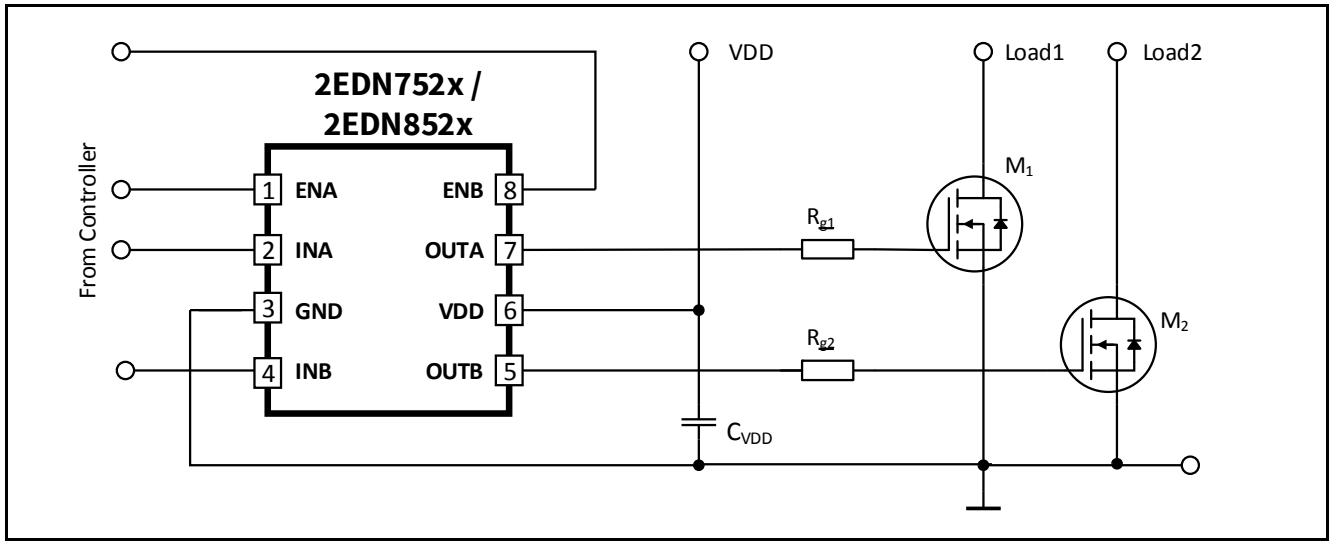


Figure 0-1 Typical Application

1 Product Versions

The 2EDN752x / 2EDN852x is available in 2 different logic, 2 different undervoltage lockout and 3 package versions.

Table 1-1 Product Versions

Part Number	Description	Package	Order Code	IC Topside Marking Code
2EDN7524F	standard input. standard UVLO	PG-DSO-8	SP001339264	2N7524AF EiceDRIV XXHYYWW
2EDN7524R	standard input, standard UVLO	PG-TSSOP-8	SP001391096	2N7524 AR_XXX HYYWW
2EDN8524R	standard input, super junction UVLO	PG-TSSOP-8	SP001391100	2N8524 AR_XXX HYYWW
2EDN7523F	inverted input, standard UVLO	PG-DSO-8	SP001358244	2N7523AF EiceDRIV XXHYYWW
2EDN7524G	standard input, standard UVLO	PG-WSON-8	SP001391108	2N7524 AG_XXX HYYWW
2EDN7523R	inverted input. standard UVLO	PG-TSSOP-8	SP001391098	2N7523 AR_XXX HYYWW
2EDN8523R	inverted input. super junction UVLO	PG-TSSOP-8	SP001391102	2N8523 AR_XXX HYYWW
2EDN7523G	inverted input. standard UVLO	PG-WSON-8	SP001391114	2N7523 AG_XXX HYYWW

1.1 Undervoltage Lockout Versions

The two Undervoltage Lockout versions are indicated by the variable x in the product version 2EDNy52x:

- y=7: lower voltage level (4.2V)
- y=8: higher voltage level (8.0V)

Please go to the functional description section for more details in **Chapter 4 Undervoltage Lockout (UVLO)**.

1.2 Logic Versions

The 2 logic versions are indicated by the variable y in the product version 2EDNy52x:

- x=3: inverting
- x=4: standard (non-inverting)

The logic relations between inputs, enable pins and outputs are given in **Table 1-2** for the inverting and standard version 2EDNx523 and 2EDNx524. The state of the driving output is defined by the state of the respective input, if the enable inputs ENA and ENB are high (or left open). A logic “low” at an enable input or an undervoltage lockout event, due to low voltage at VDD, causes the respective output to be low too, regardless of the input signal.

Table 1-2 Logic Table

Inputs					Output Inverting		Output non-inverting	
ENA	**ENB**	**INA**	**INB**	**UVLO[1)]**	**OUTA**	**OUTB**	**OUTA**	**OUTB**
x	x	x	x	active	L	L	L	L
L	L	x	x	inactive	L	L	L	L
H	L	L	x	inactive	H	L	L	L
H	L	H	x	inactive	L	L	H	L
L	H	x	L	inactive	L	H	L	L
L	H	x	H	inactive	L	L	L	H
H	H	L	L	inactive	H	H	L	L
H	H	H	L	inactive	L	H	H	L
H	H	L	H	inactive	H	L	L	H
H	H	H	H	inactive	L	L	H	H

1) Active means that Vcc is above UVLO threshold voltage and release logic to control output stage.
Inactive means that UVLO disabel active the output stage.

1.3 Package Versions

Most of the logic versions and UVLO versions are available in 3 different packages.

- a standard PG-DSO-8 (designated by “F”)
- a leadless PG-WSON-8 (designated by “G”)
- a small PG-TSSOP-8 (designated by “R”)

Drawings can be viewed in **Chapter 8 Outline Dimensions**.

2 Pin Configuration and Description

The pin configuration for the inverting and standard input version of 2EDN7524F and 2EDN7523F in the PG-DSO-8 package is shown in **Figure 2-1**.

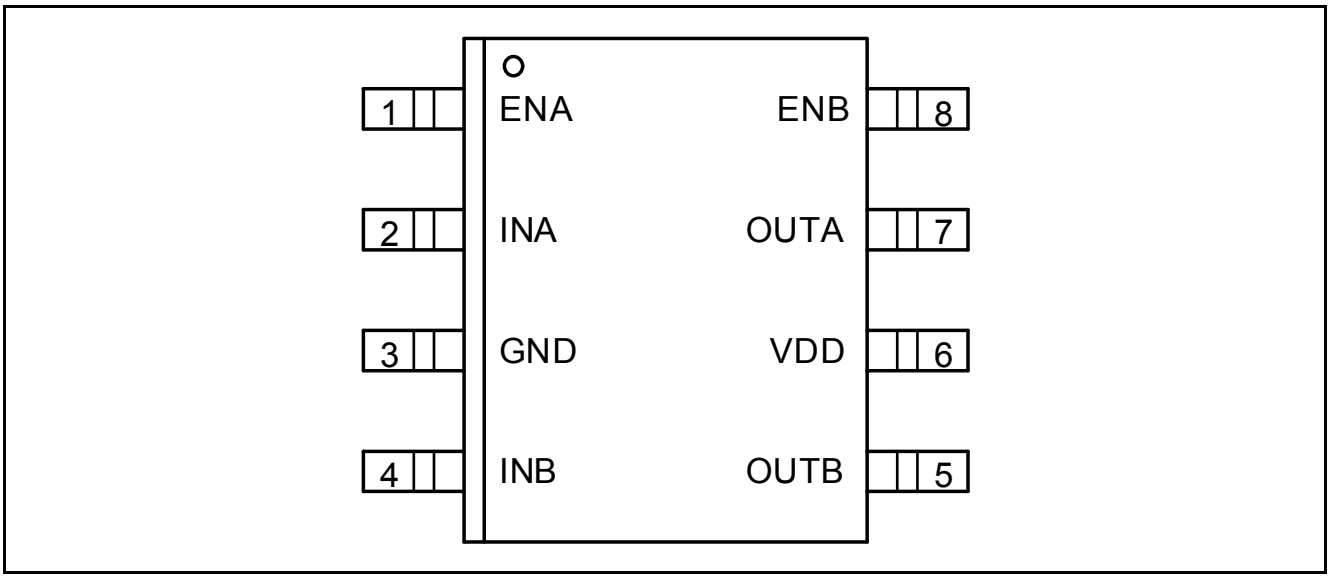


Figure 2-1 Pin Configuration PG-DSO-8, Top View

Table 2-1 Pin Configuration 2EDN7524F and 2EDN7523F in the PG-DSO-8 Package

Pin	Symbol	Description
1	ENA	Enable input channel A Logic input; if ENA is high or left open, OUTA is controlled by INA; ENA low causes OUTA low
2	INA	Input signal channel A Logic input, controlling OUTA (inverting or non-inverting)
3	GND	Ground
4	INB	Input signal channel B Logic input, controlling OUTB (inverting or non-inverting)
5	OUTB	Driver output channel B Low-impedance output with source and sink capability
6	VDD	Positive supply voltage Operating range 4.5 to 20V
7	OUTA	Driver output channel A Low-impedance output with source and sink capability
8	ENB	Enable input channel B Logic Input; if ENA is high or left open, OUTA is controlled by INA; ENA low causes OUTA low

The pin configuration for standard input version of 2EDN7524R, 2EDN8524R, 2EDN7523R and 2EDN8523R in the PG-TSSOP-8 package is shown in **Figure 2-2**.

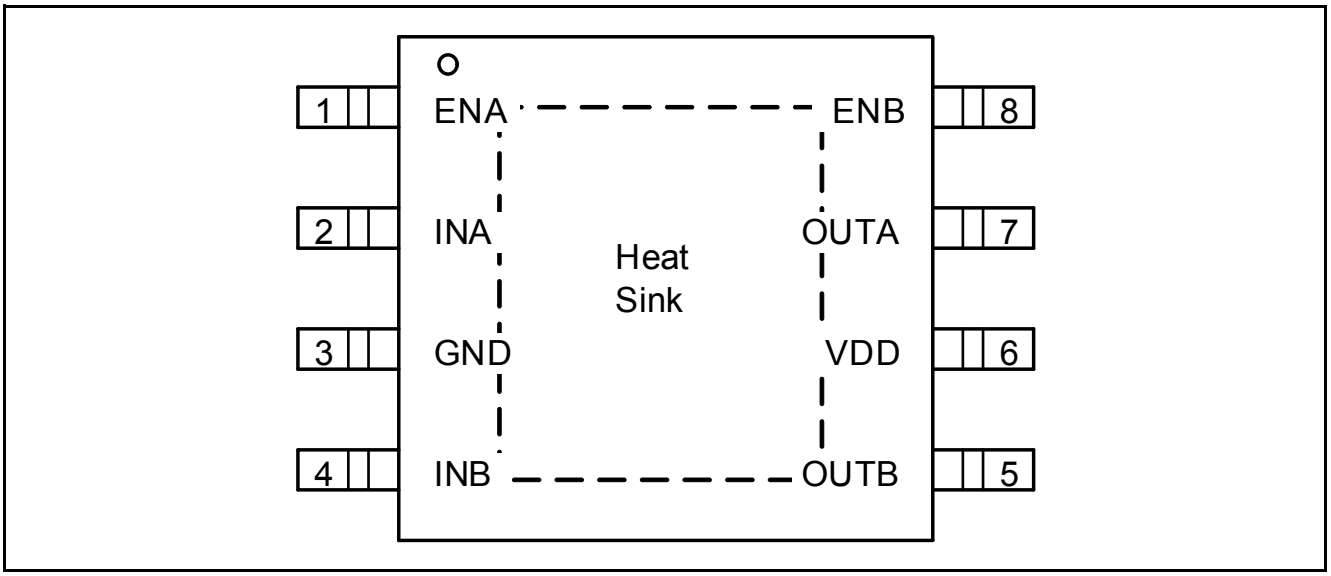


Figure 2-2 Pin Configuration PG-TSSOP-8, Top View

Table 2-2 Pin Configuration 2EDN7524R, 2EDN8524R, 2EDN7523R and 2EDN8523R in the PG-TSSOP-8 Package

Pin	Symbol	Description
1	ENA	Enable input channel A Logic input; if ENA is high or left open, OUTA is controlled by INA; ENA low causes OUTA low
2	INA	Input signal channel A Logic input, controlling OUTA (non-inverting)
3	GND	Ground
4	INB	Input signal channel B Logic input, controlling OUTB (non-inverting)
5	OUTB	Driver output channel B Low-impedance output with source and sink capability
6	VDD	Positive supply voltage Operating range 4.5 to 20V
7	OUTA	Driver output channel A Low-impedance output with source and sink capability
8	ENB	Enable input channel B Logic Input; if ENA is high or left open, OUTA is controlled by INA; ENA low causes OUTA low

Heat sink of PG-TSSOP-8 packages has to be connected to GND pin.

The pin configuration for standard input version of 2EDN7524G and 2EDN7523G. In the PG-WSON-8 package is shown in **Figure 2-3**.

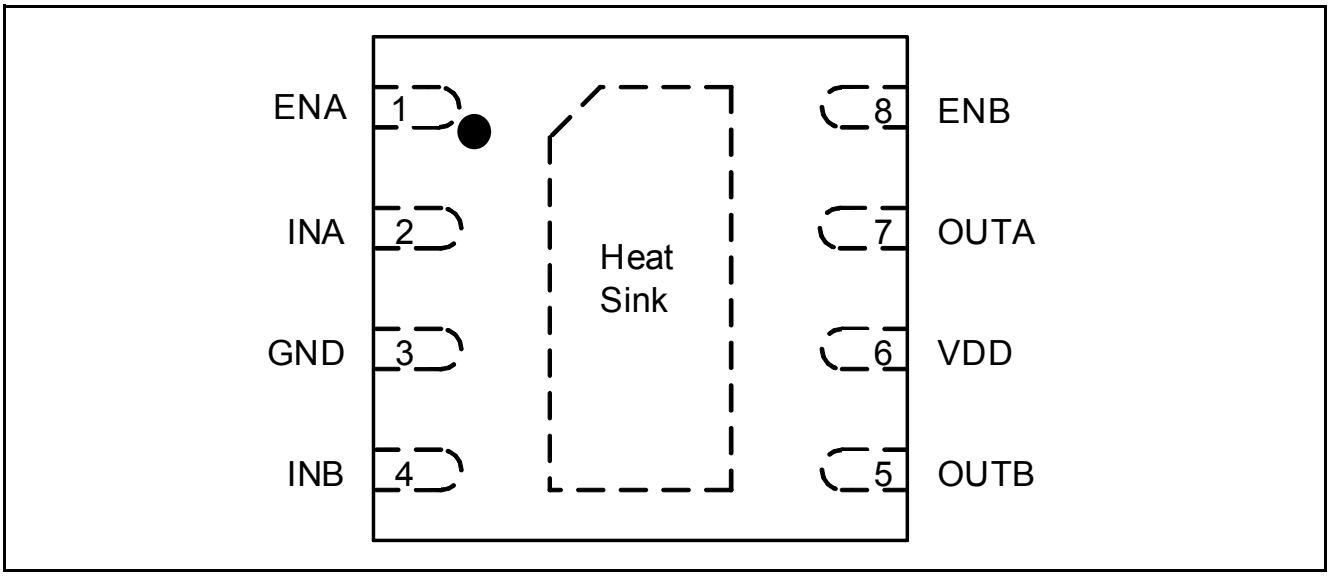


Figure 2-3 Pin Configuration PG-WSON-8, Top View

Table 2-3 Pin Configuration 2EDN7524G and 2EDN7523Gin the PG-WSON-8 Package

Pin	Symbol	Description
1	ENA	Enable input channel A Logic input; if ENA is high or left open, OUTA is controlled by INA; ENA low causes OUTA low
2	INA	Input signal channel A Logic input, controlling OUTA (non-inverting)
3	GND	Ground
4	INB	Input signal channel B Logic input, controlling OUTB (non-inverting)
5	OUTB	Driver output channel B Low-impedance output with source and sink capability
6	VDD	Positive supply voltage Operating range 4.5 to 20V
7	OUTA	Driver output channel A Low-impedance output with source and sink capability
8	ENB	Enable input channel B Logic Input; if ENA is high or left open, OUTA is controlled by INA; ENA low causes OUTA low

Heat sink of PG-WSON-8 packages has to be connected to GND pin.

3 Block Diagram

A simplified functional block diagram for the **non-inverted version** is given in **Figure 3-1**

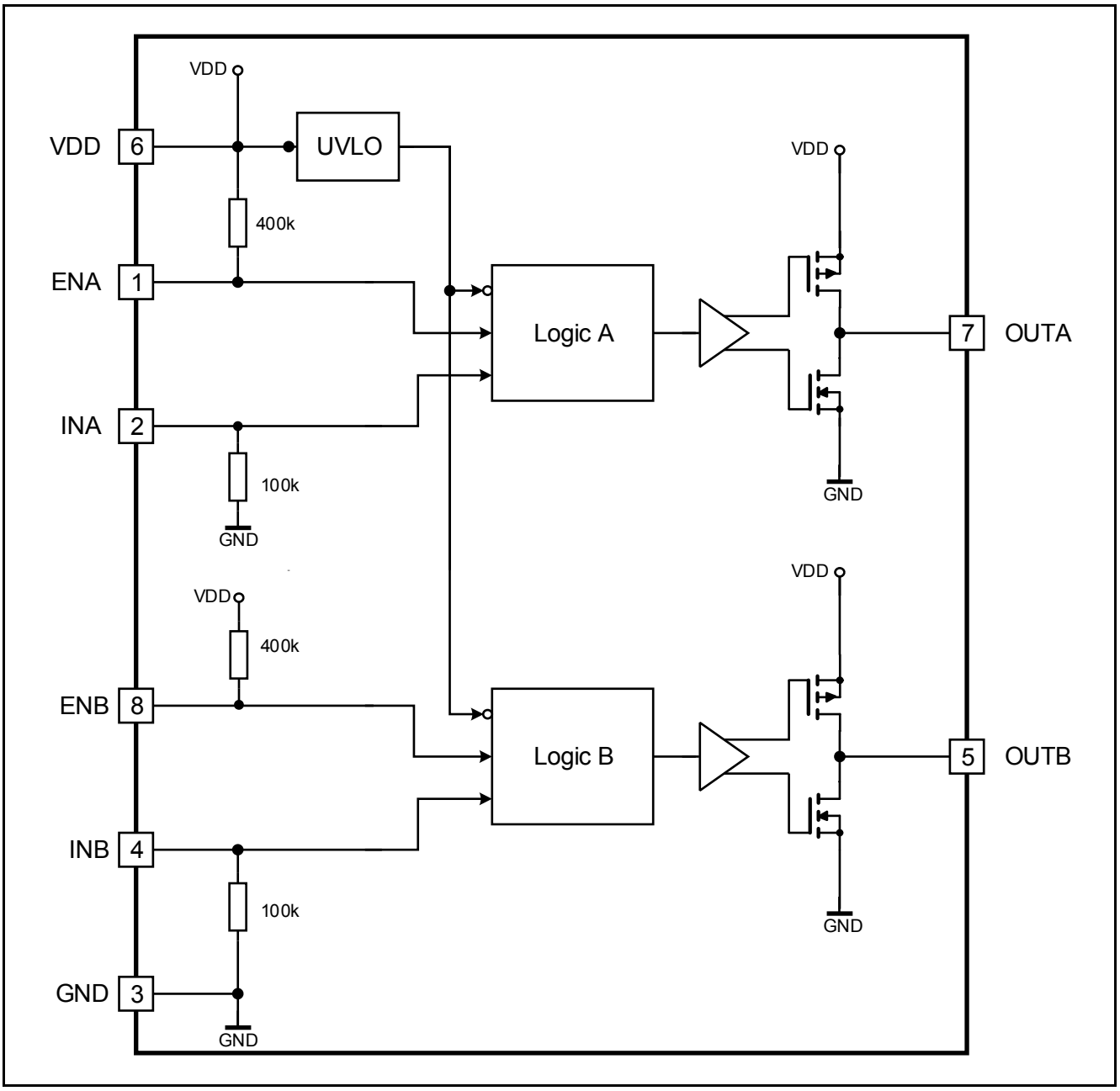


Figure 3-1 Block Diagram, standard input, pull-up/pull-down resistor configuration

Block Diagram

A simplified functional block diagram for the **inverted version** is given in **Figure 3-2**.

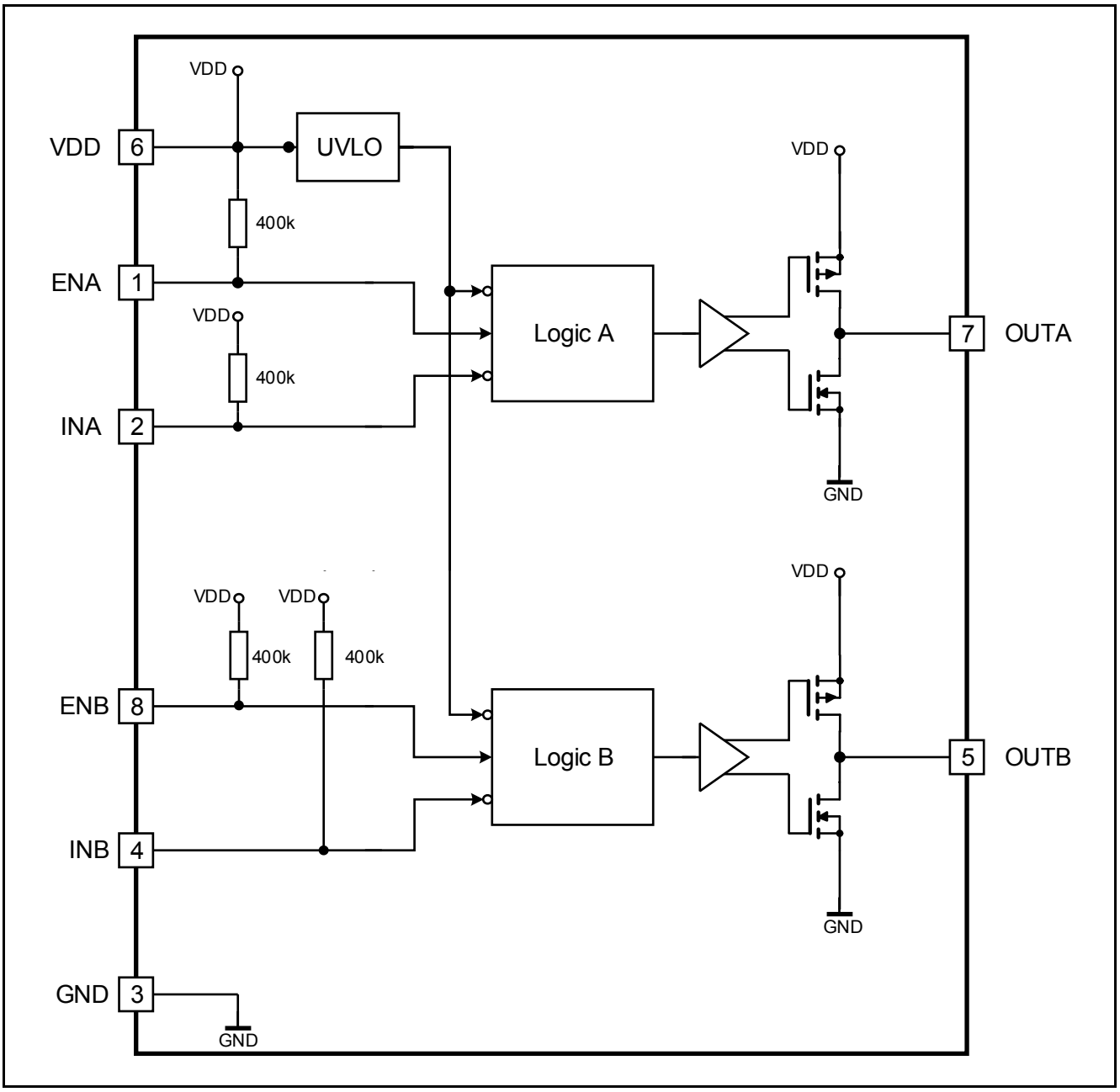


Figure 3-2 Block Diagram, inverting input, pull-up/pull-down resistor configuration

4 Functional Description

4.1 Introduction

The 2EDN752x / 2EDN852x is a fast dual-channel driver for low-side switches. Two true rail-to-rail output stages with very low output impedance and high current capability are chosen to ensure highest flexibility and cover a high variety of applications.

The focus on robustness at input and output side gives this device even a safety margin on critical abnormal situations. An extended negative voltage range protects input pins against ground shifts. No current flows over the ESD structure of the IC during a negative input level. All outputs are robust against reverse current. The interaction with the power MOSFET, even reverse reflected power can be covered by the strong internal output stage.

All inputs are compatible with LVTTL signal levels. The threshold voltages with a typical hysteresis of 1V are kept constant over the supply voltage range.

Since the 2EDN752x / 2EDN852x aims particularly at fast-switching applications, signal delays and rise/fall times have been minimized. Special effort has been made towards minimizing delay differences between the 2 channels to very low values of typically 1ns.

4.2 Supply Voltage

The maximum supply voltage is 20V. This high voltage can be valuable in order to exploit the full current capability of 2EDN752x / 2EDN852x when driving very large MOSFETs. The minimum operating supply voltage is set by the undervoltage lockout function to a typical default value of 4.2V or of 8V. This lockout function protects power MOSFET from running into linear mode with high power dissipation.

4.3 Input Configurations

As described in **Chapter 1**, 2EDN752x / 2EDN852x is available in 2 different configurations with respect to the logic configuration of the 4 input pins (input plus enable).

The enable inputs are internally pulled up to a logic high voltage, i.e. the driver is enabled with these pins left open. The standard PWM inputs are internally pulled down to a logic low voltage. This prevents a switch-on event during power up and a not driven input condition. Version with inverted PWM input have a internal pull up resistor to prevent unwanted switch-on.

All inputs are compatible with LVTTL levels and provide a hysteresis of 1V typ. It is independent of the supply voltage.

All input pins have a negative extended voltage range. This prevents cross current over single wires during GND shifts between signal source (controller) and driver input.

4.4 Driver Outputs

The two rail-to-rail output stages realized with complementary MOS transistors are able to provide a typical 5A of sourcing and sinking current. This output stage has a shoot through protection and current limiting behavior. The on-resistance is very low with a typical value below 0.7 Ω for the sourcing p-channel MOS and 0.5 Ω for the sinking n-channel MOS transistor. The use of a p-channel sourcing transistor is crucial for achieving real rail-to-rail behaviour and not suffering from a source follower's voltage drop.

Gate Drive Outputs held active low in case of floating inputs ENx, INx or during startup or power down once UVLO is not exceeded. Under any situation, startup, UVLO or shutdown, outputs are held under defined conditions.

4.5 Undervoltage Lockout (UVLO)

The Undervoltage Lockout function ensures that the output can be switched to its high level only, if the supply voltage exceeds the UVLO threshold voltage. Thus it can be guaranteed, that the switch transistor is not operated if the driving voltage is too low to completely switch it on, thereby avoiding excessive power dissipation.

The default UVLO level is set to a typical value of 4.2V / 8V (with some hysteresis). UVLO of 4.2V is normally used for low voltage and TTL based MOSFETs. For higher level, like high voltage super junction MOSFETS, an active voltage of minimum 8V version is available.

5 Characteristics

The absolute maximum ratings are listed in **Table 5-1**. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Positive supply voltage	V_{VDD}	-0.3		22	V	
Voltage at pins INA, INB, ENA, ENB	V_{IN}	-10		22	V	
Voltage at pins OUTA, OUTB	V_{OUT}	-0.3		V_{VDD}+0.3	V	Note[1)]
Reverse current peak at pins OUTA, OUTB	I_{SNK_rev} I_{SRC_rev}			-5 5	A_{pk}	< 500ns[2)]
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_S	-55		150	°C	
ESD capability	V_{ESD}			1.5	kV	Charged Device Mode (CDM) [3)]
				2.5	kV	Human Body Model (HBM) [4)]

1) Voltage spikes resulting from reverse current peaks are allowed.

2) I_{SNK_rev} < -2A or I_{SRC_rev} > 2 A may reduce life time; No limitation by design; Parameter verified by design, not 100% tested in production; max. power dissipation must be observed (see **Figure 7-8**)

3) According to JESD22-C101

4) According to JESD22-A114

5.2 Thermal Characteristics

Table 5-2 Thermal Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction-ambient [1)]	R_{thJA25}		125		K/W	PG-DSO-8, T_{amb}=25°C
Thermal resistance junction-case (top) [2)]	R_{thJC25}		66		K/W	PG-DSO-8, T_{amb}=25°C
Thermal resistance junction-board [3)]	R_{thJB25}		62		K/W	PG-DSO-8, T_{amb}=25°C
Characterization parameter junction-top [4)]	Ψ_{thJC25}		16		K/W	PG-DSO-8, T_{amb}=25°C

Table 5-2 Thermal Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Characterization parameter junction-board [5]	Ψ_{thJB25}		55		K/W	PG-DSO-8, T_{amb}=25°C
Thermal resistance junction-ambient [1]	R_{thJA25}		64		K/W	PG-TSSOP-8, T_{amb}=25°C
Thermal resistance junction-case (top) [2]	R_{thJP25}		56		K/W	PG-TSSOP-8, T_{amb}=25°C
Thermal resistance junction-board [3]	R_{thJB25}		55		K/W	PG-TSSOP-8, T_{amb}=25°C
Characterization parameter junction-top [4]	Ψ_{thJC25}		9		K/W	PG-TSSOP-8, T_{amb}=25°C
Characterization parameter junction-board [5]	Ψ_{thJB25}		13		K/W	PG-TSSOP-8, T_{amb}=25°C
Thermal resistance junction-ambient [1]	R_{thJA25}		61		K/W	PG-WSON-8, T_{amb}=25°C
Thermal resistance junction-case (top) [2]	R_{thJP25}		54		K/W	PG-WSON-8, T_{amb}=25°C
Thermal resistance junction-board [3]	R_{thJB25}		52		K/W	PG-WSON-8, T_{amb}=25°C
Characterization parameter junction-top [4]	Ψ_{thJC25}		8		K/W	PG-WSON-8, T_{amb}=25°C
Characterization parameter junction-board [5]	Ψ_{thJB25}		11		K/W	PG-WSON-8, T_{amb}=25°C

1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

4) The characterization parameter junction-top, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining R_{th}, using a procedure described in JESD51-2a (sections 6 and 7).

5) The characterization parameter junction-board, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining R_{th}, using a procedure described in JESD51-2a (sections 6 and 7).

5.3 Operating Range

Table 5-3 Operating Range

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{VDD}	4.5		20	V	Min defined by UVLO
Logic input voltage	V_{IN}	-5		20	V	
Junction temperature	T_J	-40		150	°C	1)

1) Continuous operation above 125 °C may reduce life time.

5.4 Electrical Characteristics

Unless otherwise noted, min./max. values of characteristics are the lower and upper limits respectively. They are valid within the full operating range. The supply voltage is V_{VDD}= 12 V. Typical values are given at T_J=25°C.

Table 5-4 Power Supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VDD quiescent current	I_{VDDqu1}	0.5	0.7	1.2	mA	OUT = high, V_{VDD}= 12 V
VDD quiescent current	I_{VDDqu2}	0.3	0.48	0.7	mA	OUT = low, V_{VDD}= 12 V

Table 5-5 Undervoltage Lockout Standard MOSFET Version

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold	$UVLO_{on}$	3.9	4.2	4.5	V	
Undervoltage Lockout (UVLO) turn off threshold	$UVLO_{off}$	3.6	3.9	4.2	V	
UVLO threshold hysteresis	$UVLO_{hys}$		0.3		V	

Table 5-6 Undervoltage Lockout Superjunction MOSFET Version

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold	$UVLO_{on}$	7.4	8.0	8.6	V	
Undervoltage Lockout (UVLO) turn off threshold	$UVLO_{off}$	6.5	7.0	7.5	V	
UVLO threshold hysteresis	$UVLO_{hys}$	—	1.0	—	V	

Table 5-7 Logic Inputs INA, INB, ENA, ENB

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	V_{INH}	1.9	2.1	2.3	V	
Input voltage threshold for transition HL	V_{INL}	0.8	1.0	1.2	V	
Input pull up resistor[1)]	$R_{IN\ H}$		400		kΩ	
Input pull down resistor[2)]	$R_{IN\ L}$		100		kΩ	

1) Inputs with initial high logic level
2) Inputs with initial low logic level

Table 5-8 Static Output Caracteristics (see Figure 6-2)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High Level (Sourcing) Output Resistance	R_{on_SNK}	0.35	0.7	1.2	Ω	I_{SNK} = 50mA
High Level (Sourcing) Output Current	I_{SNK_peak}		5.0	1)	A	
Low Level (Sinking) Output Resistance	R_{on_SRC}	0.28	0.55	1.0	Ω	I_{SRC} = 50mA
High Level (Sinking) Output Current	I_{SRC_Peak}		-5.0	2)	A	

1) Active limited by design at apox. 6.5A_{pk}, parameter is not subject to production test - verified by design / characterization, max. power dissipation must be observed
2) Active limited by design at apox. -6.5A_{pk}, parameter is not subject to production test - verified by design / characterization, max. power dissipation must be observed

Table 5-9 Dynamic Characteristics (see Figure 6-1, Figure 6-2, Figure 6-3 and Figure 6-4)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input/Enable to output propagation delay	T_{PDON}	15	19	25	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Input/Enable to output propagation delay	T_{PDOFF}	15	19	25	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Input/Enable to output propagation delay mismatch between channels	Dt_{PD}		1	4	ns	
Rise Time	T_{RISE}	—	5.3	10[1)]	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Fall Time	T_{FAll}	—	4.5	10[1)]	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Minimum input pulse width that changes output state	T_{PW}	—	10	20	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V

1) Parameter verified by design, not 100% tested in production.

6 Timing Diagrams

Figure 6-1 shows the definition of rise, fall and delay times for the inputs of the non-inverting version (with Enable pin high or open).

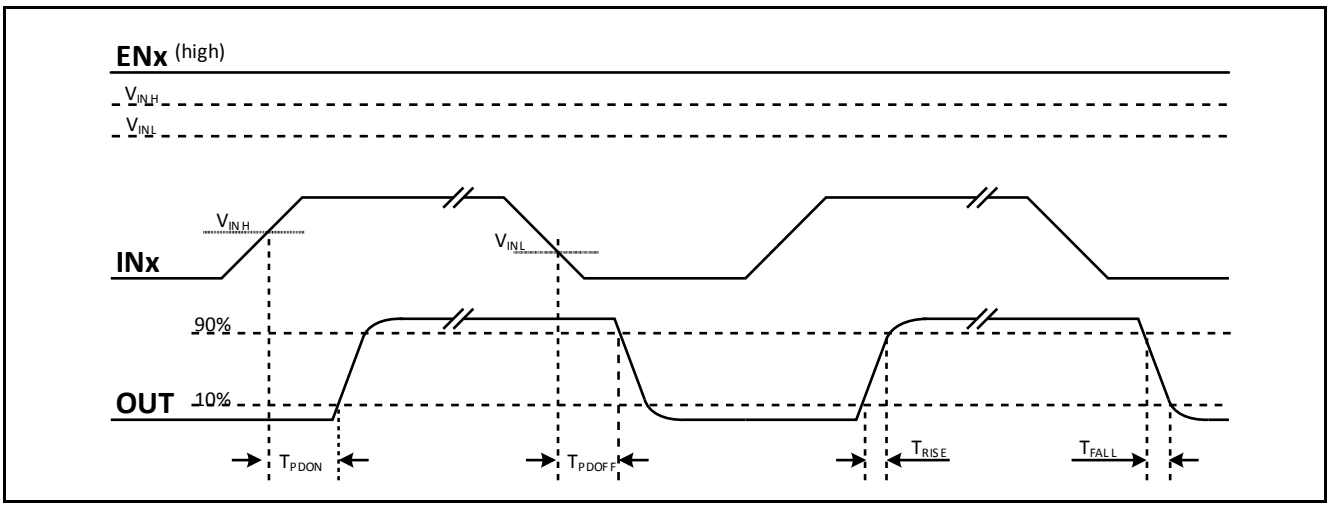


Figure 6-1 Propagation delay, rise and fall time, non-inverted

Figure 6-2 shows the definition of rise, fall and delay times for the inputs of the inverting version (with enable pins high or open).

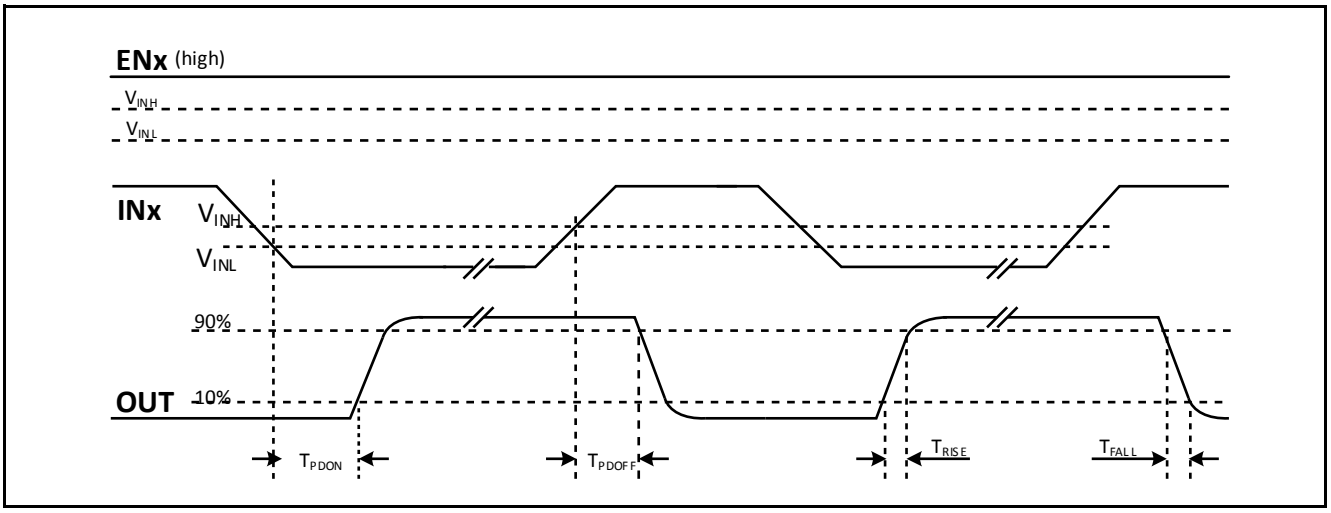


Figure 6-2 Propagation delay, rise and fall Time, inverted

Figure 6-3 illustrates the undervoltage lockout function.

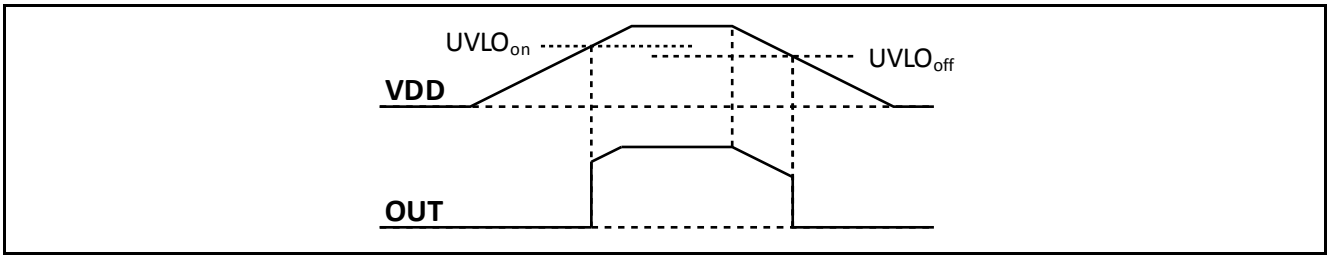


Figure 6-3 UVLO behaviour, input ENx and INx drives OUT normally high

Figure 6-4 illustrates the minimum input pulse width that changes output state.

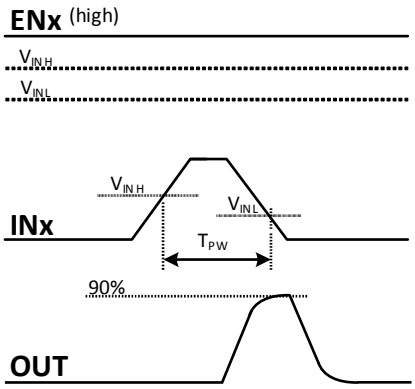


Figure 6-4 T_{PW}, minimum input pulse width that changes output state

7 Typical Characteristics

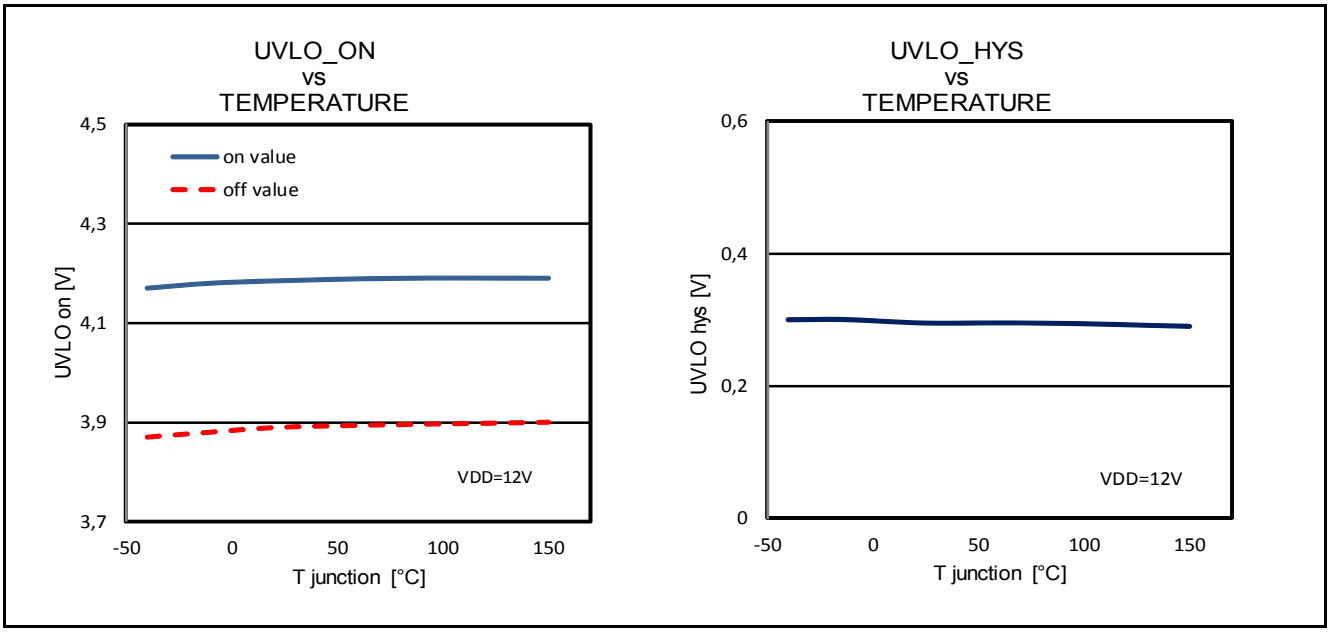


Figure 7-1 Undervoltage lockout

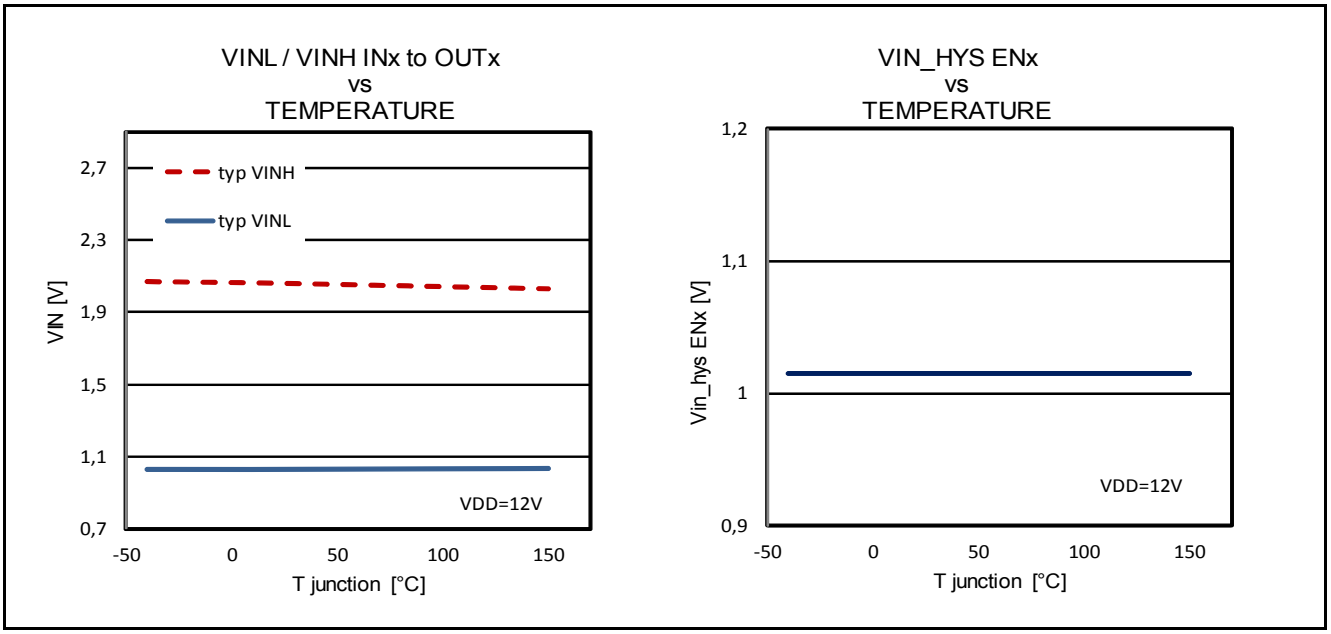


Figure 7-2 Input (INx) characteristic

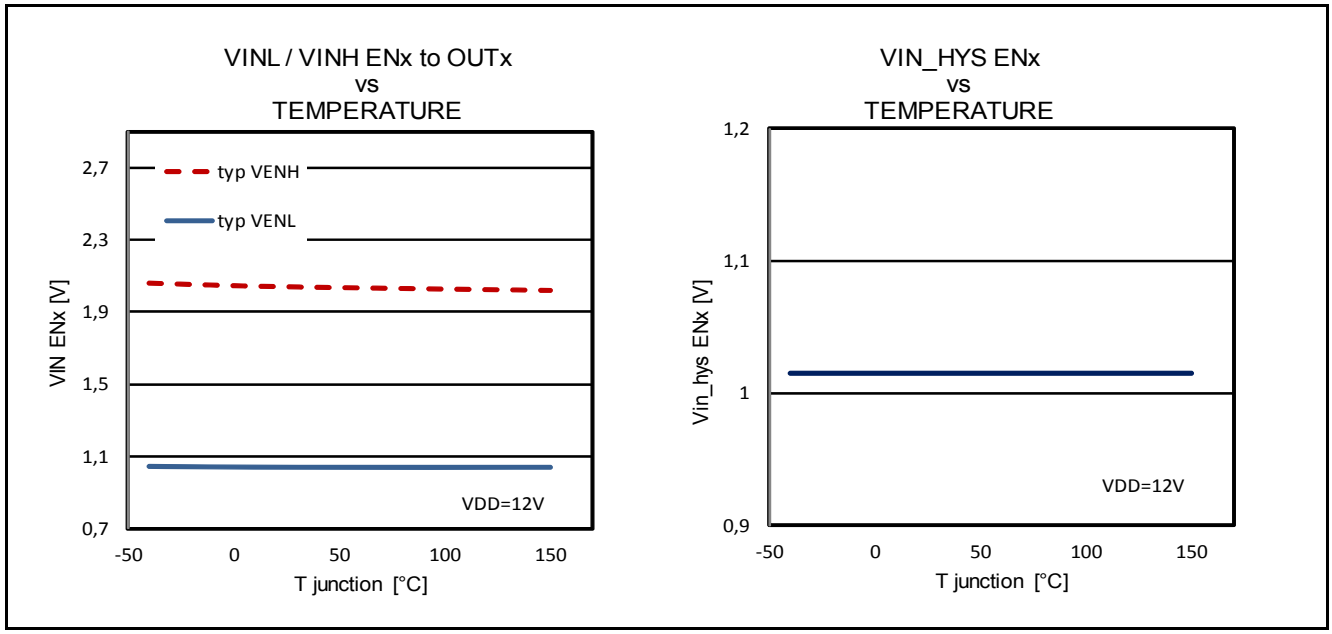


Figure 7-3 Input (ENx) characteristic

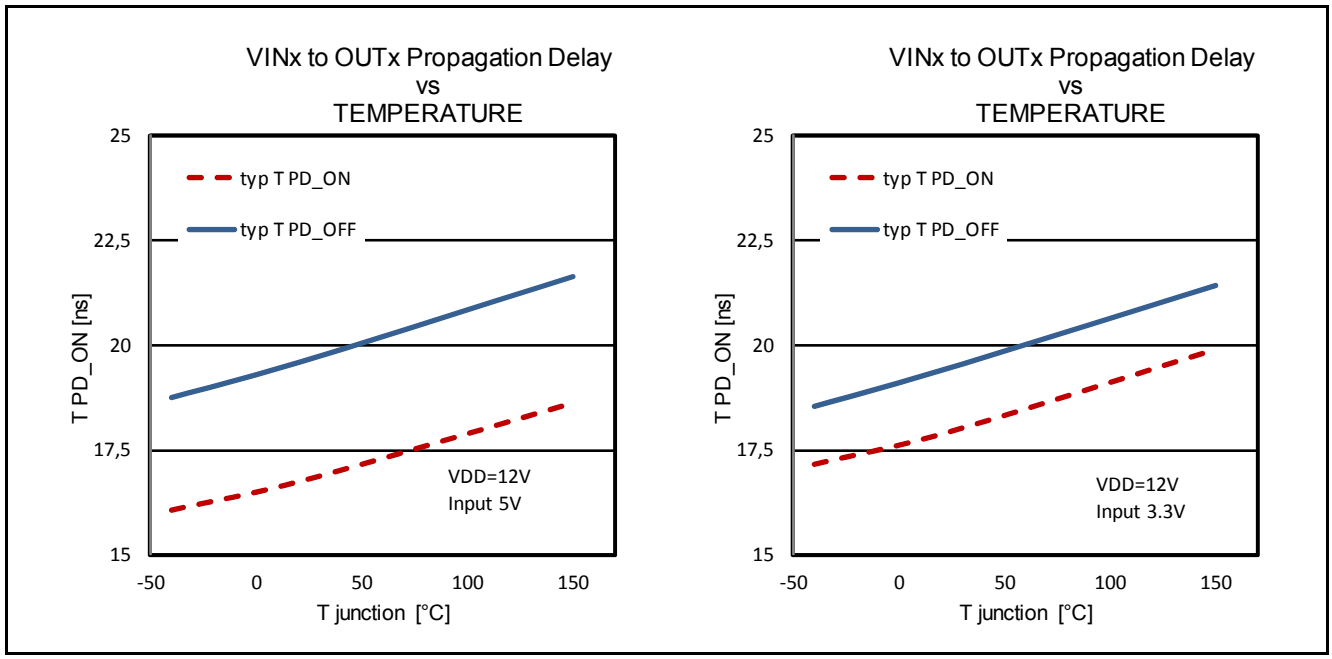


Figure 7-4 Propagation delay (INx) on different input logic levels (see Figure 6-1)

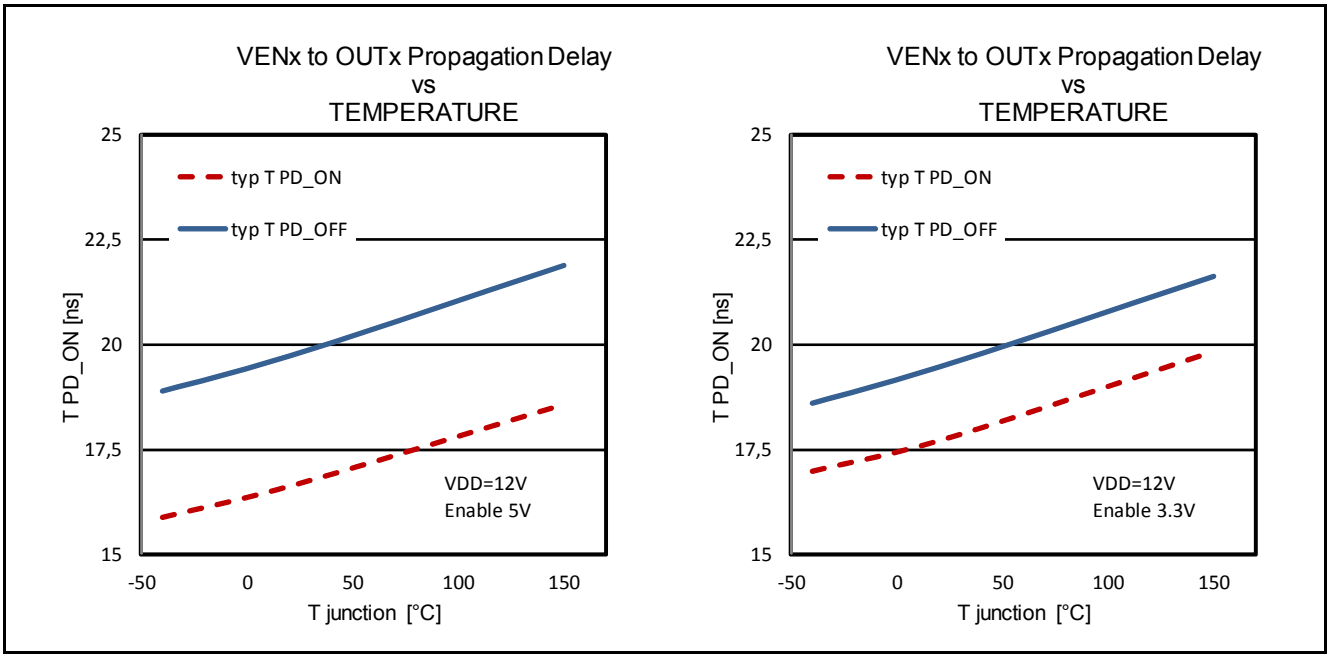


Figure 7-5 Propagation delay (ENx) on different input logic levels (see Figure 6-1)

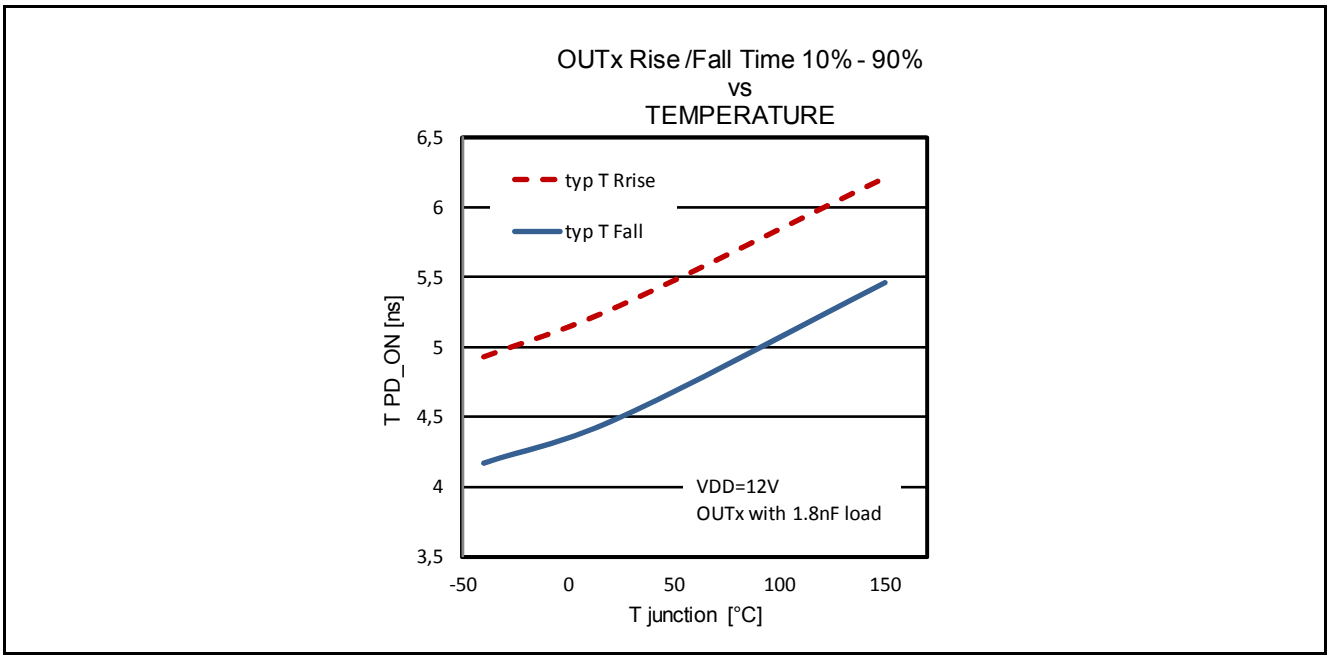


Figure 7-6 Rise / fall times with load on output (see Figure 6-1)

Typical Characteristics

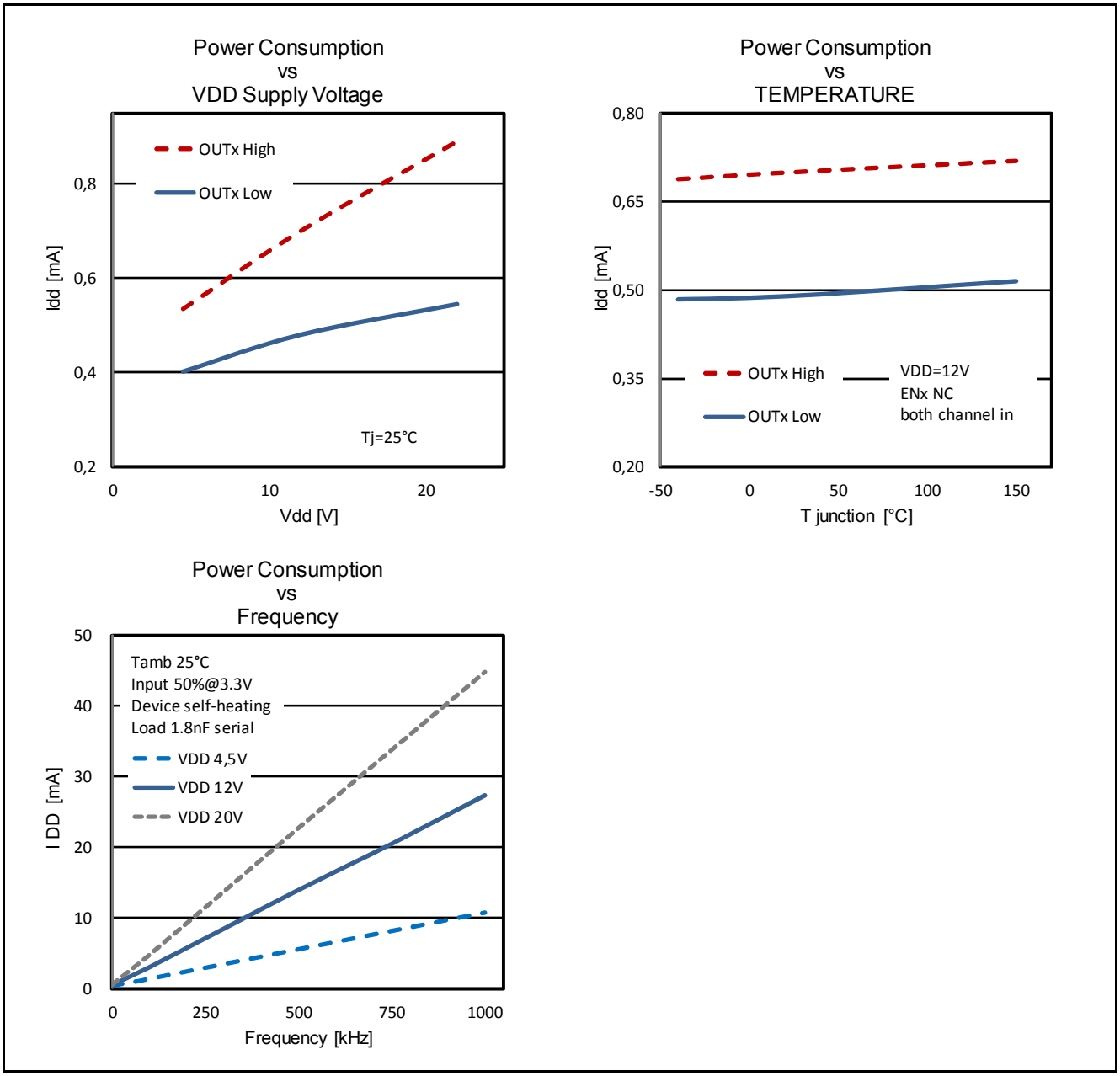


Figure 7-7 Power consumption related to temperature, supply voltage and frequency

Typical Characteristics

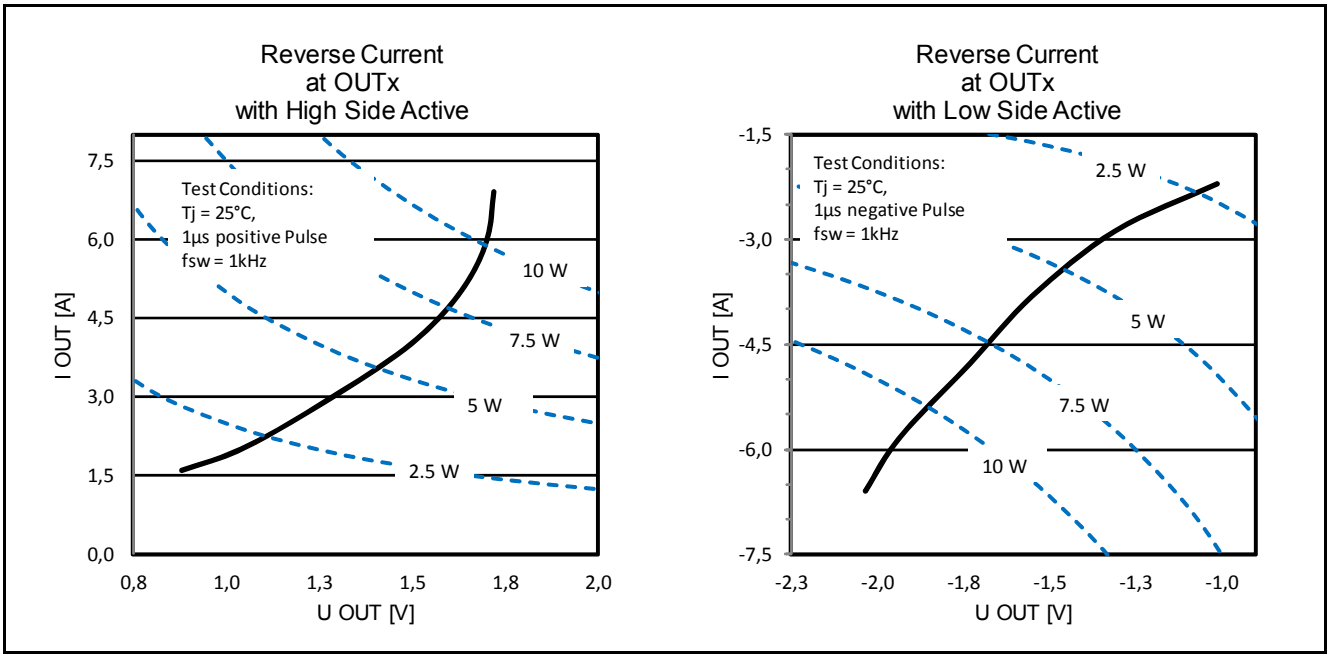
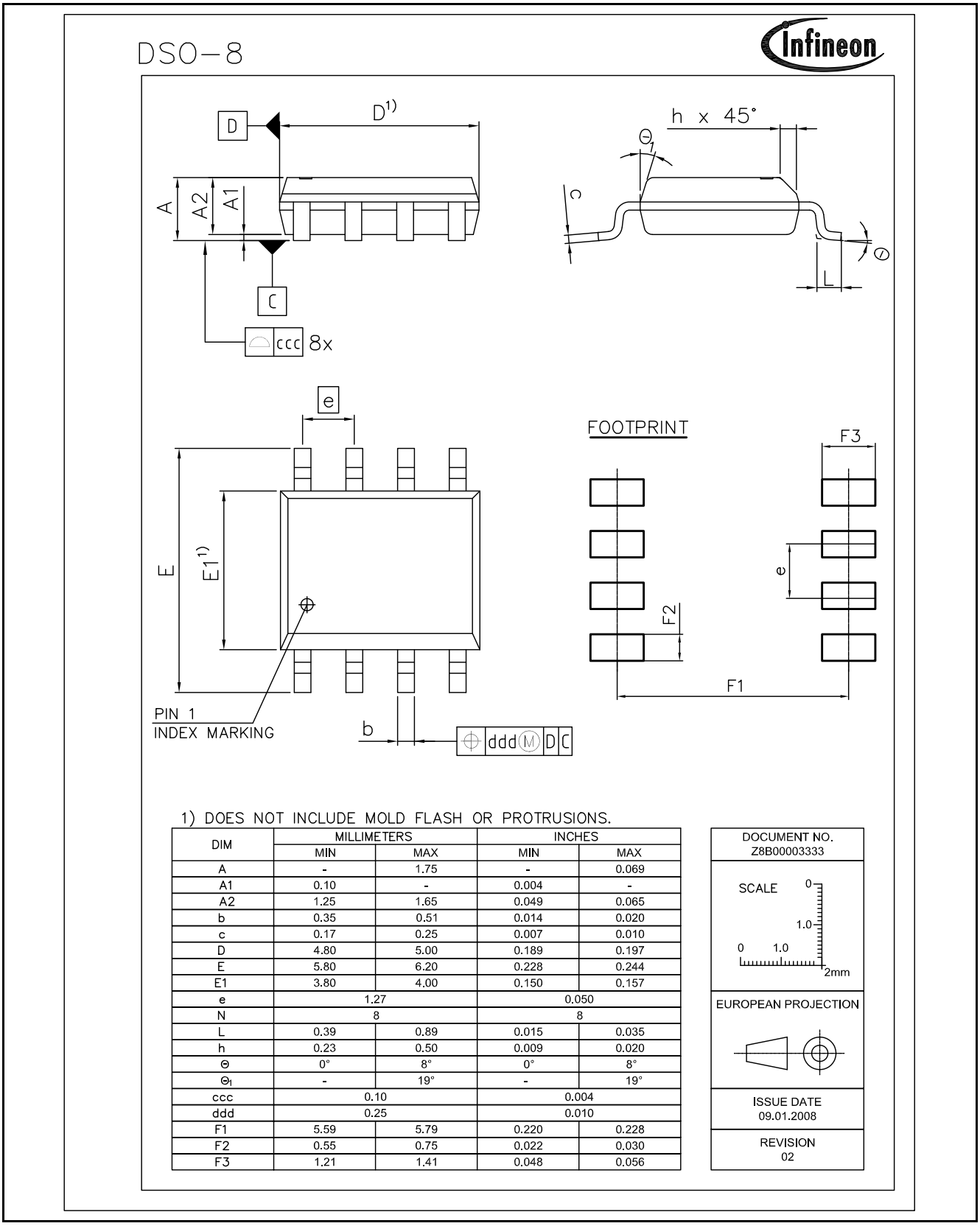


Figure 7-8 Output OUTx with reverse current and resulting power dissipation

8 Outline Dimensions



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ1	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

DOCUMENT NO.
Z8B00003333

SCALE 0 1.0 0 1.0 2mm

EUROPEAN PROJECTION

ISSUE DATE
09.01.2008

REVISION
02

Figure 8-1 PG-DSO-8

Outline Dimensions

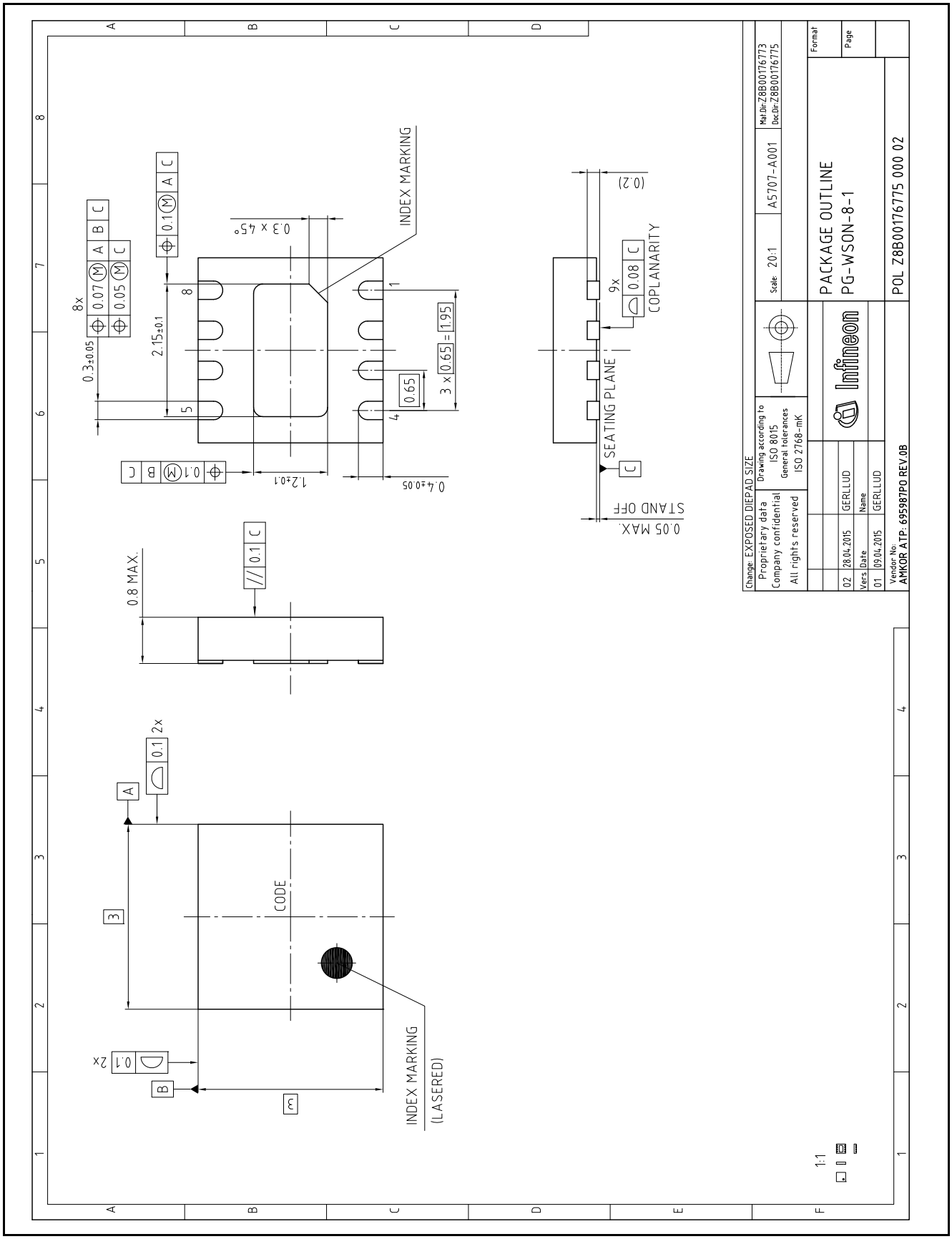


Figure 8-2 PG-TSSOP-8 (see notes)

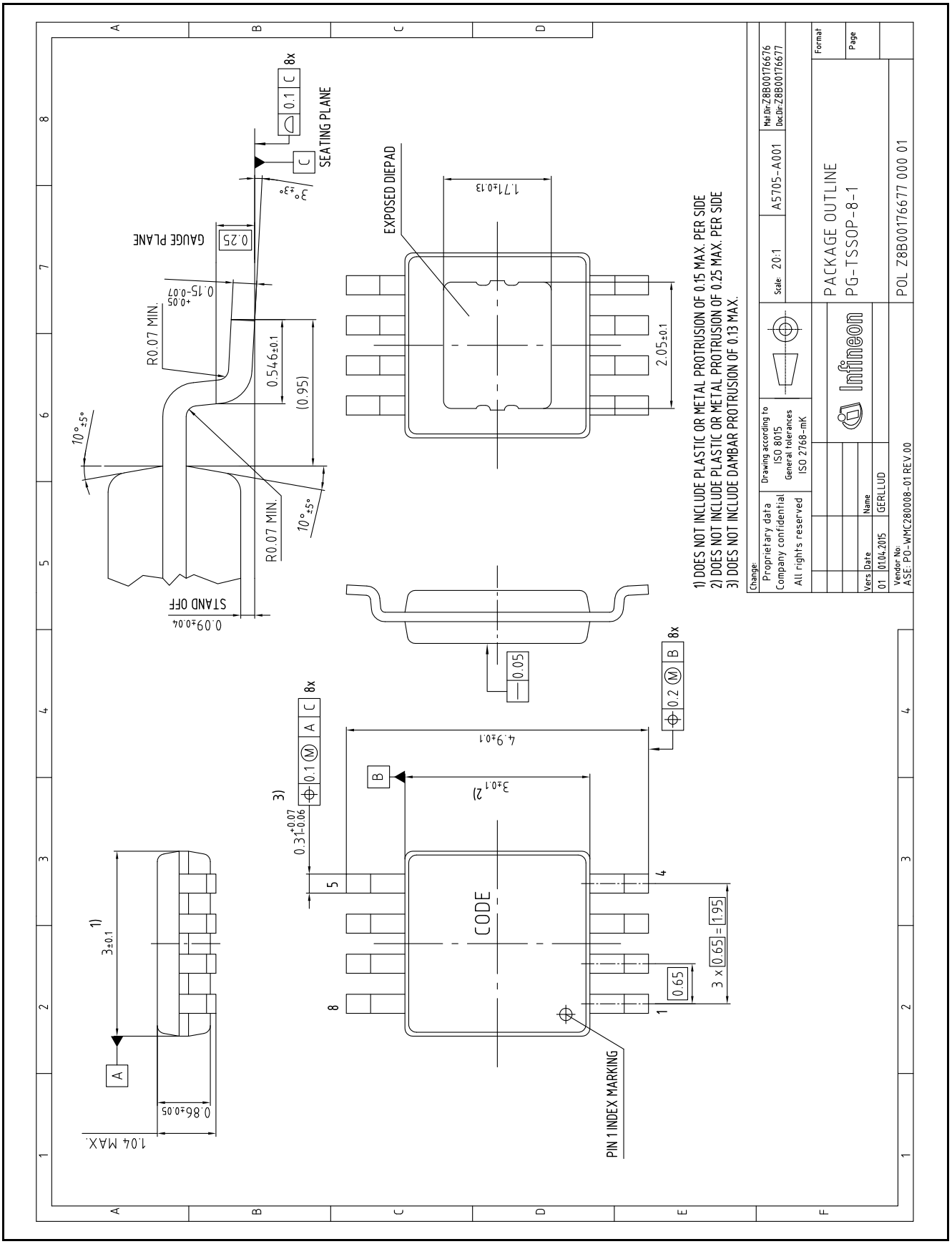


Figure 8-3 PG-TSSOP-8

Outline Dimensions

Notes

1. *For further information on package types, recommendation for board assembly, please go to: http://www.infineon.com/cms/en/product/technology/packages/.*

www.infineon.com

Edition 2015-07-22
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about any aspect of this document?
Email: erratum@infineon.com

Document reference
Doc_Number

Legal Disclaimer
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information
For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings
Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office. Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.