TS1110 Electronic Circuit Breaker and TS1107 Current Limiter User's Guide

The TS1110 combines a very low power bidirectional current-sense amplifier (CSA) with a circuit breaker feature. The circuit breaker feature is supplied within the TS1110 as an FET control that drives the gate drive of an external P-channel MOSFET, disconnecting the load from the power supply. The TS1110 provides a comparator that can be used for current limit detection with a latch-capable output. A digital SIGN output that indicates the direction of current flow depending on the external connections to the RS+ and RS– input terminals is also provided. The TS1110 requires a very low 0.68 µA CSA and 1.16 µA VDD supply current while combining a 150 µV(MAX) input offset voltage with a 0.6% gain error (MAX) for high-precision current measurements. The TS1110 provides a buffered CSA output, which can be connected with an RC Filter to reduce noise.

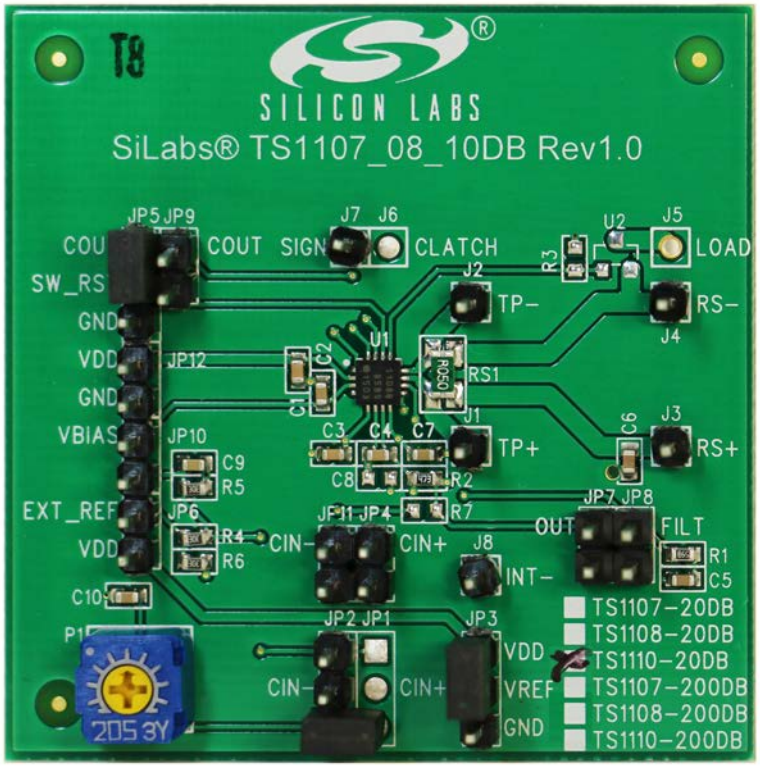
The TS1107 Current Limiter is a subset of the TS1110 Electronic Circuit Breaker and provides the same functionality minus the load disconnect feature. The TS1107 combines the very low power bidirectional current-sense amplifier (CSA) with a latch-capable current limiter comparator featuring an adjustable current threshold. The TS1107's CSA buffered output plus the current limiter comparator require a very low nominal supply current of 1.15 µA.

KEY FEATURES

- R_{SENSE}: 50 mΩ ± 0.5%
- External Circuit Breaker PMOS Included
- Adjustable Reference for Current Limiter
- Compatible for Both Gain Options
  - 20 V/V
  - 200 V/V

ORDERING INFORMATION

- TS1110-20DB
- TS1110-200DB
- TS1107-20DB
- TS1107-200DB



1. TS1110-EVB Description

The TS1110 Evaluation Board is intended for evaluating the circuit breaker feature of the TS1110. The evaluation board includes a variable reference scheme so that the threshold for the current limit comparator can be adjusted. The jumper, JP1, can be connected so that the included potentiometer can be used to adjust the threshold. A P-channel MOSFET is included, enabling the circuit breaker feature. When CLATCH is tied HIGH, the current limit comparator's output, COUT, indicates when the load has exceeded the current limit threshold and has thus been disconnected from the power supply. The Quick Start Procedure details two different load connections. The first load connection corresponds to a load under the current limiter's threshold, while the second load connection results in the current limiter's output enabling the circuit breaker.

Table 1.1. Component List

Designation	Quantity	Description
U1	1	TS1110-20, TS1110-200
U2	1	DMP2066LSN-7
RS1	1	50 mΩ ± 0.5%, 1/2 W (1206)
C1, C6	2	1 µF ± 10%, 10 V (0603)
C2, C7, C9, C10	4	0.1 µF ± 10%, 10 V (0603)
C5	1	0.47 µF ± 10%, 10 V (0603)
C8	1	1 nF ± 10%, 25 V (0603)
R1	1	4.02 kΩ ± 1%, 1/16 W (0603)
R3	1	1 MΩ ±1%, 1/16 W (0603)
R4, R5, R6	3	2 MΩ ±1%, 1/10 W (0603)
R7	1	0 Ω, 1 A (0603)
J1, J2, J3, J4, J5, J6, J7	7	Header 1x1
JP1, JP3	2	Header 1x3
JP4, JP6, JP7, JP8, JP9, JP10, JP11, JP12	8	Jumper
JS1, JS4	2	Jumper Shunt

2. TS1110-EVB Quick Start Procedure

Required Equipment

- 3 V Power Supply or 3 V Battery
- 2 Digital Multimeters
- 1 Potentiometer

To use the TS1110 evaluation board, perform the following steps:

1. Configure JP3 so that the Jumper Shunt is connecting VDD to VREF. Configure JP1 so that the Jumper Shunt is connecting CIN+ to the bottom header.
2. Connect a Jumper Shunt so that EXT_REF is connected to VDD.
3. Connect CLATCH to GND.
4. Connect the 3 V power source to RS+ and VDD.
5. Use a voltmeter to measure the V_{BIAS} and the CIN+ voltage. V_{BIAS} should be 50% of VDD, 1.5 V. CIN+ should be 40% of VDD, 1.2 V. The P1 potentiometer can be adjusted so that the CIN+ voltage can be increased or decreased.
6. Once CIN+ and V_{BIAS} voltages are confirmed, connect CLATCH to VDD.
7. Connect a voltmeter to measure V_{OUT}. With no load connected V_{OUT} should be equal to V_{BIAS}. The expression for the V_{OUT} output voltage is defined by:

$$V_{OUT} = V_{BIAS} - (GAIN \times I_{SENSE} \times R_{SENSE})$$

8. Connect a voltmeter to measure COUT. COUT should be LOW.
9. Connect an ammeter in series from LOAD to a potentiometer. Adjust the POT until the ammeter reads:
   - TS1110-20: 200 mA
   - TS1110-200: 20 mA

   V_{OUT} should equal 1.3 V and COUT should be LOW.
10. To enable the circuit breaker, adjust the LOAD POT until the ammeter reads a value greater than:
    - TS1110-20: 300 mA
    - TS1110-200: 30 mA

    Once COUT transitions to HIGH, V_{OUT} should read 1.5V and the ammeter measurement should read 0mA signaling that the P-channel FET has disconnected the load from the power supply.

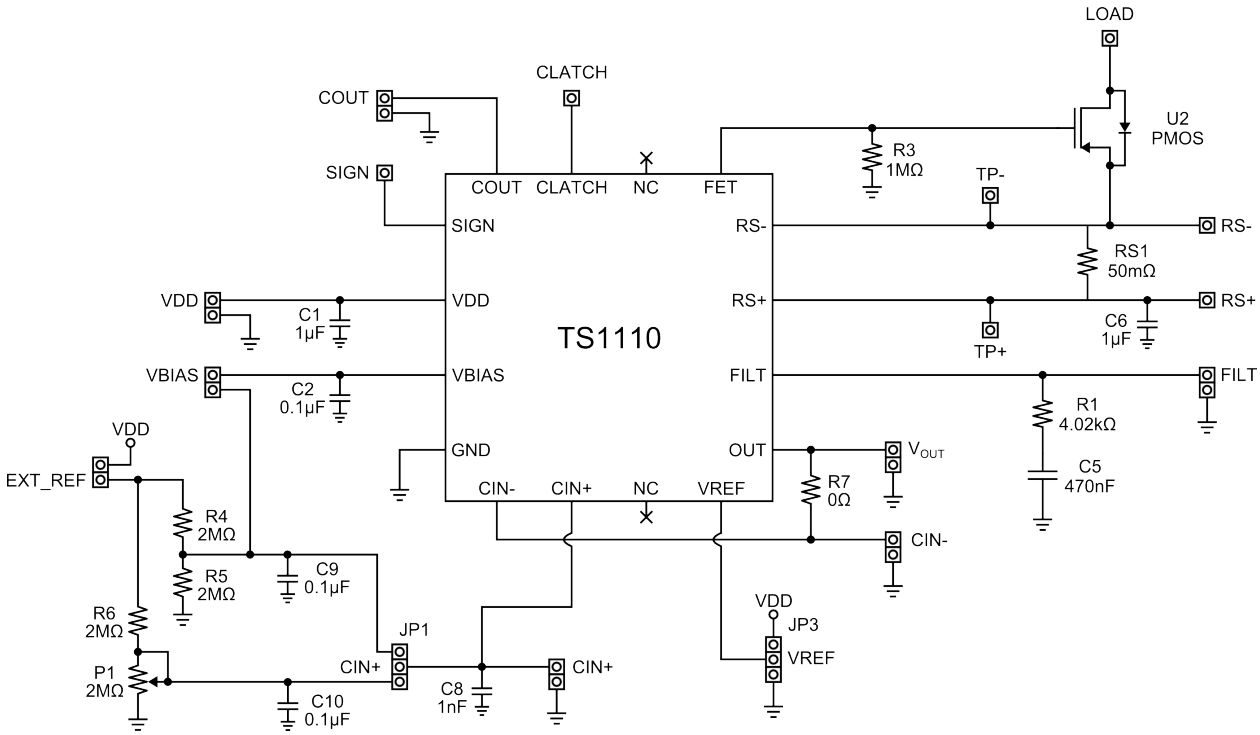


Figure 2.1. TS1110DB Circuit Schematic

3. TS1107-EVB Description

The TS1107 Evaluation Board is intended for evaluating the current limit detection feature of the TS1107. The evaluation board includes a variable reference scheme so that the threshold for the current limit comparator can be adjusted. The jumper, JP1, can be connected so that the included potentiometer can be used to adjust the threshold. When CLATCH is tied HIGH, the current limit comparator's output, COUT, indicates when the load has exceeded the current limit threshold and latches HIGH until the fault condition has been removed and the comparator has been reset. The Quick Start Procedure details two different load connections. The first load connection corresponds to a load under the current limiter's threshold, while the second load connection results in fault condition resulting in COUT latching HIGH.

Table 3.1. Component List

Designation	Quantity	Description
U1	1	TS1107-20, TS1107-200
RS1	1	50 mΩ ±0.5%, 1/2 W (1206)
C1, C6	2	1 µF ± 10%, 10 V (0603)
C2, C7, C9, C10	4	0.1 µF ± 10%, 10 V (0603)
C5	1	0.47 µF ± 10%, 10 V (0603)
C8	1	1 nF ± 10%, 25 V (0603)
R1	1	4.02 kΩ ± 1%, 1/16 W (0603)
R4, R5, R6	3	2 MΩ ± 1%, 1/10 W (0603)
R7	1	0 Ω, 1 A (0603)
J1, J2, J3, J4, J5, J6, J7	7	Header 1x1
JP1, JP3	2	Header 1x3
JP4, JP6, JP7, JP8, JP9, JP10, JP11, JP12	8	Jumper
JS1, JS4	2	Jumper Shunt

4. TS1107-EVB Quick Start Procedure

Required Equipment

- 3 V Power Supply or 3 V Battery
- 2 Digital Multimeters
  - 1 ammeter
  - 1 voltmeter
- Potentiometer

To use the TS1107 evaluation board, perform the following steps:

1. Configure JP3 so that the Jumper Shunt is connecting VDD to VREF. Configure JP1 so that the Jumper Shunt is connecting CIN+ to the bottom header.
2. Connect a Jumper Shunt so that EXT_REF is connected to VDD.
3. Connect CLATCH to GND.
4. Connect the 3 V power source to RS+ and VDD.
5. Use a voltmeter to measure the V_{BIAS} and the CIN+ voltage. V_{BIAS} should be 50% of VDD, 1.5 V. CIN+ should be 40% of VDD, 1.2 V. The P1 potentiometer can be adjusted so that the CIN+ voltage can be increased or decreased.
6. Once CIN+ and V_{BIAS} voltages are confirmed, connect CLATCH to VDD.
7. Connect a voltmeter to measure V_{OUT}. With no load connected V_{OUT} should be equal to V_{BIAS}. The expression for the V_{OUT} output voltage is defined by:

$$V_{OUT} = V_{BIAS} - (GAIN \times I_{SENSE} \times R_{SENSE})$$

8. Connect a voltmeter to measure COUT. COUT should be LOW.
9. Connect an ammeter in series from RS– to a potentiometer. Adjust the POT until the ammeter reads:
   - TS1107-20: 200 mA
   - TS1107-200: 20 mA

   V_{OUT} should equal 1.3 V and COUT should be LOW.
10. To enable the current limit detection, adjust the LOAD POT until the ammeter reads a value greater than:
    - TS1107-20: 400 mA
    - TS1107-200: 40 mA

    V_{OUT} should read 1.1 V, and COUT should latch HIGH detecting that the load current has exceeded the set current limit:
    - TS1107-20 Current Limit: 300 mA
    - TS1107-200 Current Limit: 30 mA

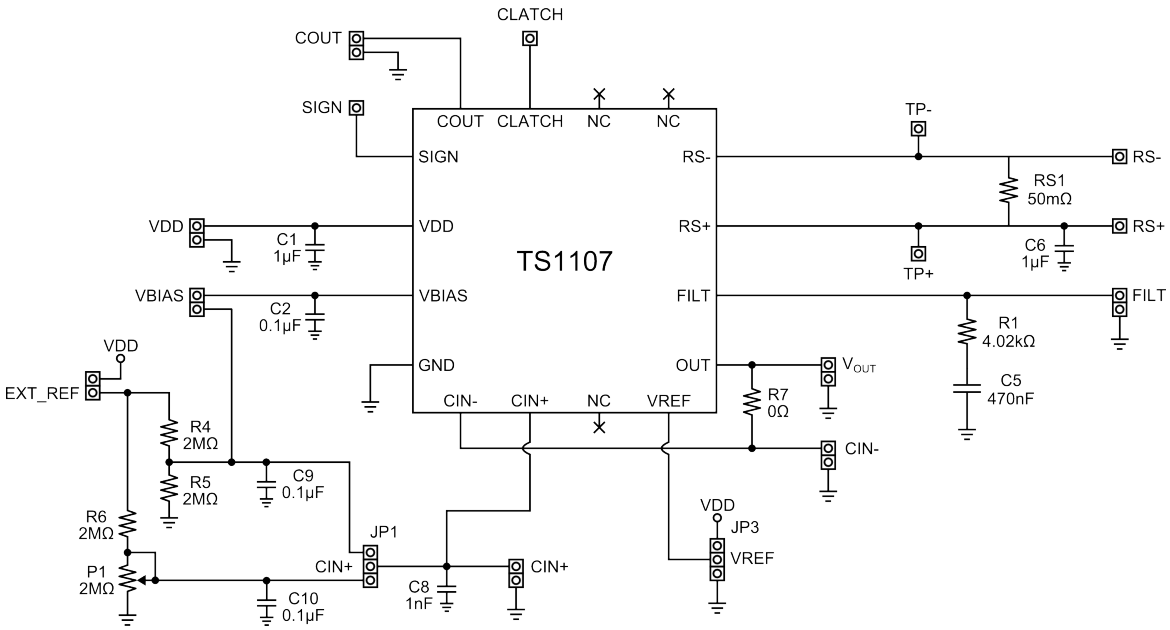
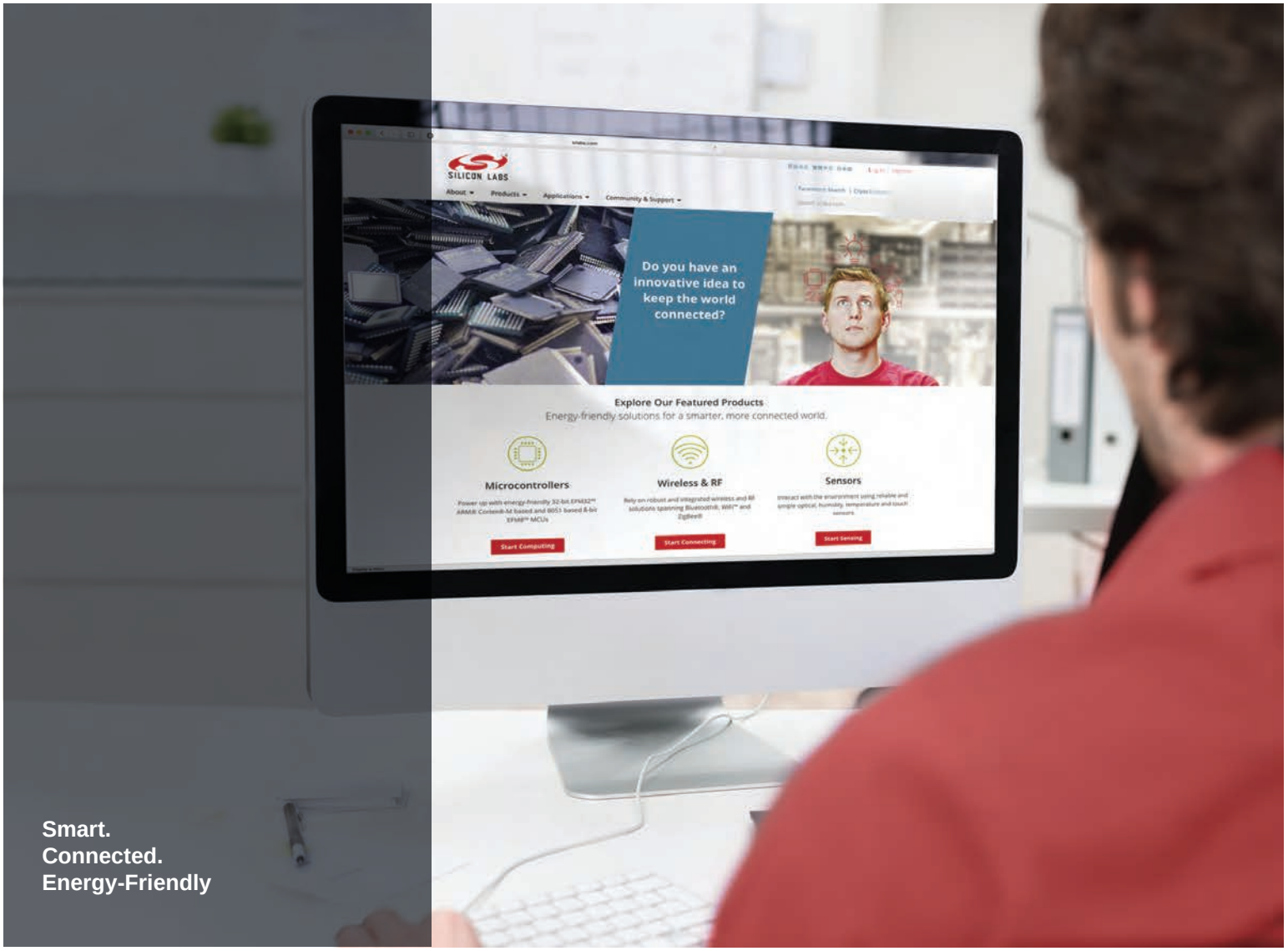


Figure 4.1. TS1107DB Circuit Schematic



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