

# LMC6482 CMOSデュアル・レール・ツー・レール入出力オペアンプ

## 1 特長

- 特に記述のない限り標準値
- レール・ツー・レールの入力同相電圧範囲 (全温度範囲で規定)
- レール・ツー・レールの出力スイング (電源レールの 20mV 以内、100k $\Omega$  負荷)
- 3V、5V、15V での性能を規定
- 非常に優れたCMRRおよびPSRR: 82dB
- 非常に低い入力電流: 20fA
- 高い電圧ゲイン (RL = 500k $\Omega$ ): 130dB
- 2k $\Omega$  および 600 $\Omega$  負荷について動作を規定
- パワー・グッド出力
- パッケージ: PDIP、SOIC、VSSOP

## 2 アプリケーション

- データ・アキュイジション (DAQ)
- 貨幣計数機
- オシロスコープ (DSO)
- DC (データ・センター) 内部の相互接続 (都市部)
- マクロ・リモート無線ユニット (RRU)
- マルチパラメータ患者モニタ
- 商用テレコム整流器
- 列車制御 / 管理
- プロセス分析 (pH、ガス、濃度、力、湿度)
- 3相 UPS
- TLC272、TLC277 の改良版

## 3 概要

LMC6482デバイスは、両方の電源レールまでに及ぶ同相範囲を実現しています。レール・ツー・レール性能と、高いCMRRによる非常に優れた精度から、レール・ツー・レール入力アンプの中でも出色の製品です。このデバイスは、データ収集など、広い入力信号範囲を必要とするシステムに最適です。また、LMC6482はTLC272やTLC277など同相範囲の限られたアンプを使用する回路のアップグレードとしても優れています。

LMC6482のレール・ツー・レール出力スイングにより、低電圧および単一電源のシステムで最大のダイナミック信号範囲を確保できます。レール・ツー・レール出力スイングは、600 $\Omega$ までの負荷に対して可能です。低電圧特性と低消費電力により、LMC6482はバッテリー駆動システムに最適です。

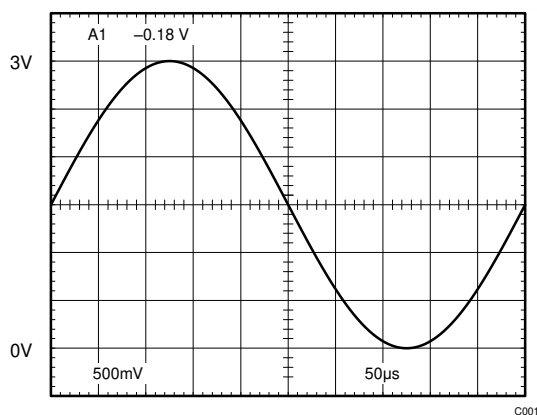
LMC6482は8ピンのPDIPおよびSOICパッケージで供給されます。また、SOIC-8デバイスのほぼ半分の大きさである、VSSOPパッケージでも供給されます。これと同じ特長を持つワイドCMOSオペアンプについては、LMC6484を参照してください。

### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
LMC6482	SOIC (8)	4.90mm×3.91mm
	VSSOP (8)	3.00mm×3.00mm
	PDIP (8)	9.81mm×6.35mm

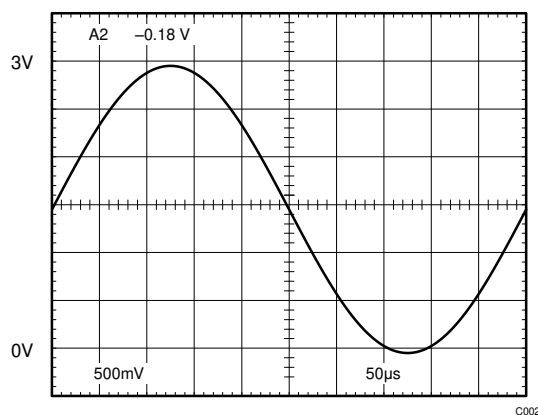
(1) 提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。

レール・ツー・レール入力



C001

レール・ツー・レール出力



C002



## 目次

1	特長	1	7.3	Feature Description	18
2	アプリケーション	1	7.4	Device Functional Modes	19
3	概要	1	<b>8</b>	<b>Application and Implementation</b>	<b>20</b>
4	改訂履歴	2	8.1	Application Information	20
5	<b>Pin Configuration and Functions</b>	<b>3</b>	8.2	Typical Applications	22
6	<b>Specifications</b>	<b>3</b>	<b>9</b>	<b>Power Supply Recommendations</b>	<b>28</b>
6.1	Absolute Maximum Ratings	3	<b>10</b>	<b>Layout</b>	<b>28</b>
6.2	ESD Ratings	4	10.1	Layout Guidelines	28
6.3	Recommended Operating Conditions	4	10.2	Layout Example	28
6.4	Thermal Information	4	<b>11</b>	<b>デバイスおよびドキュメントのサポート</b>	<b>30</b>
6.5	Electrical Characteristics for $V^+ = 5\text{ V}$	4	11.1	ドキュメントの更新通知を受け取る方法	30
6.6	Electrical Characteristics for $V^+ = 3\text{ V}$	7	11.2	サポート・リソース	30
6.7	Typical Characteristics	9	11.3	商標	30
<b>7</b>	<b>Detailed Description</b>	<b>18</b>	11.4	静電気放電に関する注意事項	30
7.1	Overview	18	11.5	Glossary	30
7.2	Functional Block Diagram	18	<b>12</b>	<b>メカニカル、パッケージ、および注文情報</b>	<b>30</b>

## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Revision E (April 2015) から Revision F に変更

**Page**

- Changed junction temperature max value from  $-85^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  (typo) in *Recommended Operating Conditions* table..... **4**

### Revision D (March 2013) から Revision E に変更

**Page**

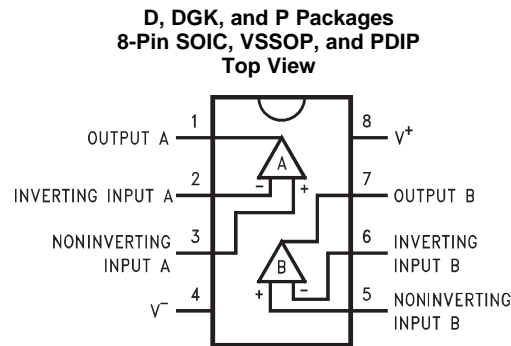
- 「ピン構成および機能」セクション、「ESD定格」の表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加..... **1**

### Revision C (March 2013) から Revision D に変更

**Page**

- Changed layout of National Semiconductor Data Sheet to TI format ..... **27**

## 5 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUTPUT A	O	Output for Amplifier A
2	INVERTING INPUT A	I	Inverting input for Amplifier A
3	NONINVERTING INPUT A	I	Noninverting input for Amplifier A
4	V <sup>-</sup>	P	Negative supply voltage input
5	NONINVERTING INPUT B	I	Noninverting input for Amplifier B
6	INVERTING INPUT B	I	Inverting input for Amplifier B
7	OUTPUT B	O	Output for Amplifier B
8	V <sup>+</sup>	P	Positive supply voltage input

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

	MIN	MAX	UNIT
Differential input voltage	±Supply Voltage		
Voltage at input/output pin	(V <sup>-</sup> ) - 0.3	(V <sup>+</sup> ) + 0.3	V
Supply voltage (V <sup>+</sup> - V <sup>-</sup> )		16	V
Current at input pin <sup>(3)</sup>	-5	5	mA
Current at output pin <sup>(4)(5)</sup>	-30	30	mA
Current at power supply pin		40	mA
Lead temperature (soldering, 10 sec.)		260	°C
Junction temperature <sup>(6)</sup>		150	°C
T <sub>stg</sub> Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
- (4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
- (5) Do not short circuit output to V<sup>+</sup>, when V<sup>+</sup> is greater than 13 V or reliability will be adversely affected.
- (6) The maximum power dissipation is a function of T<sub>J(max)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> - T<sub>A</sub>)/θ<sub>JA</sub>. All numbers apply for packages soldered directly into a PC board.

## 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
	Supply voltage		3	15.5	V
	Junction temperature	LMC6482AM	-55	125	°C
		LMC6482AI, LMC6482I	-40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMC6482	LMC6482	LMC6482	UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	155	194	90	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 6.5 Electrical Characteristics for V<sup>+</sup> = 5 V

unless otherwise specified, all limits specified for T<sub>J</sub> = 25°C, V<sup>+</sup> = 5 V, V<sup>-</sup> = 0 V, V<sub>CM</sub> = V<sub>O</sub> = V<sup>+</sup>/2 and R<sub>L</sub> > 1 MΩ.

PARAMETER	TEST CONDITIONS	T <sub>J</sub> = 25°C			AT TEMPERATURE EXTREMES <sup>(1)</sup>			UNIT
		MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	
<b>DC ELECTRICAL CHARACTERISTICS</b>								
V <sub>OS</sub>	Input offset voltage	LMC6482AI	0.11	0.75	1.35			mV
		LMC6482I	0.11	3	3.7			
		LMC6482M	0.11	3	3.8			
TCV <sub>OS</sub>	Input offset voltage average drift	1						μV/°C
I <sub>B</sub>	Input current <sup>(4)</sup>	LMC6482AI	0.02		4			pA
		LMC6482I	0.02		4			
		LMC6482M	0.02		10			
I <sub>OS</sub>	Input offset current <sup>(4)</sup>	LMC6482AI	0.01		2			pA
		LMC6482I	0.01		2			
		LMC6482M	0.01		5			
C <sub>IN</sub>	Common-mode input capacitance	3						pF
R <sub>IN</sub>	Input resistance	10						TeraΩ

(1) See [Recommended Operating Conditions](#) for operating temperature ranges.

(2) Typical values represent the most likely parametric norm.

(3) All limits are specified by testing or statistical analysis.

(4) Specified limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.



**Electrical Characteristics for  $V^+ = 5\text{ V}$  (continued)**

unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

PARAMETER		TEST CONDITIONS		$T_J = 25^\circ\text{C}$			AT TEMPERATURE EXTREMES <sup>(1)</sup>			UNIT
				MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	
CMRR	Common-mode rejection ratio	$0\text{ V} \leq V_{CM} \leq 15\text{ V}$ $V^+ = 15\text{ V}$	LMC6482AI	70	82		67		dB	
			LMC6482I	65	82		62			
			LMC6482M	65	82		60			
		$0\text{ V} \leq V_{CM} \leq 5\text{ V}$ $V^+ = 5\text{ V}$	LMC6482AI	70	82		67			
			LMC6482I	65	82		62			
			LMC6482M	65	82		60			
+PSRR	Positive power supply rejection ratio	$5\text{ V} \leq V^+ \leq 15\text{ V}$ , $V^- = 0\text{ V}$ $V_O = 2.5\text{ V}$	LMC6482AI	70	82		67		dB	
			LMC6482I	65	82		62			
			LMC6482M	65	82		60			
-PSRR	Negative power supply rejection ratio	$-5\text{ V} \leq V^- \leq -15\text{ V}$ , $V^+ = 0\text{ V}$ $V_O = -2.5\text{ V}$	LMC6482AI	70	82		67		dB	
			LMC6482I	65	82		62			
			LMC6482M	65	82		60			
$V_{CM}$	Input common-mode voltage	$V^+ = 5\text{ V}$ and $15\text{ V}$ For CMRR $\geq 50\text{ dB}$	LMC6482AI		$V^- - 0.3$	$-0.25$		0	V	
			LMC6482I		$V^- - 0.3$	$-0.25$		0		
			LMC6482M		$V^- - 0.3$	$-0.25$		0		
			LMC6482AI	$V^+ + 0.25$	$V^+ + 0.3$		$V^+$		V	
			LMC6482I	$V^+ + 0.25$	$V^+ + 0.3$		$V^+$			
			LMC6482M	$V^+ + 0.25$	$V^+ + 0.3$		$V^+$			
$A_V$	Large signal voltage gain	$R_L = 2\text{ k}\Omega$ <sup>(5)(4)</sup>	Sourcing	LMC6482AI	140	666		84	V/mV	
				LMC6482I	120	666		72		
				LMC6482M	120	666		60		
			Sinking	LMC6482AI	35	75		20	V/mV	
				LMC6482I	35	75		20		
				LMC6482M	35	75		18		
		$R_L = 600\ \Omega$ <sup>(5)(4)</sup>	Sourcing	LMC6482AI	80	300		48	V/mV	
				LMC6482I	50	300		30		
				LMC6482M	50	300		25		
			Sinking	LMC6482AI	20	35		13	V/mV	
				LMC6482I	15	35		10		
				LMC6482M	15	35		8		

(5)  $V^+ = 15\text{ V}$ ,  $V_{CM} = 7.5\text{ V}$  and  $R_L$  connected to  $7.5\text{ V}$ . For sourcing tests,  $7.5\text{ V} \leq V_O \leq 11.5\text{ V}$ . For sinking tests,  $3.5\text{ V} \leq V_O \leq 7.5\text{ V}$ .

**Electrical Characteristics for  $V^+ = 5\text{ V}$  (continued)**

unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

PARAMETER	TEST CONDITIONS	$T_J = 25^\circ\text{C}$			AT TEMPERATURE EXTREMES <sup>(1)</sup>			UNIT
		MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	
$V_O$	$V^+ = 5\text{ V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$	LMC6482AI	4.8	4.9	4.7		V	
		LMC6482I	4.8	4.9	4.7			
		LMC6482M	4.8	4.9	4.7			
		LMC6482AI	0.1 0.18		0.24			
		LMC6482I	0.1 0.18		0.24			
		LMC6482M	0.1 0.18		0.24			
	$V^+ = 5\text{ V}$ $R_L = 600\ \Omega$ to $V^+/2$	LMC6482AI	4.5	4.7	4.24		V	
		LMC6482I	4.5	4.7	4.24			
		LMC6482M	4.5	4.7	4.24			
		LMC6482AI	0.3 0.5		0.65			
		LMC6482I	0.3 0.5		0.65			
		LMC6482M	0.3 0.5		0.65			
	$V^+ = 15\text{ V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$	LMC6482AI	14.4	14.7	14.2		V	
		LMC6482I	14.4	14.7	14.2			
		LMC6482M	14.4	14.7	14.2			
		LMC6482AI	0.16 0.32		0.45			
		LMC6482I	0.16 0.32		0.45			
		LMC6482M	0.16 0.32		0.45			
	$V^+ = 15\text{ V}$ $R_L = 600\ \Omega$ to $V^+/2$	LMC6482AI	13.4	14.1	13		V	
		LMC6482I	13.4	14.1	13			
		LMC6482M	13.4	14.1	13			
		LMC6482AI	0.5 1		1.3			
		LMC6482I	0.5 1		1.3			
		LMC6482M	0.5 1		1.3			
$I_{SC}$	Output short circuit current $V^+ = 5\text{ V}$	Sourcing, $V_O = 0\text{ V}$	LMC6482AI	16	20	12		mA
		LMC6482I	16	20	12			
		LMC6482M	16	20	10			
	Sinking, $V_O = 5\text{ V}$	LMC6482AI	11	15	9.5		mA	
		LMC6482I	11	15	9.5			
		LMC6482M	11	15	8			
$I_{SC}$	Output short circuit current $V^+ = 15\text{ V}$	Sourcing, $V_O = 0\text{ V}$	LMC6482AI	28	30	22		mA
			LMC6482I	28	30	22		
			LMC6482M	28	30	20		
	Sinking, $V_O = 12\text{ V}^{(6)}$	LMC6482AI	30	30	24		mA	
		LMC6482I	30	30	24			
		LMC6482M	30	30	22			
$I_S$	Supply current	Both Amplifiers $V^+ = +5\text{ V}$ , $V_O = V^+/2$	LMC6482AI	1 1.4		1.8		mA
			LMC6482I	1 1.4		1.8		
			LMC6482M	1 1.4		1.9		
		Both Amplifiers $V^+ = 15\text{ V}$ , $V_O = V^+/2$	LMC6482AI	1.3 1.6		1.9		mA
			LMC6482I	1.3 1.6		1.9		
			LMC6482M	1.3 1.6		2		

(6) Do not short circuit output to  $V^+$ , when  $V^+$  is greater than 13 V or reliability will be adversely affected.

## Electrical Characteristics for $V^+ = 5\text{ V}$ (continued)

unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

PARAMETER	TEST CONDITIONS	$T_J = 25^\circ\text{C}$			AT TEMPERATURE EXTREMES <sup>(1)</sup>			UNIT
		MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	
<b>AC ELECTRICAL CHARACTERISTICS</b>								
SR	Slew rate <sup>(7)</sup>	LMC6482AI		1	1.3	0.7		V/ $\mu\text{s}$
		LMC6482I		0.9	1.3	0.63		
		LMC6482M		0.9	1.3	0.54		
GBW	Gain-bandwidth product	$V^+ = 15\text{ V}$		1.5			MHz	
$\phi_m$	Phase margin				50			Deg
$G_m$	Gain margin				15			dB
	Amp-to-amp isolation	See <sup>(8)</sup>		150			dB	
$e_n$	Input-referred voltage noise	F = 1 kHz $V_{cm} = 1\text{ V}$		37			nV/ $\sqrt{\text{Hz}}$	
$I_n$	Input-referred current noise	F = 1 kHz		0.03			pA/ $\sqrt{\text{Hz}}$	
T.H.D.	Total harmonic distortion	F = 10 kHz, $A_V = -2$ $R_L = 10\text{ k}\Omega$ , $V_O = 4.1\text{ V}_{PP}$		0.01%				
		F = 10 kHz, $A_V = -2$ $R_L = 10\text{ k}\Omega$ , $V_O = 8.5\text{ V}_{PP}$ $V^+ = 10\text{ V}$		0.01%				

(7)  $V^+ = 15\text{ V}$ . Connected as voltage follower with 10-V step input. Number specified is the slower of either the positive or negative slew rates.

(8) Input referred,  $V^+ = 15\text{ V}$  and  $R_L = 100\text{ k}\Omega$  connected to 7.5 V. Each amp excited in turn with 1 kHz to produce  $V_O = 12\text{ V}_{PP}$ .

## 6.6 Electrical Characteristics for $V^+ = 3\text{ V}$

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 3\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

PARAMETER	TEST CONDITIONS	$T_J = 25^\circ\text{C}$			AT TEMPERATURE EXTREMES <sup>(1)</sup>			UNIT
		MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	
<b>DC ELECTRICAL CHARACTERISTICS</b>								
$V_{OS}$	Input offset voltage	LMC6482AI		0.9	2	2.7		mV
		LMC6482I		0.9	3	3.7		
		LMC6482M		0.9	3	3.8		
$TCV_{OS}$	Input offset voltage average drift	2			$\mu\text{V}/^\circ\text{C}$			
$I_B$	Input bias current	0.02			pA			
$I_{OS}$	Input offset current	0.01			pA			
CMRR	Common mode rejection ratio	$0\text{ V} \leq V_{CM} \leq 3\text{ V}$	LMC6482AI		64	74	dB	
			LMC6482I		60	74		
			LMC6482M		60	74		

(1) See [Recommended Operating Conditions](#) for operating temperature ranges.

(2) Typical values represent the most likely parametric norm.

(3) All limits are specified by testing or statistical analysis.

**Electrical Characteristics for  $V^+ = 3\text{ V}$  (continued)**

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 3\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $V_{CM} = V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

PARAMETER		TEST CONDITIONS		$T_J = 25^\circ\text{C}$			AT TEMPERATURE EXTREMES <sup>(1)</sup>			UNIT
				MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	MIN	TYP <sup>(2)</sup>	MAX <sup>(3)</sup>	
PSRR	Power supply rejection ratio	$3\text{ V} \leq V^+ \leq 15\text{ V}$ , $V^- = 0\text{ V}$	LMC6482AI	68	80					dB
			LMC6482I	60	80					
			LMC6482M	60	80					
$V_{CM}$	Input common-mode voltage	For CMRR $\geq 50\text{ dB}$	LMC6482AI		$V^- - 0.25$	0				V
			LMC6482I		$V^- - 0.25$	0				
			LMC6482M		$V^- - 0.25$	0				
			LMC6482AI	$V^+$	$V^+ + 0.25$					V
			LMC6482I	$V^+$	$V^+ + 0.25$					
			LMC6482M	$V^+$	$V^+ + 0.25$					
$V_O$	Output swing	$R_L = 2\text{ k}\Omega$ to $V^+/2$			2.8				V	
					0.2					
		$R_L = 600\ \Omega$ to $V^+/2$	LMC6482AI	2.5	2.7					
			LMC6482I	2.5	2.7					
			LMC6482M	2.5	2.7					
			LMC6482AI		0.37	0.6				
			LMC6482I		0.37	0.6				
			LMC6482M		0.37	0.6				
$I_S$	Supply current	Both amplifiers	LMC6482AI		0.825	1.2		1.5	mA	
			LMC6482I		0.825	1.2		1.5		
			LMC6482M		0.825	1.2		1.6		
<b>AC ELECTRICAL CHARACTERISTICS</b>										
SR	Slew rate	See <sup>(4)</sup>			0.9					$\text{V}/\mu\text{s}$
GBW	Gain-bandwidth product				1					MHz
T.H.D.	Total harmonic distortion	$f = 10\text{ kHz}$ , $A_V = -2$ $R_L = 10\text{ k}\Omega$ , $V_O = 2\text{ V}_{PP}$			0.01%					

(4) Connected as voltage follower with 2-V step input. Number specified is the slower of either the positive or negative slew rates.

### 6.7 Typical Characteristics

at  $V_S = 15\text{ V}$ , single supply, and  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

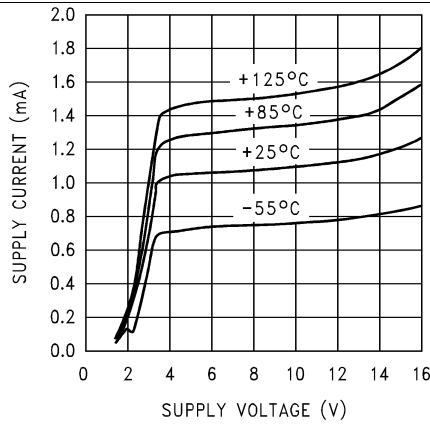


Figure 1. Supply Current vs Supply Voltage

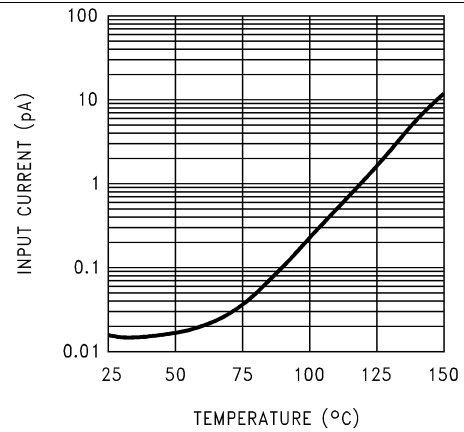


Figure 2. Input Current vs Temperature

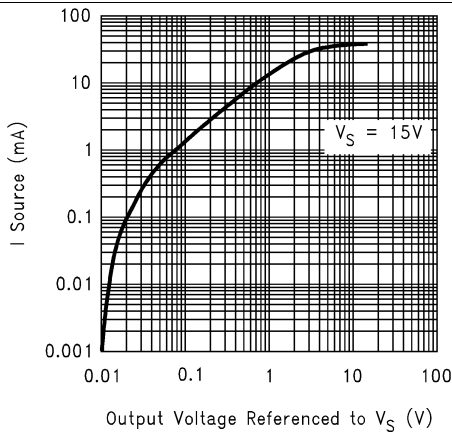


Figure 3. Sourcing Current vs Output Voltage

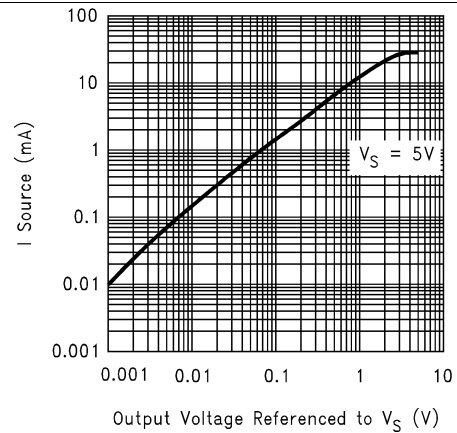


Figure 4. Sourcing Current vs Output Voltage

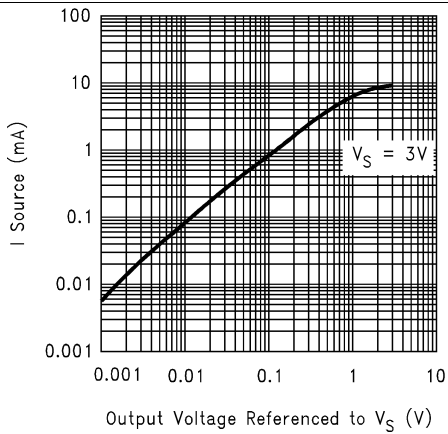


Figure 5. Sourcing Current vs Output Voltage

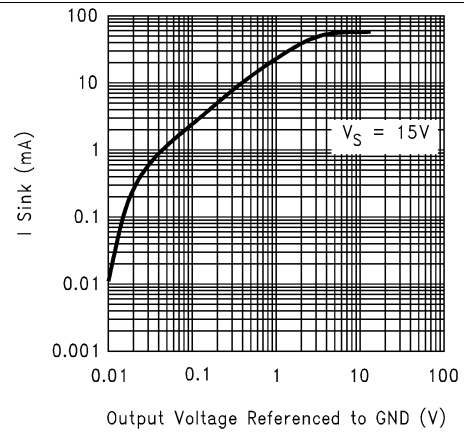


Figure 6. Sinking Current vs Output Voltage

### Typical Characteristics (continued)

at  $V_S = 15\text{ V}$ , single supply, and  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

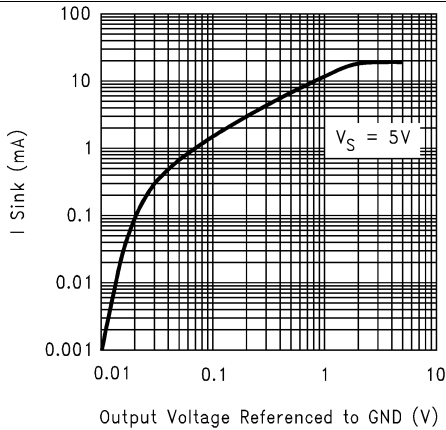


Figure 7. Sinking Current vs Output Voltage

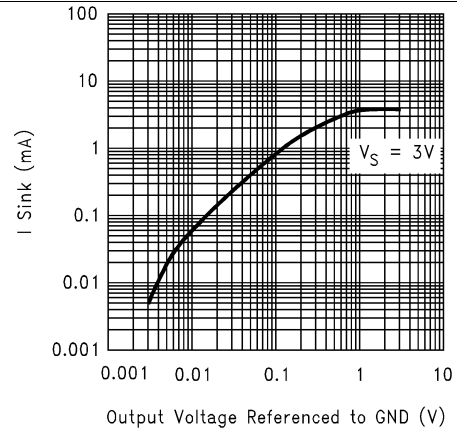


Figure 8. Sinking Current vs Output Voltage

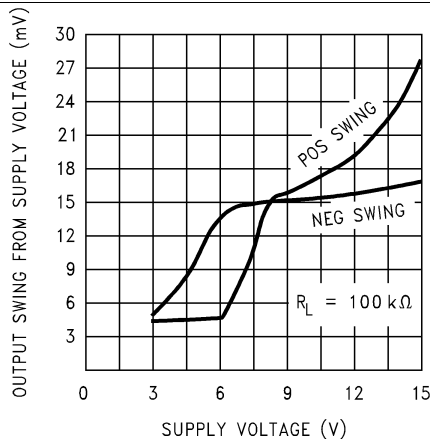


Figure 9. Output Voltage Swing vs Supply Voltage

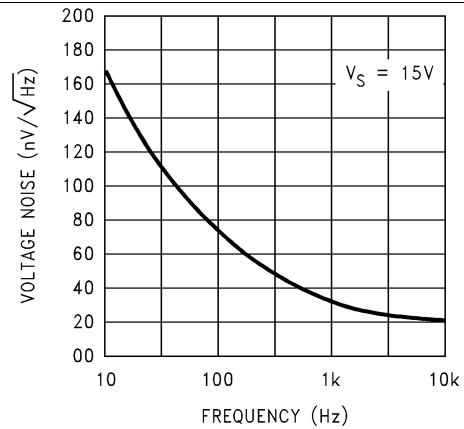


Figure 10. Input Voltage Noise vs Frequency

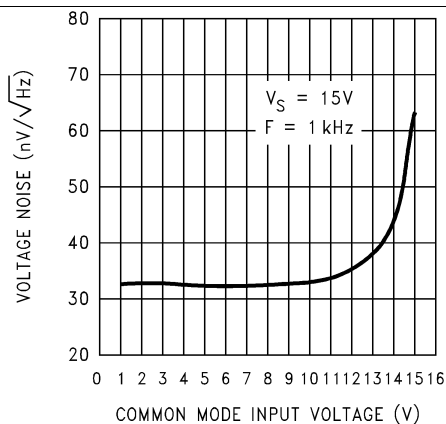


Figure 11. Input Voltage Noise vs Input Voltage

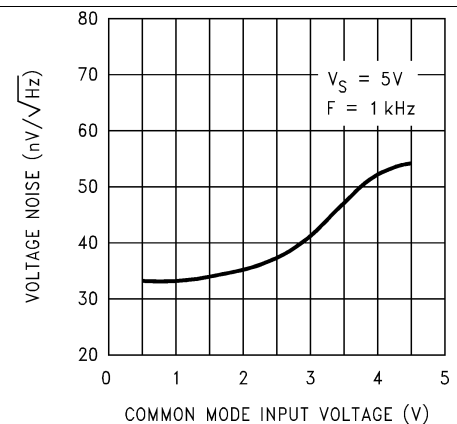


Figure 12. Input Voltage Noise vs Input Voltage

Typical Characteristics (continued)

at  $V_S = 15\text{ V}$ , single supply, and  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

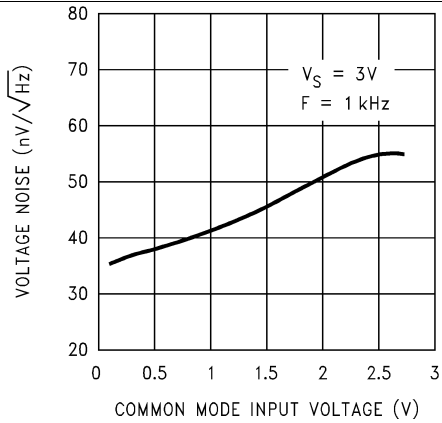


Figure 13. Input Voltage Noise vs Input Voltage

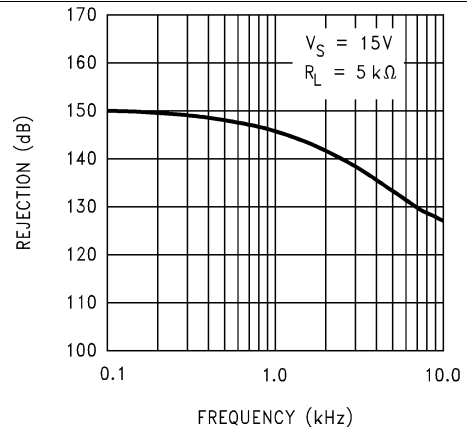


Figure 14. Crosstalk Rejection vs Frequency

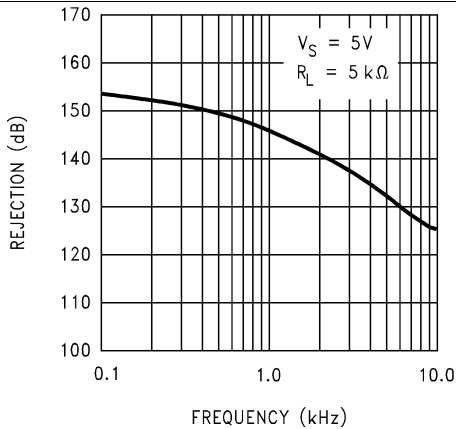


Figure 15. Crosstalk Rejection vs Frequency

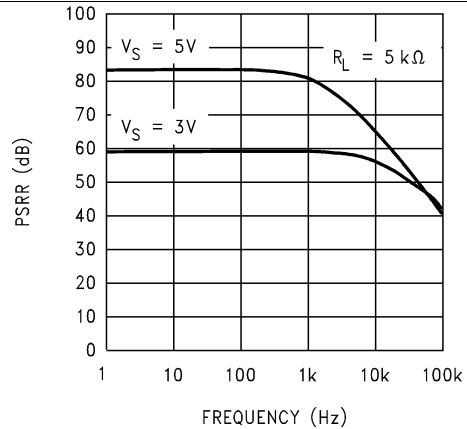


Figure 16. Positive PSRR vs Frequency

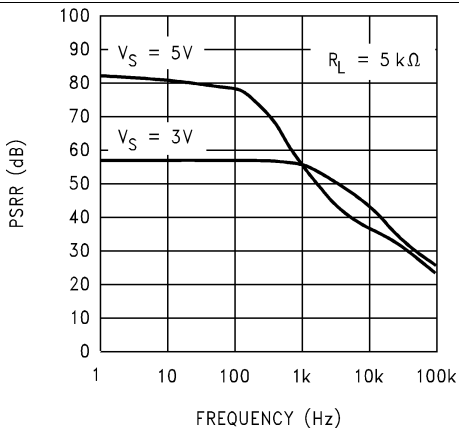


Figure 17. Negative PSRR vs Frequency

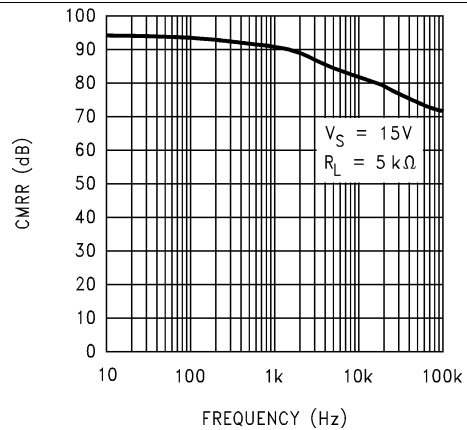


Figure 18. CMRR vs Frequency

Typical Characteristics (continued)

at  $V_S = 15\text{ V}$ , single supply, and  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

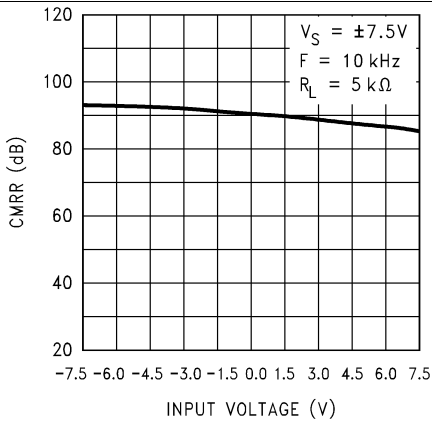


Figure 19. CMRR vs Input Voltage

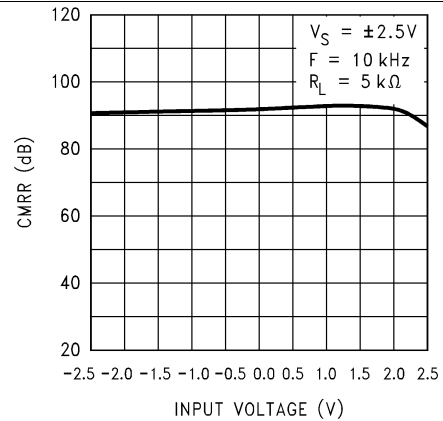


Figure 20. CMRR vs Input Voltage

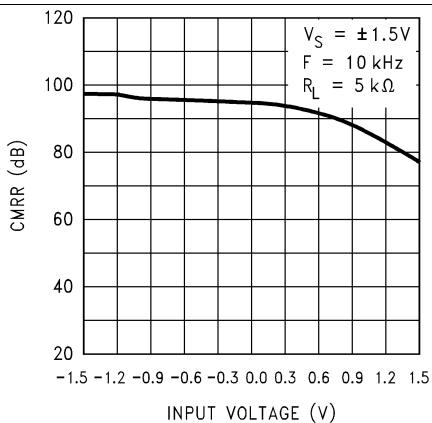


Figure 21. CMRR vs Input Voltage

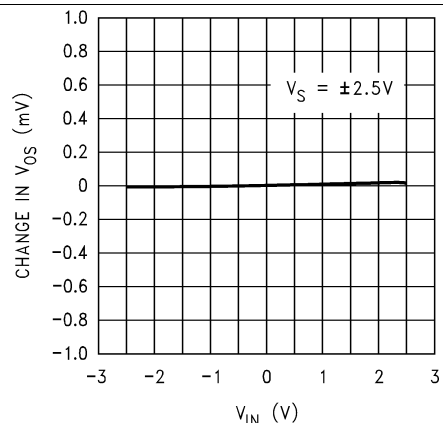


Figure 22.  $\Delta V_{OS}$  vs CMR

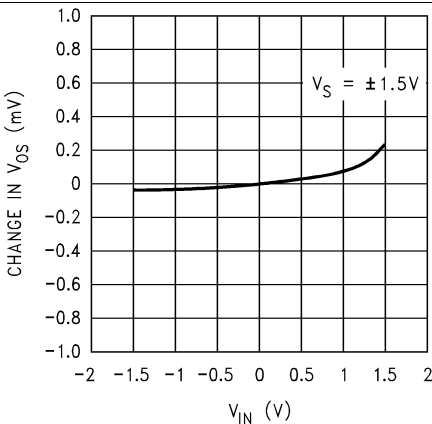


Figure 23.  $\Delta V_{OS}$  vs CMR

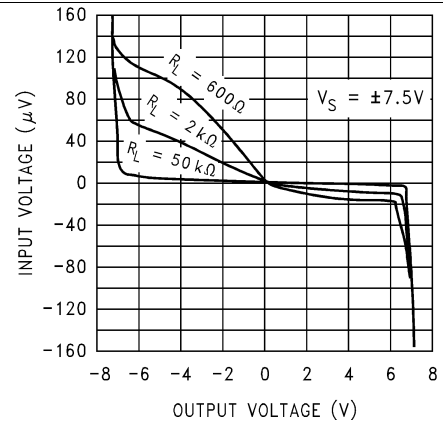


Figure 24. Input Voltage vs Output Voltage



Typical Characteristics (continued)

at  $V_S = 15\text{ V}$ , single supply, and  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

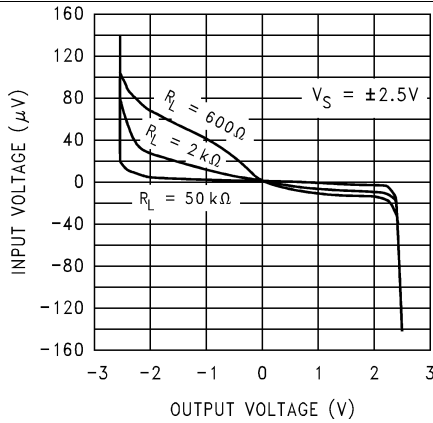


Figure 25. Input Voltage vs Output Voltage

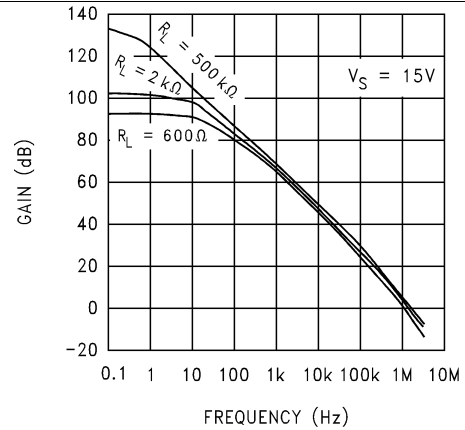


Figure 26. Open-Loop Frequency Response

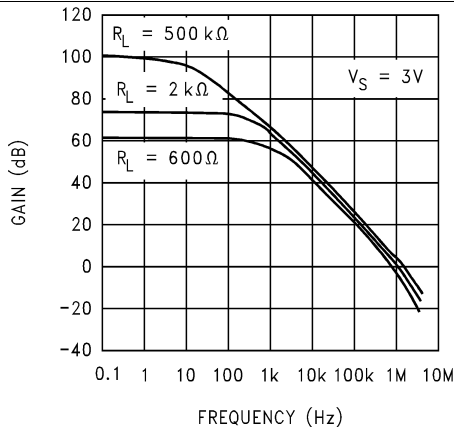


Figure 27. Open-Loop Frequency Response

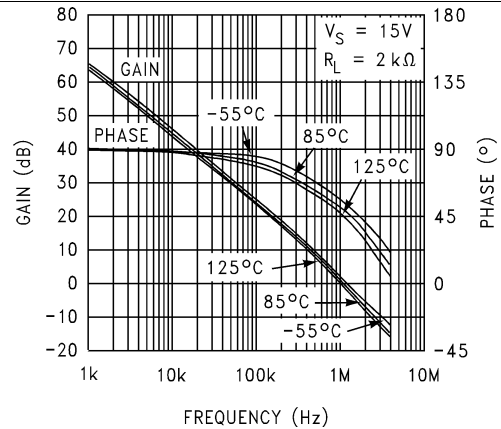


Figure 28. Open-Loop Frequency Response vs Temperature

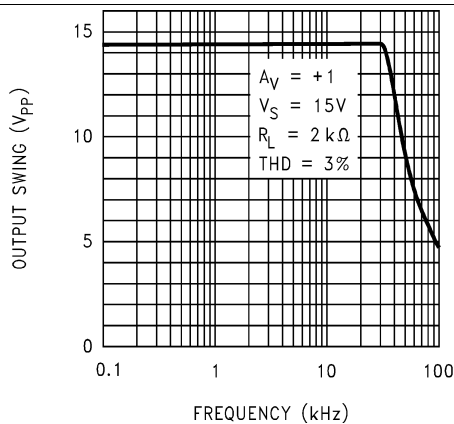


Figure 29. Maximum Output Swing vs Frequency

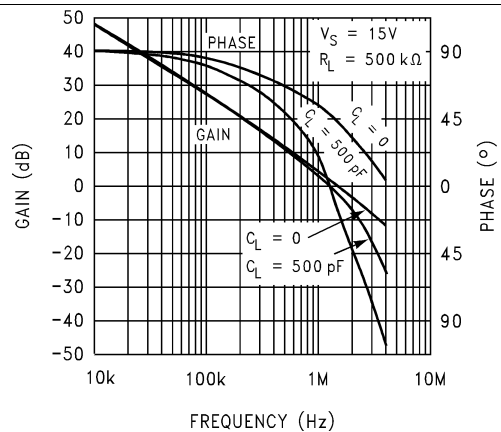
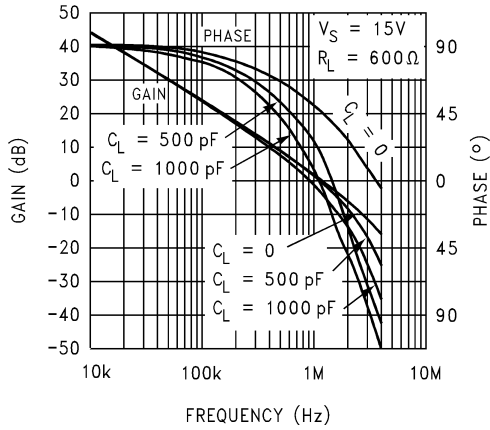


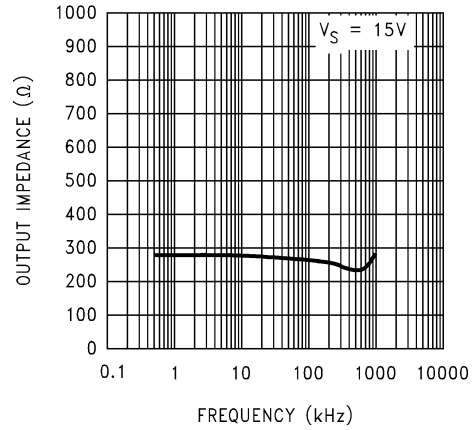
Figure 30. Gain and Phase vs Capacitive Load

**Typical Characteristics (continued)**

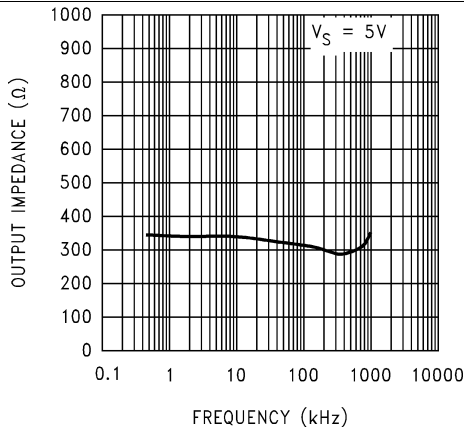
at  $V_S = 15\text{ V}$ , single supply, and  $T_A = 25^\circ\text{C}$  (unless otherwise specified)



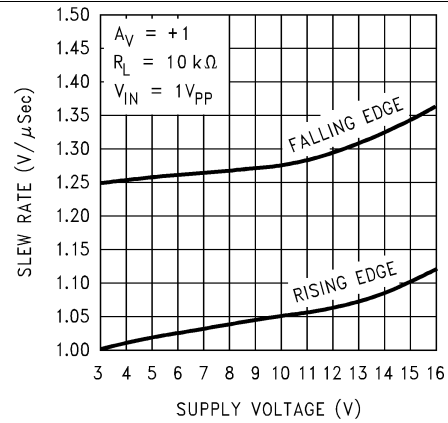
**Figure 31. Gain and Phase vs Capacitive Load**



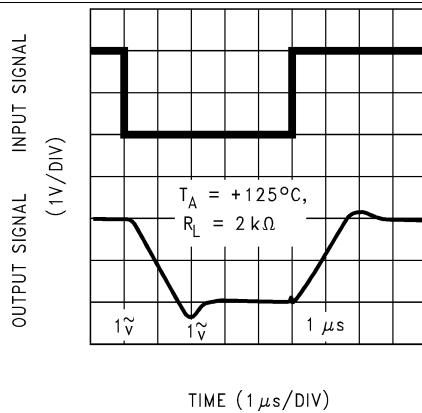
**Figure 32. Open-Loop Output Impedance vs Frequency**



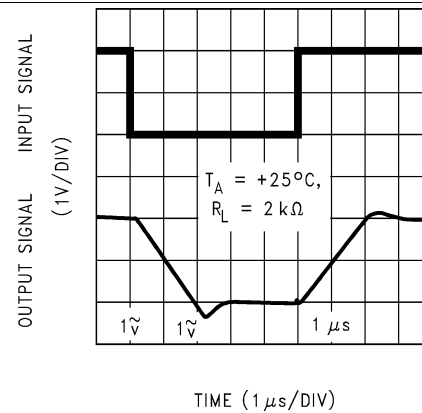
**Figure 33. Open-Loop Output Impedance vs Frequency**



**Figure 34. Slew Rate vs Supply Voltage**



**Figure 35. Noninverting Large Signal Pulse Response**



**Figure 36. Noninverting Large Signal Pulse Response**

Typical Characteristics (continued)

at  $V_S = 15\text{ V}$ , single supply, and  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

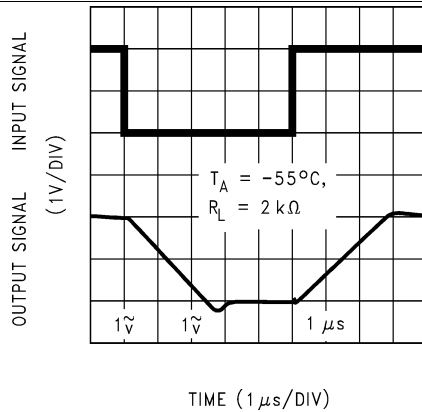


Figure 37. Noninverting Large Signal Pulse Response

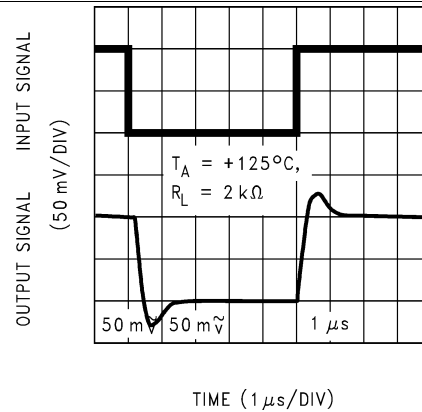


Figure 38. Noninverting Small Signal Pulse Response

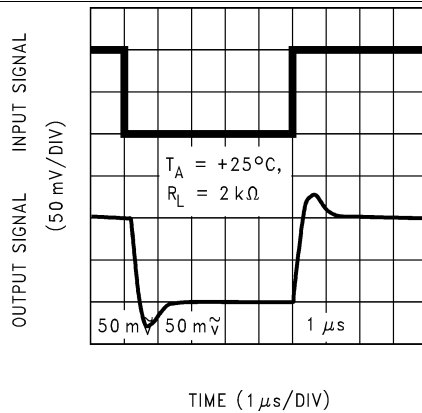


Figure 39. Noninverting Small Signal Pulse Response

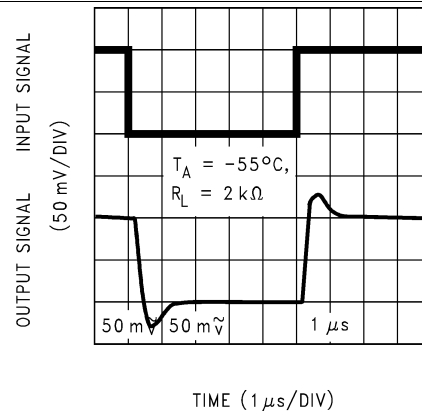


Figure 40. Noninverting Small Signal Pulse Response

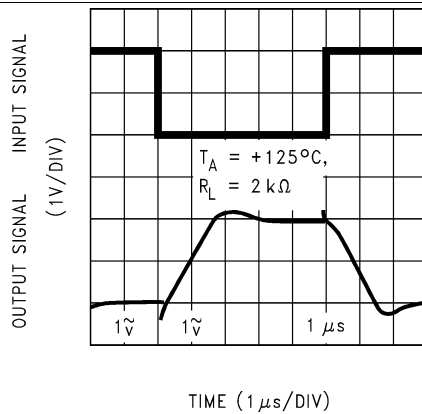


Figure 41. Inverting Large Signal Pulse Response

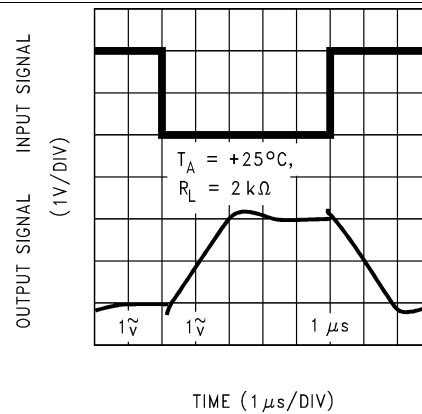


Figure 42. Inverting Large Signal Pulse Response

Typical Characteristics (continued)

at  $V_S = 15\text{ V}$ , single supply, and  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

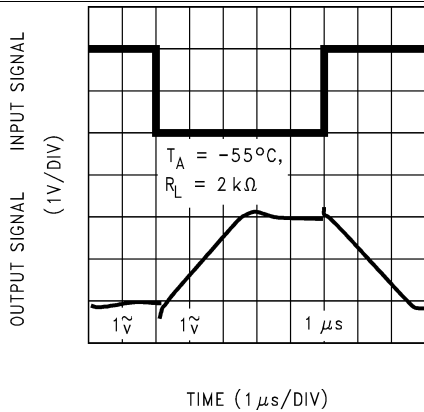


Figure 43. Inverting Large Signal Pulse Response

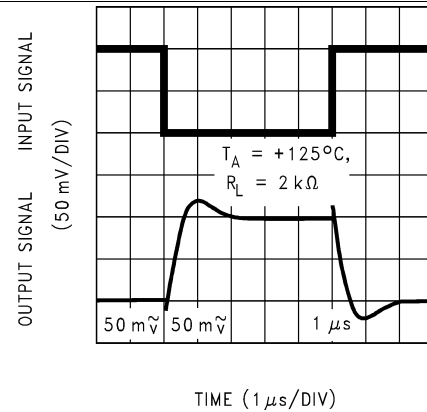


Figure 44. Inverting Small Signal Pulse Response

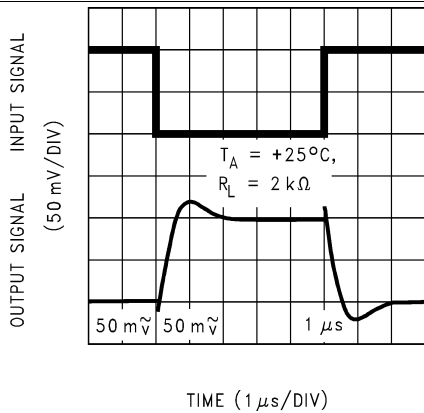


Figure 45. Inverting Small Signal Pulse Response

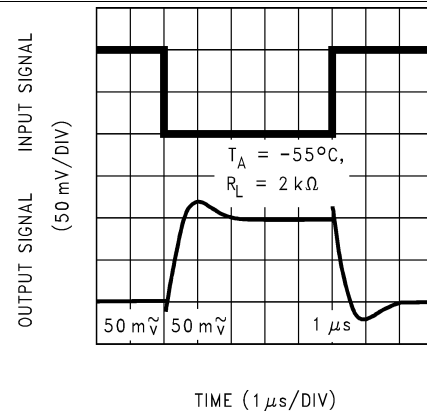


Figure 46. Inverting Small Signal Pulse Response

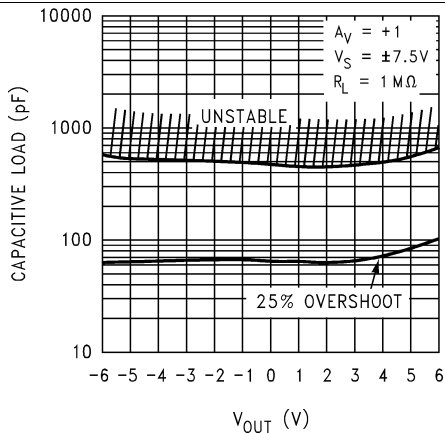


Figure 47. Stability vs Capacitive Load

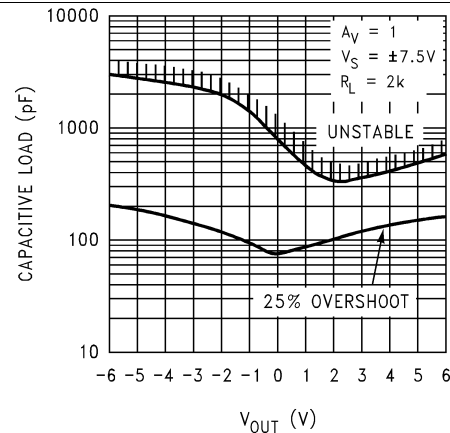


Figure 48. Stability vs Capacitive Load

Typical Characteristics (continued)

at  $V_S = 15\text{ V}$ , single supply, and  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

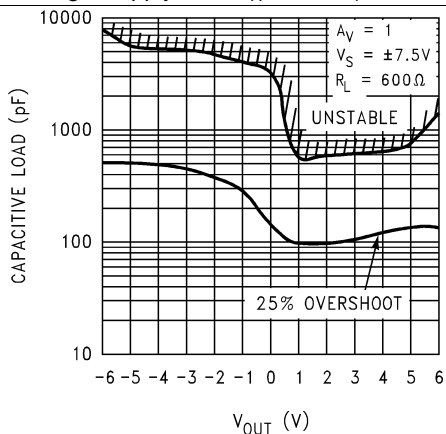


Figure 49. Stability vs Capacitive Load

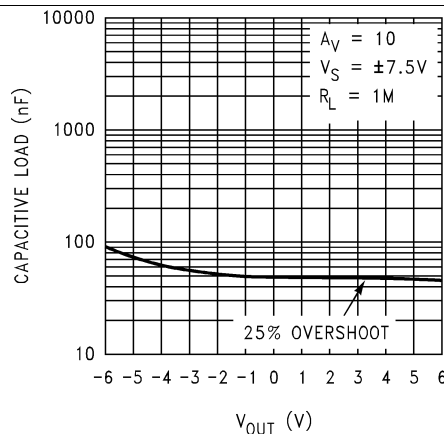


Figure 50. Stability vs Capacitive Load

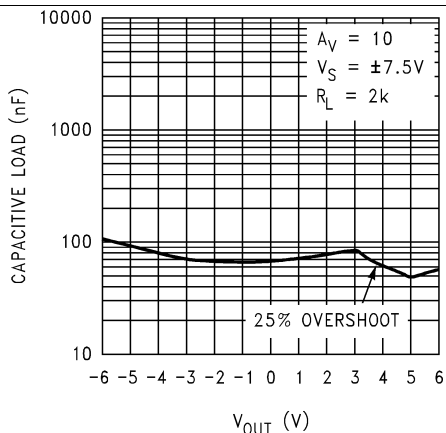


Figure 51. Stability vs Capacitive Load

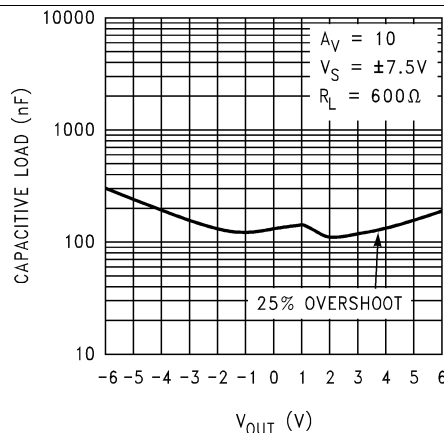


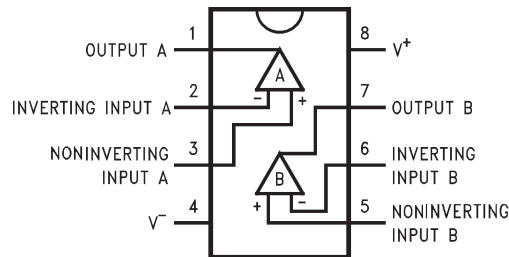
Figure 52. Stability vs Capacitive Load

## 7 Detailed Description

### 7.1 Overview

The LMC6482 is a dual CMOS operational amplifier that supports both rail-to-rail inputs and outputs. The device can be operated in both dual-supply mode and single-supply mode.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

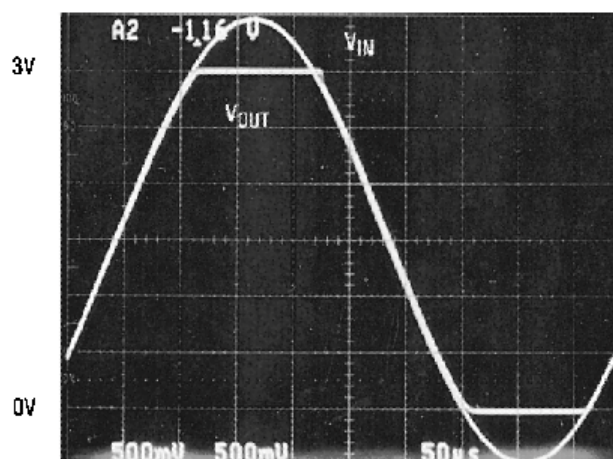
#### 7.3.1 Amplifier Topology

The LMC6482 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common-mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, crossover distortion, and open-loop gain variation.

The LMC6482s input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

#### 7.3.2 Input Common-Mode Voltage Range

Unlike Bi-FET amplifier designs, the LMC6482 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 53 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

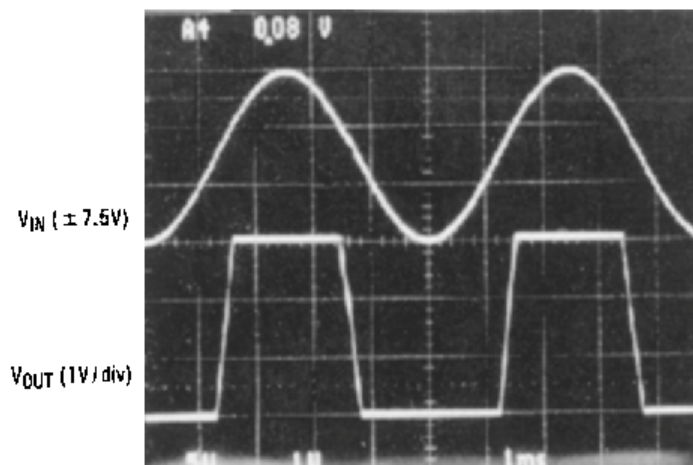


An input voltage signal exceeds the LMC6482 power supply voltages with no output phase inversion.

**Figure 53. Input Voltage**

## Feature Description (continued)

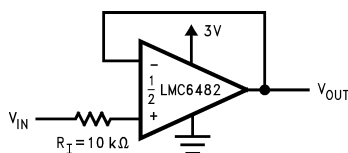
The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 54, can cause excessive current to flow in or out of the input pins possibly affecting reliability.



NOTE: A  $\pm 7.5\text{-V}$  input signal greatly exceeds the 3-V supply in Figure 55 causing no phase inversion due to  $R_I$ .

Figure 54. Input Signal

Applications that exceed this rating must externally limit the maximum input current to  $\pm 5\text{ mA}$  with an input resistor ( $R_I$ ) as shown in Figure 55.



NOTE:  $R_I$  input current protection for voltages exceeding the supply voltages.

Figure 55.  $R_I$  Input Current Protection for Voltages Exceeding the Supply Voltages

### 7.3.3 Rail-to-Rail Output

The approximated output resistance of the LMC6482 is 180- $\Omega$  sourcing and 13-0 $\Omega$  sinking at  $V_S = 3\text{ V}$  and 110- $\Omega$  sourcing and 80- $\Omega$  sinking at  $V_S = 5\text{ V}$ . Using the calculated output resistance, the maximum output voltage swing can be estimated as a function of load.

## 7.4 Device Functional Modes

The LMC6482 can be used in applications where each amplifier channel is used independently, or in applications in which the channels are cascaded. See the [Typical Applications](#) section for more information.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

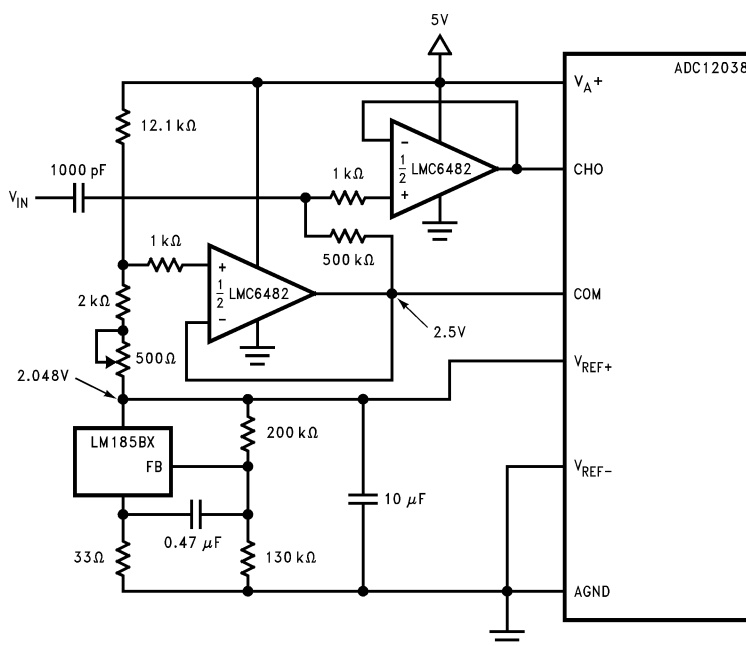
#### 8.1.1 Upgrading Applications

The LMC6484 quads and LMC6482 duals have industry-standard pin outs to retrofit existing applications. System performance can be greatly increased by the features of the LMC6482. The key benefit of designing in the LMC6482 is increased linear signal range. Most op-amps have limited input common-mode ranges. Signals that exceed this range generate a nonlinear output response that persists long after the input signal returns to the common-mode range.

Linear signal range is vital in applications such as filters where signal peaking can exceed input common-mode ranges resulting in output phase inversion or severe distortion.

#### 8.1.2 Data Acquisition Systems

Low power, single supply data acquisition system solutions are provided by buffering the ADC12038 with the LMC6482 (Figure 56). Capable of using the full supply range, the LMC6482 does not require input signals to be scaled down to meet limited common-mode voltage ranges. The LMC6482 CMRR of 82 dB maintains integral linearity of a 12-bit data acquisition system to  $\pm 0.325$  LSB. Other rail-to-rail input amplifiers with only 50 dB of CMRR will degrade the accuracy of the data acquisition system to only 8 bits.



NOTE: Operating from the same supply voltage, the LMC6482 buffers the ADC12038 maintaining excellent accuracy.

**Figure 56. Buffering the ADC12038 With the LMC6482**



## Application Information (continued)

### 8.1.3 Instrumentation Circuits

The LMC6482 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6482 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6482 an excellent choice of noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with  $R_G$  to set the differential gain of the 3-op-amp instrumentation circuit in Figure 57. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

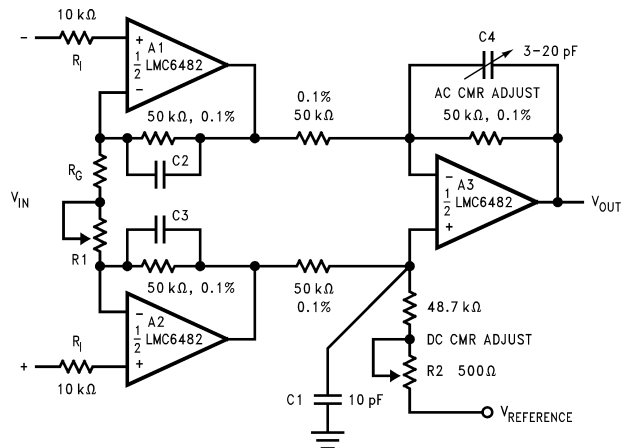


Figure 57. Low-Power, Three-Op-Amp Instrumentation Amplifier

A two-op-amp instrumentation amplifier designed for a gain of 100 is shown in Figure 58. Low sensitivity trimming is made for offset voltage, CMRR, and gain. Low cost and low power consumption are the main advantages of this two-op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three-op-amp instrumentation amplifier.

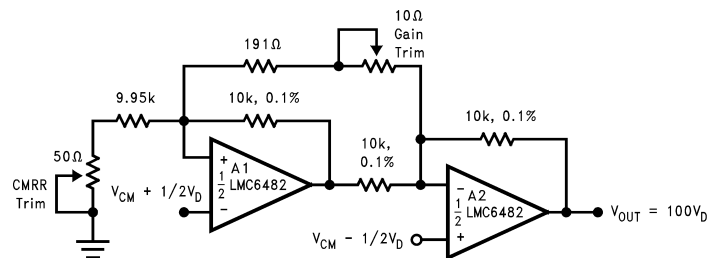


Figure 58. Low-Power, Two-Op-Amp Instrumentation Amplifier

### 8.1.4 Spice Macromodel

A spice macromodel is available for the LMC6482. This model includes accurate simulation of the following:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

Many more characteristics are listed on the macromodel disk.

Contact your local TI sales office to obtain an operational amplifier spice model library disk.

## 8.2 Typical Applications

### 8.2.1 3-V Single-Supply Buffer Circuit

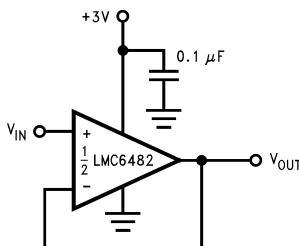


Figure 59. 3-V Single-Supply Buffer Circuit

#### 8.2.1.1 Design Requirements

For best performance, make sure that the input voltage swing is between  $V+$  and  $V-$ .

Also, make certain that the input does not exceed the common-mode input range.

To reduce the risk of destabilizing the output, use resistive isolation on the output when driving capacitive loads (see the [Detailed Design Procedure](#) section).

When large feedback resistors are used, compensation for parasitic capacitance on the input may be necessary. See the [Detailed Design Procedure](#) section.

#### 8.2.1.2 Detailed Design Procedure

##### 8.2.1.2.1 Capacitive Load Compensation

Capacitive load compensation can be accomplished using resistive isolation as shown in [Figure 60](#). This simple technique is useful for isolating the capacitive inputs of multiplexers and A/D converters.

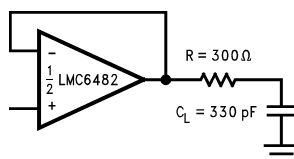


Figure 60. Resistive Isolation of a 330-pF Capacitive Load

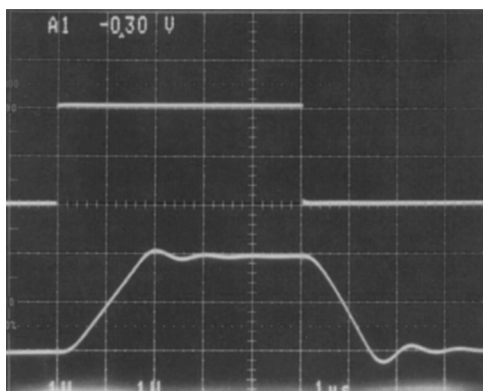


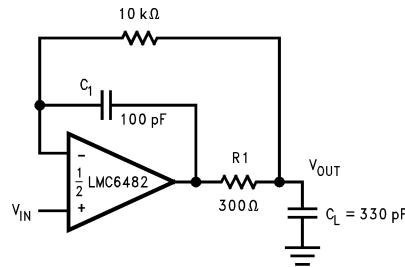
Figure 61. Pulse Response of the LMC6482 Circuit in [Figure 60](#)

## Typical Applications (continued)

### 8.2.1.2.2 Capacitive Load Tolerance

The LMC6482 can typically directly drive a 100-pF load with  $V_S = 15\text{ V}$  at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the output impedance of the op-amp and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

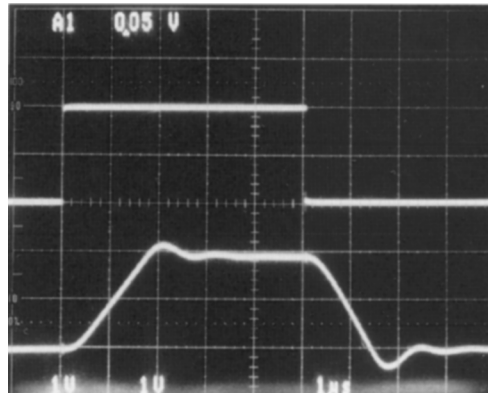
Improved frequency response is achieved by indirectly driving capacitive loads, as shown in [Figure 62](#).



NOTE: Compensated to handle a 330-pF capacitive load.

**Figure 62. LMC6482 Noninverting Amplifier**

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high-frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response is shown in [Figure 63](#).



**Figure 63. Pulse Response of Lmc6482 Circuit in [Figure 62](#)**

### 8.2.1.2.3 Compensating For Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6482. Large feedback resistors can react with small values of input capacitance due to transducers, photo diodes, and circuits board parasitics to reduce phase margins.

Typical Applications (continued)

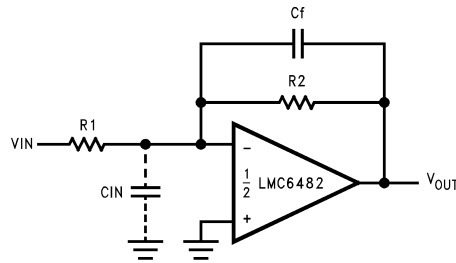


Figure 64. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 64),  $C_f$ , is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \tag{1}$$

or

$$R_1 C_{IN} \leq R_2 C_f \tag{2}$$

which typically provides significant overcompensation.

Printed-circuit-board stray capacitance may be larger or smaller than that of a bread-board, so the actual optimum value for  $C_f$  may be different. The values of  $C_f$  should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

8.2.1.2.4 Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in Figure 65 and Figure 66. Large value resistances and potentiometers are used to reduce power consumption while providing typically  $\pm 2.5$  mV of adjustment range, referred to the input, for both configurations with  $V_S = \pm 5$  V.

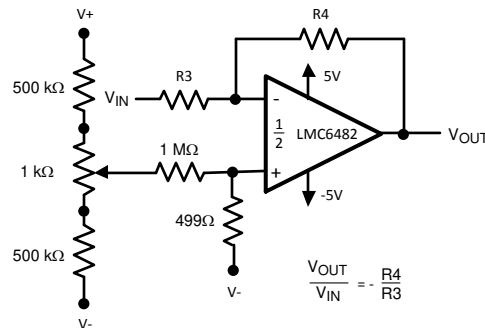


Figure 65. Inverting Configuration Offset Voltage Adjustment

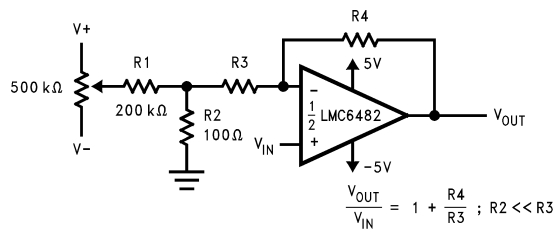
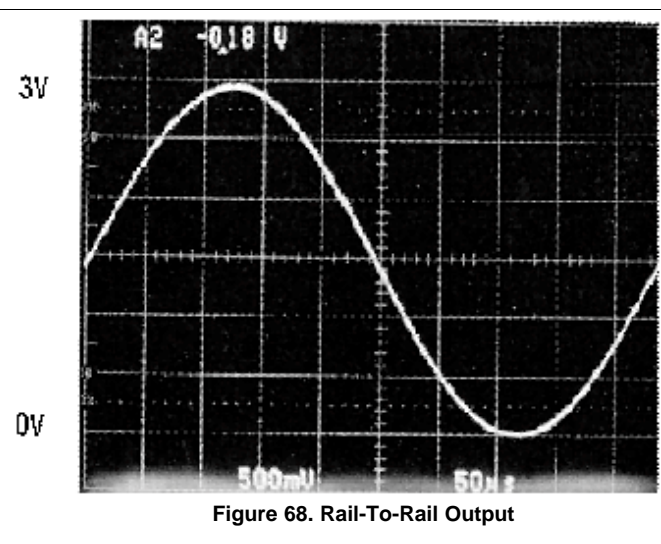
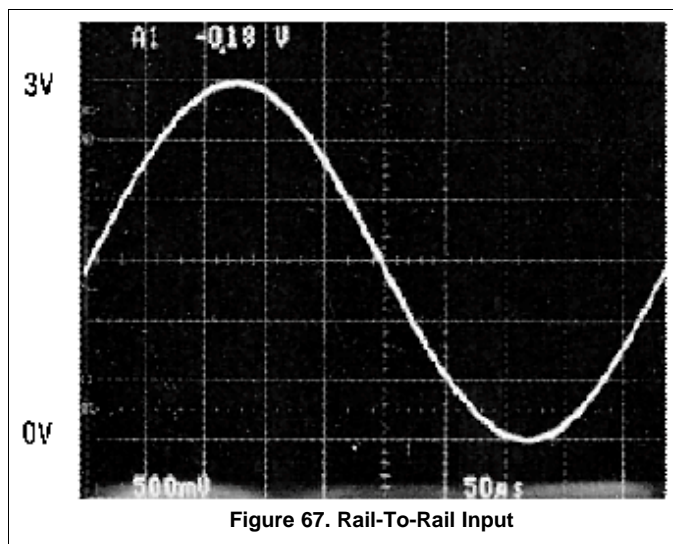


Figure 66. Noninverting Configuration Offset Voltage Adjustment

## Typical Applications (continued)

### 8.2.1.3 Application Curves



### 8.2.2 Typical Single-Supply Applications

The circuit in Figure 69 uses a single supply to half-wave rectify a sinusoid centered about ground.  $R_1$  limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full-wave rectification is provided by the circuit in Figure 71.

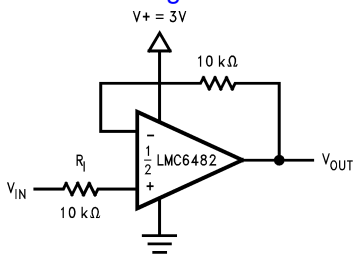
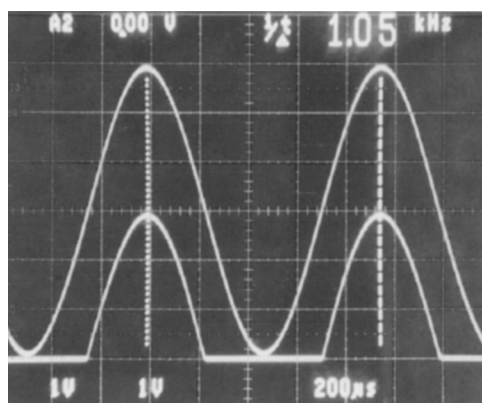
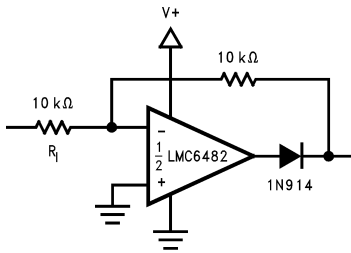


Figure 69. Half-Wave Rectifier With Input Current Protection ( $R_1$ )

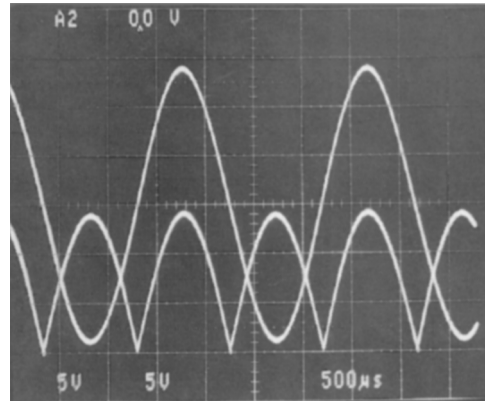


**Typical Applications (continued)**

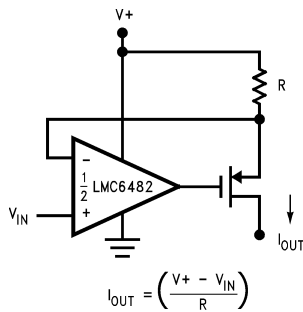
In [Figure 75](#) dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of  $C_H$  and diode leakage current. The ultra-low input current of the LMC6482 has a negligible effect on droop.



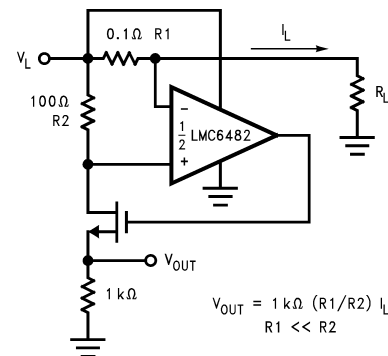
**Figure 71. Full-Wave Rectifier With Input Current Protection ( $R_1$ )**



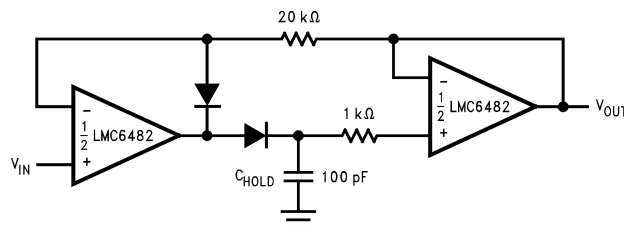
**Figure 72. Full-Wave Rectifier Waveform**



**Figure 73. Large Compliance Range Current Source**



**Figure 74. Positive Supply Current Sense**



**Figure 75. Low-Voltage Peak Detector With Rail-To-Rail Peak Capture Range**

### Typical Applications (continued)

The high CMRR (82 dB) of the LMC6482 allows excellent accuracy throughout the rail-to-rail dynamic capture range of the circuit.

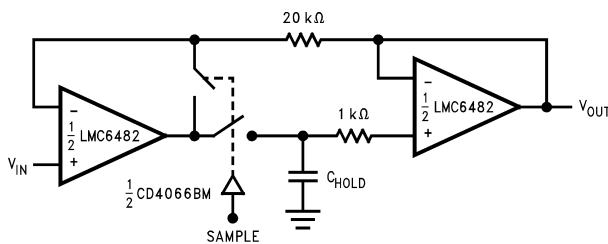


Figure 76. Rail-To-Rail Sample and Hold

The low-pass filter circuit in Figure 77 can be used as an antialiasing filter with the same voltage supply as the A/D converter.

Filter designs can also take advantage of the LMC6482 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors that take less board space and cost less.

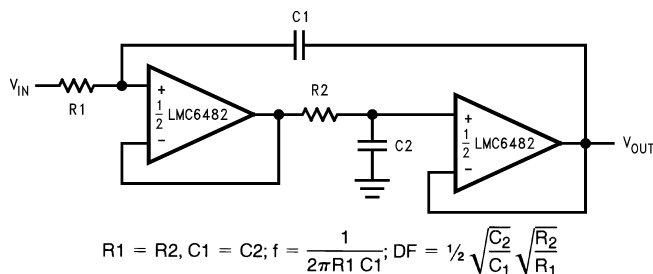


Figure 77. Rail-To-Rail Single Supply Low Pass Filter

## 9 Power Supply Recommendations

The LMC6482 can be operated over a supply range of 3 V to 15 V. To achieve noise immunity as appropriate to the application, make sure to use good PCB layout practices for power supply rails and planes, as well as using bypass capacitors connected between the power supply pins and ground.

## 10 Layout

### 10.1 Layout Guidelines

It is generally recognized that any circuit that must operate with less than 1000 pA of leakage current requires special layout of the PC board. To take advantage of the ultra-low input current of the LMC6482, typically less than 20 fA, an excellent layout is essential. Fortunately, the techniques of obtaining low leakages are quite simple. First, do not ignore the surface leakage of the PCB. Even though the leakage current may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LM6482s inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and so forth connected to the inputs of the op amp, as in [Figure 78](#). To have a significant effect, place guard rings on both the top and bottom of the PCB. This PC foil must then be connected to a voltage that is at the same voltage as the amplifier inputs, because no leakage current can flow between two points at the same potential. For example, a PCB trace-to-pad resistance of  $10^{12} \Omega$ , which is normally considered a very large resistance, could leak 5 pA if the trace were a 5-V bus adjacent to the pad of the input. This leakage would cause a 250 times degradation from the actual performance of the LMC6482. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of  $10^{11} \Omega$  causes only 0.05 pA of leakage current. See [Figure 79](#) through [Figure 81](#) for typical connections of guard rings for standard op-amp configurations.

Be aware that when it is inappropriate to lay out a PCB for the sake of just a few circuits, another technique is even better than a guard ring on a PCB: Do not insert the input pin of the amplifier into the PCB at all, but bend it up in the air, and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PCB construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See [Figure 82](#).

### 10.2 Layout Example

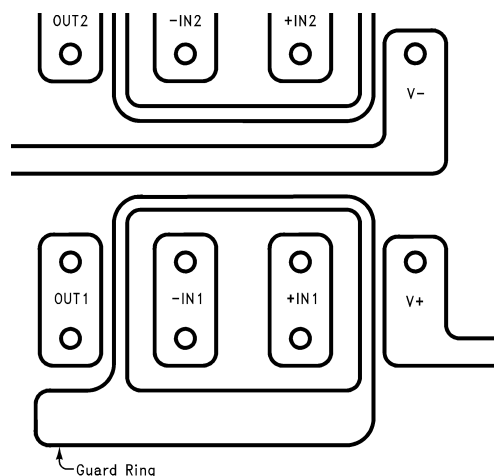
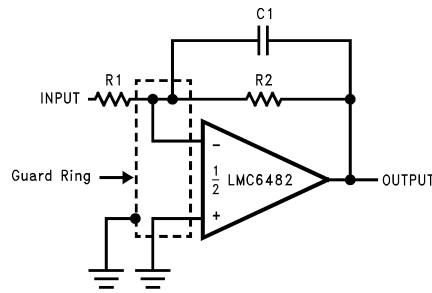


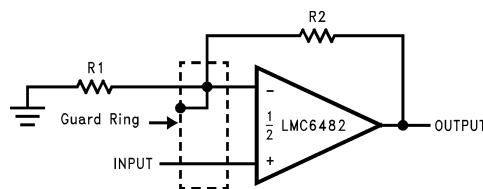
Figure 78. Example of Guard Ring in PCB Layout Typical Connections of Guard Rings



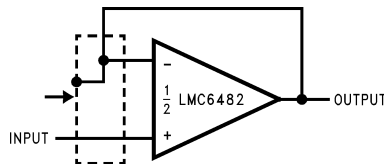
**Layout Example (continued)**



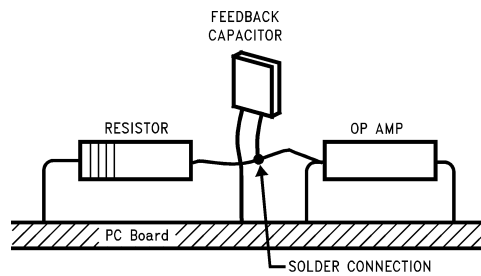
**Figure 79. Inverting Amplifier Typical Connections of Guard Rings**



**Figure 80. Noninverting Amplifier Typical Connections of Guard Rings**



**Figure 81. Follower Typical Connections of Guard Rings**



NOTE: Input pins are lifted out of PCB and soldered directly to components. All other pins connected to PCB.

**Figure 82. Air Wiring**

## 11 デバイスおよびドキュメントのサポート

### 11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 11.2 サポート・リソース

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 11.3 商標

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.4 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件 ([www.tij.co.jp/ja-jp/legal/termssofsale.html](http://www.tij.co.jp/ja-jp/legal/termssofsale.html))、または [ti.com](http://ti.com) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

Copyright © 2020, Texas Instruments Incorporated  
日本語版 日本テキサス・インスツルメンツ株式会社

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6482AIM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMC6482AIM	
LMC6482AIM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC6482AIM	<a href="#">Samples</a>
LMC6482AIMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMC6482AIM	
LMC6482AIMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC6482AIM	<a href="#">Samples</a>
LMC6482AIN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 85	LMC6482AIN	<a href="#">Samples</a>
LMC6482IM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMC6482IM	
LMC6482IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC6482IM	<a href="#">Samples</a>
LMC6482IMM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	A10	
LMC6482IMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	A10	<a href="#">Samples</a>
LMC6482IMMX	NRND	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 85	A10	
LMC6482IMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	A10	<a href="#">Samples</a>
LMC6482IMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMC6482IMX	
LMC6482IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	LMC6482IMX	<a href="#">Samples</a>
LMC6482IN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	Call TI   SN	Level-1-NA-UNLIM	-40 to 85	LMC6482IN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6482AIMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6482AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6482IMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6482IMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6482IMMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6482IMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6482IMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6482IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6482AIMX	SOIC	D	8	2500	367.0	367.0	35.0
LMC6482AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6482IMM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMC6482IMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMC6482IMMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC6482IMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC6482IMX	SOIC	D	8	2500	367.0	367.0	35.0
LMC6482IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0



# D0008A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

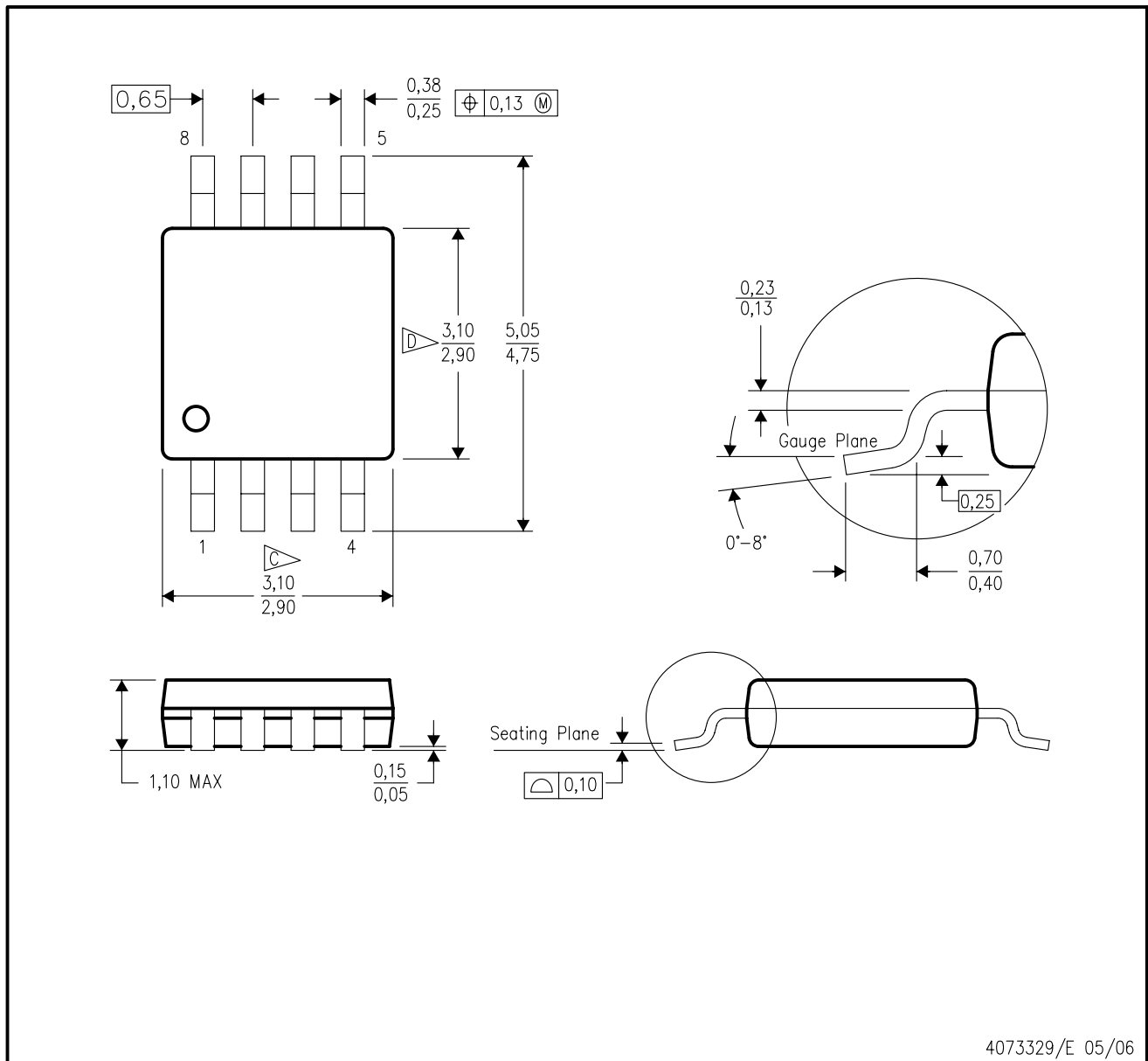
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件 ([www.tij.co.jp/ja-jp/legal/termsofsale.html](http://www.tij.co.jp/ja-jp/legal/termsofsale.html))、または [ti.com](http://ti.com) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

Copyright © 2020, Texas Instruments Incorporated

日本語版 日本テキサス・インスツルメンツ株式会社