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## I<sup>2</sup>C-Compatible (2-wire) Serial EEPROM

### 2-Kbit (256 x 8)

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## DATASHEET

### Features

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- Write Protect pin for hardware data protection
  - Utilizes different array protection compared to the AT24C02C
- Low-voltage operation
  - $V_{CC} = 1.7V$  to  $5.5V$
- Internally organized as 128 x 8 (1K) or 256 x 8 (2K)
- I<sup>2</sup>C compatible (2-wire) serial interface
- Schmitt Trigger, filtered inputs for noise suppression
- Bidirectional data transfer protocol
- 400kHz (1.7V) and 1MHz (2.5V, 2.7V, 5.0V) compatibility
- 8-byte Page Write mode
  - Partial Page Writes allowed
- Self-timed write cycle (5ms max)
- High-reliability
  - Endurance: 1,000,000 write cycles
  - Data retention: 100 years
- Green package options (Pb/Halide-free/RoHS-compliant)
  - 8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP
- Die sale options: wafer form and tape and reel available

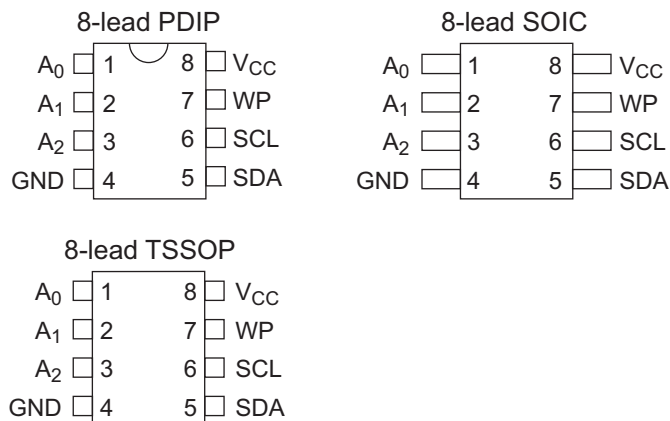
### Description

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The Atmel® AT24HC02C provides 2048-bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 256 words of eight bits each. The device include a cascading feature that allows up to eight devices to share a common 2-wire bus. These devices are optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24HC02C are available in space saving 8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP packages. In addition, the product operates from 1.7V to 5.5V  $V_{CC}$ .

## 1. Pin Configurations and Pinouts

Pin Name	Function
A <sub>0</sub> - A <sub>2</sub>	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
GND	Ground
V <sub>CC</sub>	Power Supply

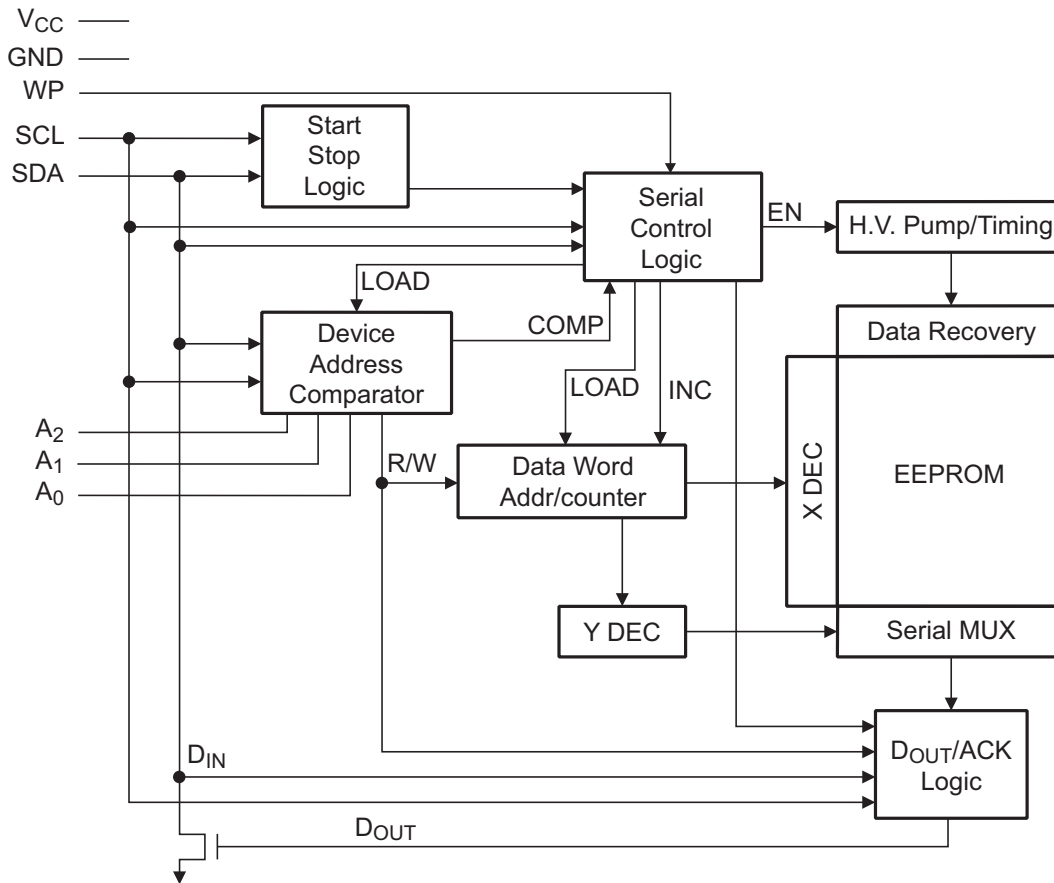


## 2. Absolute Maximum Ratings

Operating Temperature .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on any pin with respect to ground .....	-1.0V to +7.0V
Maximum Operating Voltage .....	6.25V
DC Output Current.....	5.0mA

\*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 3. Block Diagram



### 4. Pin Description

**Serial Clock (SCL):** The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

**Serial Data (SDA):** The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-ORed with any number of other open drain or open collector devices.

**Device Addresses (A<sub>2</sub>, A<sub>1</sub>, A<sub>0</sub>):** The A<sub>2</sub>, A<sub>1</sub>, and A<sub>0</sub> pins are device address inputs that are hard wired for the AT24HC02C. As many as eight 2-Kbit devices may be addressed on a single bus system. See [Section 7. “Device Addressing” on page 9](#) for more details.

**Write Protect (WP):** The AT24HC02C have a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V<sub>CC</sub>, the write protection feature is enabled and operates as shown below in [Table 4-1](#).

**Table 4-1. Write Protect**

WP Pin Status	Part of the Array Protected
	Atmel AT24HC02C
At V <sub>CC</sub>	Upper Half (1K) of Array
At GND	Normal Read/Write Operations

## 5. Memory Organization

**Atmel AT24HC02C, 2K Serial EEPROM:** Internally organized with 32 pages of 8-bytes each, the 2K requires an 8-bit data word address for random word addressing.

**Table 5-1. Pin Capacitance<sup>(1)</sup>**

Applicable over recommended operating range from  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ ,  $V_{CC} = 1.7\text{V}$  to  $5.5\text{V}$

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0\text{V}$
$C_{IN}$	Input Capacitance ( $A_0, A_1, A_2, \text{SCL}$ )	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

**Table 5-2. DC Characteristics**

Applicable over recommended operating range from:  $T_{AI} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 1.7\text{V}$  to  $5.5\text{V}$  (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$V_{CC1}$	Supply Voltage		1.7		5.5	V
$V_{CC2}$	Supply Voltage		2.5		5.5	V
$V_{CC3}$	Supply Voltage		4.5		5.5	V
$I_{CC1}$	Supply Current $V_{CC} = 5.0\text{V}$	Read at 400kHz		0.4	1.0	mA
$I_{CC2}$	Supply Current $V_{CC} = 5.0\text{V}$	Write at 400kHz		2.0	3.0	mA
$I_{SB1}$	Standby Current $V_{CC} = 1.7\text{V}$	$V_{IN} = V_{CC}$ or $V_{SS}$			1.0	$\mu\text{A}$
$I_{SB2}$	Standby Current $V_{CC} = 2.5\text{V}$	$V_{IN} = V_{CC}$ or $V_{SS}$			2.0	$\mu\text{A}$
$I_{SB3}$	Standby Current $V_{CC} = 5.5\text{V}$	$V_{IN} = V_{CC}$ or $V_{SS}$			6.0	$\mu\text{A}$
$I_{LI}$	Input Leakage Current	$V_{IN} = V_{CC}$ or $V_{SS}$		0.10	3.0	$\mu\text{A}$
$I_{LO}$	Output Leakage Current	$V_{OUT} = V_{CC}$ or $V_{SS}$		0.05	3.0	$\mu\text{A}$
$V_{IL}$	Input Low Level <sup>(1)</sup>		-0.6		$V_{CC} \times 0.3$	V
$V_{IH}$	Input High Level <sup>(1)</sup>		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
$V_{OL1}$	Output Low Level $V_{CC} = 1.7\text{V}$	$I_{OL} = 0.15\text{mA}$			0.2	V
$V_{OL2}$	Output Low Level $V_{CC} = 3.0\text{V}$	$I_{OL} = 2.1\text{mA}$			0.4	V

Note: 1.  $V_{IL}$  min and  $V_{IH}$  max are reference only and are not tested.

**Table 5-3. AC Characteristics**

Applicable over recommended operating range from  $T_{AI} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 1.7\text{V}$  to  $5.5\text{V}$ ,  $CL = 1\text{TTL Gate}$  and  $100\text{pF}$  (unless otherwise noted). Test conditions are listed in [Note 2](#).

Symbol	Parameter	1.7V		2.5V, 5.0V		Units
		Min	Max	Min	Max	
$f_{SCL}$	Clock Frequency, SCL		400		1000	kHz
$t_{LOW}$	Clock Pulse Width Low	1.2		0.4		$\mu\text{s}$
$t_{HIGH}$	Clock Pulse Width High	0.6		0.4		$\mu\text{s}$
$t_i$	Noise Suppression Time		100		50	ns
$t_{AA}$	Clock Low to Data Out Valid	0.1	0.9	0.05	0.55	$\mu\text{s}$
$t_{BUF}$	Time the bus must be free before a new transmission can start.	1.2		0.5		$\mu\text{s}$
$t_{HD,STA}$	Start Hold Time	0.6		0.25		$\mu\text{s}$
$t_{SU,STA}$	Start Setup Time	0.6		0.25		$\mu\text{s}$
$t_{HD,DAT}$	Data In Hold Time	0		0		$\mu\text{s}$
$t_{SU,DAT}$	Data In Setup Time	100		100		ns
$t_R$	Inputs Rise Time <sup>(1)</sup>		0.3		0.3	$\mu\text{s}$
$t_F$	Inputs Fall Time <sup>(1)</sup>		300		100	ns
$t_{SU,STO}$	Stop Setup Time	0.6		.25		$\mu\text{s}$
$t_{DH}$	Data Out Hold Time	50		50		ns
$t_{WR}$	Write Cycle Time		5		5	ms
Endurance <sup>(1)</sup>	25°C, Page Mode, 3.3V	1,000,000				Write Cycles

- Note:
- This parameter is ensured by characterization only.
  - AC measurement conditions:
    - $R_L$  (connects to  $V_{CC}$ ):  $1.3\text{ k}\Omega$  (2.5V, 5V),  $10\text{ k}\Omega$  (1.7V)
    - Input pulse voltages:  $0.3 V_{CC}$  to  $0.7 V_{CC}$
    - Input rise and fall times:  $\leq 50\text{ns}$
    - Input and output timing reference voltages:  $0.5 V_{CC}$

## 6. Device Operation

**Clock and Data Transitions:** The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see [Figure 6-4 on page 8](#)). Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

**Start Condition:** A high-to-low transition of SDA with SCL high is a Start condition which must precede any other command (see [Figure 6-5 on page 8](#)).

**Stop Condition:** A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the Stop command will place the EEPROM in a standby power mode (see [Figure 6-5 on page 8](#)).

**Acknowledge:** All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

**Standby Mode:** The AT24HC02C features a low power standby mode which is enabled:

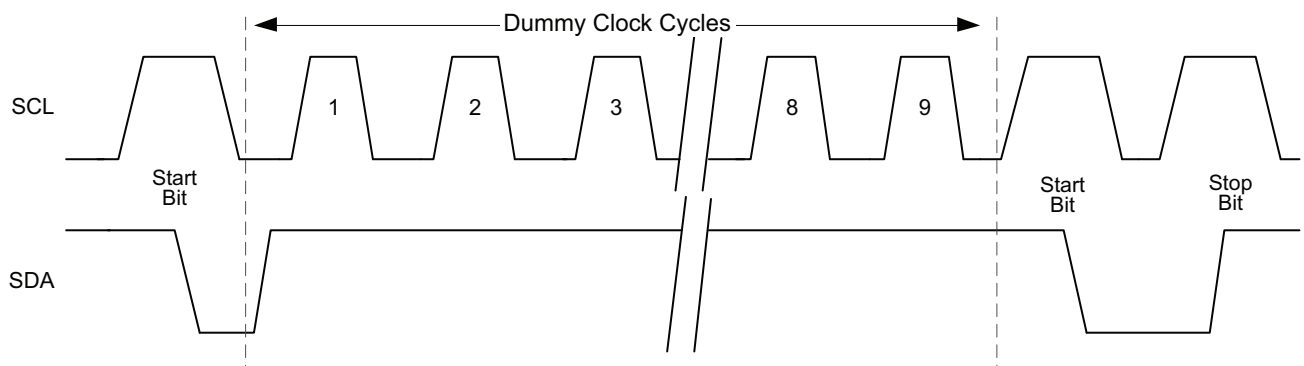
- Upon power-up
- After the receipt of the stop bit and the completion of any internal operations

**2-wire Software Reset:** After an interruption in protocol, power loss, or system reset, any 2-wire part can be reset by following these steps:

1. Create a start bit condition
2. Clock nine cycles
3. Create another start bit followed by stop bit condition as shown in [Figure 6-1](#).

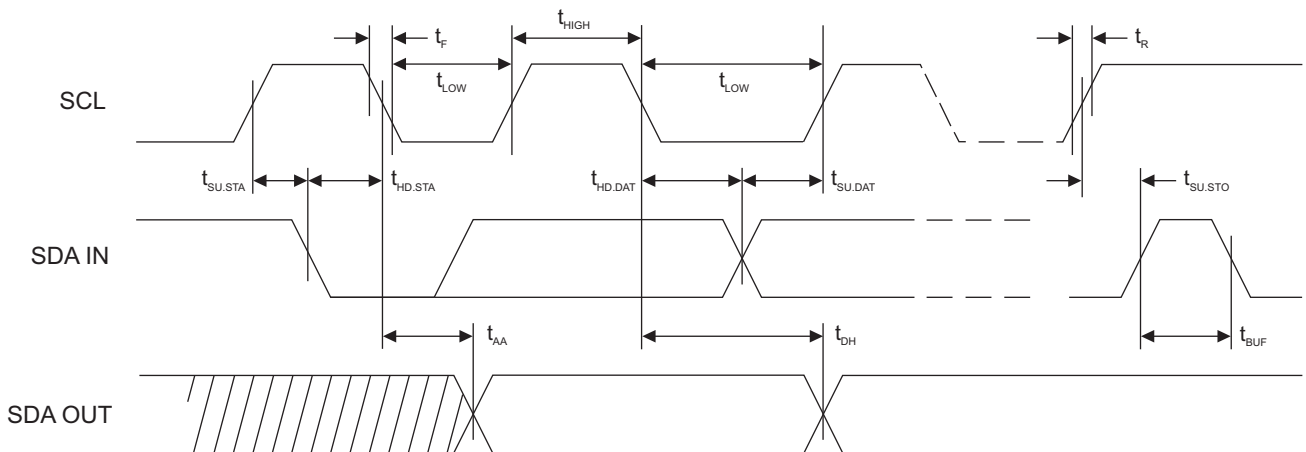
The device is ready for the next communication after above steps have been completed.

**Figure 6-1. Software reset**



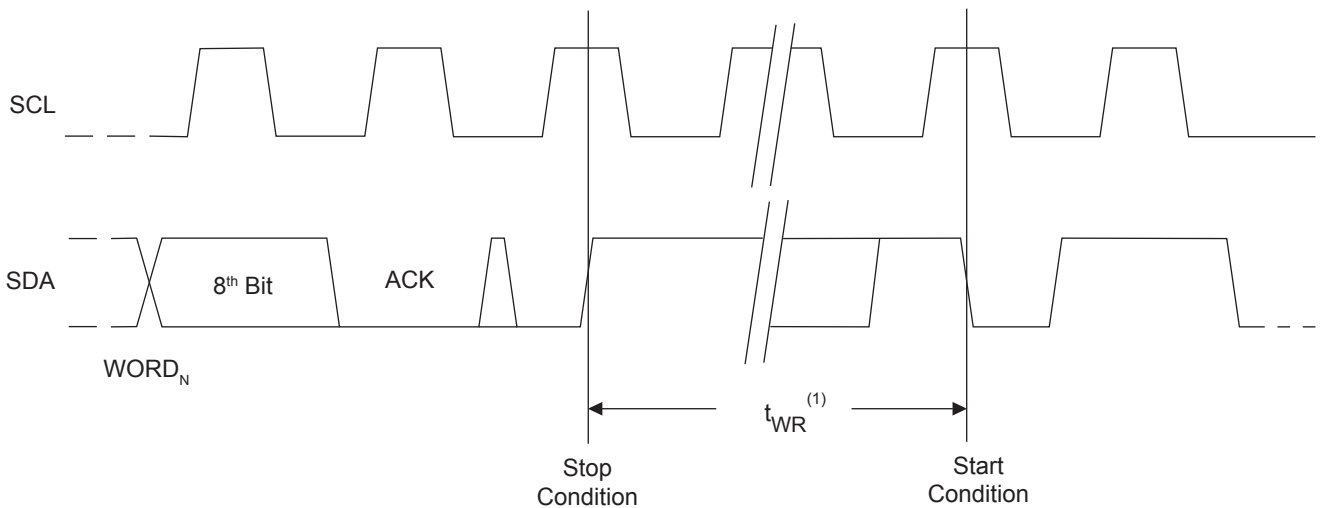
**Figure 6-2. Bus Timing**

SCL: Serial Clock, SDA: Serial Data I/O



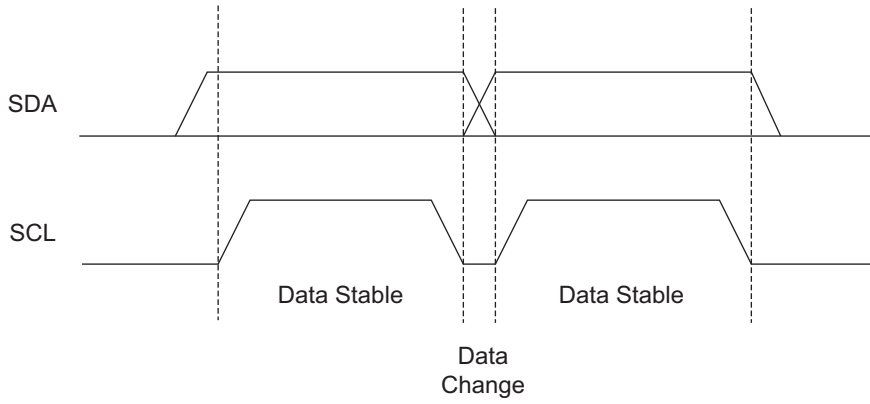
**Figure 6-3. Write Cycle Timing**

SCL: Serial Clock, SDA: Serial Data I/O

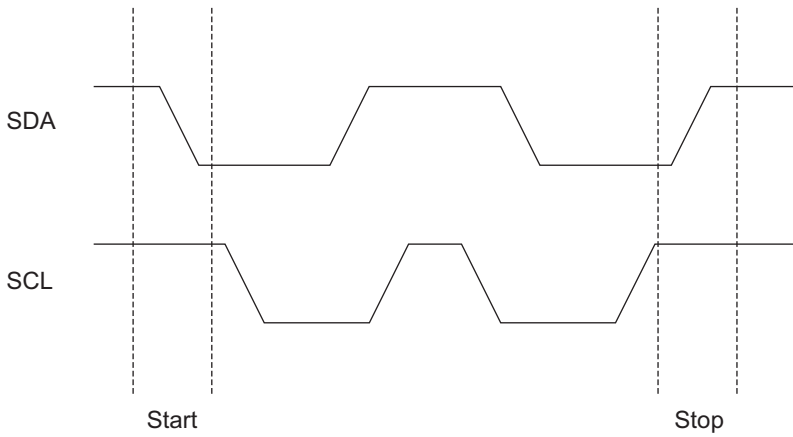


Notes: 1. The write cycle time  $t_{WR}$  is the time from a valid Stop condition of a write sequence to the end of the internal clear/write cycle.

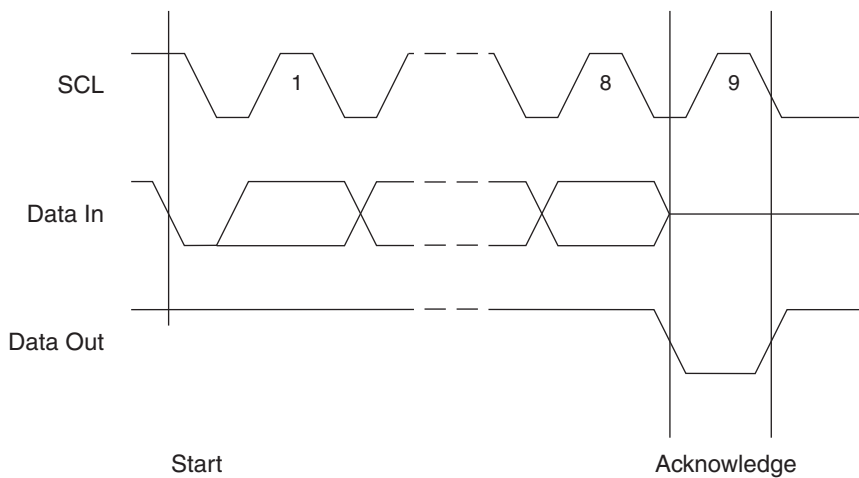
**Figure 6-4. Data Validity**



**Figure 6-5. Start and Stop Definition**



**Figure 6-6. Output Acknowledge**





## 7. Device Addressing

The 2-Kbit EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a Read or Write operation.

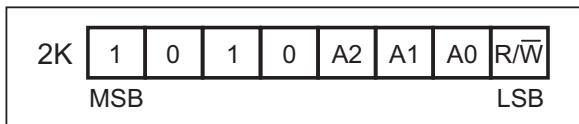
The device address word consists of a mandatory '1010' (Ah) sequence for the first four most significant bits as shown in Figure 7-1. This is common to all Serial EEPROM devices.

The next three bits are the A<sub>2</sub>, A<sub>1</sub>, and A<sub>0</sub> device address bits for the EEPROM. These three bits must compare to their corresponding hard-wired input pins A<sub>2</sub>, A<sub>1</sub>, and A<sub>0</sub> in order for the part to acknowledge.

The eighth bit of the device address is the Read/Write operation select bit. A Read operation is initiated if this bit is high and a Write operation is initiated if this bit is low.

Upon a valid compare of the device address with hard-wired input pins A<sub>2</sub>, A<sub>1</sub>, and A<sub>0</sub>, the EEPROM will output a zero. If a compare is not successfully made, the chip will return to a standby state.

Figure 7-1. Device Address



## 8. Write Operations

**Byte Write:** A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a Stop condition. At this time, the EEPROM enters an internally timed write cycle,  $t_{WR}$ , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 9-1 on page 10).

**Page Write:** The 2-Kbit EEPROM is capable of an 8-byte Page Write.

A Page Write is initiated the same as a Byte Write, but the microcontroller does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a Stop condition (see Figure 9-2 on page 10).

The data word address lower three bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

**Acknowledge Polling:** Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a Start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

**Data Security:** The Atmel AT24HC02C has a hardware data protection scheme that allows the user to write protect the upper half of the memory (80h - FFh) when the WP pin is at  $V_{CC}$ .

## 9. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: Current Address Read, Random Address Read, and Sequential Read.

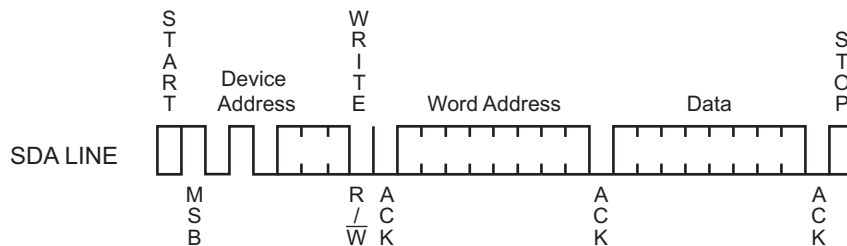
**Current Address Read:** The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page to the first byte of the first page. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with a zero but does generate a following Stop condition (see [Figure 9-3 on page 11](#)).

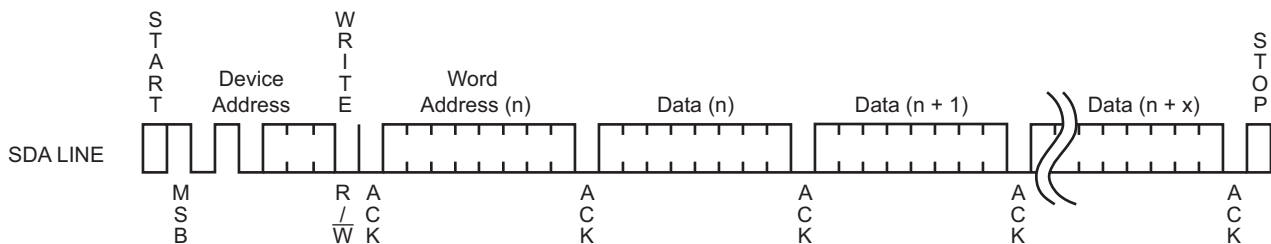
**Random Read:** A Random Read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a Current Address Read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see [Figure 9-4 on page 11](#)).

**Sequential Read:** Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see [Figure 9-5 on page 11](#)).

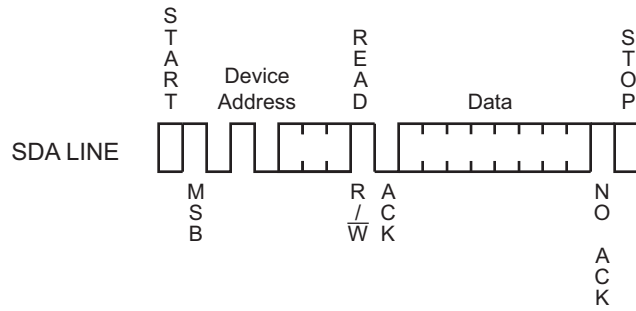
**Figure 9-1. Byte Write**



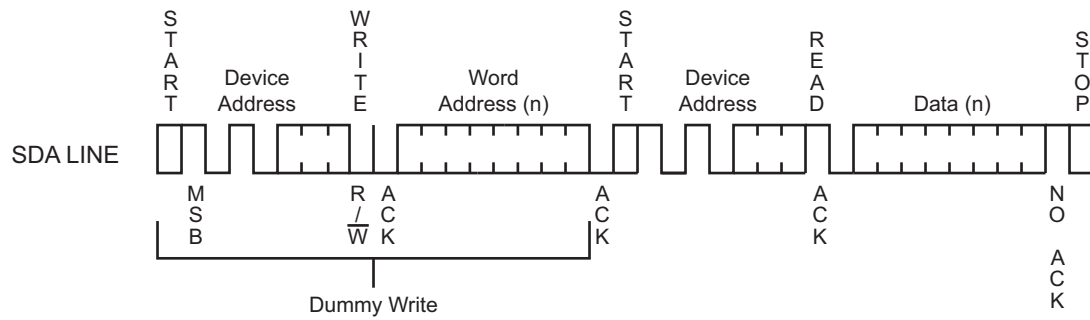
**Figure 9-2. Page Write**



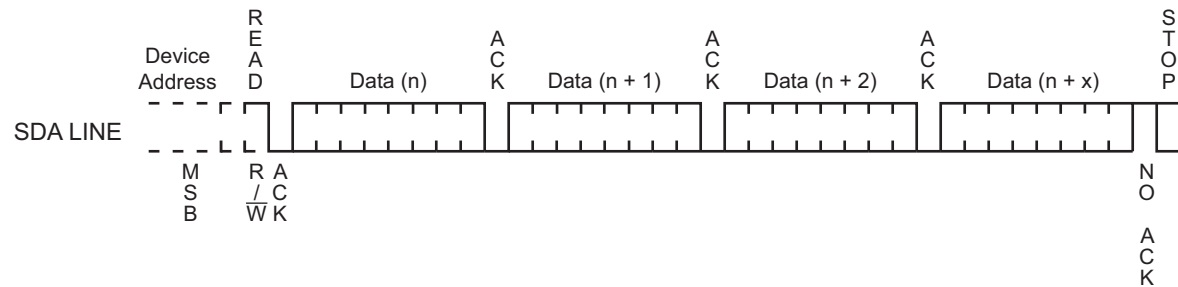
**Figure 9-3. Current Address Read**



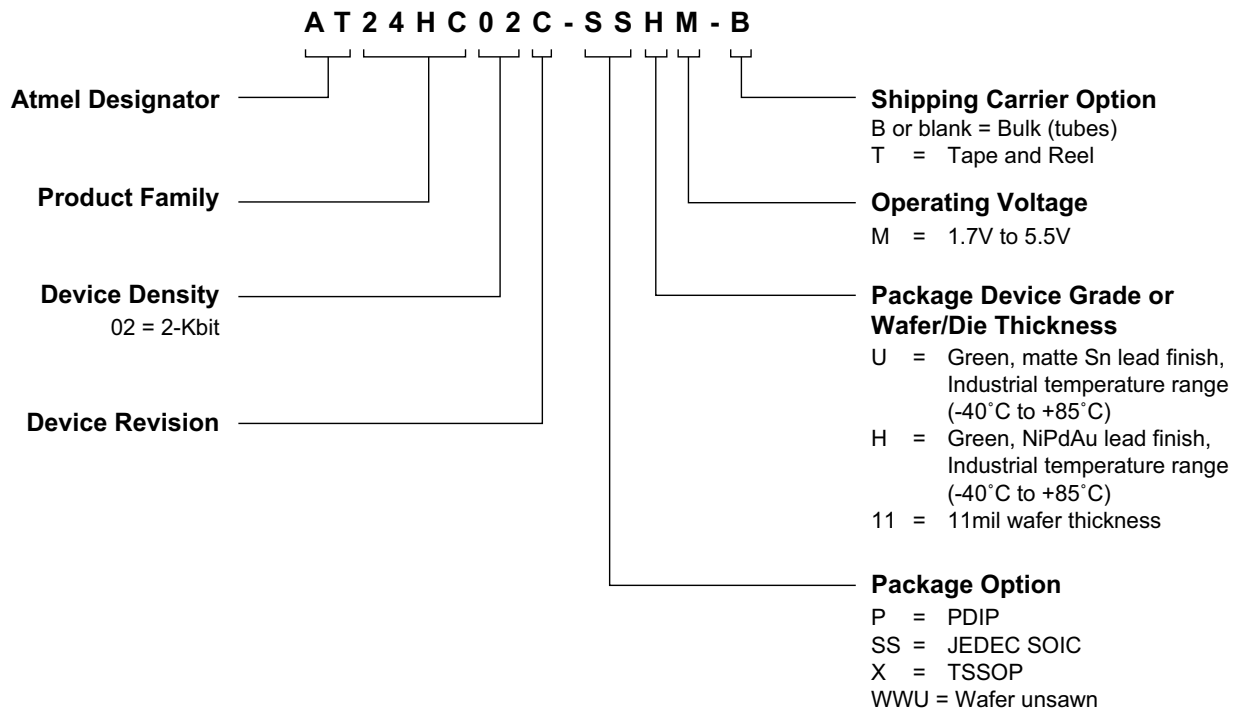
**Figure 9-4. Random Read**



**Figure 9-5. Sequential Read**

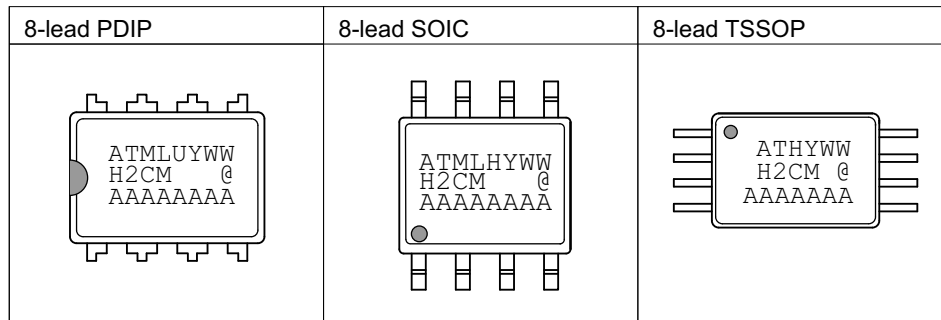


## 10. Ordering Code Detail



# 11. Part Markings

## AT24HC02C: Package Marking Information



Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

Catalog Number Truncation			
AT24HC02C		Truncation Code ###: H2C	
Date Codes			Voltages
Y = Year	M = Month	WW = Work Week of Assembly	M: 1.7V min
2: 2012    6: 2016	A: January	02: Week 2	
3: 2013    7: 2017	B: February	04: Week 4	
4: 2014    8: 2018	...	...	
5: 2015    9: 2019	L: December	52: Week 52	
Country of Assembly		Lot Number	Grade/Lead Finish Material
@ = Country of Assembly		AAA...A = Atmel Wafer Lot Number	U: Industrial/Matte Tin H: Industrial/NiPdAu
Trace Code			Atmel Truncation
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

5/21/12

 Package Mark Contact: DL-CSO-Assy_eng@atmel.com	TITLE	DRAWING NO.	REV.
	24HC02CSM, AT24HC02C Package Marking Information	24HC02CSM	B

## 12. Ordering Codes

### 12.1 Atmel AT24HC02C Ordering Information

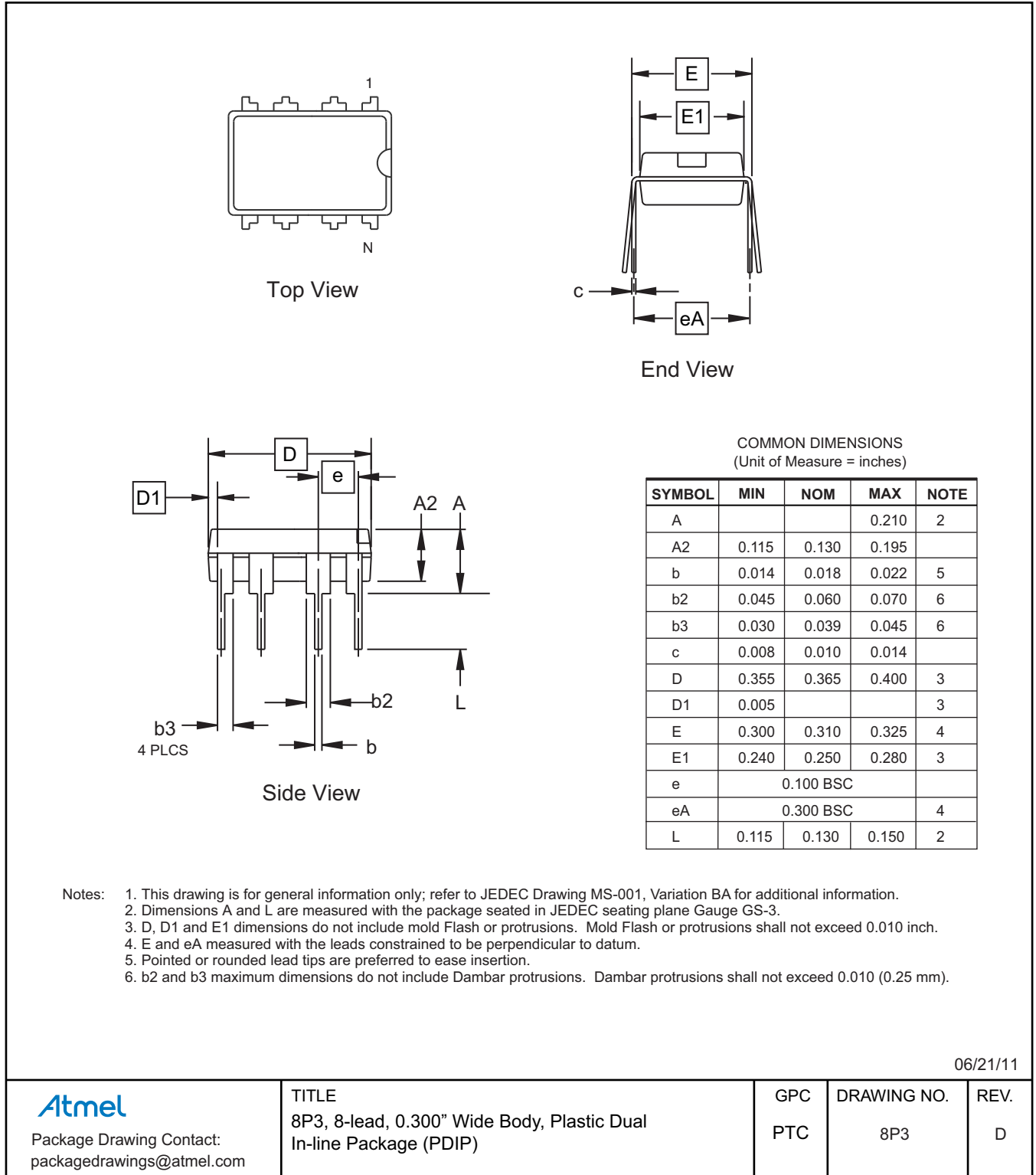
Ordering Code	Lead Finish	Package	Voltage	Operation Range
AT24HC02C-PUM	Matte Tin (Lead-free/Halogen-free)	8P3	1.7V to 5.5V	Industrial Temperature (-40°C to 85°C)
AT24HC02C-SSHM-B <sup>(1)</sup>	NiPdAu (Lead-free/Halogen-free)	8S1		
AT24HC02C-SSHM-T <sup>(2)</sup>				
AT24HC02C-XHM-B <sup>(1)</sup>		8X		
AT24HC02C-XHM-T <sup>(2)</sup>				
AT24HC02C-WWU11M <sup>(3)</sup>	—	Wafer Sale		

- Notes:
1. B = Bulk (tubes)
  2. T = Tape and reel
    - SOIC = 4K per reel
    - TSSOP = 5K per reel
  3. For Wafer sales, please contact Atmel Sales.

Package Type	
<b>8P3</b>	8-lead, 0.300" wide, Plastic Dual Inline (PDIP)
<b>8S1</b>	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
<b>8X</b>	8-lead, 4.4mm body, Plastic Thin Shrink Small Outline (TSSOP)

# 13. Packaging Information

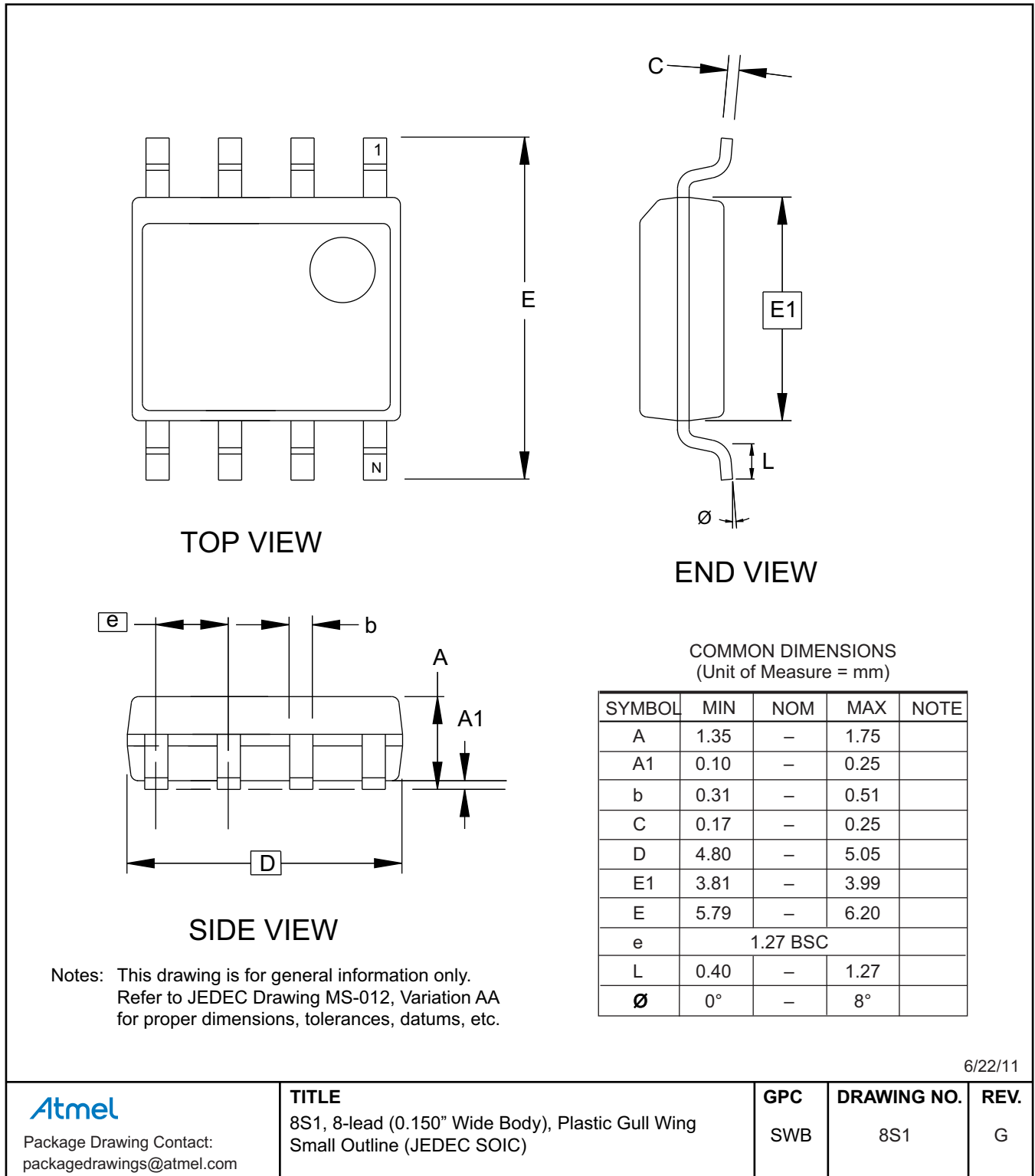
## 13.1 8P3 — 8-lead PDIP



06/21/11

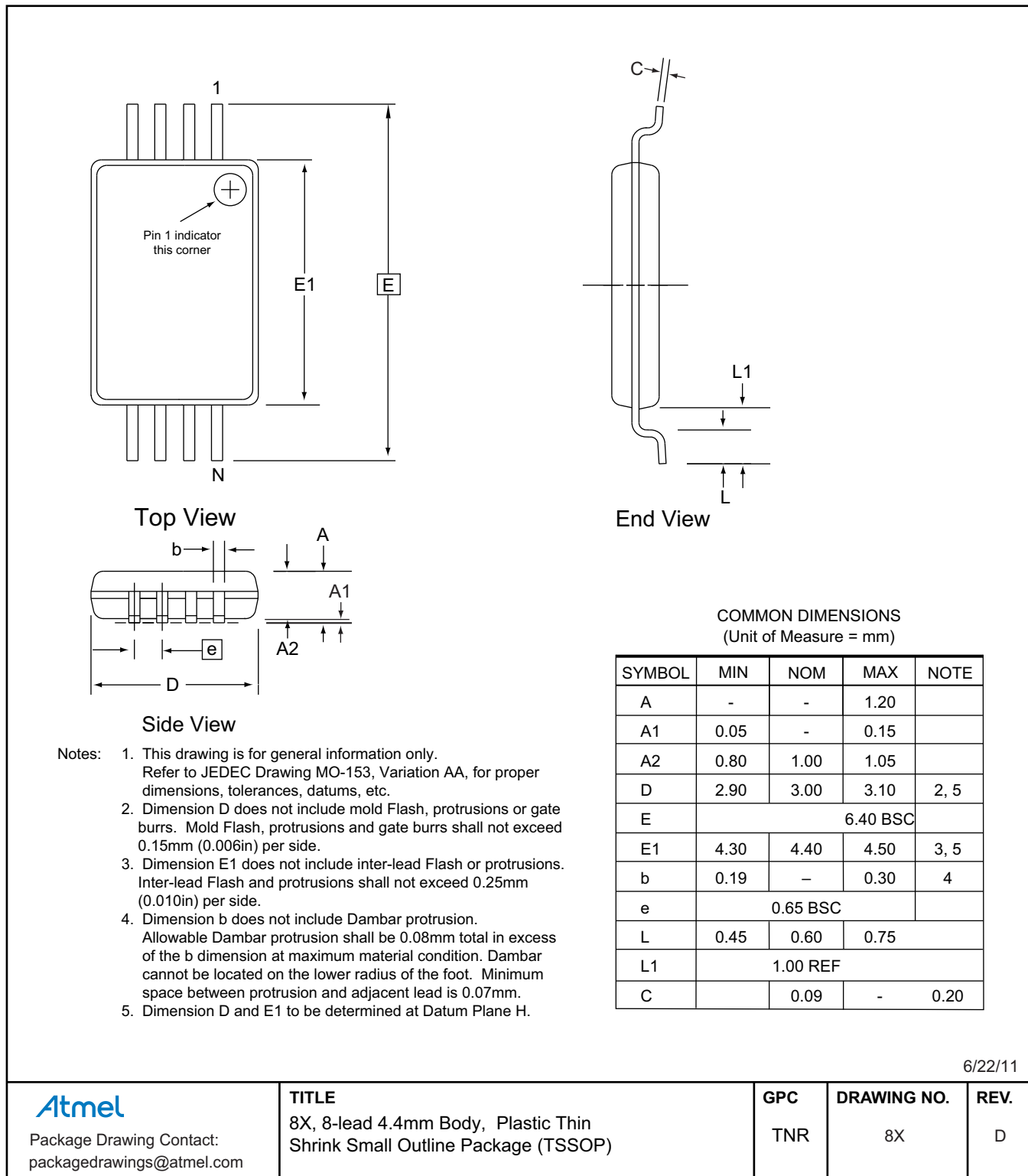
<p>Package Drawing Contact: packagedrawings@atmel.com</p>	TITLE	GPC	DRAWING NO.	REV.
	8P3, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	PTC	8P3	D

## 13.2 8S1 — 8-lead JEDEC SOIC





### 13.3 8X — 8-lead TSSOP



## 14. Revision History

Doc. Rev.	Date	Comments
8779B	04/2013	Corrected Write Protect address range. Update footers and disclaimer page.
8779A	06/2012	Initial document release.



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