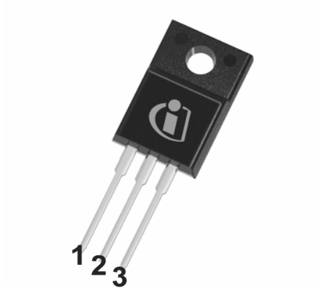
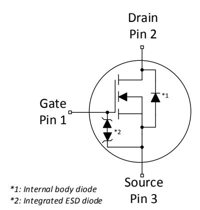
MOSFET

700V CoolMOS™ P7 Power Device

PG-TO 220 FP



CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.
The latest CoolMOS™ P7 is an optimized platform tailored to target cost sensitive applications in consumer markets such as charger, adapter, lighting, TV, etc.
The new series provides all the benefits of a fast switching Superjunction MOSFET, combined with an excellent price/performance ratio and state of the art ease-of-use level. The technology meets highest efficiency standards and supports high power density, enabling customers going towards very slim designs.



Features

- Extremely low losses due to very low FOM $R_{DS(on)}$*Q_g and $R_{DS(on)}$*E_{oss}
- Excellent thermal behavior
- Integrated ESD protection diode
- Low switching losses (E_{oss})
- Product validation acc. JEDEC Standard

Benefits

- Cost competitive technology
- Lower temperature
- High ESD ruggedness
- Enables efficiency gains at higher switching frequencies
- Enables high power density designs and small form factors

Potential applications

Recommended for Flyback topologies for example used in Chargers, Adapters, Lighting Applications, etc.

Product validation

Qualified according to JEDEC Standard

Please note: For MOSFET paralleling the use of ferrite beads on the gate or seperate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j=25°C}$	700	V
$R_{DS(on),max}$	0.45	Ω
$Q_{g,typ}$	13.1	nC
$I_{D,pulse}$	26	A
E_{oss} @ 400V	1.4	µJ
$V_{(GS)th,typ}$	3	V
ESD class (HBM)	2	

Type / Ordering Code	Package	Marking	Related Links
IPA70R450P7S	PG-TO 220 FullPAK	70S450P7	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	10.0 6.5	A	T_C = 20°C T_C = 100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	25.9	A	T_C=25°C
Application (Flyback) relevant avalanche current, single pulse[3]	I_{AS}	-	-	3.5	A	measured with standard leakage inductance of transformer of 7µH
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	V_{DS} =0...400V
Gate source voltage	V_{GS}	-16 -30	- -	16 30	V	static; AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	22.7	W	T_C=25°C
Operating and storage temperature	T_j, T_{stg}	-40	-	150	°C	-
Continuous diode forward current	I_S	-	-	4.7	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	25.9	A	T_C = 25°C
Reverse diode dv/dt[4]	dv/dt	-	-	1	V/ns	V_{DS} =0...400V, I_{SD}<=I_S, T_j=25°C
Maximum diode commutation speed[4]	di_f/dt	-	-	50	A/µs	V_{DS} =0...400V, I_{SD}<=I_S, T_j=25°C
Insulation withstand voltage	V_{ISO}	-	-	2500	V	V_{rms}, T_C=25°C, t=1min

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction	R_{thJC}	-	-	5.5	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10s

1) DPAK / IPAK equivalent. Limited by $T_{j\,max}$. T_j = 20°C. Maximum duty cycle D=0.5
2) Pulse width t_p limited by $T_{j,max}$
3) Proven during verification test. For explanation please read AN - CoolMOS™ 700V P7.
4) V_{DClink}=400V; $V_{DS,peak}$<$V_{(BR)DSS}$; identical low side and high side switch with identical R_G

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	700	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	2.50	3	3.50	V	V_{DS}=V_{GS}, I_D=0.12mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=700V, V_{GS}=0V, T_j=25°C V_{DS}=700V, V_{GS}=0V, T_j=150°C
Gate-source leakage current incl. Zener diode	I_{GSS}	-	-	1	µA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.37 0.84	0.45 -	Ω	V_{GS}=10V, I_D=2.3A, T_j=25°C V_{GS}=10V, I_D=2.3A, T_j=150°C
Gate resistance	R_G	-	10	-	Ω	f=1 MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	424	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	8	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	21	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	251	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	16	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=1.7A, R_G=5.3Ω
Rise time	t_r	-	6.5	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=1.7A, R_G=5.3Ω
Turn-off delay time	$t_{d(off)}$	-	70	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=1.7A, R_G=5.3Ω
Fall time	t_f	-	20	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=1.7A, R_G=5.3Ω

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1.9	-	nC	V_{DD}=400V, I_D=1.7A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	5.0	-	nC	V_{DD}=400V, I_D=1.7A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	13.1	-	nC	V_{DD}=400V, I_D=1.7A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	V_{DD}=400V, I_D=1.7A, V_{GS}=0 to 10V

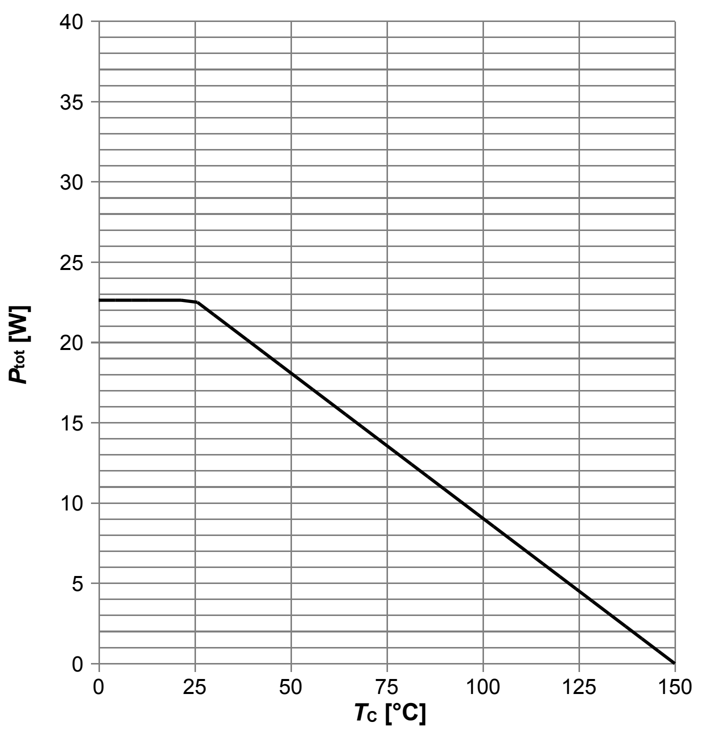
[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=2.6A, T_j=25°C
Reverse recovery time	t_{rr}	-	200	-	ns	V_R=400V, I_F=1.7A, di_F/dt=50A/µs
Reverse recovery charge	Q_{rr}	-	0.7	-	µC	V_R=400V, I_F=1.7A, di_F/dt=50A/µs
Peak reverse recovery current	I_{rrm}	-	8	-	A	V_R=400V, I_F=1.7A, di_F/dt=50A/µs

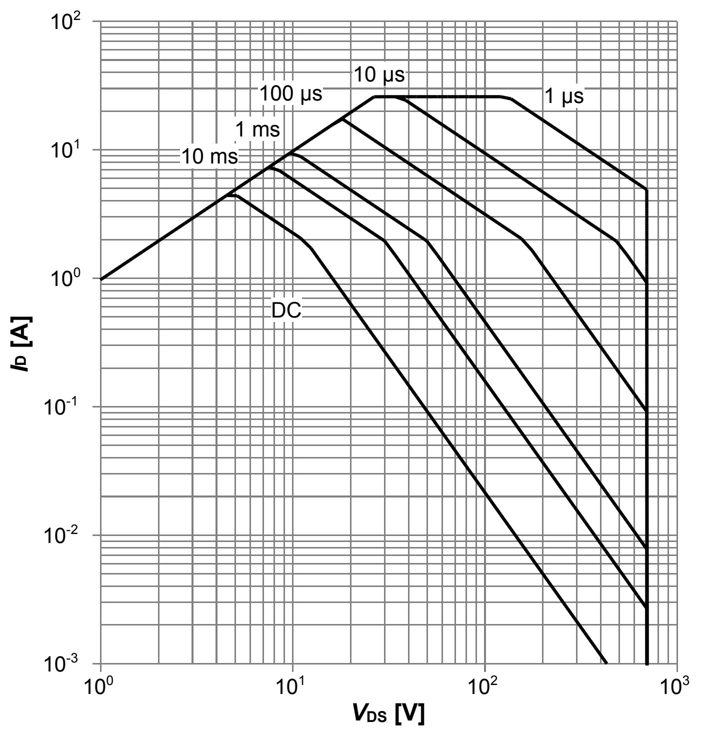
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



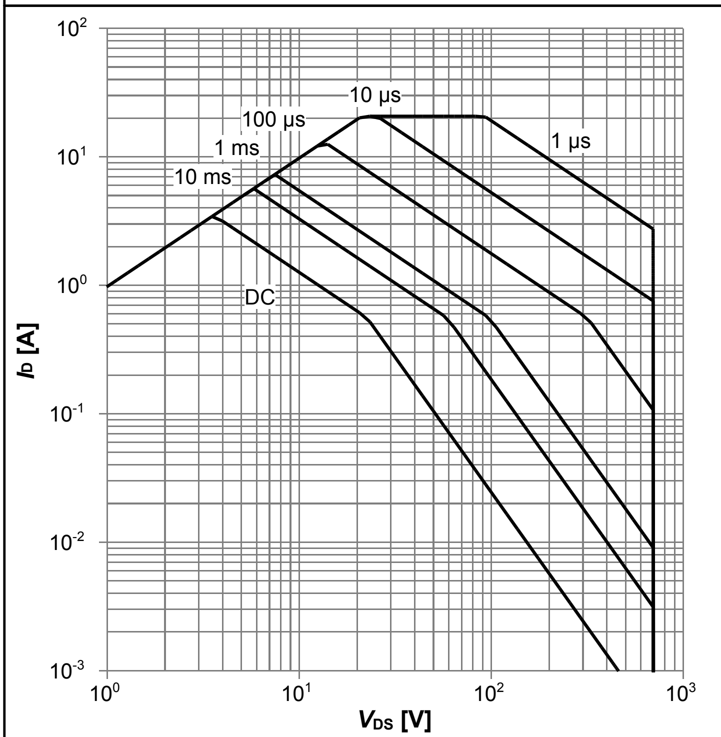
P_{tot}=f(T_C)

Diagram 2: Safe operating area



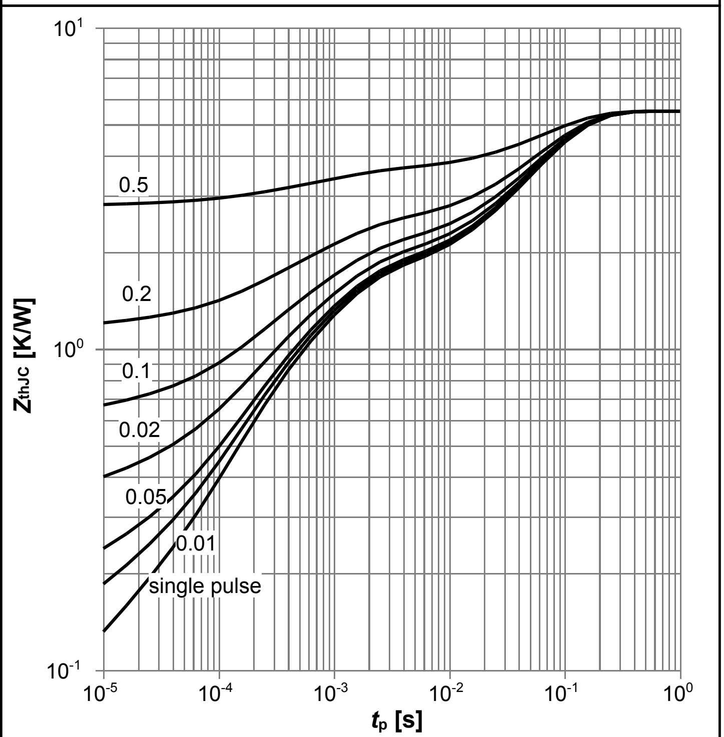
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



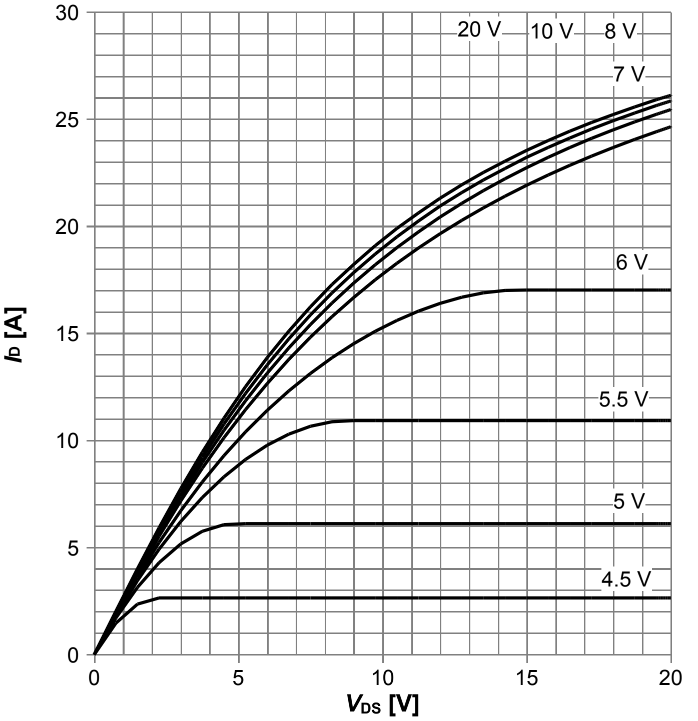
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



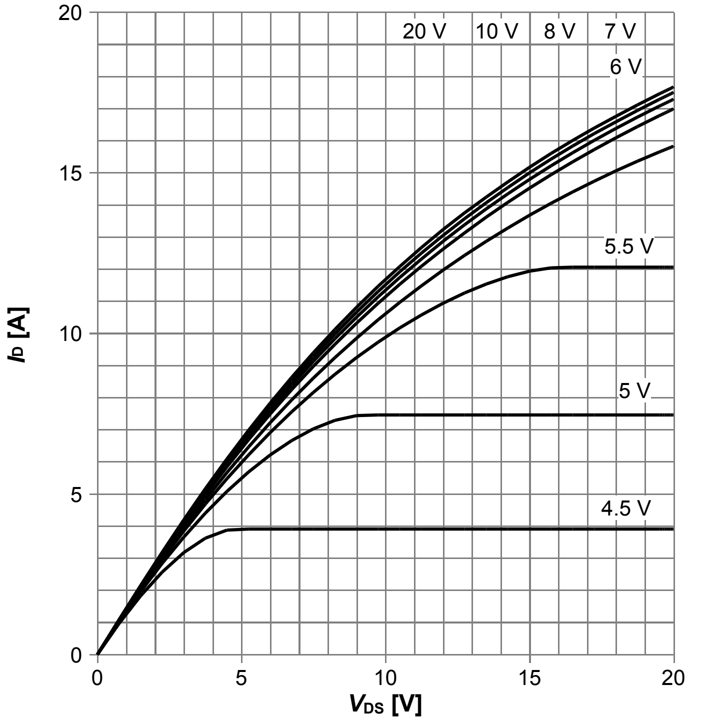
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



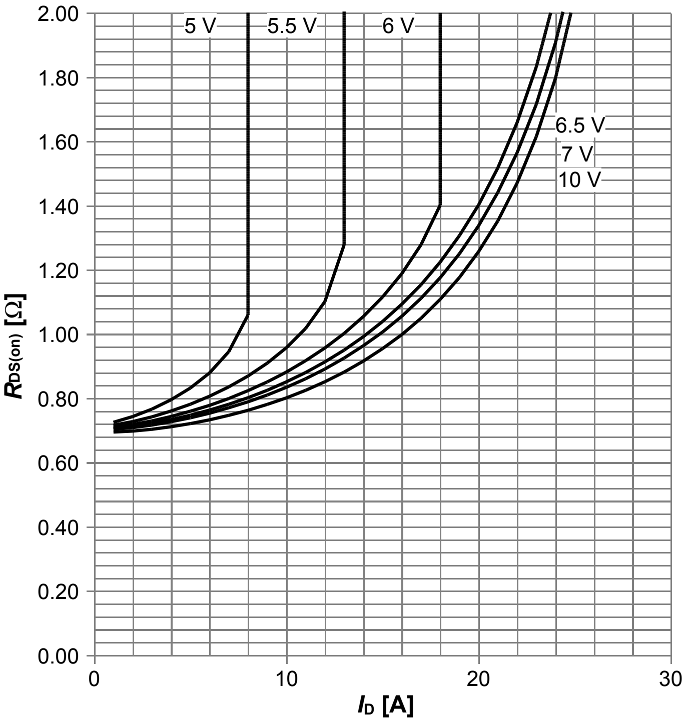
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



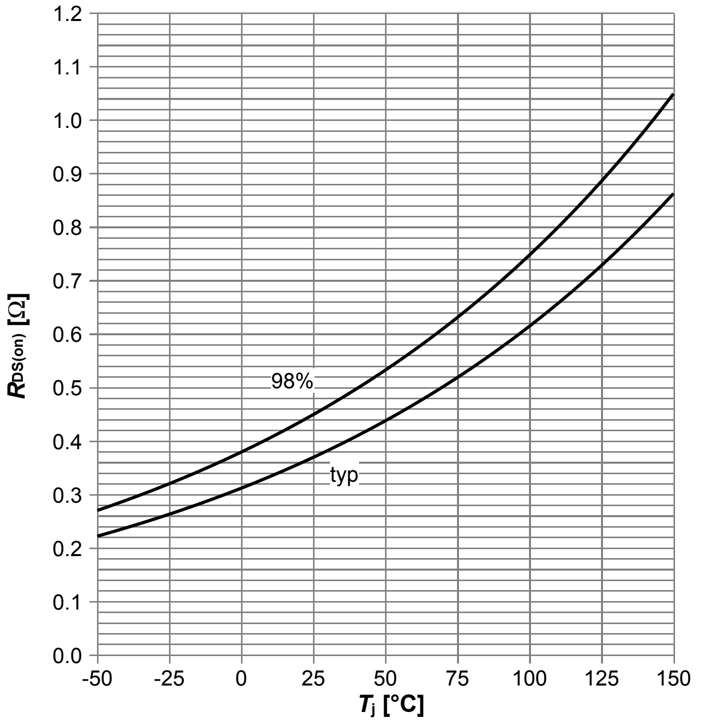
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



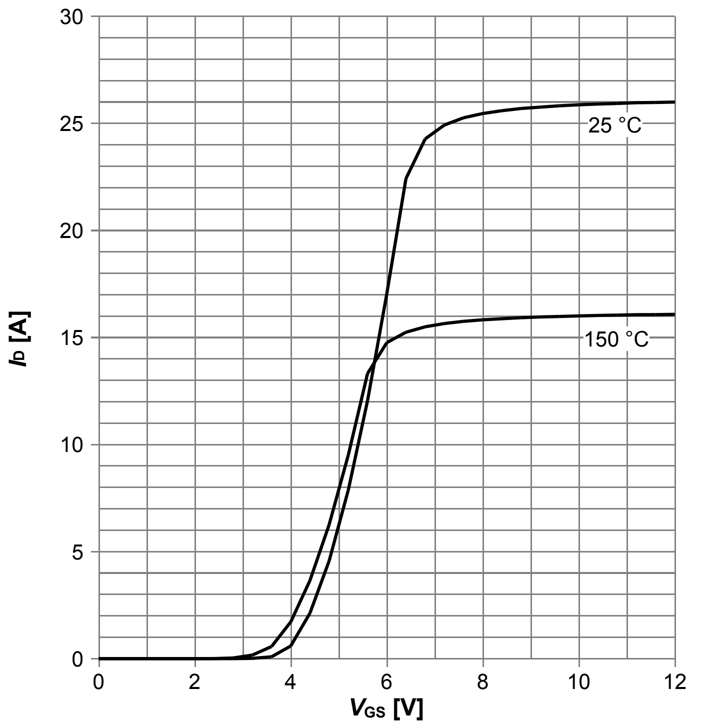
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



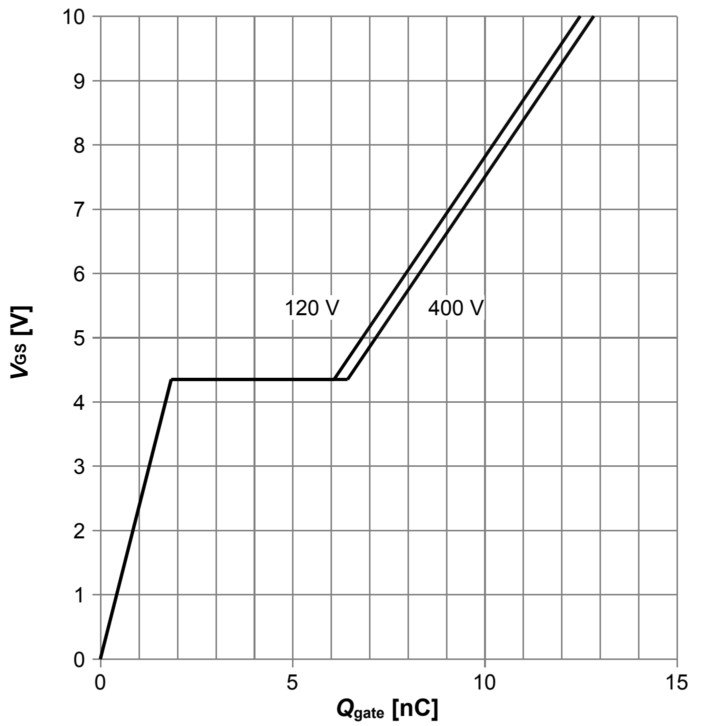
$R_{DS(on)}$=f(T_j); I_D=2.3 A; V_{GS}=10 V

Diagram 9: Typ. transfer characteristics



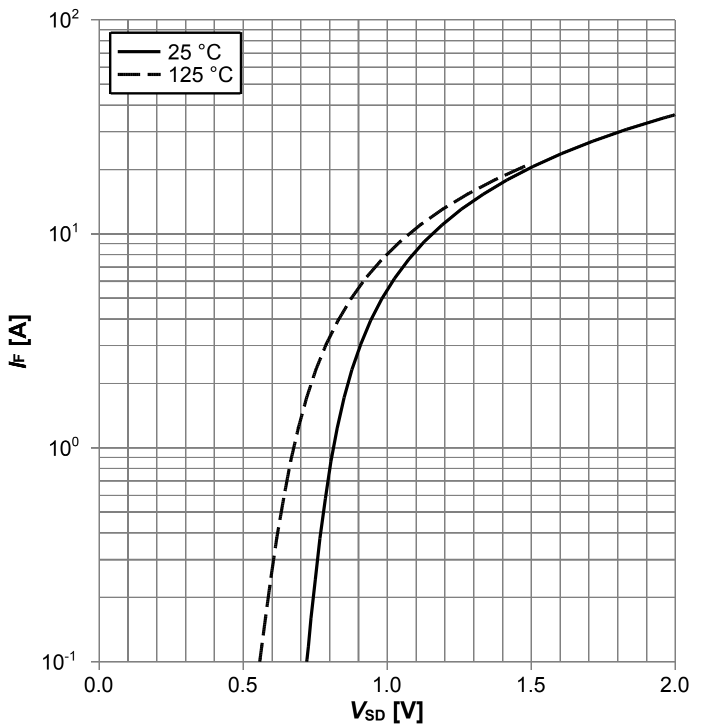
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



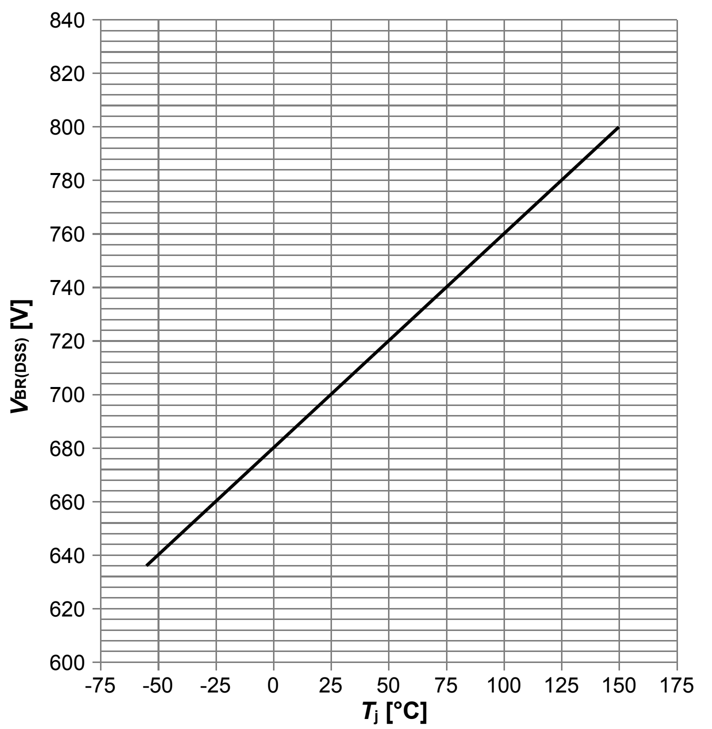
V_{GS}=f(Q_{gate}); I_D=1.7 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode

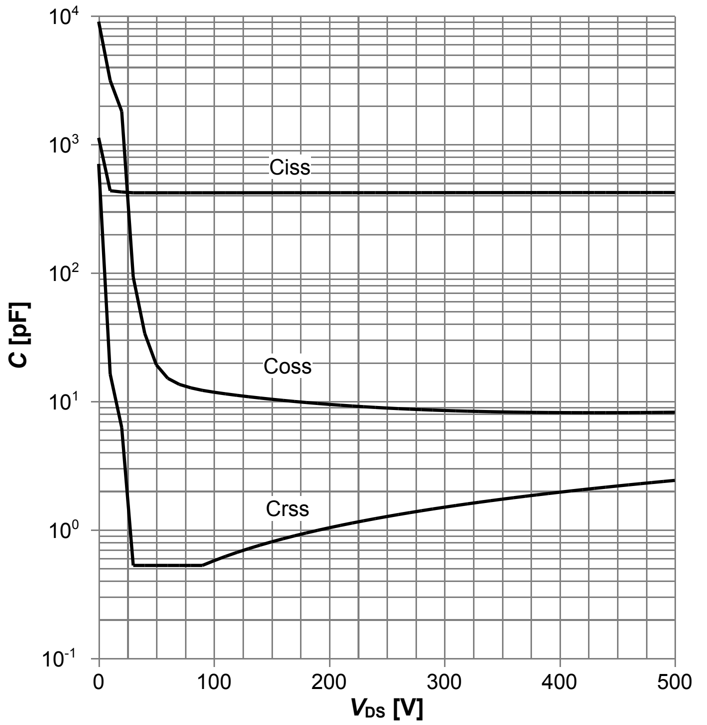
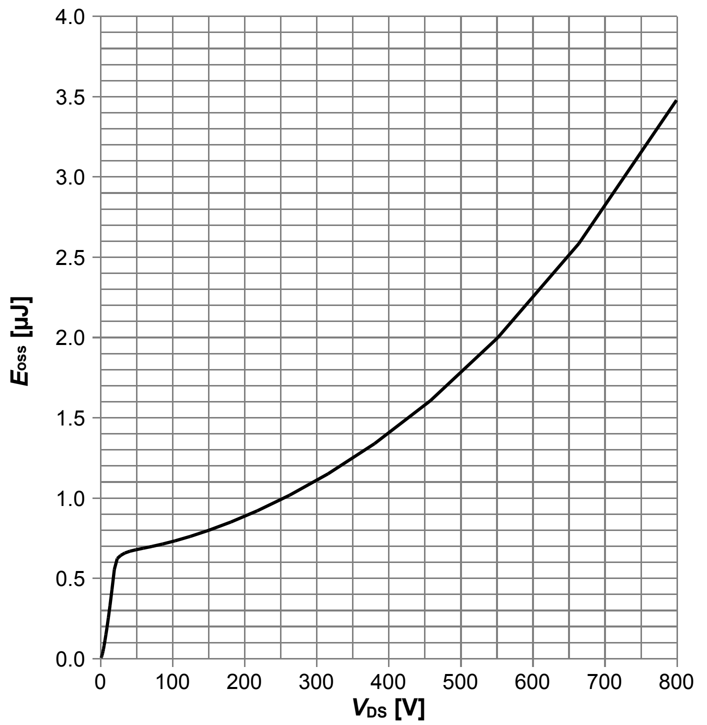


I_F=f(V_{SD}); parameter: T_j

Diagram 13: Drain-source breakdown voltage



$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances	**Diagram 15: Typ. Coss stored energy**
	
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=250$ kHz	$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

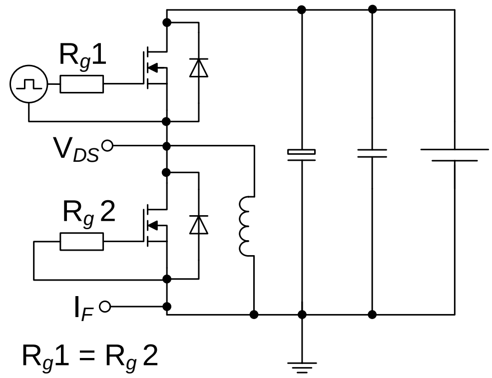
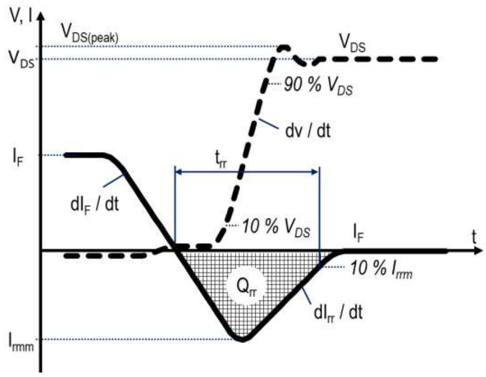
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

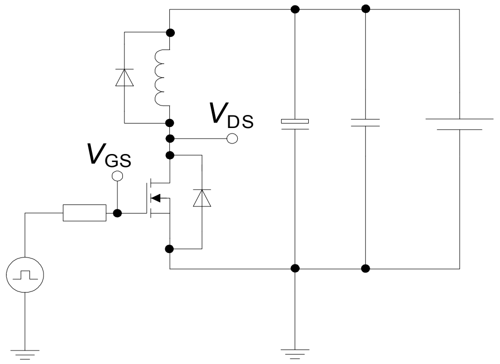
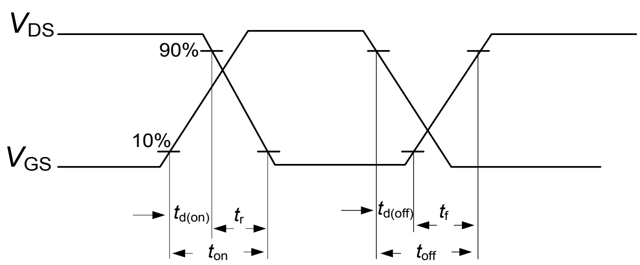
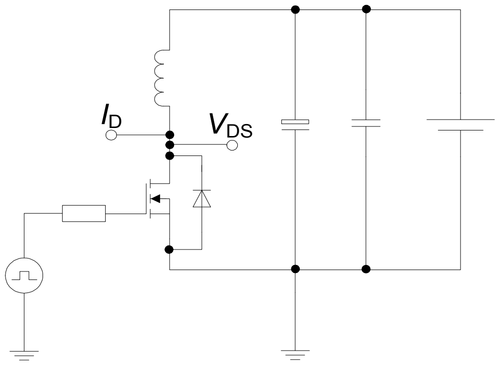
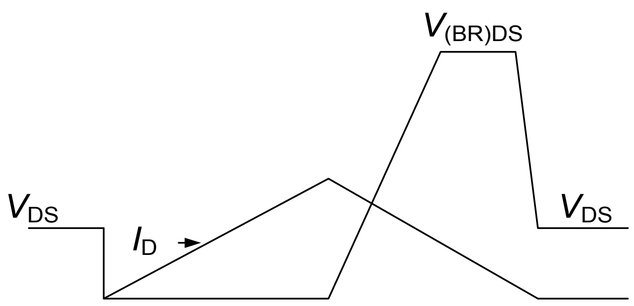
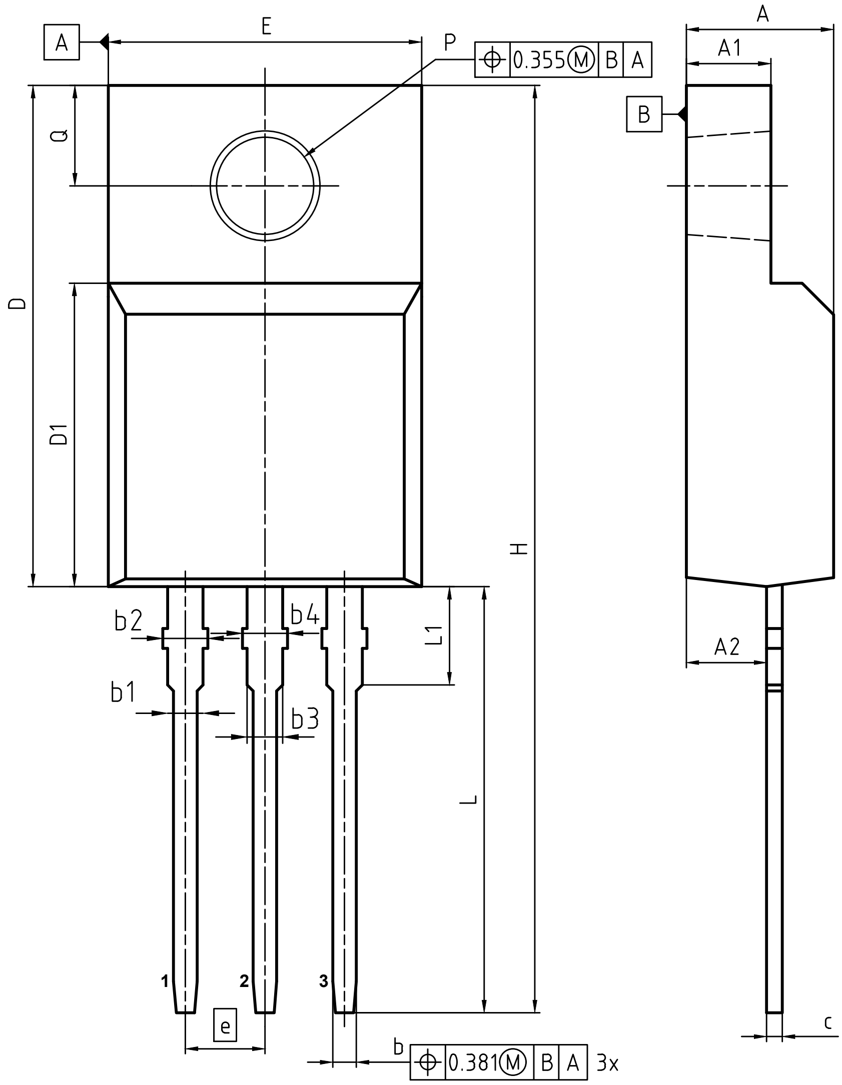
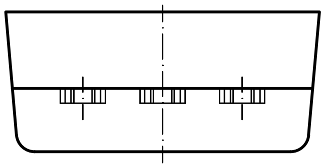
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines





NOTES:
STANDARD QUALITY GRADE
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PRO-
TRUSIONS OR GATE BURRS

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.50	4.90
A1	2.34	2.80
A2	2.42	2.86
b	0.65	0.90
b1	0.95	1.38
b2	1.20	1.50
b3	0.65	1.38
b4	1.20	1.50
c	0.40	0.63
D	15.67	16.15
D1	8.97	9.83
E	10.00	10.65
e	2.54	
H	28.70	29.75
L	12.78	13.75
L1	2.83	3.45
øP	3.00	3.38
Q	3.15	3.50

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Z8B00181328

REVISION
03

ISSUE DATE
23.07.2018

SCALE 5:1
0 1 2 3 4 5mm

EUROPEAN PROJECTION

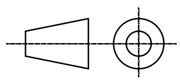

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS™ P7 Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPA70R450P7S

Revision: 2020-01-27, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2017-09-15	Release of final version
2.1	2018-02-12	Corrected front page text
2.2	2020-01-27	Updated package drawing, symbol ID and product validation

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