ANALOG DEVICES

5.5 GHz to 18 GHz, GaAs, pHEMT, MMIC, Medium Power Amplifier

Data Sheet **HMC1082CHIP**

FEATURES

High saturated output power: 26 dBm with 24% PAE
High gain: 24 dB typical
High output IP3: 36 dBm typical
High output P1dB: 25.5 dBm
Die size: 2.19 mm × 1.05 × 0.1 mm

APPLICATIONS

Software defined radios
Electronics warfare (EW)
Radar applications
Electronic countermeasures (ECMs)

FUNCTIONAL BLOCK DIAGRAM

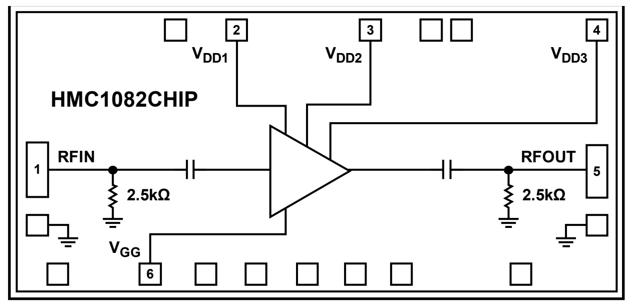

Figure 1.

GENERAL DESCRIPTION

The HMC1082CHIP is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT), driver amplifier that operates from 5.5 GHz to 18 GHz. The HMC1082CHIP provides a typical gain of 24 dB, 36 dBm output IP3, and 25.5 dBm of output power for 1 dB compression, requiring only 220 mA from a 5 V supply voltage. The saturated output power (P_{SAT}) is 26 dBm with 24% power added efficiency (PAE).

The HMC1082CHIP is an ideal driver amplifier for a wide range of applications including point to point radios from 5.5 GHz to 18 GHz and marine radars at 9 GHz. The HMC1082CHIP can also be used for 6 GHz to 18 GHz EW and ECM applications.

Rev. B Document Feedback

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REVISION HISTORY

8/2020—Rev. A to Rev. B

Change to Features Section ... 1

3/2020—Rev. 0 to Rev. A

Changes to General Description ... 1

6/2019—Revision 0: Initial Version

SPECIFICATIONS

5.5 GHz TO 7 GHz FREQUENCY RANGE

T_A = 25°C, drain bias voltage (V_{DD}) = 5 V, and I_{DQ} = 220 mA, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		5.5		7	GHz	
GAIN		22	24		dB	
Gain Variation Over Temperature			0.006		dB/°C	
RETURN LOSS						
Input			14		dB	
Output			11		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	23	25		dBm	
Saturated Output Power	P_{SAT}		25.5		dBm	
Output Third-Order Intercept	IP3		37.5		dBm	Measurement taken at output power (P_{OUT}) per tone = 12 dBm
SUPPLY						
Current	I_{DQ}		220		mA	Adjust V_{GG} to achieve I_{DQ} = 220 mA typical
Voltage	V_{DD}	4	5		V	

7 GHz TO 15.5 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 220 mA, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		7		15.5	GHz	
GAIN		22	24		dB	
Gain Variation Over Temperature			0.008		dB/°C	
RETURN LOSS						
Input			11.5		dB	
Output			13		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	23.5	25.5		dBm	
Saturated Output Power	P_{SAT}		26		dBm	With 24% PAE
Output Third-Order Intercept	IP3		36		dBm	Measurement taken at P_{OUT} per tone = 12 dBm
SUPPLY						
Current	I_{DQ}		220		mA	Adjust V_{GG} to achieve I_{DQ} = 220 mA typical
Voltage	V_{DD}	4	5		V	

15.5 GHz TO 18 GHz FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 220 mA, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		15.5		18	GHz	
GAIN		23	25		dB	
Gain Variation Over Temperature			0.009		dB/°C	
RETURN LOSS						
Input			14.5		dB	
Output			20		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	22	24		dBm	
Saturated Output Power	P_{SAT}		24.5		dBm	
Output Third-Order Intercept	IP3		35.5		dBm	Measurement taken at P_{OUT} per tone = 12 dBm
SUPPLY						
Current	I_{DQ}		220		mA	Adjust V_{GG} to achieve I_{DQ} = 220 mA typical
Voltage	V_{DD}	4	5		V	

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Drain Bias Voltage (V_{DD})	5.5 V dc
Radio Frequency (RF) Input Power (RFIN)	20 dBm
Continuous Power Dissipation (P_{DISS}), T = 85°C (Derate 20.4 mW/°C Above 85°C)	1.84 W
Channel Temperature	175°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C
Junction Temperature to Maintain 1,000,000 Hour Mean Time to Failure (MTTF)	175°C
Nominal Junction Temperature (T = 85°C, V_{DD} = 5 V, I_{DQ} = 220 mA)	138.8°C
ESD Sensitivity	
Human Body Model (HBM)	Class 1A (passed 250 V)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JC} is the junction to case thermal resistance, channel to bottom of die.

Table 5. Thermal Resistance

Package Type	θ_{JC}	Unit
C-6-13	48.9	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

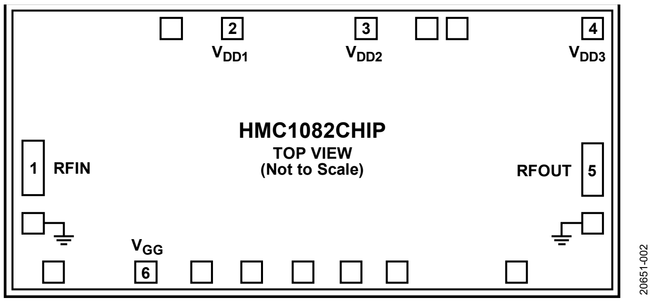

Figure 2. Pad Configuration

Table 6. Pad Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Signal Input. This pad is dc-coupled and matched to 50 Ω.
2, 3, 4	V_{DD1}, V_{DD2}, V_{DD3}	Drain Bias for the Amplifier.
5	RFOUT	RF Signal Output. This pad is dc-coupled and matched to 50 Ω.
6	V_{GG}	Amplifier Gate Control.
Die Bottom	GND	Ground. Die bottom must be connected to RF and dc ground.

INTERFACE SCHEMATICS

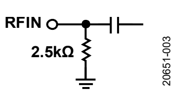

Figure 3. RFIN Interface Schematic

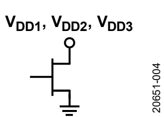

Figure 4. V_{DD1}, V_{DD2}, and V_{DD3} Interface Schematic

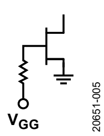

Figure 5. V_{GG} Interface Schematic

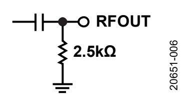

Figure 6. RFOUT Interface Schematic

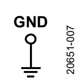

Figure 7. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

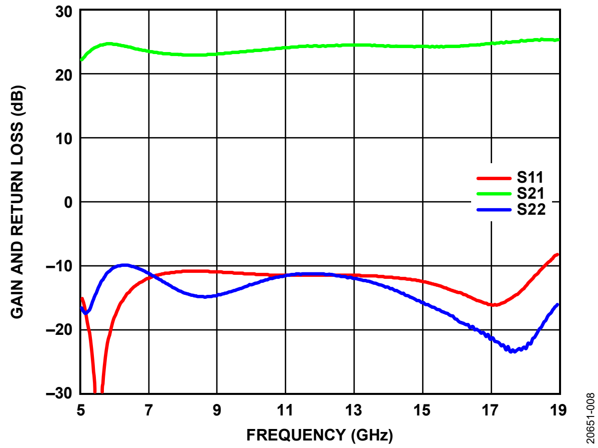

Figure 8. Gain and Return Loss vs. Frequency

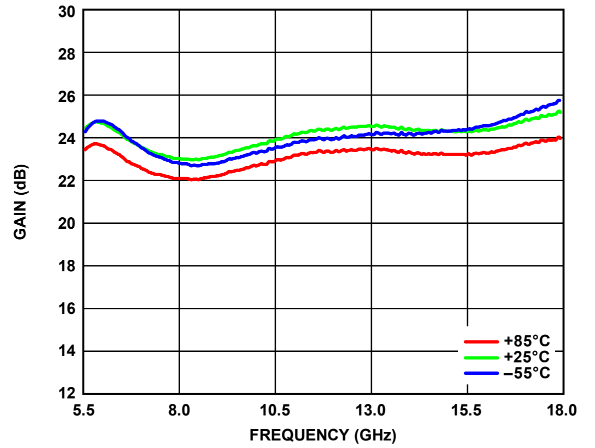

Figure 11. Gain vs. Frequency for Various Temperatures

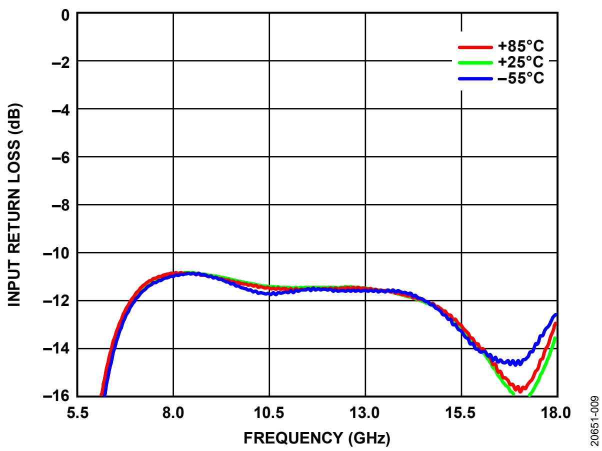

Figure 9. Input Return Loss vs. Frequency for Various Temperatures

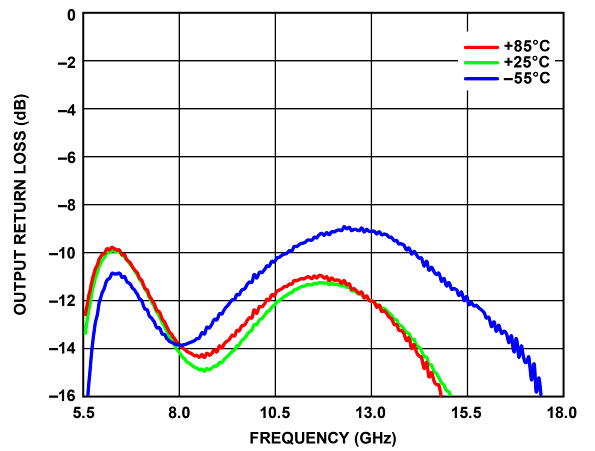

Figure 12. Output Return Loss vs. Frequency for Various Temperatures

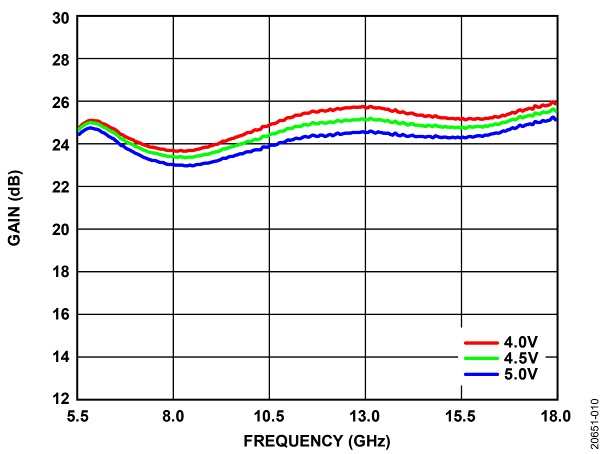

Figure 10. Gain vs. Frequency for Various Supply Voltages (V_{DD}), I_{DQ} = 220 mA

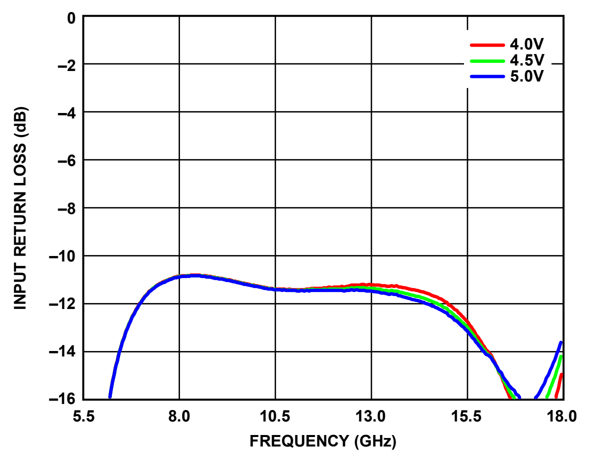

Figure 13. Input Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 220 mA

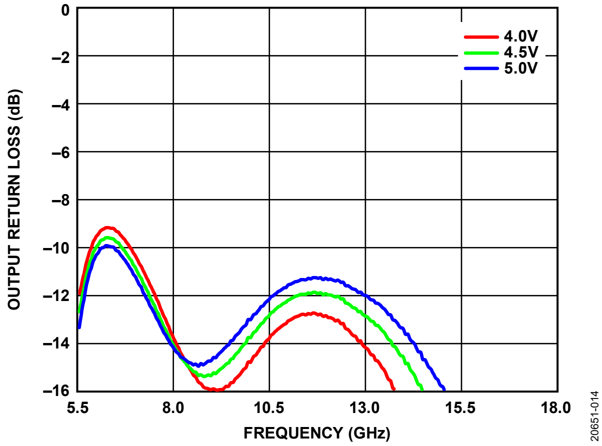

Figure 14. Output Return Loss vs. Frequency for Various Supply Voltages (V_{DD}), I_{DQ} = 220 mA

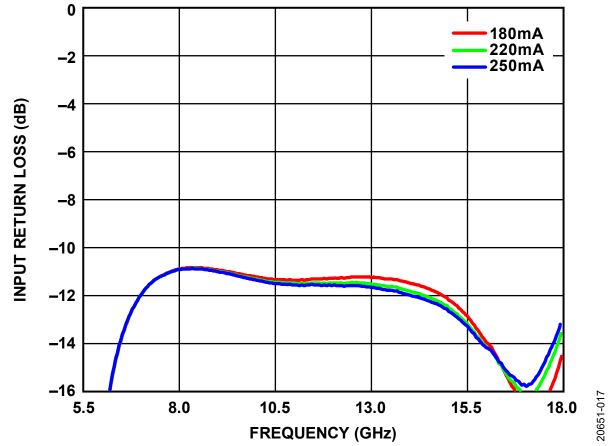

Figure 17. Input Return Loss vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V

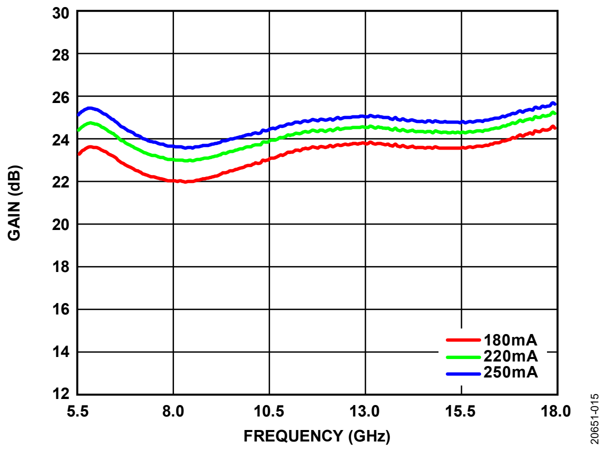

Figure 15. Gain vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V

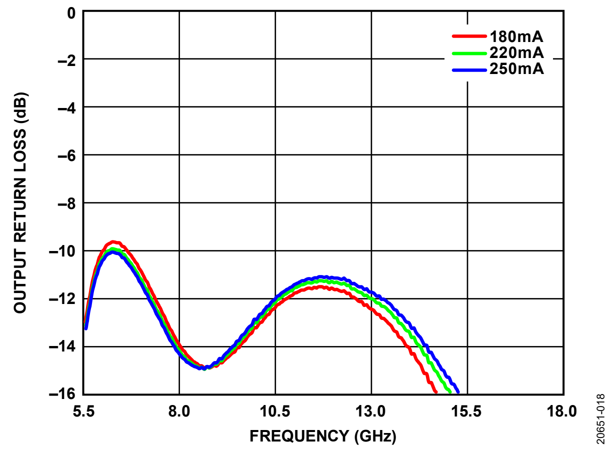

Figure 18. Output Return Loss vs. Frequency for Various Supply Currents (I_{DQ}), V_{DD} = 5 V

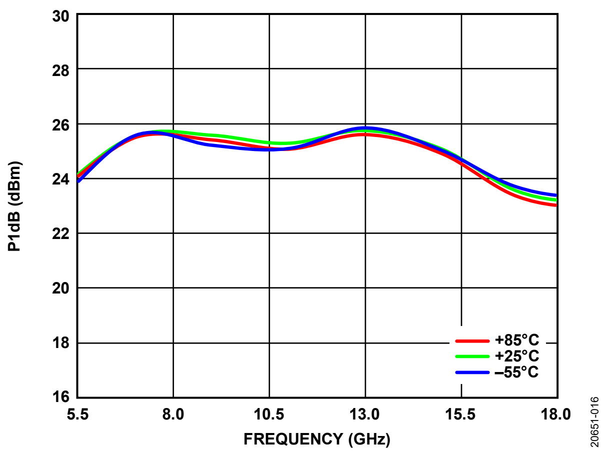

Figure 16. P1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 220 mA

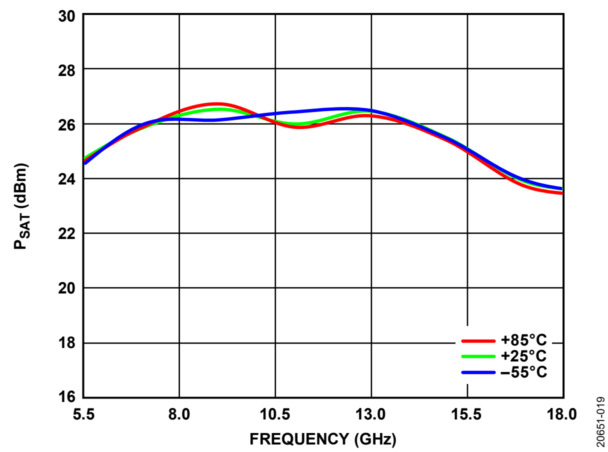

Figure 19. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 220 mA

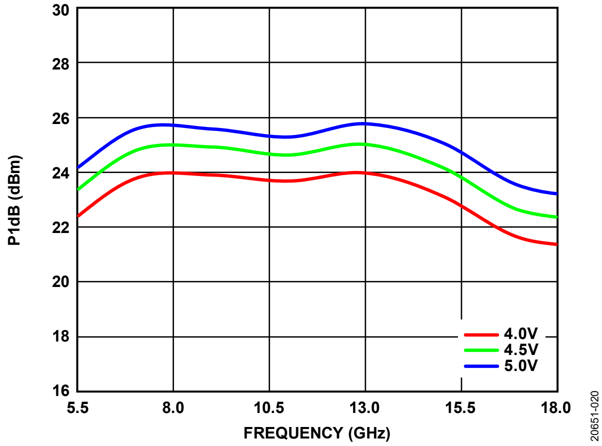

Figure 20. P1dB vs. Frequency for Various V_{DD}, I_{DQ} = 220 mA

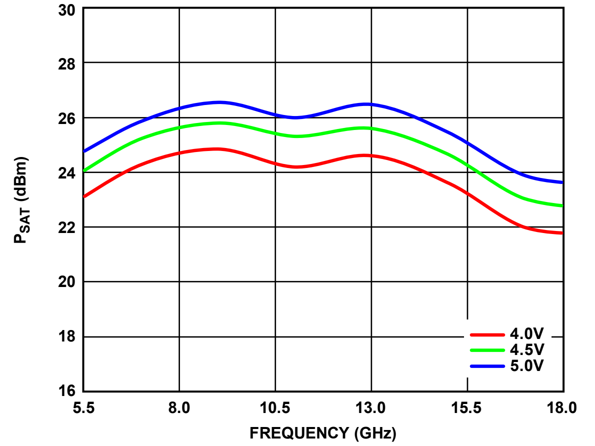

Figure 23. P_{SAT} vs. Frequency for Various V_{DD}, I_{DQ} = 220 mA

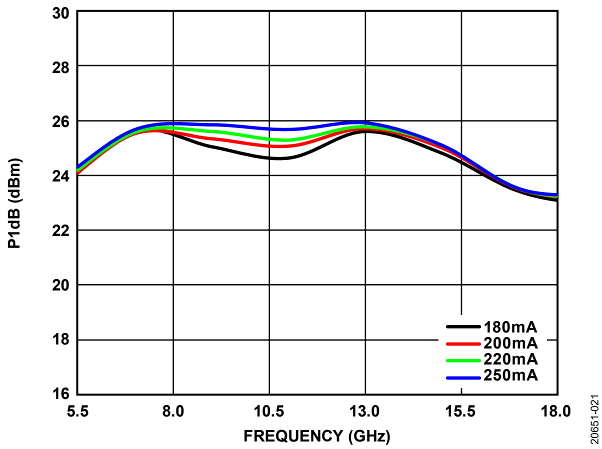

Figure 21. P1dB vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

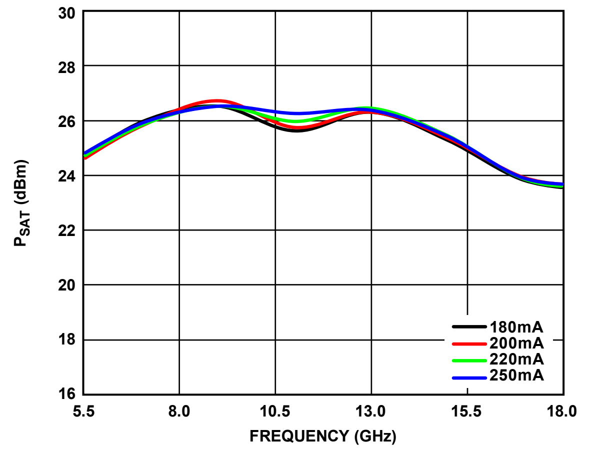

Figure 24. P_{SAT} vs. Frequency for Various I_{DQ}, V_{DD} = 5 V

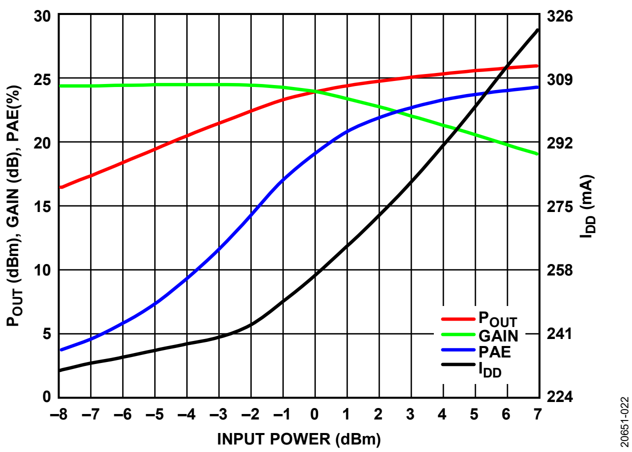

Figure 22. P_{OUT}, Gain, PAE, and Drain Current (I_{DD}) vs. Input Power, Frequency = 11 GHz

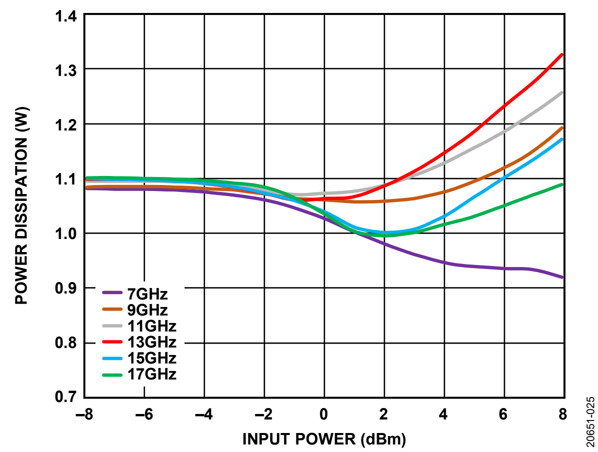

Figure 25. Power Dissipation vs. Input Power at T = 85°C, V_{DD} = 5 V, I_{DD} = 220 mA

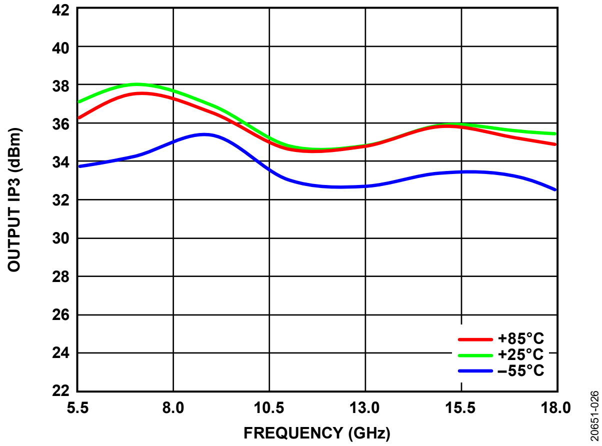

Figure 26. Output IP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 12 dBm, V_{DD} = 5 V, I_{DQ} = 220 mA

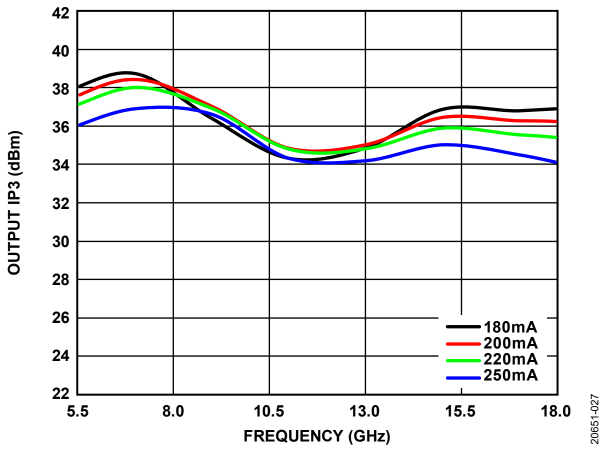

Figure 27. Output IP3 vs. Frequency for Various I_{DQ}, P_{OUT} per Tone = 12 dBm, V_{DD} = 5 V

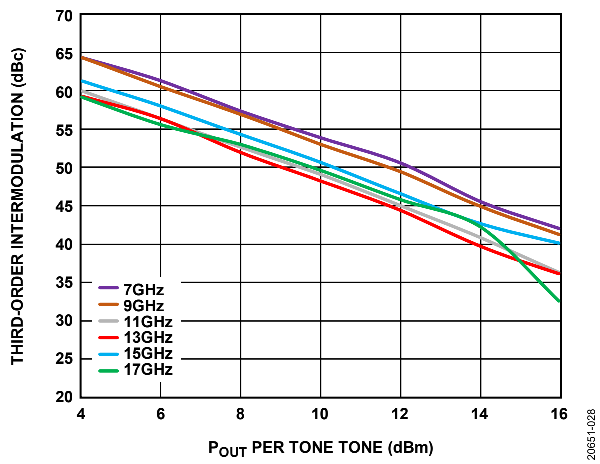

Figure 28. Third-Order Intermodulation vs. P_{OUT} per Tone, V_{DD} = 4.5 V, I_{DQ} = 220 mA

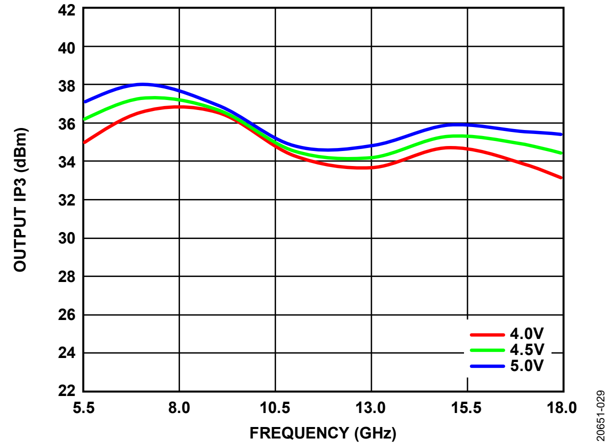

Figure 29. Output IP3 vs. Frequency for Various V_{DD}, P_{OUT} per Tone = 12 dBm, I_{DQ} = 220 mA

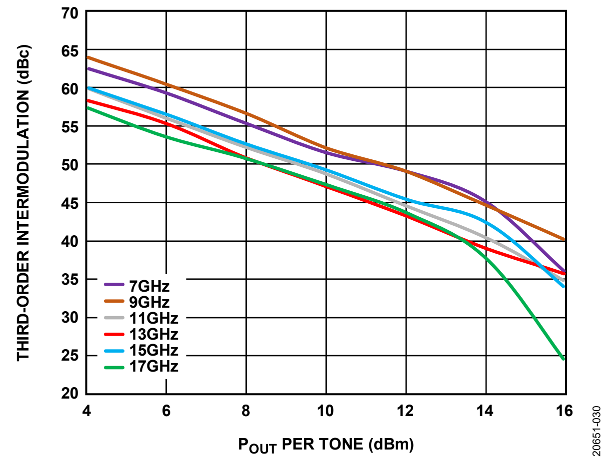

Figure 30. Third-Order Intermodulation vs. P_{OUT} per Tone, V_{DD} = 4 V, I_{DQ} = 220 mA

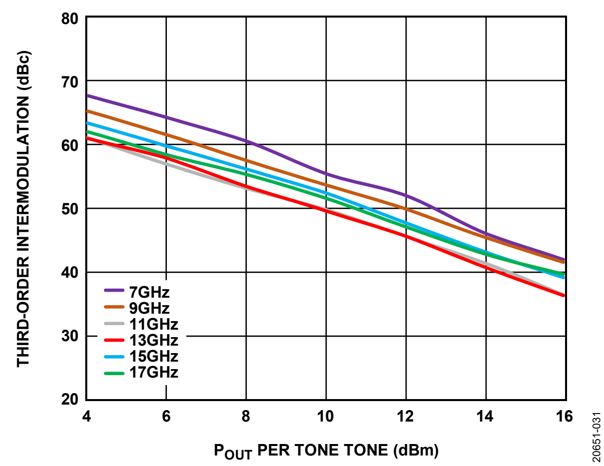

Figure 31. Third-Order Intermodulation vs. P_{OUT} per Tone, V_{DD} = 5 V, I_{DQ} = 220 mA

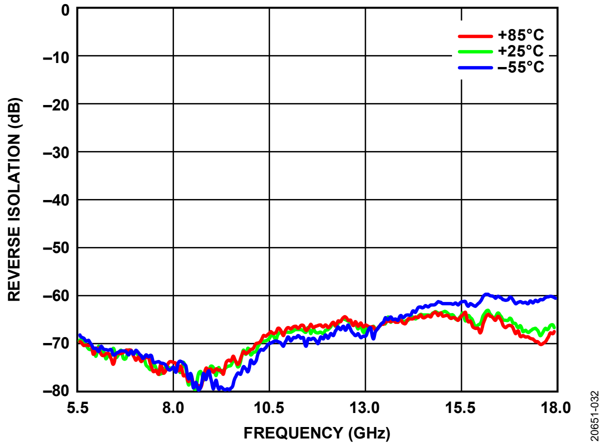

Figure 32. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 220 mA

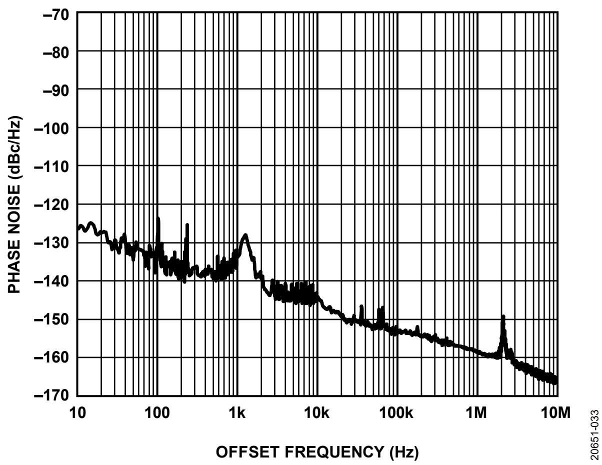

Figure 33. Phase Noise vs. Offset Frequency, RF Frequency = 8 GHz, RF Input Power = 3 dBm (P1dB)

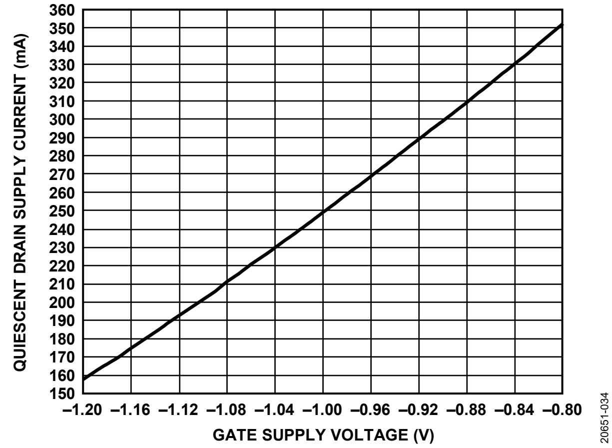

Figure 34. Quiescent Drain Supply Current vs. Gate Supply Voltage

THEORY OF OPERATION

The architecture of the HMC1082CHIP medium power amplifier is shown in Figure 35. The HMC1082CHIP uses cascaded three-stage amplifiers. The nominal V_{DD} voltage of each stage is 5 V.

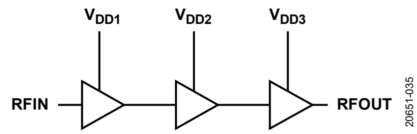

Figure 35. Basic Schematic for HMC1082CHIP

APPLICATIONS INFORMATION

The HMC1082CHIP is a GaAs, pHEMT, MMIC medium power amplifier. Capacitive bypassing is required for all V_{GG} and V_{DDx} pads.

All measurements for this device were taken using the application circuit (see Figure 38) and were configured as shown in the assembly diagram (see Figure 39).

RECOMMENDED BIAS SEQUENCING

The recommended bias sequence during power-up is as follows:

1. Connect GND to RF and dc ground.
2. Set the gate bias voltage, V_{GG} to −2.0 V.
3. Set all the drain bias voltages, V_{DDx}, to 5 V.
4. Increase the gate bias voltage to achieve a quiescent current, and set I_{DQ} = 220 mA.
5. Apply the RF signal.

The recommended bias sequence during power-down is as follows:

1. Turn off the RF signal.
2. Decrease the primary gate bias voltage, V_{GG}, to −2.0 V to achieve I_{DQ} = 0 mA (approximately).
3. Decrease all drain bias voltages to 0 V.
4. Increase the gate bias voltage to 0 V.

Simplified bias pad connections to dedicated gain stages and dependence and independence among pads are shown in Figure 35.

The V_{DD} = 5 V and I_{DQ} = 220 mA bias conditions are recommended to optimize overall performance. Unless otherwise noted, the data shown was taken using the recommended bias conditions. Operation of the HMC1082CHIP at different bias conditions may provide performance that differs from what is shown in the Typical Performance Characteristics section with nominal (V_{DD} = 5 V and I_{DQ} = 220 mA) conditions.

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane eutectically or with conductive epoxy (see the Handling Precautions section).

To bring the radio frequency to and from the chip, implementing 50 Ω transmission lines using a microstrip or coplanar waveguide on 0.127 mm (5 mil) thick alumina, thin film substrates is recommended (see Figure 36). When using 0.254 mm (10 mil) thick alumina, it is recommended that the die be raised to ensure that the die and substrate surfaces are coplanar. Raise the die 0.150 mm (6 mil) to ensure that the surface of the die is coplanar with the surface of the substrate. To accomplish this, attach the 0.102 mm (4 mil) thick die to a 0.150 mm (6 mil) thick, molybdenum (Mo) heat spreader (moly tab), which can then be attached to the ground plane (see Figure 36 and Figure 37).

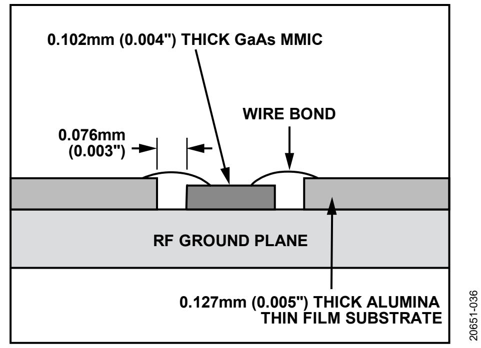

Figure 36. Die Without the Moly Tab

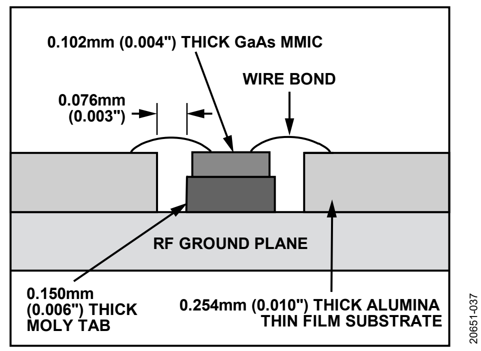

Figure 37. Die With the Moly Tab

Place microstrip substrates as close to the die as possible to minimize bond wire length. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

Handling Precautions

To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. After the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pickup.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip may have fragile air bridges and must not be touched with a vacuum collet, tweezers, or fingers.

APPLICATION CIRCUIT

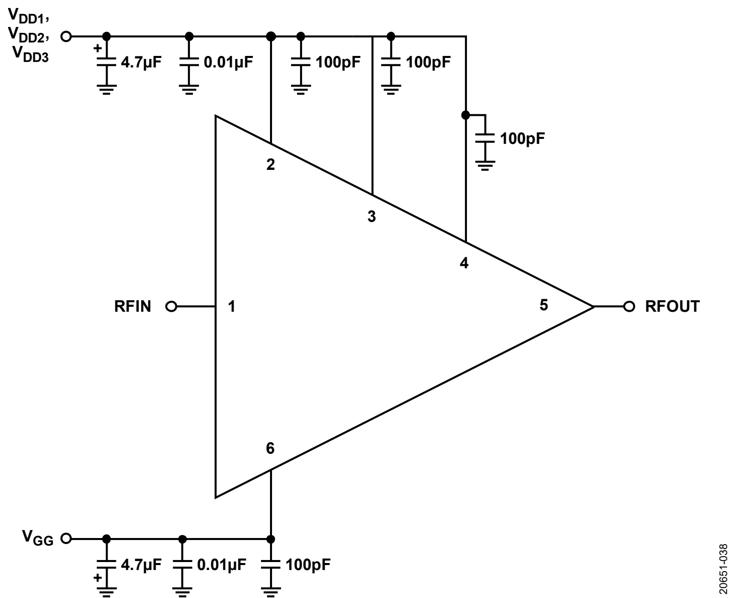

Figure 38. Application Circuit

ASSEMBLY DIAGRAM

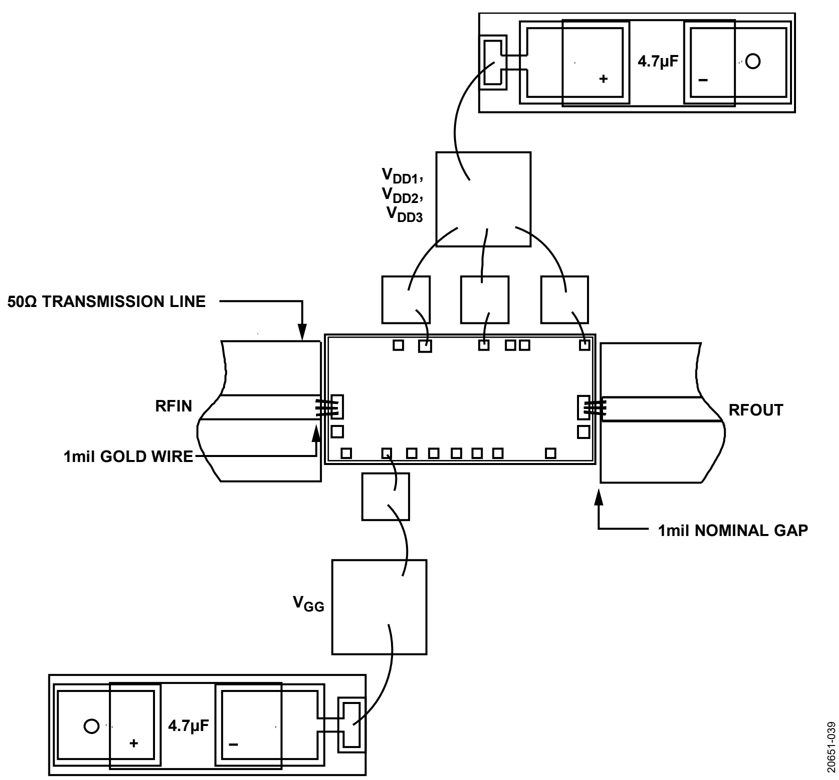

Figure 39. Assembly Diagram

OUTLINE DIMENSIONS

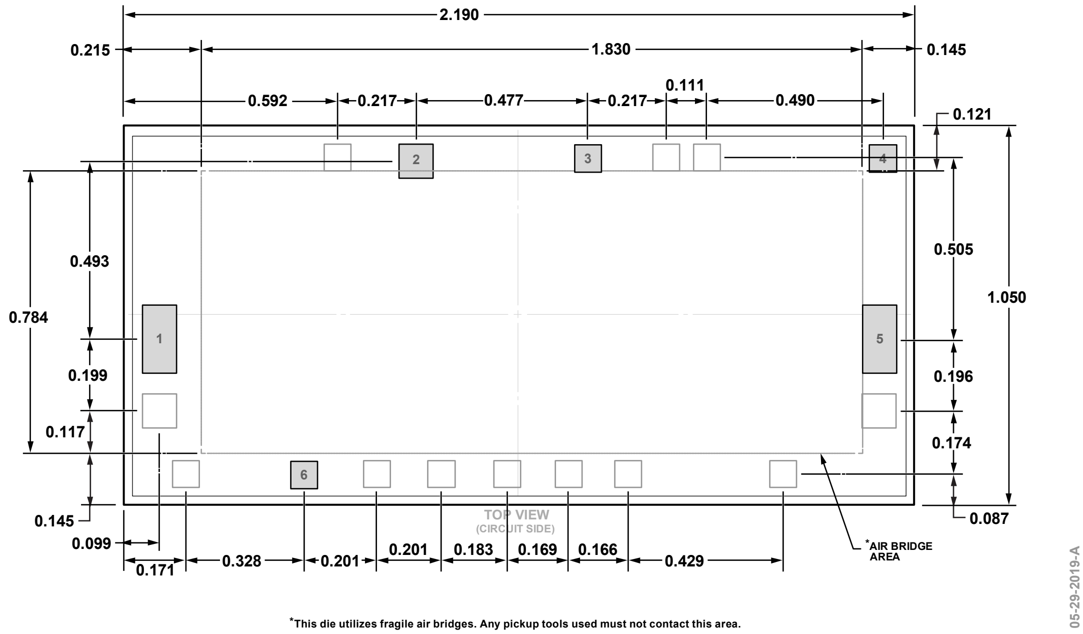

Figure 40. 6-Pad Bare Die [CHIP]
(C-6-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
HMC1082C-KIT	−55°C to +85°C	6-Pad Bare Die [CHIP]	C-6-13
HMC1082CHIP	−55°C to +85°C	6-Pad Bare Die [CHIP]	C-6-13

[1] The HMC1082CHIP and HMC1082C-KIT are RoHS compliant parts.