SY89875U

2.5V, 2.0 GHz Any Differential IN-to-LVDS Programmable Clock Divider and 1:2 Fanout Buffer with Internal Termination

Features

- Integrated programmable clock divider and 1:2 fanout buffer
- Guaranteed AC performance over temperature and voltage:
  - > 2.0 GHz f_{MAX}
  - < 200 ps t_r/t_f
  - < 15 ps within device skew
- Low jitter design:
  - < 10 ps_{PP} total jitter
  - < 1 ps_{RMS} cycle-to-cycle jitter
- Unique input termination and VT Pin for DC-coupled and AC-coupled Inputs; CML, PECL, LVDS, and HSTL
- LVDS compatible outputs
- TTL/CMOS inputs for select and reset
- Parallel programming capability
- Programmable divider ratios of 1, 2, 4, 8 and 16
- Low voltage operation 2.5V
- Output disable function
- –40°C to 85°C temperature range
- Available in 16-pin (3 mm × 3 mm) VQFN package

Applications

- SONET/SDH Line Cards
- Transponders
- High-end Multiprocessor Servers

General Description

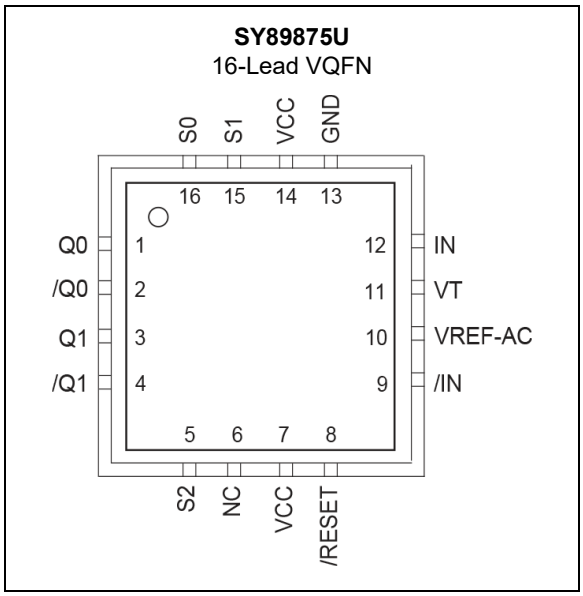
This low-skew, low-jitter device is capable of accepting a high-speed (e.g., 622 MHz or higher) CML, LVPECL, LVDS or HSTL clock input signal and dividing down the frequency using a programmable divider to create a lower speed version of the input clock. Available divider ratios are 2, 4, 8. and 16, or straight pass-through.

The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A V_{REF-AC} reference is included for AC-coupled applications.

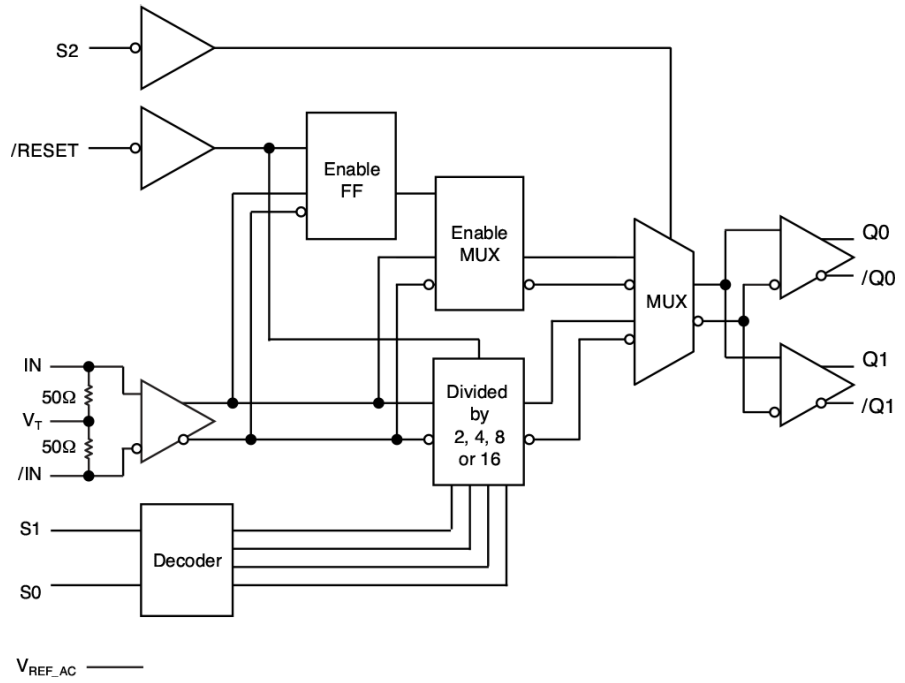
The /RESET input asynchronously resets the divider. In the pass-through function (divide by 1) the /RESET synchronously enables or disables the outputs on the next falling edge of IN (rising edge of /IN).

Package Type

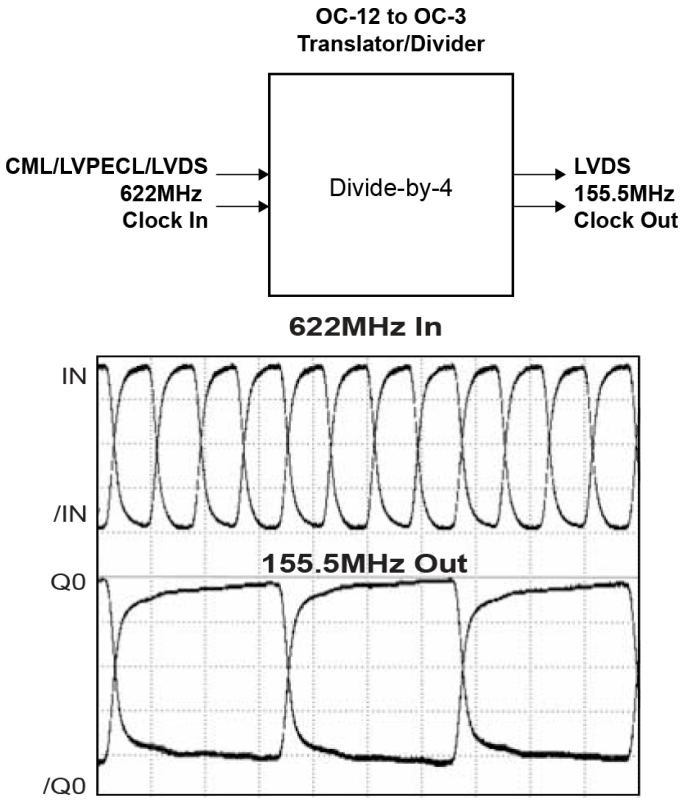
SY89875U
16-Lead VQFN



Functional Block Diagram



Typical Performance



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to VCC+0.3
ECL Output Current (I_{OUT}), Continuous ..... 50 mA
ECL Output Current (I_{OUT}), Surge ..... 100 mA
Input Current IN, /IN (I_{IN}) ..... ±50 mA
VT Current (I_{VT}) ..... ±100 mA
VREF-AC Sink/Source Current ($I_{VREF-AC}$), Note 1 ..... ±2 mA

Operating Ratings††

Supply Voltage (V_{CC}) ..... +2.5V ±5%

† **Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†† **Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 1: Due to the limited drive capability, use for input of the same package only.

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS

All values applicable for when T_A = –40°C to +85°C unless otherwise stated. (Note 1, Note 2)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Supply	V_{CC}	2.375	—	2.625	V	—
Power Supply Current	I_{CC}	—	70	95	mA	No load, max. V_{CC}
Differential Input Resistance (IN-to-/IN)	R_{IN}	90	100	110	Ω	—
Input High Voltage (IN, /IN)	V_{IH}	0.1	—	V_{CC} + 0.3	V	Note 3
INput Low Voltage (IN, /IN)	V_{IL}	–0.3	—	V_{IH} – 0.1	V	Note 3
Input Voltage Swing	V_{IN}	0.1	—	V_{CC}	V	Note 4
Differential Input voltage Swing	V_{DIFF_IN}	0.2	—	—	V	Note 5
Input Current (IN, /IN)	$\|I_{IN}\|$	—	—	45	mA	Note 3
Reference Voltage	V_{REF-AC}	V_{CC} – 1.525	V_{CC} – 1.425	V_{CC} – 1.325	V	Note 6

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: Specification for packaged product only.

3: Due to the internal termination (see Figure 8-1), the input current depends on the applied voltages at IN, /IN and V_T inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit.

4: See Section 6.0, Timing Diagram for V_{IN} definition. V_{IN} (Max) is specified when V_T is floating.

5: See Section 3.0, Typical Operating Characteristics for V_{DIFF} definition.

6: Operating using V_{IN} is limited to AC-coupled PECL or CML applications only. Connect directly to VT pin.

TABLE 1-2: LVDS DC ELECTRICAL CHARACTERISTICS

V_{CC} = +2.5V ±5% and T_A = –40°C to +85°C, unless otherwise stated. (Note 1, Note 2)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output Voltage Swing	V_{OUT}	250	350	400	mV	Note 3, Note 4
Output High Voltage	V_{OH}	—	—	1.475	V	Note 3
Output Low Voltage	V_{OL}	0.925	—	—	V	Note 3
Output Common Mode Voltage	V_{OCM}	1.125	—	1.375	V	Note 4
	ΔV_{OCM}	–50	—	50	mV	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: Specification for packaged product only.

3: Measured as per Figure 8-1, 100Ω across Q and /Q outputs.

4: Measured as per Figure 8-2.

TABLE 1-3: LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS

V_{CC} = +2.5V ±5% and T_A = –40°C to +85°C, unless otherwise stated. (Note 1, Note 2)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input HIGH Voltage	V_{IH}	2.0	—	—	V	—
Input LOW Voltage	V_{IL}	—	—	0.8	V	—
Input HIGH Current	I_{IH}	–125	—	20	µA	—
Input LOW Current	I_{IL}	—	—	–300	µA	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: Specification for packaged product only.

TABLE 1-4: AC ELECTRICAL CHARACTERISTICS

V_{CC} = +2.5V ±5% and T_A = –40°C to +85°C, unless otherwise stated. (Note 1, Note 2)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Maximum Operating Frequency	f_{MAX}	2.0	2.5	—	GHz	Output Swing >200 mV
Differential Propagation Delay (IN-to-Q)	t_{pd}	590	690	870	ps	Input Swing <400 mV
		540	690	820	ps	Input Swing >200 mV
Within-Device Skew	t_{SKEW}	—	5	15	ps	Note 3
Part-to-Part Skew		—	—	280	ps	Note 3
Reset Recovery Time	t_{RR}	600	—	—	ps	Note 4
Cycle-to-Cycle Jitter)	t_{JITTER}	—	—	1	ps_{RMS}	Note 5
Total Jitter		—	—	10	ps_{PP}	Note 6
Rise/Fall Time (20% to 80%)	t_r, t_f	70	120	200	ps	—

Note 1: Measured with 400 mV input signal, 50% duty cycle, all outputs loaded with 100Ω across each output pair, unless otherwise stated.

2: Specification for packaged product only.

3: Skew is measured between outputs under identical transitions.

4: See Section 6.0, Timing Diagram.

5: Cycle-to-cycle jitter definition: the variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{JITTER\_CC} = T_n – T_{n+1}$, where T is the time between rising edges of the output signal.

6: Total jitter definition: with an ideal clock input of frequency - f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

TABLE 1-5: TEMPERATURE SPECIFICATIONS

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Range						
Operating Ambient Temperature	T_A	–40	—	+85	°C	—
Lead Temperature	T_{LEAD}	—	+260	—	°C	Soldering, 20 sec.
Storage Temperature	T_S	–65	—	+150	°C	—
Package Thermal Resistance						
VQFN, Still Air	θ_{JA}	—	+60	—	°C/W	—
VQFN, 500 lfpm		—	+54	—	°C/W	—
VQFN, Junction-to-Board (Note 1)	ψ_{JB}	—	+32	—	°C/W	—

Note 1: Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the pcb.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
12, 9	IN, /IN	**Differential Input:** Internal 50Ω termination resistors to VT input. Flexible input accepts any differential input. See Section 9.0, Input Interface Applications.
1, 2, 3, 4	Q0, /Q0 Q1, /Q1	**Differential Buffered LVDS Outputs:** Divided by 1, 2, 4, 8 or 16. See Table 2-2. Unused output pairs must be terminated with 100Ω across the different pair.
16, 15, 5	S0, S1, S2	**Select Pins:** See Table 2-2. LVTTL/CMOS logic levels. Internal 25 kΩ pull-up resistor. Logic HIGH if left unconnected (divided by 16 mode). Input threshold is $V_{CC}/2$.
6	NC	**No Connect.**
8	/RESET, /DISABLE	**LVTTL/CMOS Logic Levels:** Internal 25 kΩ pull-up resistor. Logic HIGH if left unconnected. Apply LOW to reset the divider (divided by 2, 4, 8, or 16 mode). Also acts as a disable/enable function. The reset and disable function occurs on the next high-to-low clock input transition. Input threshold is $V_{CC}/2$.
10	VREF-AC	**Reference Voltage:** Equal to V_{CC} –1.4V (approx.). Used for AC-coupled applications only. Decouple the VREF–AC pin with a 0.01 µF capacitor. See Section 9.0, Input Interface Applications.
11	VT	**Termination Center-Tap:** For CML or LVDS inputs, leave this pin floating. Otherwise, See Section 9.0, Input Interface Applications.
7, 14	VCC	**Positive Power Supply:** Bypass with 0.1 µF || 0.01 µF low ESR capacitor.
13	GND Exposed	**Ground.** Exposed pad must be connected to the same potential as the GND pin.

TABLE 2-2: TRUTH TABLE

/RESET (Note 1)	S2	S1	S0	Outputs
1	0	X	X	Reference Clock (pass through)
1	1	0	0	Reference Clock ÷2
1	1	0	1	Reference Clock ÷4
1	1	1	0	Reference Clock ÷8
1	1	1	1	Reference Clock ÷16
0 (Note 1)	X	X	X	Q = LOW, /Q = HIGH Clock Disable

Note 1: Reset/Disable function is asserted on the next clock input (IN, /IN) high-to-low transition.

3.0 TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 2.5V and T_A = 25°C, unless otherwise stated.

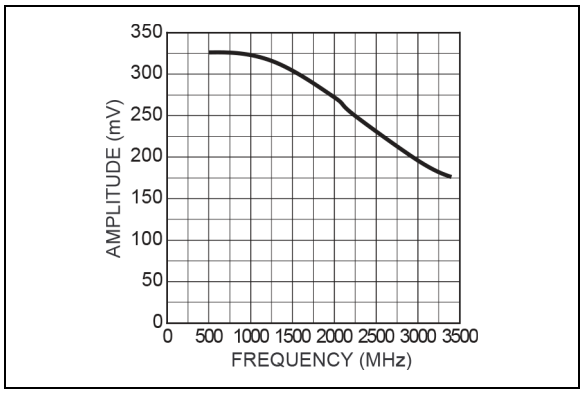


FIGURE 3-1: OUTPUT AMPLITUDE VS. FREQUENCY.

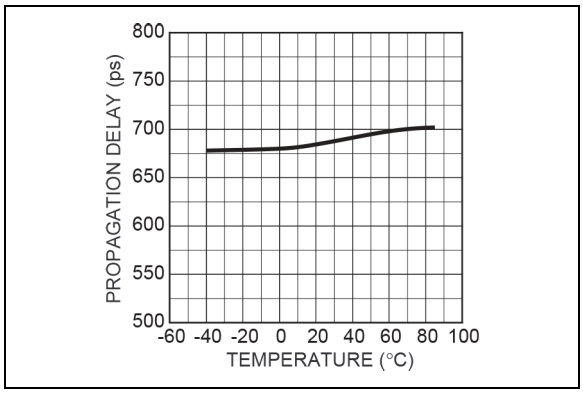


FIGURE 3-3: IN TO Q PROPAGATION DELAY VS. TEMPERATURE.

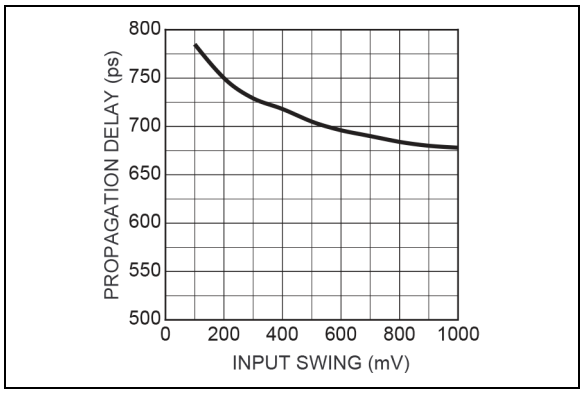


FIGURE 3-2: IN TO Q PROPAGATION DELAY VS. INPUT SWING.

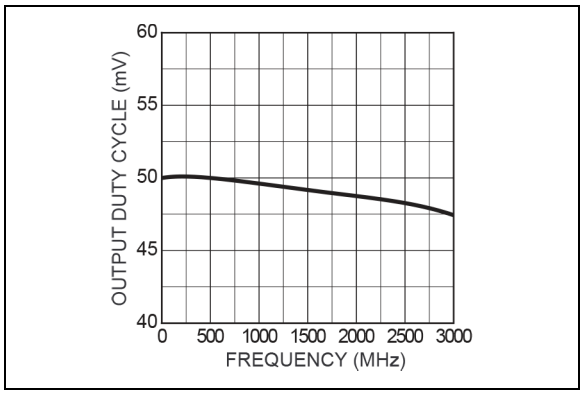


FIGURE 3-4: OUTPUT DUTY CYCLE VS. FREQUENCY.

4.0 TYPICAL FUNCTIONAL CHARACTERISTICS

V_{CC} = 2.5V and T_A = 25°C, unless otherwise stated.

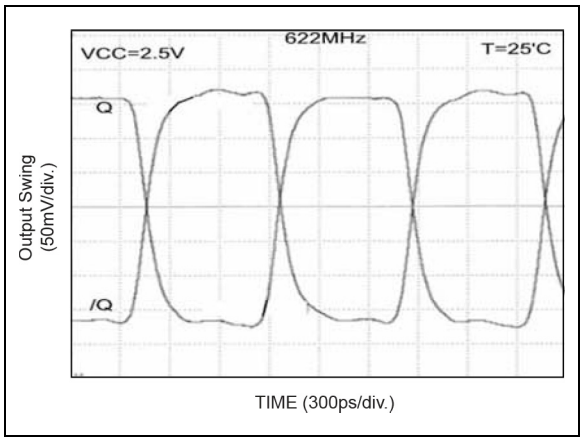


FIGURE 4-1: 622 MHZ OUTPUT.

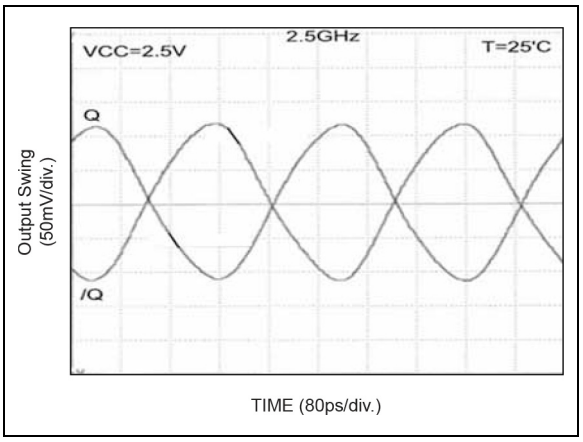


FIGURE 4-3: 2.5 GHZ OUTPUT.

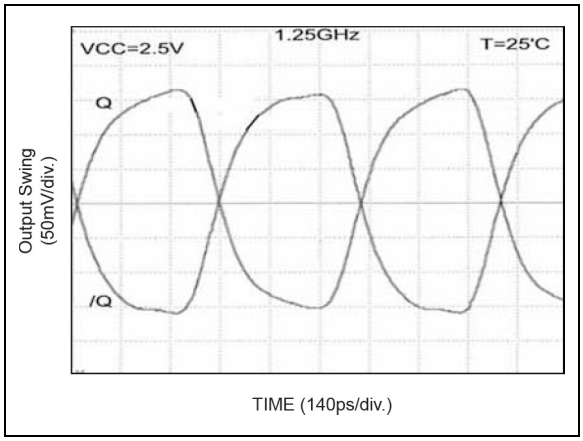


FIGURE 4-2: 1.25 GHZ OUTPUT.

5.0 LVDS OUTPUTS

LVDS (Low Voltage Differential Swing) specifies a small swing of 350 mV typical, on a nominal 1.25V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is also kept tight to keep EMI low.

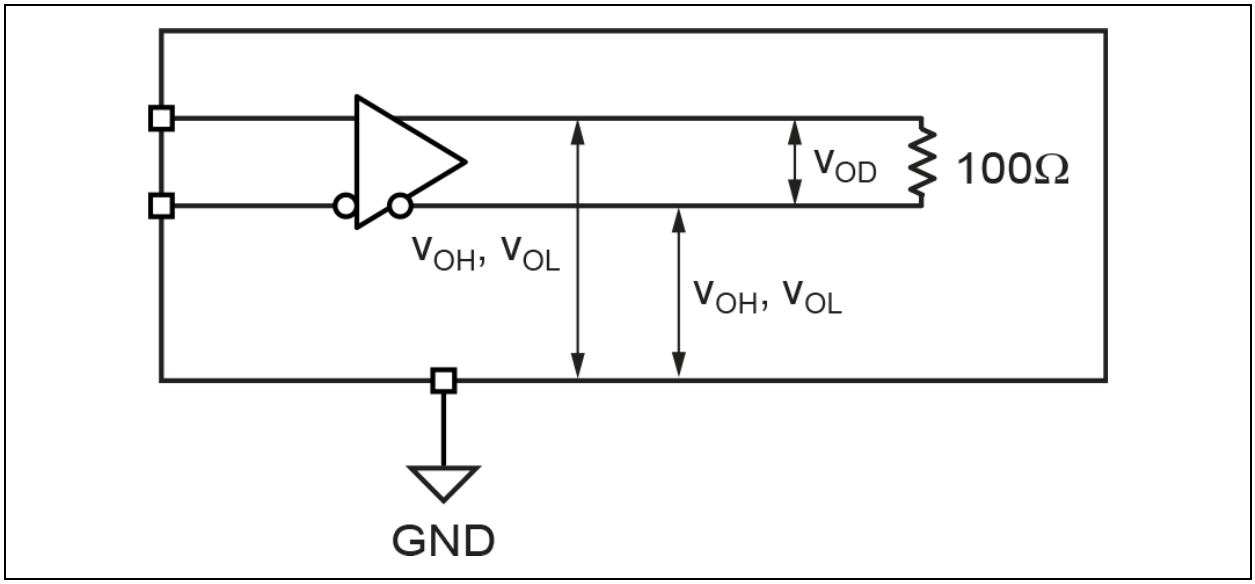


FIGURE 5-1: LVDS DIFFERENTIAL MEASUREMENT.

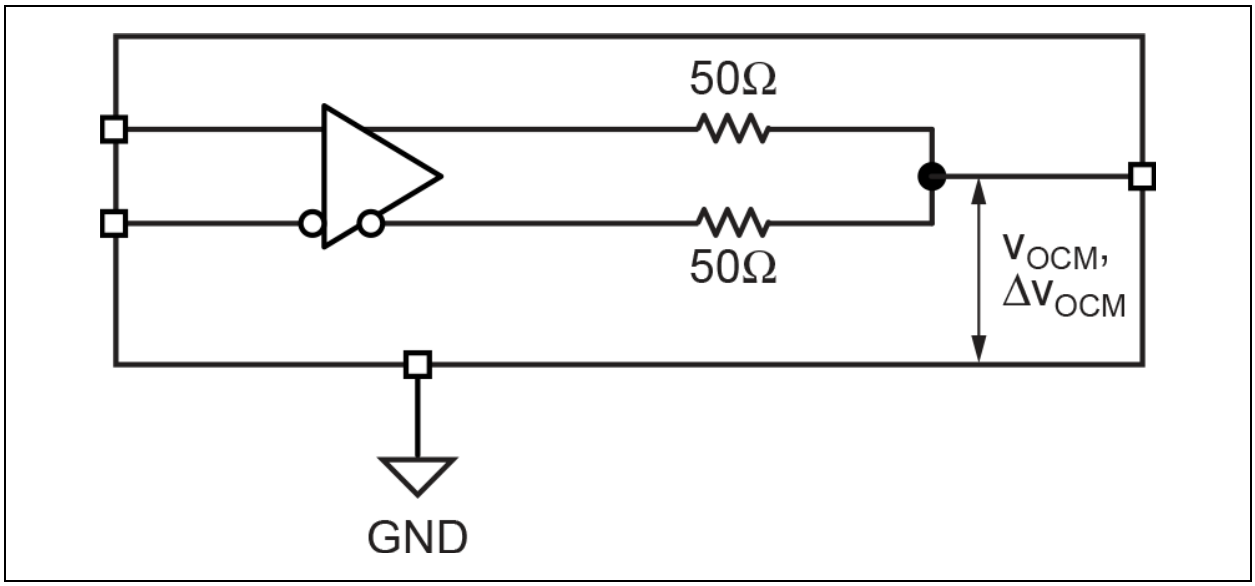


FIGURE 5-2: LVDS COMMON MODE MEASUREMENT.

6.0 TIMING DIAGRAM

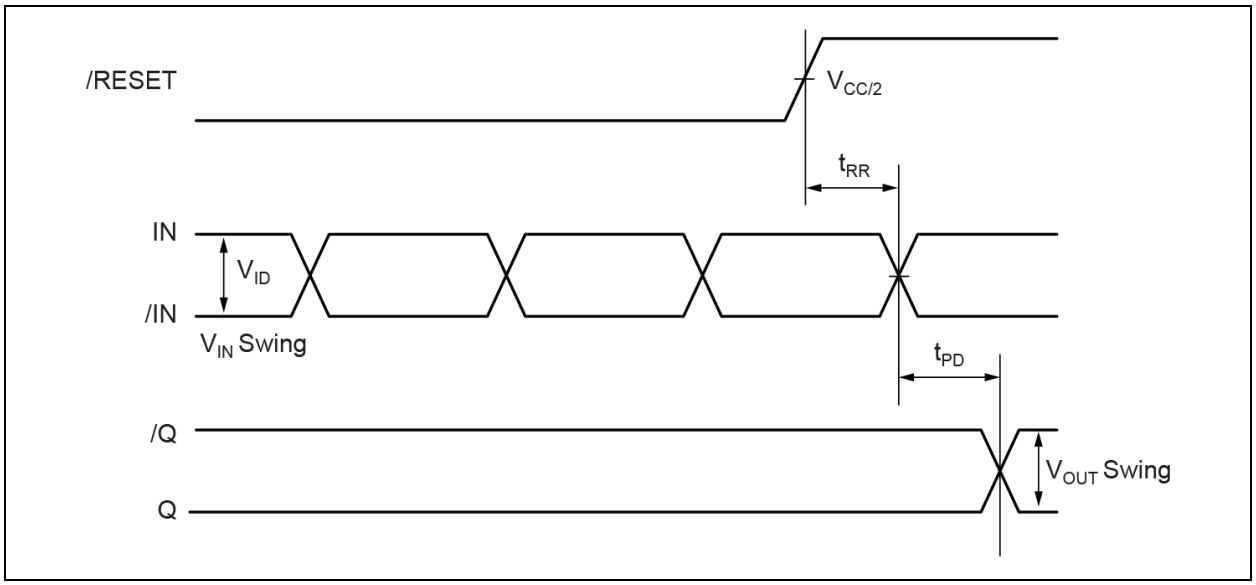


FIGURE 6-1: TIMING DIAGRAM.

7.0 SINGLE-ENDED AND DIFFERENTIAL SWINGS

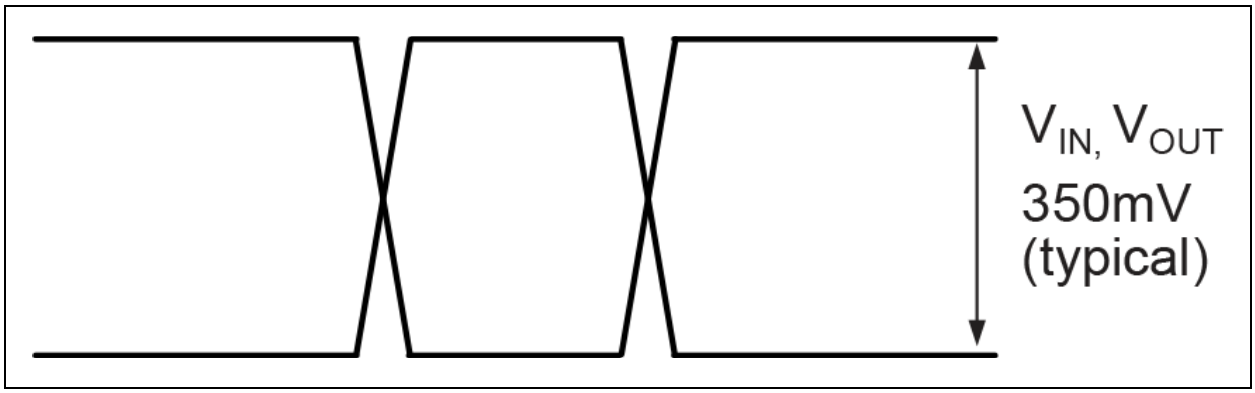


FIGURE 7-1: SINGLE-ENDED SWING.

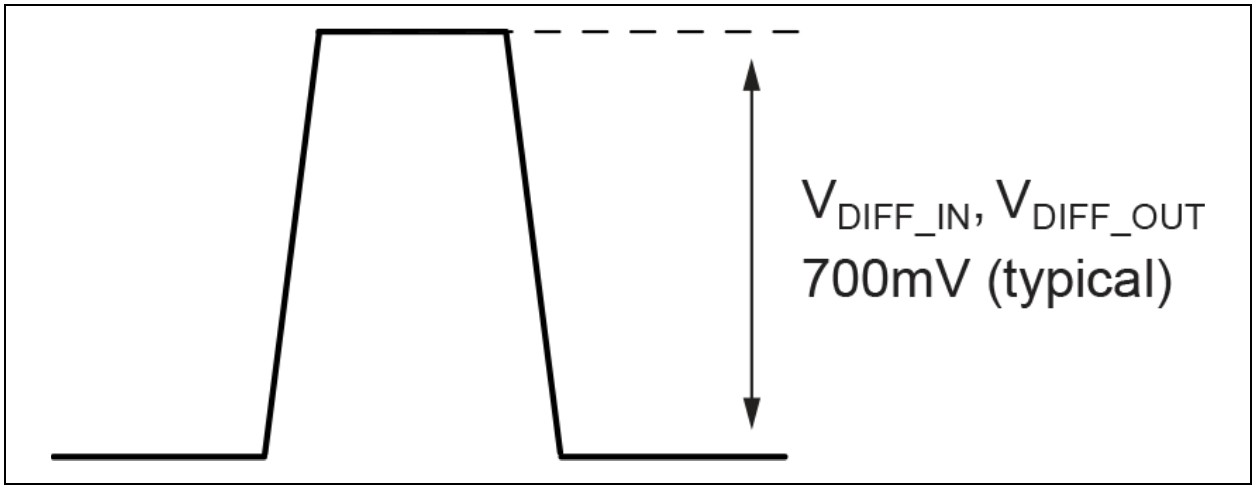


FIGURE 7-2: DIFFERENTIAL SWING.

8.0 INPUT INTERFACE BUFFERS

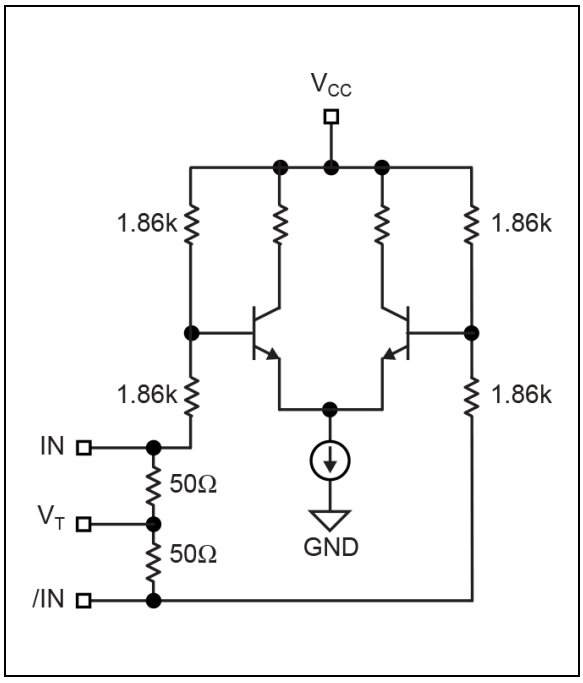


FIGURE 8-1: SIMPLIFIED DIFFERENTIAL INPUT BUFFER.

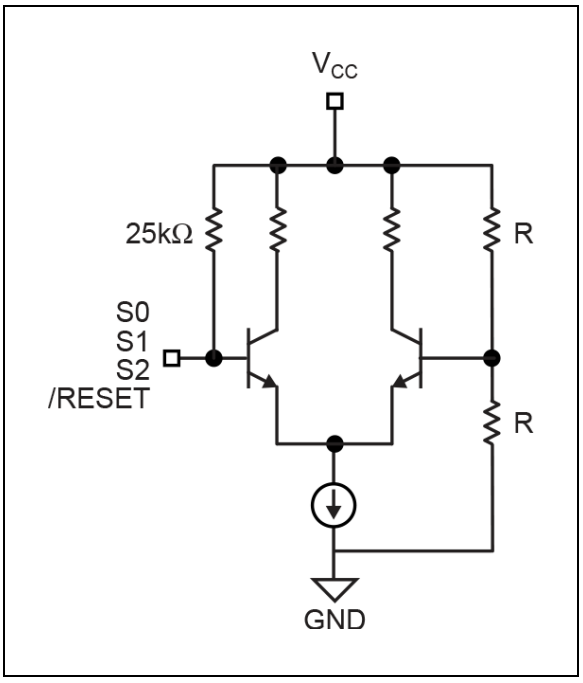


FIGURE 8-2: SIMPLIFIED TTL/CMOS INPUT BUFFER.

9.0 INPUT INTERFACE APPLICATIONS

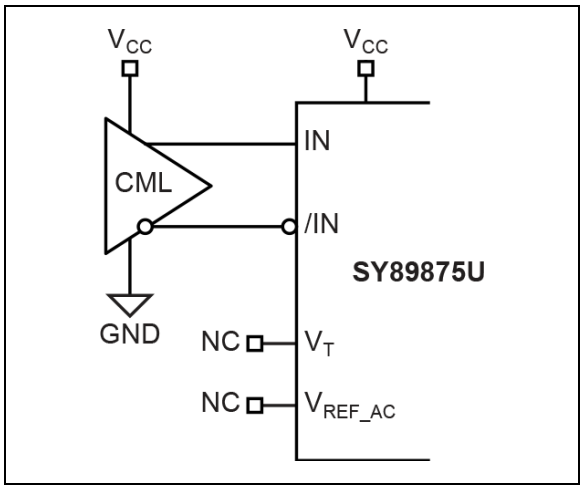


FIGURE 9-1: DC-COUPLED CML INPUT INTERFACE.

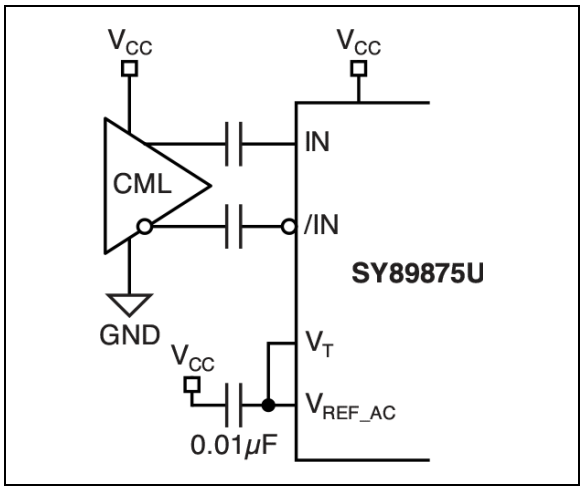


FIGURE 9-2: AC-COUPLED CML INPUT INTERFACE.

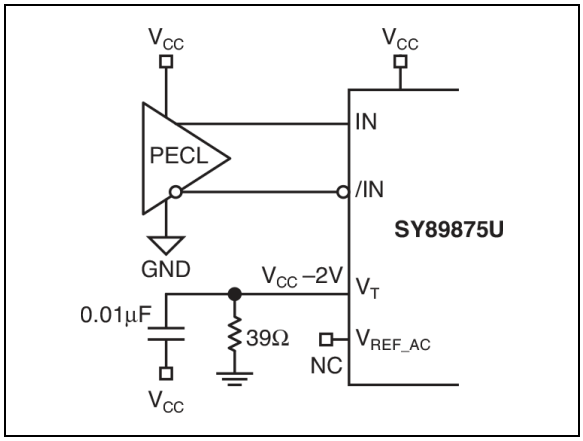


FIGURE 9-3: DC-COUPLED PECL INPUT INTERFACE.

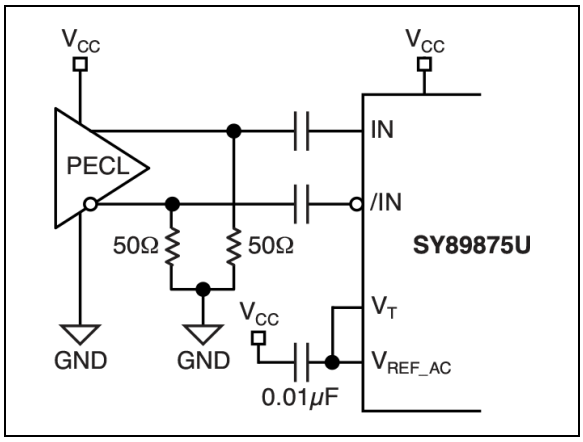


FIGURE 9-4: AC-COUPLED PECL INPUT INTERFACE.

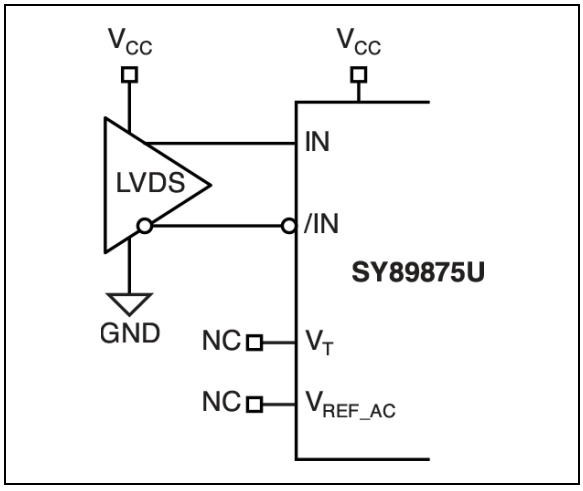


FIGURE 9-5: DC-COUPLED LVDS INPUT INTERFACE.

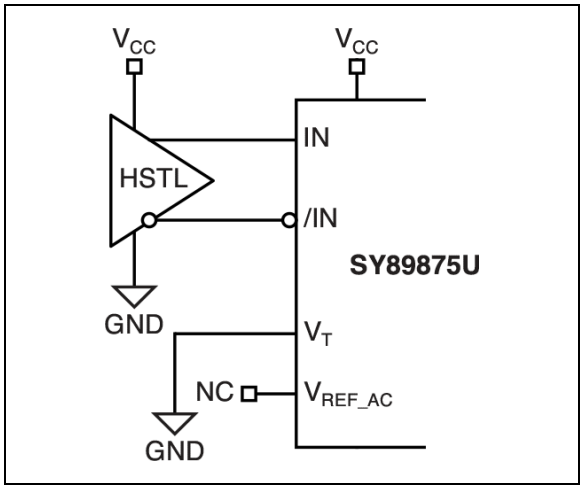
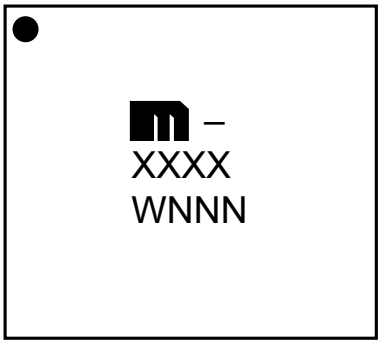


FIGURE 9-6: DC-COUPLED HSTL INPUT INTERFACE.

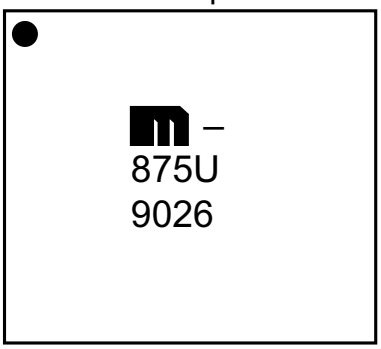
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

16-Lead VQFN*



Example*



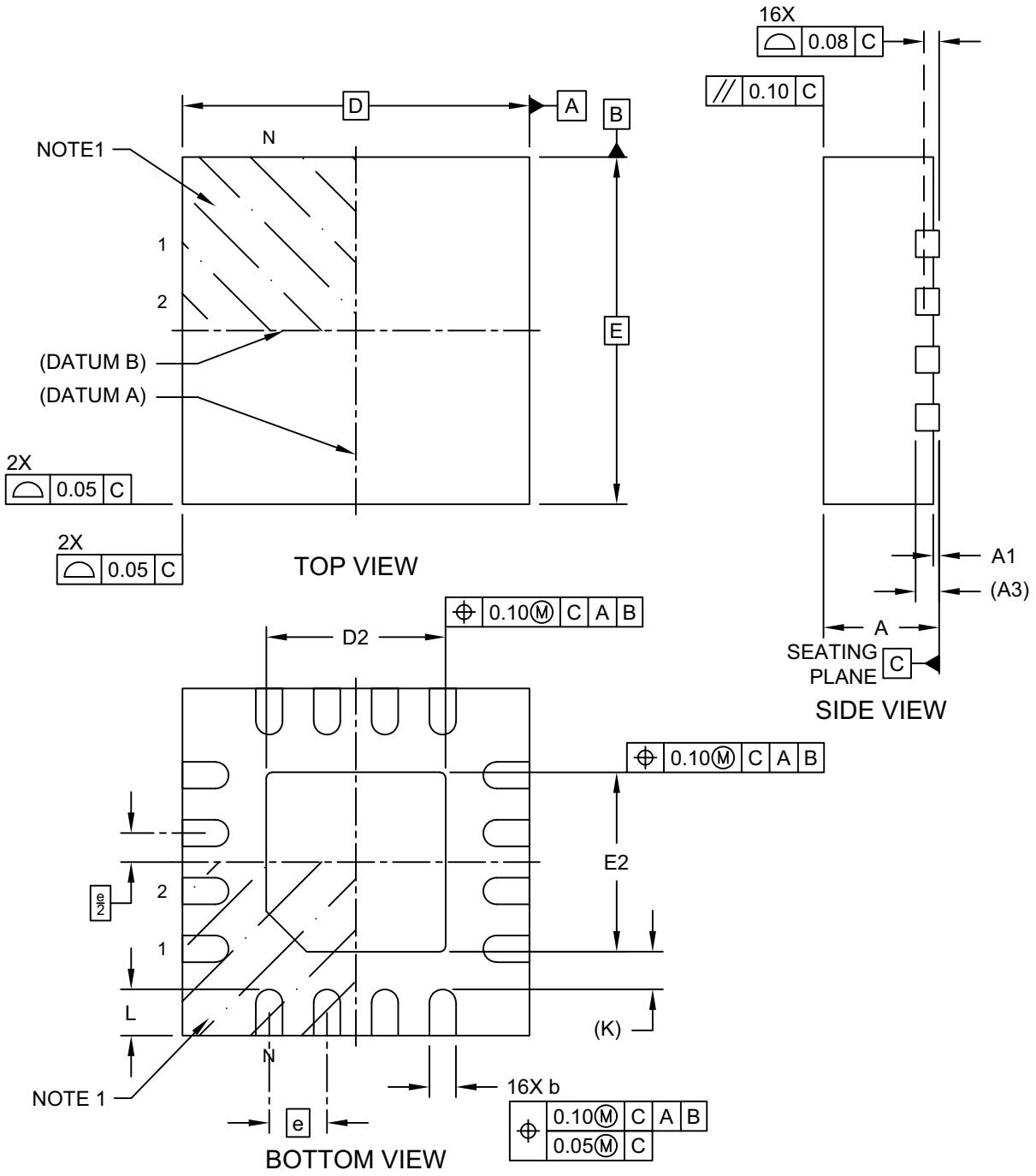
Legend:	XX...X	Product code or customer-specific information
	W	Week code
	NNN	Alphanumeric traceability code (week)
	*	This package is Pb-free. The Pb-free JEDEC designator can be found on the outer packaging for this package.
	●	Pin one index is identified by a dot

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

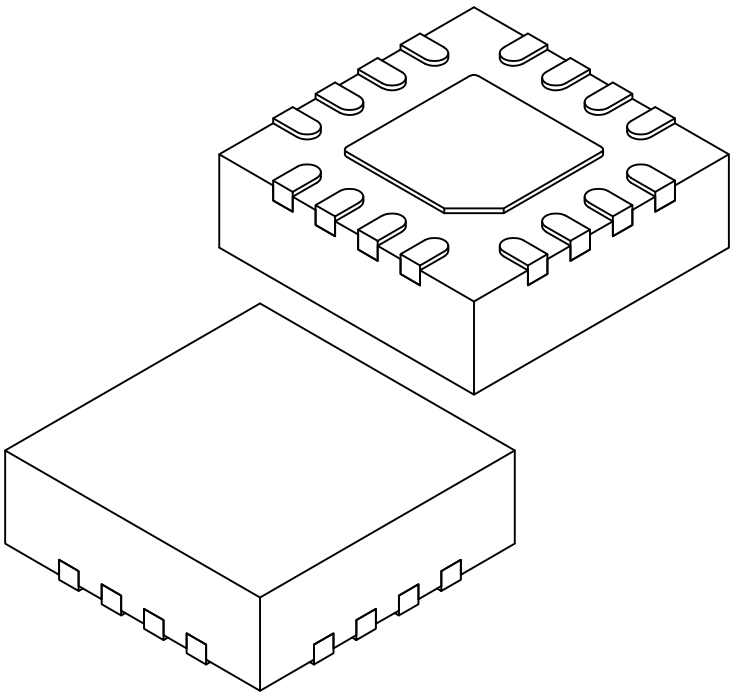
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1103-NCA Rev C Sheet 1 of 2

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.50	1.55	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.55	1.60
Terminal Width	b	0.18	0.23	0.28
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.33 REF	

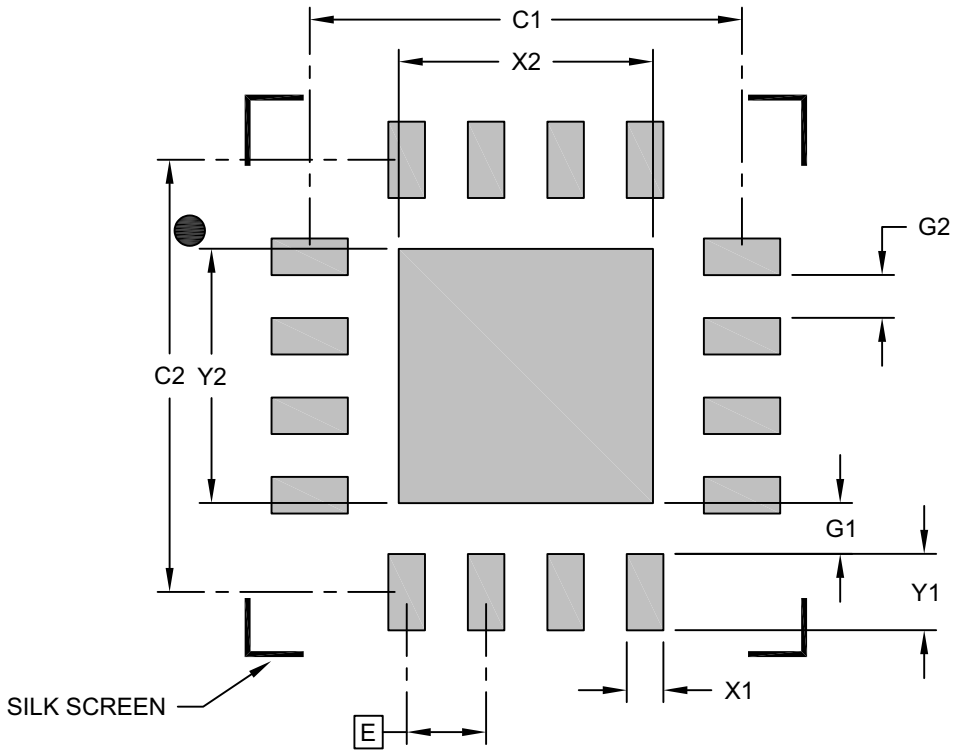
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1103-NCA Rev C Sheet 2 of 2

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.60
Center Pad Length	Y2			1.60
Contact Pad Spacing	C1		2.72	
Contact Pad Spacing	C2		2.72	
Contact Pad Width (Xnn)	X1			0.23
Contact Pad Length (Xnn)	Y1			0.48
Contact Pad to Center Pad (Xnn)	G1	0.32		
Contact Pad to Contact Pad (Xnn)	G2	0.27		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3103-NCA Rev C

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (March 2024)

- Converted Micrel data sheet for SY89875U to Microchip format as DS20006884A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Supply Voltage Range	Package	Temperature Range	Special Processing

Device:	SY89875	=	2.5V, 2.0 GHz Any Differential IN-to-LVDS Programmable Clock Divider and 1:2 Fanout Buffer with Internal Termination
Voltage Option:	U	=	2.5V
Package:	M	=	16-Lead VQFN
Temperature Range:	G	=	–40°C to 85°C
Special Processing:	<blank>	=	100/Tube
	TR	=	1,000/Reel

Examples:

a) **SY89875UMG**

2.5V, 16-Lead VQFN, –40°C to 85°C, 100/Tube

b) **SY89875UMG-TR**

2.5V, 16-Lead VQFN, –40°C to 85°C, 1,000/Reel

NOTES:

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