SY100EP14U

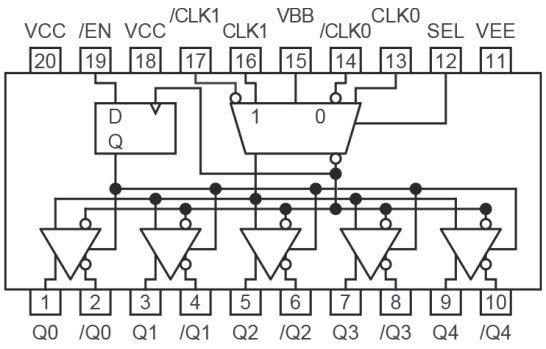
2.5V/3.3V/5V 1:5 LVPECL/PECL/ECL/HSTL 2 GHz Clock Driver with 2:1 Differential Input MUX

Features

- Guaranteed AC parameters over temp/voltage:
  - 2 GHz f_{MAX}
  - 25 ps within-device skew
  - 275 ps tr/tf time
  - 525 ps prop delay
- 2:1 Differential MUX input
- Flexible supply voltage: 2.5V/3.3V/5V
- Wide operating temperature range: –40°C to +85°C
- V_{BB} reference for single-ended or AC-coupled PECL inputs
- 100K ECL compatible outputs
- Inputs accept PECL/LVPECL/ECL/HSTL logic
- 75 kΩ internal input pull-down resistors
- Available in a 20-Lead TSSOP package

Package Type

SY100EP14U
20-Lead TSSOP



General Description

The SY100EP14U is a high-speed, 2 GHz differential PECL/ECL 1:5 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 25 ps over temperature and supply voltage. The wide supply voltage operation allows this fanout buffer to operate in 2.5V, 3.3V, and 5V systems.

A V_{BB} reference is included for single-supply or AC-coupled PECL/ECL input applications, thus eliminating resistor networks. When interfacing to a single-ended or AC-coupled PECL/ECL input signal, connect the VBB pin to the unused /CLK pin, and bypass the pin to VCC through a 0.01 µF capacitor.

The SY100EP14U features a 2:1 input MUX, making it an ideal solution for redundant clock switchover applications. If only one input pair is used, the other pair may be left floating. In addition, this device includes a synchronous enable pin that forces the outputs into a fixed logic state. Enable or disable state is initiated only after the outputs are in a LOW state, thus eliminating the possibility of a “runt” clock pulse.

The SY100EP14U I/O are fully differential and 100K ECL compatible. Differential 10K ECL logic can interface directly into the SY100EP14U inputs.

The SY100EP14U is part of Micrel’s high-speed clock synchronization family. For applications that require a different I/O combination, consult the Microchip website at www.microchip.com, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators, and clock generators.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Power Supply Voltage (V_{CC} – V_{EE}) ..... +6.0V
Input Voltage (V_{IN}), Note 1 ..... –6.0V to V_{CC} 0V
Input Voltage (V_{IN}), Note 2 ..... +6.0V to V_{EE} 0V
Continuous Output Current (I_{OUT}) ..... 50 mA
Surge Output Current (I_{OUT}) ..... 100 mA
V_{BB} Source or Sink Current (I_{BB}), Note 3 ..... ±0.5 mA
ESD, Note 4 ..... >1.5 kV

Operating Ratings ††

Supply Voltage Range (V_{CC}) for PECL ..... +4.5V to +5.5V
Supply Voltage Range (V_{CC}) for LVPECL ..... +2.37V to +3.8V
Supply Voltage Range (V_{CC}) for ECL ..... –4.5V to –5.5V
Supply Voltage Range (V_{CC}) for LVECL ..... –3.8V to –2.37V

† Notice: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†† Notice: The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 1: V_{CC} = 0V, V_{IN} not more negative than V_{EE}.

2: V_{EE} = 0V, V_{IN} not more positive than V_{CC}.

3: Due to the limited drive capability, use for inputs of same package only (i.e., do not use for other devices).

4: MIL-STD-883 Test Method 3015.7, Human Body Model, all pins.

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS (Note 1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
When T_A = –40°C, then:						
Power Supply Voltage for PECL	V_{CC}	4.5	5.0	5.5	V	—
Power Supply Voltage for LVPECL		2.37	3.3	3.8	V	—
Power Supply Voltage for ECL		–4.5	–5.0	–5.5	V	—
Power Supply Voltage for LVECL		–3.8	–3.3	–2.37	V	—
Power Supply Current	I_{CC}	—	—	75	mA	—
Input HIGH Current	I_{IH}	—	—	150	µA	V_{IN} = V_{IH}
Input LOW Current (D)	I_{IL}	0.5	—	—	µA	V_{IN} = V_{IL}
Input LOW Current (/D)		–150	—	—	µA	V_{IN} = V_{IL}
Input Capacitance (TSSOP)	C_{IN}	—	0.75	—	pF	—

Note 1: 100 KEP circuits are designed to meet the DC specifications shown in this table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse air-flow greater than 500 lfpm is maintained.

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS (Note 1) (CONTINUED)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
When T_A = +25°C, then:						
Power Supply Voltage for PECL	V_{CC}	4.5	5.0	5.5	V	—
Power Supply Voltage for LVPECL		2.37	3.3	3.8	V	—
Power Supply Voltage for ECL		–4.5	–5.0	–5.5	V	—
Power Supply Voltage for LVECL		–3.8	–3.3	–2.37	V	—
Power Supply Current	I_{CC}	—	—	78	µA	—
Input HIGH Current	I_{IH}	—	—	150	µA	$V_{IN} = V_{IH}$
Input LOW Current (D)	I_{IL}	0.5	—	—	µA	$V_{IN} = V_{IL}$
Input LOW Current (/D)		–150	—	—	pF	$V_{IN} = V_{IL}$
Input Capacitance (TSSOP)	C_{IN}	—	0.75	—	V	—
When T_A = +85°C, then:						
Power Supply Voltage for PECL	V_{CC}	4.5	5.0	5.5	V	—
Power Supply Voltage for LVPECL		2.37	3.3	3.8	V	—
Power Supply Voltage for ECL		–4.5	–5.0	–5.5	V	—
Power Supply Voltage for LVECL		–3.8	–3.3	–2.37	V	—
Power Supply Current	I_{CC}	—	—	82	mA	—
Input HIGH Current	I_{IH}	—	—	150	µA	$V_{IN} = V_{IH}$
Input LOW Current (D)	I_{IL}	0.5	—	—	µA	$V_{IN} = V_{IL}$
Input LOW Current (/D)		–150	—	—	µA	$V_{IN} = V_{IL}$
Input Capacitance (TSSOP)	C_{IN}	—	0.75	—	pF	—

Note 1: 100 KEP circuits are designed to meet the DC specifications shown in this table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse air-flow greater than 500 lfpm is maintained.

TABLE 1-2: (100KEP) LVPECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5%, V_{EE} = 0V. All values applicable for when T_A = –40°C, T_A = +25°C, or T_A = +85°C (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input LOW Voltage (Single-ended)	V_{IL}	555	—	875	mV	Note 2
Input HIGH Voltage (Single-ended)	V_{IH}	1335	—	1620	mV	Note 2
Output LOW Voltage	V_{OL}	555	680	805	mV	50Ω to V_{CC} – 2V
Output HIGH Voltage	V_{OH}	1355	1480	1605	mV	50Ω to V_{CC} – 2V
Input HIGH Voltage Common Mode Range	V_{IHCMR}	1.2	—	V_{CC}	V	Note 3

Note 1: 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500 lfpm is maintained. Input and output varies 1:1 with V_{CC}.

2: V_{BB} reference is not functional for V_{CC} < 3.0V. External V_{BB} equivalent is required.

3: V_{IHCMR} (min.) varies 1:1 with V_{EE}, V_{IHCMR} (max.) varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

TABLE 1-3: (100KEP) LVPECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V ±10%, V_{EE} = 0V. All values applicable for when T_A = –40°C, T_A = +25°C, or T_A = +85°C (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input LOW Voltage (Single-ended)	V_{IL}	1355	—	1675	mV	—
Input HIGH Voltage (Single-ended)	V_{IH}	2075	—	2420	mV	—
Output LOW Voltage	V_{OL}	1355	1480	1605	mV	50Ω to V_{CC} – 2V
Output HIGH Voltage	V_{OH}	2155	2280	2405	mV	50Ω to V_{CC} – 2V
Reference Voltage	V_{BB}	1775	1875	1975	mV	V_{CC} = +3.3V, Note 2
Input HIGH Voltage Common Mode Range	V_{IHCMR}	1.2	—	V_{CC}	V	Note 3

Note 1: 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500 lfpm is maintained. Input and output varies 1:1 with V_{CC}.

2: Single-ended input operation is limited $V_{CC} \geq 3.0V$ in LVPECL mode. V_{BB} reference varies 1:1 with V_{CC}.

3: V_{IHCMR} (min.) varies 1:1 with V_{EE}, V_{IHCMR} (max.) varies 1:1 with VCC. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

TABLE 1-4: (100KEP) PECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{EE} = 0V. All values applicable for when T_A = –40°C, T_A = +25°C, or T_A = +85°C (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input LOW Voltage (Single-ended)	V_{IL}	3055	—	3375	mV	—
Input HIGH Voltage (Single-ended)	V_{IH}	3775	—	4120	mV	—
Output LOW Voltage	V_{OL}	3055	3180	3305	mV	50Ω to V_{CC} – 2V
Output HIGH Voltage	V_{OH}	3855	3980	4105	mV	50Ω to V_{CC} – 2V
Output Voltage Reference	V_{BB}	3475	3575	3675	mV	V_{CC} = +5.0V, Note 2
Input HIGH Voltage Common Mode Range	V_{IHCMR}	2.0	—	V_{CC}	V	Note 3

Note 1: 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500 lfpm is maintained. Input and output parameters are at V_{CC} = 5.0V. They vary 1:1 with V_{CC}.

2: V_{BB} reference varies 1:1 with V_{CC}.

3: The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Single-ended input CLK pin operation is limited to VCC ≥ 3.0V in PECL mode.

TABLE 1-5: (100KEP) LVECL DC ELECTRICAL CHARACTERISTICS

V_{EE} = –2.37V to –3.8V; V_{CC} = 0V. All values applicable for when T_A = –40°C, T_A = +25°C, or T_A = +85°C (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input LOW Voltage (Single-ended)	V_{IL}	–1945	—	–1625	mV	—
Input HIGH Voltage (Single-ended)	V_{IH}	–1165	—	–880	mV	—
Output LOW Voltage	V_{OL}	–1945	–1820	–1695	mV	50Ω to V_{CC} – 2V
Output HIGH Voltage	V_{OH}	–1145	–1020	–895	mV	50Ω to V_{CC} – 2V
Output Voltage Reference	V_{BB}	–1525	–1425	–1325	mV	Note 2
Input HIGH Voltage Common Mode Range	V_{IHCMR}	V_{EE} + 1.2		0.0	V	Note 3

Note 1: 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500 lfpm is maintained. Input and output parameters vary 1:1 with V_{CC}.

2: Single-ended input operation is limited $V_{EE} \leq -3.0V$ in ECL/LVECL mode. V_{BB} reference varies 1:1 with V_{CC}.

3: V_{IHCMR} (min.) varies 1:1 with V_{EE}, V_{IHCMR} (max.) varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

TABLE 1-6: (100K) ECL/LVECL DC ELECTRICAL CHARACTERISTICS

V_{CC} = 0V, V_{EE} = –5.5V to –3.0V. All values applicable for when T_A = –40°C, T_A = +25°C, or T_A = +85°C. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input LOW Voltage (Single-ended)	V_{IL}	–1945	—	–1625	mV	—
Input HIGH Voltage (Single-ended)	V_{IH}	–1225	—	–880	mV	—
Output LOW Voltage	V_{OL}	–1945	–1820	–1695	mV	50Ω to V_{CC} – 2V, Note 2
Output HIGH Voltage	V_{OH}	–1145	–1020	–895	mV	50Ω to V_{CC} – 2V, Note 2
Output Voltage Reference	V_{BB}	–1525	–1425	–1325	mV	Note 3
Input HIGH Voltage Common Mode Range	V_{IHCMR}	V_{EE} + 1.2		0.0	V	Note 4

Note 1: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500 lfpm is maintained. Input and output parameters vary 1:1 with V_{CC}.

2: All loading with 50Ω to V_{CC} –2.0V.

3: Single-ended input operation is limited $V_{EE} \leq -3.0V$ in ECL/LVECL mode. V_{BB} reference varies 1:1 with V_{CC}.

4: V_{IHCMR} (min.) varies 1:1 with V_{EE}, (max.) varies 1:1 with V_{CC}. The V_{IHCMR} is referenced to the most positive side of the differential input signal.

TABLE 1-7: HSTL INPUT DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.37V to 3.8V; V_{EE} = 0V. All values applicable for when T_A = –40°C, T_A = +25°C, or T_A = +85°C.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Condition**
Input HIGH Voltage	V_{IH}	1200	—	—	mV	—
Input LOW Voltage	V_{IL}	—	—	400	mV	—
Input Crossover Voltage	V_X	680	—	900	mV	—

TABLE 1-8: AC ELECTRICAL CHARACTERISTICS

LVPECL: V_{CC} = 2.37V to 2.625V, V_{EE} = 0V; **PECL:** V_{CC} = 4.50V to 5.50V, V_{EE} = 0V; **ECL:** V_{EE} = –4.50V to –5.5V, V_{CC} = 0V; **LVECL:** V_{EE} = –2.37V to –3.8V, V_{CC} = 0V						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
When T_A = –40°C, then:						
Maximum Frequency	f_{MAX}	2.0	—	—	GHz	V_{OUT} ≥ 200 mV, Note 1
PECL/ECL IN (Differential)	t_{PLH}	250	330	400	ps	V_{CC} = 5V PropagationDelay to Output
PECL/ECL IN (Single-ended)	t_{PHL}	—	—	—	ps	V_{CC} = 5V PropagationDelay to Output
LVPECL/LVECL IN (Differential)	t_{PLH}	275	350	425	ps	V_{CC} = 2.37V to 3.8V PropagationDelay to Output
LVPECL/LVECL IN (Single-ended)	t_{PHL}	—	—	—	ps	V_{CC} = 2.37V to 3.8V PropagationDelay to Output
PECL/ECL Within-Device Skew (Differential)	t_{SKEW}	—	25	35	ps	V_{CC} = 5V, Note 2
PECL/ECL Part-to-Part Skew (Differential)	t_{SKEW}	—	100	125	ps	V_{CC} = 5V, Note 2
LVPECL/LVECL Within-Device Skew (Differential)	t_{SKEW}	—	10	25	ps	V_{CC} = 2.37V to 3.8V, Note 2
LVPECL/LVECL Part-to-Part Skew (Differential)	t_{SKEW}	—	100	125	ps	V_{CC} = 2.37V to 3.8V, Note 2
Set-up Time	t_S	100	50	—	ps	/EN to CLK, Note 3
Hold Time	t_H	200	140	—	ps	/EN to CLK, Note 3
Minimum Input Swing	V_{PP}	150	800	1200	mV	—
PECL/ECL Output Rise/Fall Times (20% to 80%)	t_r, t_f	100	180	240	ps	—
LVPECL/LVECL Output Rise/Fall Times	t_r, t_f	90	130	225	ps	V_{CC} = 2.37V to 3.8V
When T_A = +25°C, then:						
Maximum Frequency	f_{MAX}	2.0	—	—	GHz	V_{OUT} ≥ 200 mV, Note 1
PECL/ECL IN (Differential)	t_{PLH}	250	330	450	ps	V_{CC} = 5V PropagationDelay to Output
PECL/ECL IN (Single-ended)	t_{PHL}	—	355	—	ps	V_{CC} = 5V PropagationDelay to Output
LVPECL/LVECL IN (Differential)	t_{PLH}	275	350	475	ps	V_{CC} = 2.37V to 3.8V PropagationDelay to Output
LVPECL/LVECL IN (Single-ended)	t_{PHL}	—	375	—	ps	V_{CC} = 2.37V to 3.8V PropagationDelay to Output
PECL/ECL Within-Device Skew (Differential)	t_{SKEW}	—	30	45	ps	V_{CC} = 5V, Note 2
PECL/ECL Part-to-Part Skew (Differential)	t_{SKEW}	—	150	175	ps	V_{CC} = 5V, Note 2
LVPECL/LVECL Within-Device Skew (Differential)	t_{SKEW}	—	15	25	ps	V_{CC} = 2.37V to 3.8V, Note 2
LVPECL/LVECL Part-to-Part Skew (Differential)	t_{SKEW}	—	150	175	ps	V_{CC} = 2.37V to 3.8V, Note 2
Set-up Time	t_S	100	50	—	ps	/EN to CLK, Note 3
Hold Time	t_H	200	140	—	ps	/EN to CLK, Note 3
Minimum Input Swing	V_{PP}	150	800	1200	mV	—

TABLE 1-8: AC ELECTRICAL CHARACTERISTICS (CONTINUED)

LVPECL: V_{CC} = 2.37V to 2.625V, V_{EE} = 0V; **PECL:** V_{CC} = 4.50V to 5.50V, V_{EE} = 0V; **ECL:** V_{EE} = –4.50V to –5.5V, V_{CC} = 0V; **LVECL:** V_{EE} = –2.37V to –3.8V, V_{CC} = 0V						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PECL/ECL Output Rise/Fall Times (20% to 80%)	t_r, t_f	105	180	270	ps	—
LVPECL/LVECL Output Rise/Fall Times	t_r, t_f	95	130	250	ps	V_{CC} = 2.37V to 3.8V
When T_A = +85°C, then:						
Maximum Frequency	f_{MAX}	2.0	—	—	GHz	V_{OUT} ≥ 200 mV, Note 1
PECL/ECL IN (Differential)	t_{PLH}	250	330	600	ps	V_{CC} = 5V PropagationDelay to Output
PECL/ECL IN (Single-ended)	t_{PHL}	—	—	—	ps	V_{CC} = 5V PropagationDelay to Output
LVPECL/LVECL IN (Differential)	t_{PLH}	275	350	525	ps	V_{CC} = 2.37V to 3.8V PropagationDelay to Output
LVPECL/LVECL IN (Single-ended)	t_{PHL}	—	—	—	ps	V_{CC} = 2.37V to 3.8V PropagationDelay to Output
PECL/ECL Within-Device Skew (Differential)	t_{SKEW}	—	40	50	ps	V_{CC} = 5V, Note 2
PECL/ECL Part-to-Part Skew (Differential)	t_{SKEW}	—	175	200	ps	V_{CC} = 5V, Note 2
LVPECL/LVECL Within-Device Skew (Differential)	t_{SKEW}	—	15	25	ps	V_{CC} = 2.37V to 3.8V, Note 2
LVPECL/LVECL Part-to-Part Skew (Differential)	t_{SKEW}	—	200	225	ps	V_{CC} = 2.37V to 3.8V, Note 2
Set-up Time	t_S	100	50	—	ps	/EN to CLK, Note 3
Hold Time	t_H	200	140	—	ps	/EN to CLK, Note 3
Minimum Input Swing	V_{PP}	150	800	1200	mV	—
PECL/ECL Output Rise/Fall Times (20% to 80%)	t_r, t_f	110	225	300	ps	—
LVPECL/LVECL Output Rise/Fall Times	t_r, t_f	100	150	275	ps	V_{CC} = 2.37V to 3.8V

Note 1: f_{MAX} is defined as the maximum toggle frequency. Measured with 750 mV input signal, 50% duty cycle, all loading with 50Ω to V_{CC} – 2V.

2: Skew is measured between outputs under identical transitions.

3: Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold time does not apply.

TABLE 1-9: TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	–40	—	+85	°C	—
Lead Temperature	T_{LEAD}	—	+260	—	°C	Soldering, 20 sec.
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistance						
Package Thermal Resistance (Junction-to-Ambient) Still-air (single-layer PCB)	θ_{JA}	—	115	—	°C/W	—
Package Thermal Resistance (Junction-to-Ambient) Still-air (multi-layer PCB)	θ_{JA}	—	75	—		—
Package Thermal Resistance (Junction-to-Ambient) 500 lfpm (multi-layer PCB)	θ_{JA}	—	65	—		—
Package Thermal Resistance (Junction-to-Case)	θ_{JC}	—	21	—	°C/W	—

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Name	Pin Function
CLK0, /CLK0 CLK1, /CLK1	PECL, LVPECL, ECL, LVECL, HSTL Clock or Data Inputs. Internal 75 kΩ pull-down resistors on CLK0, CLK1, and internal 75 kΩ pull-up and 75 kΩ pull-down resistors or /CLK0, /CLK1. For single-ended applications, connect signal into CLK0 and/or CLK1 inputs. /CLK0, /CLK1 default condition is VCC/2 when left floating. CLK0, CLK1 default condition is LOW when left floating.
Q0 to Q4 /Q0 to /Q4	LVPECL, PECL, ECL Differential Outputs: Terminate with 50Ω to VCC–2V. For single-ended applications, terminate the unused output with 50Ω to VCC–2V
/EN	LVPECL, PECL, ECL compatible synchronous enable: When /EN goes HIGH, the QOUT will go LOW and /QOUT will go HIGH on the next LOW input clock transition. Includes a 75kΩ pull-down. Default state is LOW when left floating. The internal latch is clocked on the falling edge of the input clock (CLK0, CLK1).
SEL	LVPECL, PECL, ECL compatible 2:1 Mux input signal select: When SEL is LOW, CLK0 input pair is selected. When SEL is HIGH, CLK1 input pair is selected. Includes a 75kΩ pull-down. Default state is LOW and CLK0 is selected.
VBB	Output Reference Voltage: Equal to VCC–1.7V (approx.), and used for single-ended input signals or AC-coupled applications. For single-ended PECL, LVPECL applications, bypass with a 0.01 µF to VCC. For single-ended LVTTL inputs, bypass to GND. Max. sink/source current is 0.5 mA.
VCC	Positive Power Supply: Bypass with 0.1 µF//0.01 µF low ESR capacitors.
VEE	Negative Power Supply: LVPECL, PECL applications, connect to GND.

TABLE 2-2: TRUTH TABLE

CLK0	CLK1	CLK_SEL	/EN	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L

TABLE 2-3: FUNCTION TABLE

CLK_SEL	Active Input
0	CLK0, /CLK0
1	CLK1, /CLK1

3.0 TERMINATION RECOMMENDATIONS

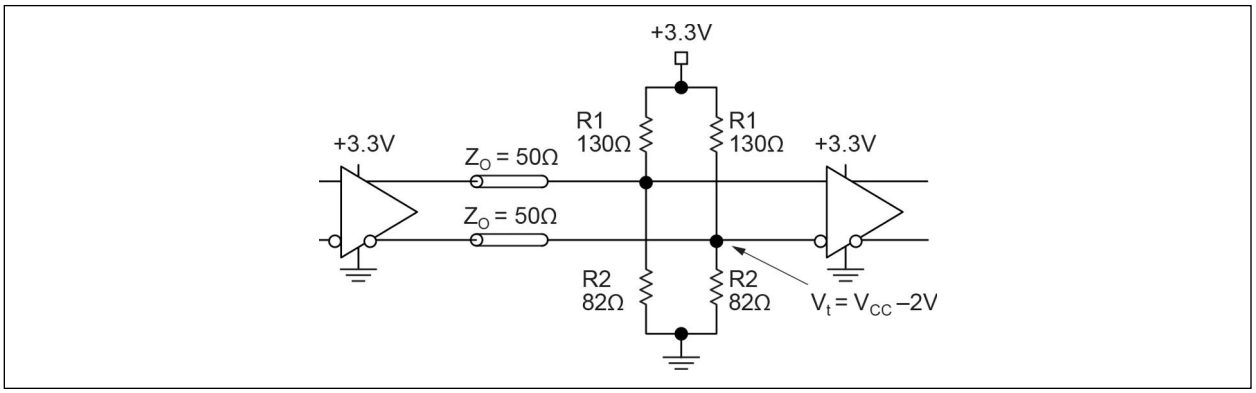


FIGURE 3-1: PARALLEL TERMINATION THEVENIN EQUIVALENT

Note 1: For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω.

2: For +5.0V systems: R1 = 82Ω, R2 = 130Ω.

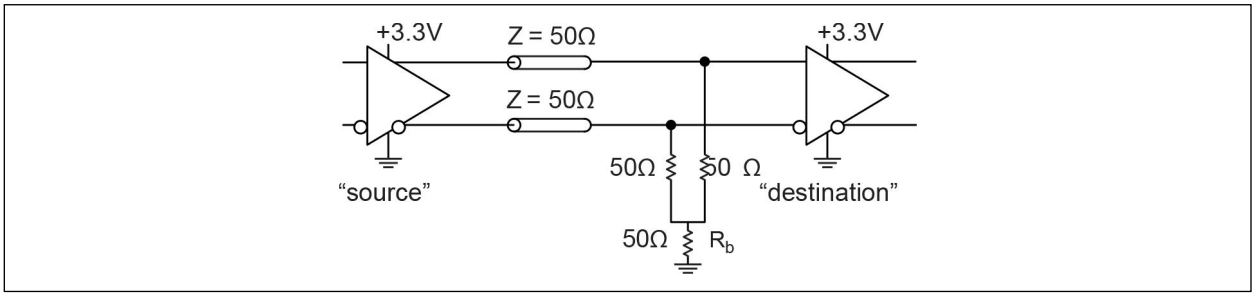


FIGURE 3-2: THREE-RESISTOR "Y-TERMINATION"

Note 1: Power-saving alternative to Thevenin termination.

2: Place termination resistors as close to destination inputs as possible.

3: R_b resistor sets the DC bias voltage, equal to V_t. For +3.3V systems R_b = 46Ω to 50Ω. For +5V systems, R_b = 110Ω.

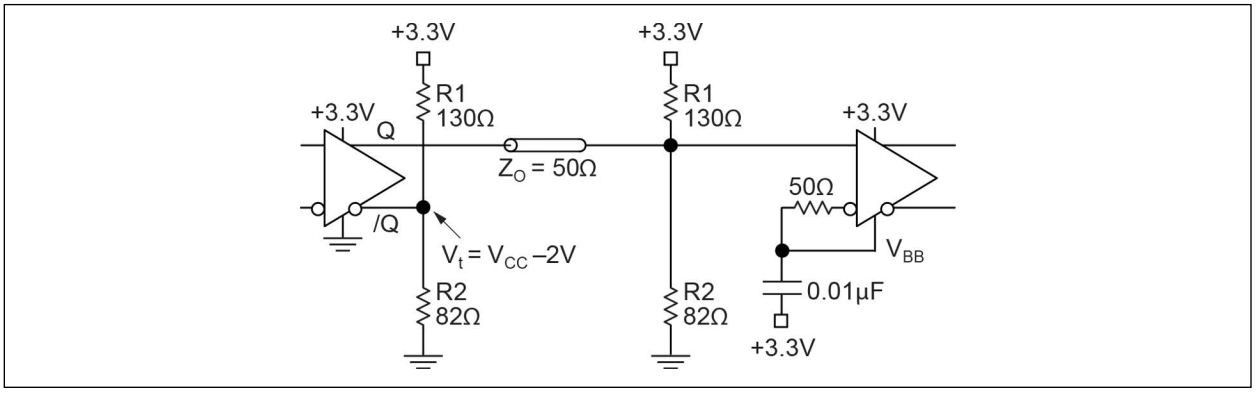


FIGURE 3-3: TERMINATING UNUSED I/O

Note 1: Unused output (/Q) must be terminated to balance the output.

2: Micrel's differential I/O logic devices include a VBB reference pin.

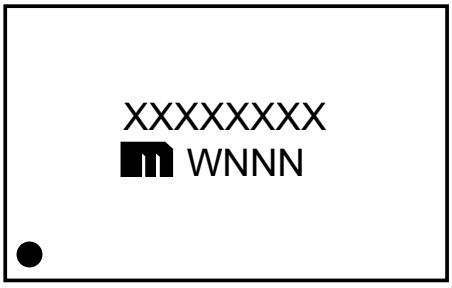
3: Connect unused input through 50Ω to VBB. Bypass with a 0.01 µF capacitor to VCC, not GND.

4: For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω.

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

20-Lead TSSOP*



Example*

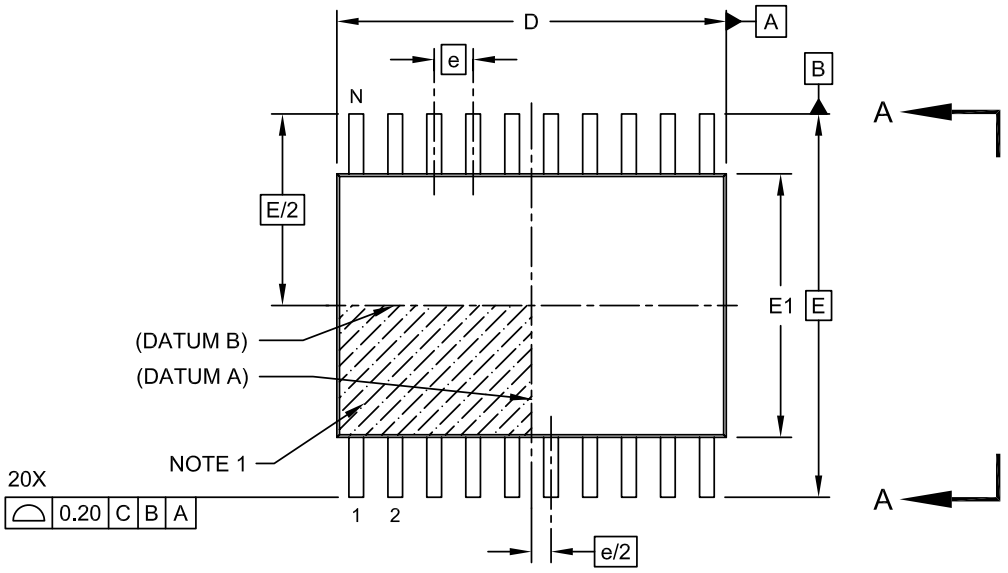
Legend:	XX...X	Product code or customer-specific information
	W	Week code
	NNN	Alphanumeric traceability code (week)
	*	This package is Pb-free. The Pb-free JEDEC designator can be found on the outer packaging for this package.
	●	Pin one index is identified by a dot

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

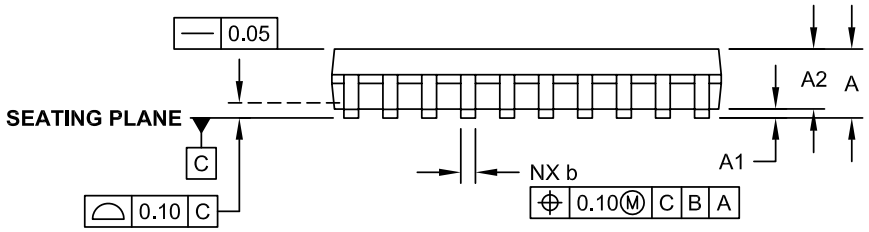
Underbar (_) and/or Overbar (¯) symbol may not be to scale.

20-Lead 4.4 mm TSSOP [G2X] Package Outline and Recommended Land Pattern

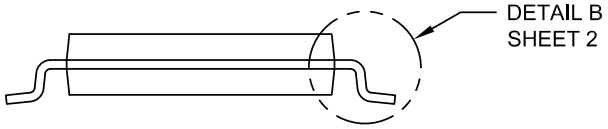
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

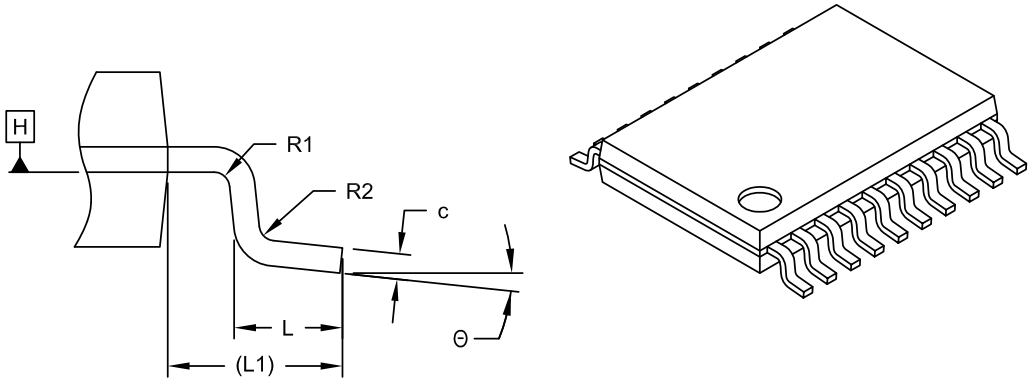


VIEW A—A

Microchip Technology Drawing C04-088C Sheet 1 of 2

20-Lead 4.4 mm TSSOP [G2X] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	6.40	6.50	6.60
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	Θ	0°	-	8°
Lead Width	b	0.19	-	0.30
Lead Thickness	c	0.09	-	0.20
Bend Radius	R1	0.09	-	-
Bend Radius	R2	0.09	-	-

Notes:

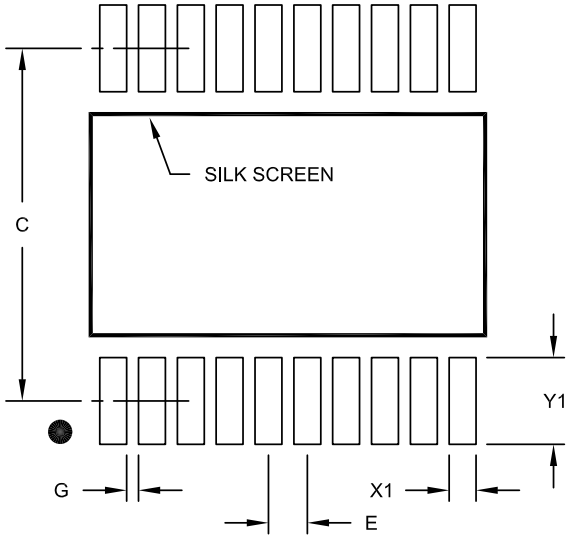
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-088C Sheet 2 of 2

20-Lead 4.4 mm TSSOP [G2X] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		5.90	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2088A

APPENDIX A: REVISION HISTORY

Revision A (January 2024)

- Converted Micrel data sheet for SY100EP14U to Microchip format as DS20006842A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Supply Voltage Range	Package	Temperature Range	Special Processing

Device:	SY100EP14:		2.5V/3.3V/5V 1:5 LVPECL/PECL/ ECL/HSTL 2 GHz Clock Driver with 2:1 Differential Input MUX
Voltage Option:	U	=	2.5/3.3/5V
Package:	K4	=	20-Lead TSSOP
Temperature Range:	G	=	–40°C to 85°C
Special Processing:	<blank>	=	74/Tube
	-TR	=	1,000/Reel

Examples:

a) **SY100EP14UK4G**

2.5/3.3/5V, 20-Lead TSSOP, –40°C to 85°C, 74/Tube

b) **SY100EP14UK4G-TR**

2.5/3.3/5V, 20-Lead TSSOP, –40°C to 85°C, 1,000/Reel

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