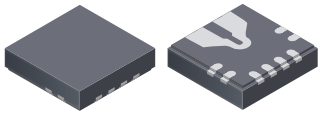
ACS71240

Automotive-Grade, Galvanically Isolated Current Sensor IC with Common-Mode Field Rejection and Overcurrent Detection in Small Footprint Low-Profile Packages

FEATURES AND BENEFITS

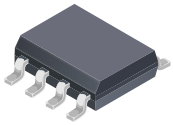
- AEC-Q100 automotive qualified
- Differential Hall sensing rejects common-mode fields
- Integrated shield virtually eliminates capacitive coupling from current conductor to die, greatly suppressing output noise due to high dv/dt transients
- Industry-leading noise performance with greatly improved bandwidth through proprietary amplifier and filter design techniques
- High bandwidth 120 kHz analog output for faster response times in control applications
- Patented integrated digital temperature compensation circuitry allows for near closed-loop accuracy over temperature in an open loop sensor
- Single supply operation with nonratiometric output at 3.3 and 5 V options
- Overcurrent $\overline{\text{FAULT}}$ available between 50% and 200% I_P with 1.5 µs (typ) response time
- Non-ratiometric output provides immunity to noisy supplies
- Small footprint QFN-12 with wettable flank and SOIC-8 suitable for space-constrained automotive applications
- 0.6 mΩ (QFN-12) or 1.2 mΩ (SOIC-8) primary conductor resistance for low power loss and high inrush current withstand capability
- UL certified package (SOIC-8 only) for voltage isolation

PACKAGES:



12-contact QFN with wettable flank
3 mm × 3 mm × 0.75 mm
(EXB package)

Not to scale



8-pin SOIC
with internally fused path
(LCB package)

DESCRIPTION

The Allegro™ ACS71240 current sensor IC is an economical and precise solution for AC or DC current sensing in industrial, automotive, commercial, and communications applications.

The device consists of a precise, low-offset linear Hall sensor circuit with a copper conduction path located near the surface of the die. Applied current flowing through this copper path generates a magnetic field which is sensed by the integrated Hall IC and converted into a proportional voltage. The resistance of the integrated conductor is far less than typical sense resistors, which reduces power loss and improves efficiency.

Rejection of external common-mode magnetic fields is achieved through differential sensing, enabling high accuracy in magnetically noisy environments. A precise voltage proportional to the measured current is generated by the low-offset, chopper-stabilized Hall front end.

Zero ampere output voltage and device sensitivity are programmed at the Allegro factory to provide a high accuracy solution across the full automotive temperature range.

The ACS71240 includes an integrated fault comparator for simplified overcurrent detection. The ultrafast response time provides the system with ample time to detect and protect against short-circuit events.

The ACS71240 is provided in small, low-profile surface-mount package options: QFN-12 with wettable flank and SOIC-8. The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free, except for flip-chip high-temperature Pb-based solder balls, currently exempt from RoHS. The device is fully calibrated prior to shipment from the factory.

SOIC-8 ONLY

TÜV America
Certificate Number:
U8V 14 11 54214 032
CB 14 11 54214 031

CB Certificate Number:
US-22334-A3-UL

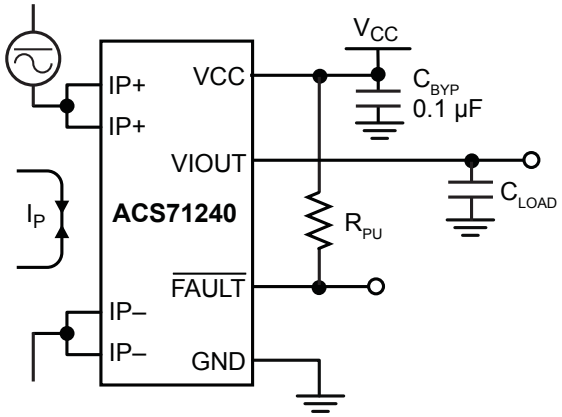


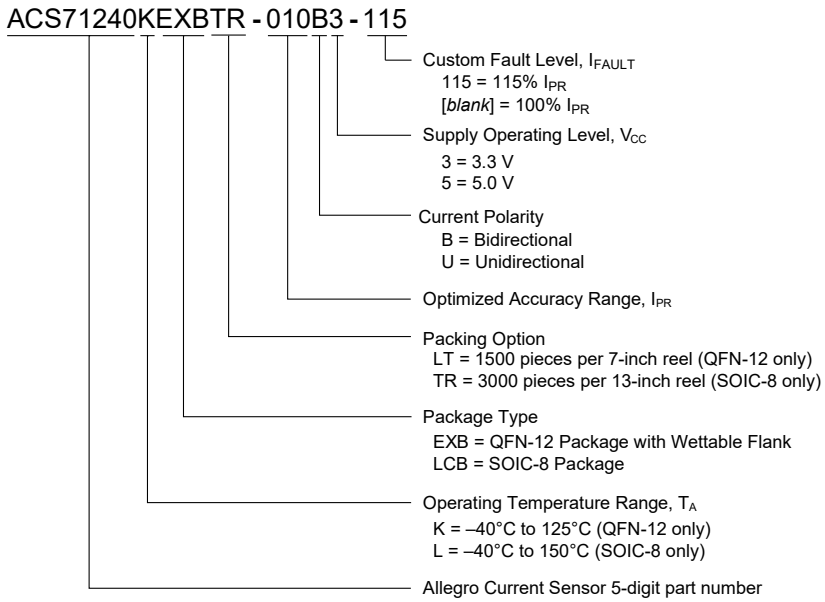
Figure 1: Typical Application

SELECTION GUIDE

Part Number	Supply Voltage, V_{CC} (V)	Optimized Accuracy Range, I_{PR} (A)	Sensitivity (Typ) (mV/A)	Fault Trip Level (A)	Operating Ambient Temperature Range, T_A (°C)	Package	Packing [1]
ACS71240KEXBLT-010B3	3.3	±10	132	±10	–40 to 125	12-contact QFN with wettable flank (EXB)	1500 pieces per 7-inch reel
ACS71240KEXBLT-030B3	3.3	±30	44	±30			
ACS71240KEXBLT-050U5	5.0	50	80	50			
ACS71240KEXBLT-010B3-115	3.3	±10	132	±11.5			
ACS71240LLCBTR-010B3	3.3	±10	132	±10	–40 to 150	8-pin SOIC with internally fused path (LCB)	3000 pieces per 13-inch reel
ACS71240LLCBTR-030B3	3.3	±30	44	±30			
ACS71240LLCBTR-045B5	5	±45	44.4	±45			
ACS71240LLCBTR-050U5	5	50	80	50			

[1] Contact Allegro for additional packing options.

Naming Specification



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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		6	V
Reverse Supply Voltage	$V_{CC(R)}$		–0.5	V
Output Voltage	V_{IOUT}		V_{CC} + 0.7	V
Reverse Output Voltage	$V_{IOUT(R)}$		–0.5	V
$\overline{\text{FAULT}}$ Voltage	$V_{\overline{FAULT}}$		25	V
Reverse $\overline{\text{FAULT}}$ Voltage	$V_{\overline{FAULT}(R)}$		–0.5	V
Operating Ambient Temperature Range	T_A	Range K (QFN-12 package)	–40 to 125	°C
		Range L (SOIC-8 package)	–40 to 150	°C
Junction Temperature	$T_{J(MAX)}$		165	°C
Storage Temperature Range	T_{stg}		–65 to 170	°C

ISOLATION CHARACTERISTICS (for SOIC-8 package only)

Characteristic	Symbol	Notes	Value	Units
Dielectric Surge Strength Test Voltage	V_{SURGE}	Tested ±5 pulses at 2/minute in compliance to IEC 61000-4-5 1.2 µs (rise) / 50 µs (width).	6000	V
Dielectric Strength Test Voltage	V_{ISO}	Agency type-tested for 60 seconds per UL 60950-1 (edition 2); production-tested at V_{ISO} for 1 second, in accordance with UL 60950-1 (edition 2)	2400	V_{RMS}
Working Voltage for Basic Isolation	V_{WVBI}	Maximum approved working voltage for basic (single) isolation according to UL 60950-1 (edition 2)	420	V_{PK} or V_{DC}
			297	V_{RMS}
Clearance	D_{cl}	Minimum distance through air from IP leads to signal leads	4.2	mm
Creepage	D_{cr}	Minimum distance along package body from IP leads to signal leads	4.2	mm

ISOLATION CHARACTERISTICS (for QFN-12 package only)

Characteristic	Symbol	Notes	Value	Units
Working Voltage for Basic Isolation [1]	V_{WVBI}	Voltage applied between pins 1-4 and 5-12	100	V_{PK} or V_{DC}

[1] Based on characterization. No agency testing was conducted.

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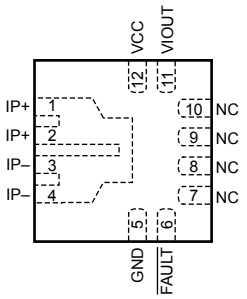
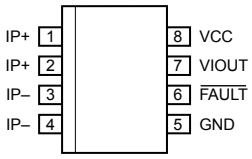
PINOUT DIAGRAMS AND TERMINAL LIST TABLES



Package EX, 12-Pin QFN Pinout Diagram

Terminal List Table (QFN-12)

Number	Name	Description
1, 2	IP+	Positive terminals for current being sensed; fused internally
3, 4	IP–	Negative terminals for current being sensed; fused internally
5	GND	Signal ground terminal
6	$\overline{\text{FAULT}}$	Overcurrent fault; active low
7, 8, 9, 10	NC	No connection; connect to ground for optimal ESD performance
11	VIOUT	Analog output signal
12	VCC	Device power supply terminal



Package LC, 8-Pin SOIC Pinout Diagram

Terminal List Table (SOIC-8)

Number	Name	Description
1, 2	IP+	Positive terminals for current being sensed; fused internally
3, 4	IP–	Negative terminals for current being sensed; fused internally
5	GND	Signal ground terminal
6	$\overline{\text{FAULT}}$	Overcurrent fault; active low
7	VIOUT	Analog output signal
8	VCC	Device power supply terminal

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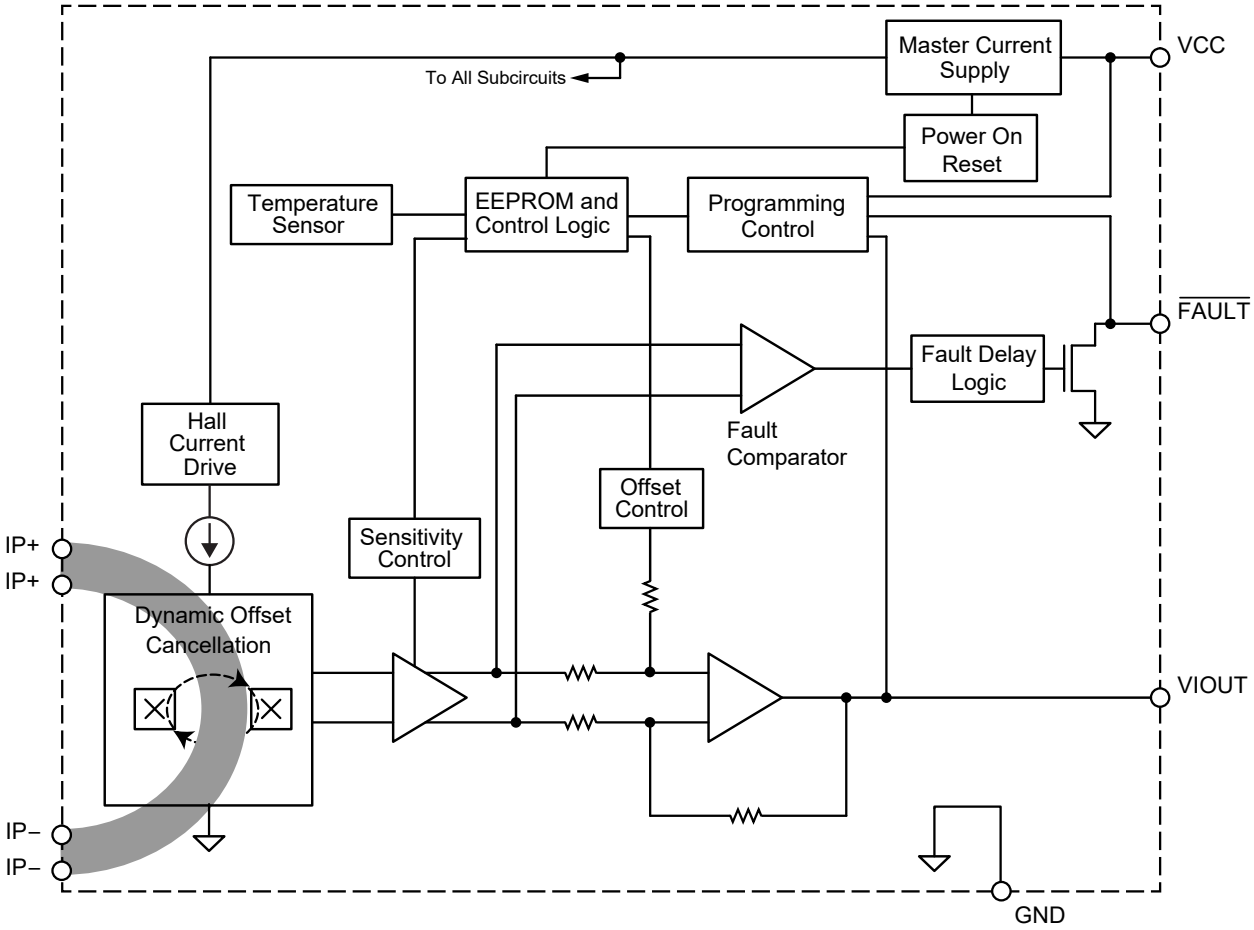

Functional Block Diagram

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COMMON ELECTRICAL CHARACTERISTICS: Valid through the full range of T_A and V_{CC}, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ. [1]	Max.	Unit
ELECTRICAL CHARACTERISTICS							
Supply Voltage	V_{CC}	5 V variant		4.5	5.0	5.5	V
		3.3 V variant		3.0	3.3	3.6	V
Supply Current	I_{CC}	5 V variant, no load on V_{IOUT}		–	10	12	mA
		3.3 V variant, no load on V_{IOUT}		–	7.5	12	mA
Output Capacitance Load	C_L	VIOUT to GND		–	–	4.7	nF
Output Resistive Load	R_L	VIOUT to GND		10	–	–	kΩ
Primary Conductor Resistance	R_{IP}	T_A = 25°C	QFN-12 package	–	0.6	–	mΩ
			SOIC-8 package	–	1.2	–	mΩ
Primary Hall Coupling Factor	G_1	T_A = 25°C	QFN-12 package	–	10	–	G/A
			SOIC-8 package	–	11	–	G/A
Secondary Hall Coupling Factor	G_2	T_A = 25°C	QFN-12 package	–	–2	–	G/A
			SOIC-8 package	–	–2.8	–	G/A
Hall Plate Sensitivity Matching	$Sens_{match}$	T_A = 25°C		–	±1	–	%
Common Mode Field Rejection	CMFR	Offset due to DC common field	QFN-12 package	–	1.2	–	mA/G
			SOIC-8 package	–	0.6	–	mA/G
Rise Time	t_r	T_A = 25°C, C_L = 1 nF; input current step causing 1 V output swing		–	3	4 [2]	µs
Propagation Delay	t_{pd}	T_A = 25°C, C_L = 1 nF; input current step causing 1 V output swing		–	1.6	2.2 [2]	µs
Response Time	$t_{RESPONSE}$	T_A = 25°C, C_L = 1 nF; input current step causing 1 V output swing		–	4	4.9 [2]	µs
Bandwidth	BW	Small signal –3 dB; C_L = 1 nF		–	120	–	kHz
Noise Density	I_{ND}	V_{CC} = 5.0 V, input referred, T_A = 25°C, C_L = 1 nF		–	100	–	$\mu A_{RMS}/\sqrt{Hz}$
		V_{CC} = 3.3 V, input referred, T_A = 25°C, C_L = 1 nF			150		$\mu A_{RMS}/\sqrt{Hz}$
Noise	I_N	V_{CC} = 5.0 V, input referred, T_A = 25°C, C_L = 1 nF		–	52	–	mA_{RMS}
		V_{CC} = 3.3 V, input referred, T_A = 25°C, C_L = 1 nF		–	78	–	mA_{RMS}
Nonlinearity	E_{LIN}	Up to I_P = 10 A	QFN-12 package	–1	–	1	%
		Through full range of I_P	SOIC-8 package	–1	–	1	%
Power Supply Rejection Ratio	PSRR	V_{CC} = V_{CC} ±10%, T_A = 25°C, DC to 1 kHz		–	40	–	dB
		V_{CC} = V_{CC} ±10%, T_A = 25°C, 1 kHz to 20 kHz		–	30	–	dB
		V_{CC} = V_{CC} ±10%, T_A = 25°C, 20 kHz to 60 kHz		–	20	–	dB
Output Saturation Voltage [3]	V_{SAT_H}	R_L = 10 kΩ		V_{CC} – 0.3	–	–	V
	V_{SAT_L}	R_L = 10 kΩ		–	–	0.3	V
Power-On Time	t_{PO}	Output reaches 90% of steady-state level, T_A = 25°C, I_P = I_{PR}(max) applied		–	80	–	µs
Shorted Output-to-Ground Current	$I_{SC(GND)}$	T_A = 25°C		–	30	–	mA
Shorted Output-to-V_{CC} Current	$I_{SC(VCC)}$	T_A = 25°C		–	1.8	–	mA

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COMMON ELECTRICAL CHARACTERISTICS (continued): Valid through the full range of T_A and V_{CC}, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
$\overline{\text{FAULT}}$ CHARACTERISTICS						
$\overline{\text{FAULT}}$ Operating Point	$I_{\overline{\text{FAULT}}}$		–	±1 × I_{PR} [4]	–	A
$\overline{\text{FAULT}}$ Current Hysteresis	$I_{F(HYS)}$	Percent of $I_{PR(MAX)}$	3	5	–	%
$\overline{\text{FAULT}}$ Output Pullup Resistor	R_{PU}		10	–	500	kΩ
$\overline{\text{FAULT}}$ Output Voltage	V_{OL}	R_{PU} = 10 kΩ, during fault condition	–	–	0.3	V
$\overline{\text{FAULT}}$ Response Time	$t_{\overline{\text{FAULT}}}$	Time from $\lvert I_P \rvert$ rising above $\lvert I_{\overline{\text{FAULT}}} \rvert$ until $V_{\overline{\text{FAULT}}} < V_{OL(MAX)}$. 100 pF from $\overline{\text{FAULT}}$ to GND. Input current step 20% above $I_{\overline{\text{FAULT}}}$ with rise time ≤ 1 µs.	–	1.5	2.5 [5]	µs
$\overline{\text{FAULT}}$ Error	E_F	$I_{\overline{\text{FAULT}}}$, T_A = 25°C	–10	±3.5	10	%
		T_A = –40°C or $T_{A(MAX)}$	–10	±5	10	%

[1] Typical values with ± are 3 sigma values.
[2] Guaranteed by design. Limit calculated using 6 sigma. Not tested in production.
[3] The sensor IC will continue to respond to current beyond the range of I_P until the high or low saturation voltage; however, the nonlinearity in this region will be worse than through the rest of the measurement range.
[4] Unless otherwise specified, contact Allegro for alternative fault levels. Available from ±0.5 to 2 × I_{PR}.
[5] Not tested in production.

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ACS71240KEXBLT-010B3 PERFORMANCE CHARACTERISTICS: Over full range of T_A, V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
NOMINAL PERFORMANCE						
Optimized Sensing Range	I_{PR}		–10	–	10	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	132	–	mV/A
Zero-Current Output Voltage	$V_{IOUT(Q)}$	Bidirectional, I_P = 0 A	–	1.65	–	V
ACCURACY PERFORMANCE						
Total Output Error [2]	E_{TOT}	I_P = 10 A, T_A = 25°C to 125°C	–2.5	±1.4	2.5	%
		I_P = 10 A, T_A = –40°C to 25°C	–6	±1.8	6	%
TOTAL OUTPUT ERROR COMPONENTS [3] $E_{TOT} = E_{SENS} + 100 \times V_{OE} / (Sens \times I_P)$						
Sensitivity Error	E_{SENS}	I_P = 10 A, T_A = 25°C to 125°C	–2	±1.1	2	%
		I_P = 10 A, T_A = –40°C to 25°C	–5.5	±1.7	5.5	%
Offset Voltage Error	V_{OE}	I_P = 0 A, T_A = 25°C to 125°C	–15	±9.7	15	mV
		I_P = 0 A, T_A = –40°C to 25°C	–30	±8.5	30	mV
ACCURACY PERFORMANCE INCLUDING LIFETIME DRIFT [4]						
Total Output Error Including Lifetime Drift [5]	E_{TOT_drift}	I_P = 10 A, T_A = 25°C to 125°C	–5.7	±1.8	5.7	%
		I_P = 10 A, T_A = –40°C to 25°C	–6	±1.5	6	%
Sensitivity Error Including Lifetime Drift [6]	E_{SENS_drift}	I_P = 10 A, T_A = 25°C to 125°C	–5.1	±1.2	5.1	%
		I_P = 10 A, T_A = –40°C to 25°C	–5.6	±1.2	5.6	%
Offset Voltage Error Including Lifetime Drift [7]	V_{OE_drift}	I_P = 0 A, T_A = 25°C to 125°C	–28	±4.5	28	mV
		I_P = 0 A, T_A = –40°C to 25°C	–30	±4.3	30	mV

[1] Typical values with ± are 3 sigma values, except for lifetime drift, which are the average value including drift (from the worst case stress) after AEC-Q100 qualification.
[2] Percentage of I_P.
[3] A single device will not have both the maximum/minimum sensitivity error and maximum/minimum offset voltage, as that would violate the maximum/minimum total output error specification.
[4] Lifetime drift characteristics are based on AEC-Q100 qualification results.
[5] All devices stayed within min/max limits throughout AEC-Q100 qualification. The worst drift observed was 6.1%.
[6] All devices stayed within min/max limits throughout AEC-Q100 qualification. The worst drift observed was 4%.
[7] All devices stayed within min/max limits throughout AEC-Q100 qualification. The worst drift observed was 22 mV.

ACS71240KEXBLT-010B3-115 Variant

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
NON-STANDARD FAULT CHARACTERISTICS						
FAULT Operating Point	I_{FAULT}		–	±1.15 × I_{PR}	–	A

[1] Typical values with ± are 3 sigma values

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ACS71240KEXBLT-030B3 PERFORMANCE CHARACTERISTICS: Over full range of T_A, V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
NOMINAL PERFORMANCE						
Optimized Sensing Range	I_{PR}		–30	–	30	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	44	–	mV/A
Zero-Current Output Voltage	$V_{IOUT(Q)}$	Bidirectional, I_P = 0 A	–	1.65	–	V
ACCURACY PERFORMANCE						
Total Output Error [2]	E_{TOT}	I_P = 10 A, T_A = 25°C to 125°C	–2.5	±0.8	2.5	%
		I_P = 10 A, T_A = –40°C to 25°C	–6	±1.9	6	%
TOTAL OUTPUT ERROR COMPONENTS [3] $E_{TOT} = E_{SENS} + 100 \times V_{OE} / (Sens \times I_P)$						
Sensitivity Error	E_{SENS}	I_P = 10 A, T_A = 25°C to 125°C	–2	±0.9	2	%
		I_P = 10 A, T_A = –40°C to 25°C	–5.5	±1.5	5.5	%
Offset Voltage Error	V_{OE}	I_P = 0 A, T_A = 25°C to 125°C	–15	±3.71	15	mV
		I_P = 0 A, T_A = –40°C to 25°C	–30	±7.1	30	mV
ACCURACY PERFORMANCE INCLUDING LIFETIME DRIFT [4]						
Total Output Error Including Lifetime Drift [5]	E_{TOT_drift}	I_P = 10 A, T_A = 25°C to 125°C	–5.7	±1.8	5.7	%
		I_P = 10 A, T_A = –40°C to 25°C	–6	±1.5	6	%
Sensitivity Error Including Lifetime Drift [6]	E_{SENS_drift}	I_P = 10 A, T_A = 25°C to 125°C	–5.1	±1.2	5.1	%
		I_P = 10 A, T_A = –40°C to 25°C	–5.6	±1.2	5.6	%
Offset Voltage Error Including Lifetime Drift [7]	V_{OE_drift}	I_P = 0 A, T_A = 25°C to 125°C	–28	±4.5	28	mV
		I_P = 0 A, T_A = –40°C to 25°C	–30	±4.3	30	mV

[1] Typical values with ± are 3 sigma values, except for lifetime drift, which are the average value including drift (from the worst case stress) after AEC-Q100 qualification.
[2] Percentage of I_P.
[3] A single device will not have both the maximum/minimum sensitivity error and maximum/minimum offset voltage, as that would violate the maximum/minimum total output error specification.
[4] Lifetime drift characteristics are based on AEC-Q100 qualification results.
[5] All devices stayed within min/max limits throughout AEC-Q100 qualification. The worst drift observed was 6.1%.
[6] All devices stayed within min/max limits throughout AEC-Q100 qualification. The worst drift observed was 4%.
[7] All devices stayed within min/max limits throughout AEC-Q100 qualification. The worst drift observed was 22 mV.

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ACS71240KEXBLT-050U5 PERFORMANCE CHARACTERISTICS: Over full range of T_A, V_{CC} = 5.0 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
NOMINAL PERFORMANCE						
Optimized Sensing Range	I_{PR}		0	–	50	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	80	–	mV/A
Zero-Current Output Voltage	$V_{IOUT(Q)}$	Unidirectional, I_P = 0 A	–	0.5	–	V
ACCURACY PERFORMANCE						
Total Output Error [2]	E_{TOT}	I_P = 10 A, T_A = 25°C to 125°C	–2.5	±1.2	2.5	%
		I_P = 10 A, T_A = –40°C to 25°C	–6	±3.6	6	%
TOTAL OUTPUT ERROR COMPONENTS [3] $E_{TOT} = E_{SENS} + 100 \times V_{OE} / (Sens \times I_P)$						
Sensitivity Error	E_{SENS}	I_P = 10 A, T_A = 25°C to 125°C	–2	±0.9	2	%
		I_P = 10 A, T_A = –40°C to 25°C	–5.5	±3.3	5.5	%
Offset Voltage Error	V_{OE}	I_P = 0 A, T_A = 25°C to 125°C	–10	±4.6	10	mV
		I_P = 0 A, T_A = –40°C to 25°C	–30	±6.3	30	mV
ACCURACY PERFORMANCE INCLUDING LIFETIME DRIFT [4]						
Total Output Error Including Lifetime Drift [5]	E_{TOT_drift}	I_P = 10 A, T_A = 25°C to 125°C	–5.7	±1.8	5.7	%
		I_P = 10 A, T_A = –40°C to 25°C	–6	±1.5	6	%
Sensitivity Error Including Lifetime Drift [6]	E_{SENS_drift}	I_P = 10 A, T_A = 25°C to 125°C	–5.1	±1.2	5.1	%
		I_P = 10 A, T_A = –40°C to 25°C	–5.6	±1.2	5.6	%
Offset Voltage Error Including Lifetime Drift [7]	V_{OE_drift}	I_P = 0 A, T_A = 25°C to 125°C	–28	±4.5	28	mV
		I_P = 0 A, T_A = –40°C to 25°C	–30	±4.3	30	mV

[1] Typical values with ± are 3 sigma values, except for lifetime drift, which are the average value including drift (from the worst case stress) after AEC-Q100 qualification.
[2] Percentage of I_P.
[3] A single device will not have both the maximum/minimum sensitivity error and maximum/minimum offset voltage, as that would violate the maximum/minimum total output error specification.
[4] Lifetime drift characteristics are based on AEC-Q100 qualification results.
[5] All devices stayed within min/max limits throughout AEC-Q100 qualification. The worst drift observed was 6.1%.
[6] All devices stayed within min/max limits throughout AEC-Q100 qualification. The worst drift observed was 4%.
[7] All devices stayed within min/max limits throughout AEC-Q100 qualification. The worst drift observed was 22 mV.

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ACS71240LLCBTR-010B3 PERFORMANCE CHARACTERISTICS: Over full range of T_A, V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
NOMINAL PERFORMANCE						
Optimized Sensing Range	I_{PR}		–10	–	10	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	132	–	mV/A
Zero-Current Output Voltage	$V_{IOUT(Q)}$	Bidirectional, I_P = 0 A	–	1.65	–	V
ACCURACY PERFORMANCE						
Total Output Error [2]	E_{TOT}	$I_P = I_{PR(max)}$, T_A = 25°C to 150°C	–2	±1	2	%
		$I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–6	±2.4	6	%
TOTAL OUTPUT ERROR COMPONENTS [3] $E_{TOT} = E_{SENS} + 100 \times V_{OE} / (Sens \times I_P)$						
Sensitivity Error	E_{SENS}	$I_P = I_{PR(max)}$, T_A = 25°C to 150°C	–1.5	±0.84	1.5	%
		$I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–5.5	±2.3	5.5	%
Offset Voltage Error	V_{OE}	I_P = 0 A, T_A = 25°C to 150°C	–10	±6.7	10	mV
		I_P = 0 A, T_A = –40°C to 25°C	–30	±10	30	mV

[1] Typical values with ± are 3 sigma values. All devices stayed within limits during AEC-Q100 qualification.
[2] Percentage of I_P, with $I_P = I_{PR(max)}$.
[3] A single device will not have both the maximum/minimum sensitivity error and maximum/minimum offset voltage, as that would violate the maximum/minimum total output error specification.

ACS71240LLCBTR-030B3 PERFORMANCE CHARACTERISTICS: Over full range of T_A, V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
NOMINAL PERFORMANCE						
Optimized Sensing Range	I_{PR}		–30	–	30	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	44	–	mV/A
Zero-Current Output Voltage	$V_{IOUT(Q)}$	Bidirectional, I_P = 0 A	–	1.65	–	V
ACCURACY PERFORMANCE						
Total Output Error [2]	E_{TOT}	$I_P = I_{PR(max)}$, T_A = 25°C to 150°C	–2	±0.6	2	%
		$I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–6	±1.4	6	%
TOTAL OUTPUT ERROR COMPONENTS [3] $E_{TOT} = E_{SENS} + 100 \times V_{OE} / (Sens \times I_P)$						
Sensitivity Error	E_{SENS}	$I_P = I_{PR(max)}$, T_A = 25°C to 150°C	–1.9	±0.53	1.9	%
		$I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–5.5	±1.1	5.5	%
Offset Voltage Error	V_{OE}	I_P = 0 A, T_A = 25°C to 150°C	–10	±7.2	10	mV
		I_P = 0 A, T_A = –40°C to 25°C	–30	±9.5	30	mV

[1] Typical values with ± are 3 sigma values. All devices stayed within limits during AEC-Q100 qualification.
[2] Percentage of I_P, with $I_P = I_{PR(max)}$.
[3] A single device will not have both the maximum/minimum sensitivity error and maximum/minimum offset voltage, as that would violate the maximum/minimum total output error specification.

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ACS71240LLCBTR-045B5 PERFORMANCE CHARACTERISTICS: Over full range of T_A, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
NOMINAL PERFORMANCE						
Optimized Sensing Range	I_{PR}		–45	–	45	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	44.4	–	mV/A
Zero-Current Output Voltage	$V_{IOUT(Q)}$	Bidirectional, I_P = 0 A	–	2.5	–	V
ACCURACY PERFORMANCE						
Total Output Error [2]	E_{TOT}	$I_P = I_{PR(max)}$, T_A = 25°C to 150°C	–2	±0.73	2	%
		$I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–6	±1.4	6	%
TOTAL OUTPUT ERROR COMPONENTS [3] $E_{TOT} = E_{SENS} + 100 \times V_{OE} / (Sens \times I_P)$						
Sensitivity Error	E_{SENS}	$I_P = I_{PR(max)}$, T_A = 25°C to 150°C	–1.9	±0.63	1.9	%
		$I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–5.5	±1.4	5.5	%
Offset Voltage Error	V_{OE}	I_P = 0 A, T_A = 25°C to 150°C	–10	±6.9	10	mV
		I_P = 0 A, T_A = –40°C to 25°C	–30	±7.2	30	mV

[1] Typical values with ± are 3 sigma values. All devices stayed within limits during AEC-Q100 qualification.
[2] Percentage of I_P, with $I_P = I_{PR(max)}$.
[3] A single device will not have both the maximum/minimum sensitivity error and maximum/minimum offset voltage, as that would violate the maximum/minimum total output error specification.

ACS71240LLCBTR-050U5 PERFORMANCE CHARACTERISTICS: Over full range of T_A, V_{CC} = 5.0 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
NOMINAL PERFORMANCE						
Optimized Sensing Range	I_{PR}		0	–	50	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	80	–	mV/A
Zero-Current Output Voltage	$V_{IOUT(Q)}$	Unidirectional, I_P = 0 A	–	0.5	–	V
ACCURACY PERFORMANCE						
Total Output Error [2]	E_{TOT}	$I_P = I_{PR(max)}$, T_A = 25°C to 150°C	–2	±1.1	2	%
		$I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–6	±3.75	6	%
TOTAL OUTPUT ERROR COMPONENTS [3] $E_{TOT} = E_{SENS} + 100 \times V_{OE} / (Sens \times I_P)$						
Sensitivity Error	E_{SENS}	$I_P = I_{PR(max)}$, T_A = 25°C to 150°C	–1.9	±1.1	1.9	%
		$I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–5.5	±3.8	5.5	%
Offset Voltage Error	V_{OE}	I_P = 0 A, T_A = 25°C to 150°C	–10	±4	10	mV
		I_P = 0 A, T_A = –40°C to 25°C	–30	±5.5	30	mV

[1] Typical values with ± are 3 sigma values. All devices stayed within limits during AEC-Q100 qualification.
[2] Percentage of I_P, with $I_P = I_{PR(max)}$.
[3] A single device will not have both the maximum/minimum sensitivity error and maximum/minimum offset voltage, as that would violate the maximum/minimum total output error specification.

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FUNCTIONAL DESCRIPTION

Power-On Reset Operation

Power-On Reset (POR) refers to the voltage at which the device effectively turns on. In order to ensure accuracy of readings, the part remains off or "in POR" until the voltage reaches a point at which the device can be trusted. At this point the output leaves high Z and begins reporting the current.

The descriptions in this section assume: T_A = 25°C, no output load (R_L, C_L), and no significant magnetic field is present. Refer to the scope plot in Figure 2 for the intended power on/off profile of the ACS71240. The device tested below contains a pull-down on V_{IOUT}, forcing the output voltage to 0 V during the high Z portion.

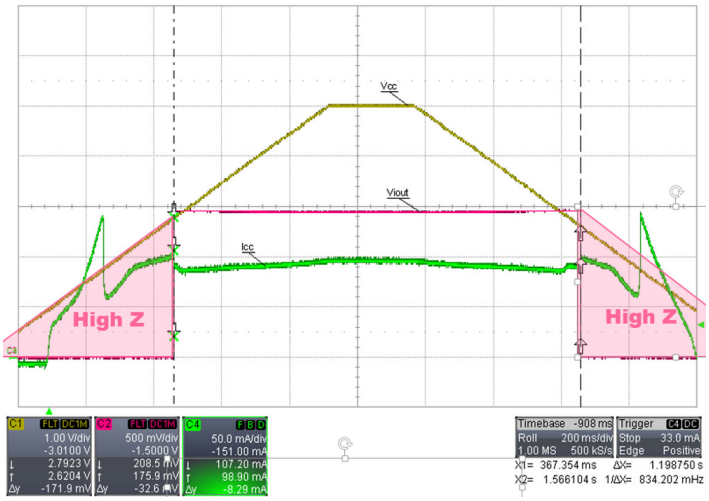

Figure 2: Power On/Off Profile of ACS71240
I_{CC} = Green, V_{IOUT} = Red, V_{CC} = Yellow

Power-On

As V_{CC} ramps up, the device output is high impedance (pink section) until V_{CC} reaches POR.

Power-Off

As V_{CC} drops below POR the device output will enter a high impedance state.

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DEFINITIONS OF ACCURACY CHARACTERISTICS

Sensitivity (Sens). The change in sensor IC output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) (1 G = 0.1 mT) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

Nonlinearity (E_{LIN}). The nonlinearity is a measure of how linear the output of the sensor IC is over the full current measurement range. The nonlinearity is calculated as:

$$E_{LIN} = \left\{1 - \left[\frac{V_{IOUT}(I_{PR(max)}) - V_{IOUT(Q)}}{2 \cdot V_{IOUT}(I_{PR(max)}/2) - V_{IOUT(Q)}}\right]\right\} \cdot 100(\%)$$

Zero-Current Output Voltage ($V_{IOUT(Q)}$). The output of the sensor when the primary current is zero. For unipolar devices this value will be 10% of operating voltage, 0.5 V and 0.33 V for 5 V and 3.3 V respectively. For bidirectional devices, the output will be 50% of the operating voltage, 2.5 V and 1.65 V for 5 V and 3.3 V devices respectively. Since the ACS71240 is a non-ratiometric part, these values will be stable over V_{CC} variations. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

Offset Voltage (V_{OE}). The deviation of the device output from its ideal quiescent value due to nonmagnetic causes. To convert this voltage to amperes, divide by the device sensitivity, Sens.

Total Output Error (E_{TOT}). The difference between the current measurement from the sensor IC and the actual current (I_P), relative to the actual current. This is equivalent to the difference between the ideal output voltage and the actual output voltage, divided by the ideal sensitivity, relative to the current flowing through the primary conduction path:

$$E_{TOT}(I_P) = \frac{V_{IOUT\_ideal}(I_P) - V_{IOUT}(I_P)}{Sens_{ideal}(I_P) \cdot I_P} \cdot 100\ (\%)$$

The Total Output Error incorporates all sources of error and is a function of I_P. At relatively high currents, E_{TOT} will be mostly due to sensitivity error, and at relatively low currents, E_{TOT} will be mostly due to Offset Voltage (V_{OE}). In fact, at $I_P = 0$, E_{TOT} approaches infinity due to the offset. This is illustrated in Figure 3 and Figure 4. Figure 3 shows a distribution of output voltages versus I_P at 25°C and across temperature. Figure 4 shows the corresponding E_{TOT} versus I_P.

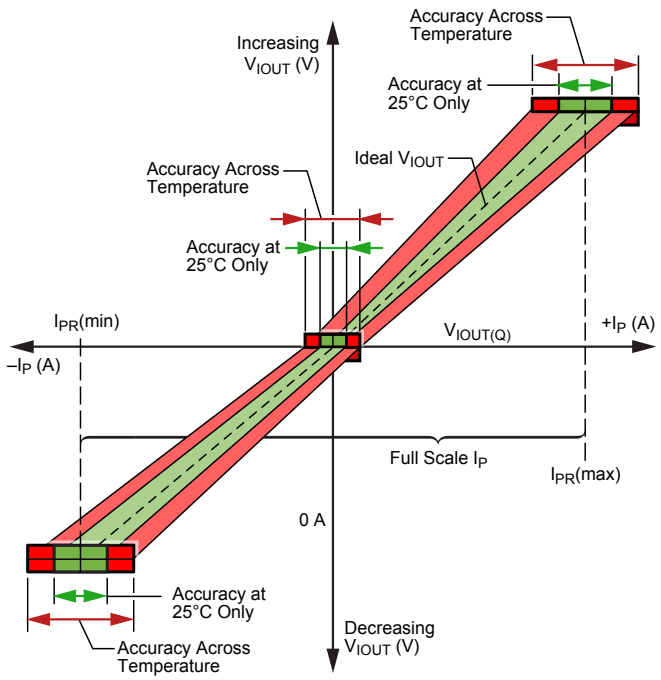

Figure 3: Output Voltage versus Sensed Current

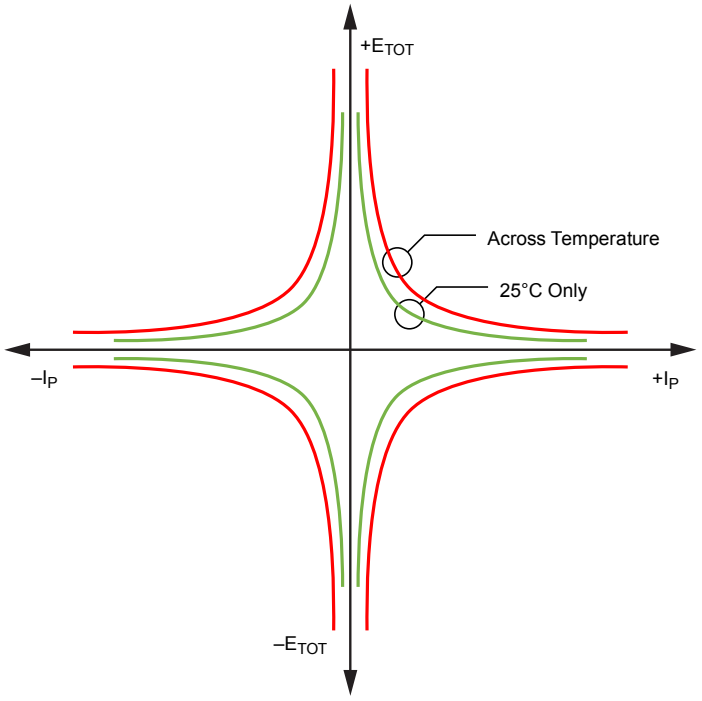

Figure 4: Total Output Error versus Sensed Current

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Power Supply Rejection Ratio (PSRR). The ratio of the change on V_{IOUT} to a change in V_{CC} in dB.

$$PSRR = 20 \log_{10} \left(\left| \frac{\Delta V_{CC}}{\Delta V_{IOUT}} \right| \right)$$

$\overline{\text{FAULT}}$ Error (E_F). The difference between the current at which the $\overline{\text{FAULT}}$ pin trips ($I_{\overline{\text{FAULT}}}$), relative to the ideal fault current ($I_{\overline{\text{FAULT}}\_ideal}$). This is equivalent to the difference between the ideal fault current and the actual fault current divided by the ideal current, and is defined as:

$$E_F = \frac{I_{\overline{FAULT}} - I_{\overline{FAULT}\_ideal}}{I_{\overline{FAULT}\_ideal}} \times 100\,(\%)$$

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Fault Behavior

The ACS71240 is available with both a latched and unlatched $\overline{\text{FAULT}}$ pin output. Unless otherwise stated, the default operation is unlatched. Contact Allegro for more details.

Unlatched Fault Behavior

In the event that the $\overline{\text{FAULT}}$ pin is unlatched, the $\overline{\text{FAULT}}$ output will only assert while an overcurrent condition is present. When an overcurrent condition occurs, the $\overline{\text{FAULT}}$ pin will be pulled low within $\overline{\text{FAULT}}$ response time, $t_{\overline{\text{FAULT}}}$. When the overcurrent condition is removed, another $t_{\overline{\text{FAULT}}}$ will delay the release of the line, after which the $\overline{\text{FAULT}}$ line will return to V_{CC} with a time constant based on the pull-up resistor and line capacitance.

Latched Fault Behavior

In the event that the fault pin is latched, the $\overline{\text{FAULT}}$ output will assert when an overcurrent condition is present. The $\overline{\text{FAULT}}$ pin will remain latched even after the overcurrent condition has subsided. The $\overline{\text{FAULT}}$ pin will remain asserted until the device is power-cycled.

Fault Filtering

To prevent nuisance tripping while in latched mode, the ACS71240 is available with a variety of minimum fault times, which are the minimum period a fault event must be present before the $\overline{\text{FAULT}}$ pin will latch. This minimum period, $t_{PW(MIN)}$, may be 0 µs, 0.5 µs, or 1 µs, and is available upon request. Contact Allegro for more details.

In latched mode, there is an additional delay of 1 clock cycle (t_{CLK} < 150 ns) after the overcurrent event occurs. The fault behavior for latched and unlatched modes are shown in Figure 6 and Figure 7.

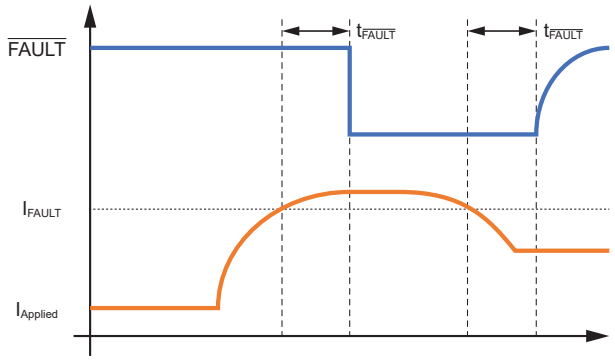

Figure 5: Fault trip with response time

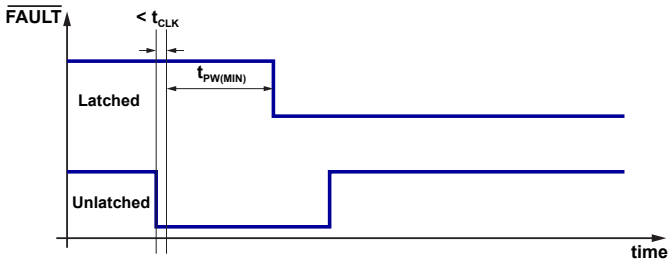

Figure 6: Fault event longer than $t_{PW(MIN)}$

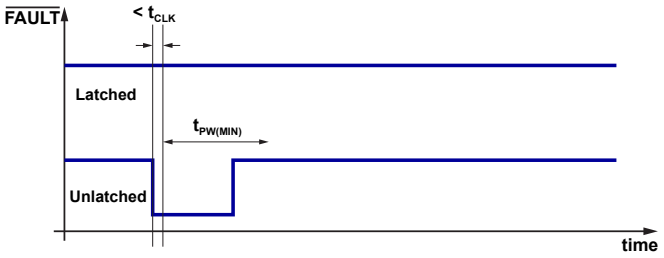

Figure 7: Fault event shorter than $t_{PW(MIN)}$

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DEFINITIONS OF DYNAMIC RESPONSE CHARACTERISTICS

Power-On Time (t_{PO}). When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Time, t_{PO} , is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in the chart at right.

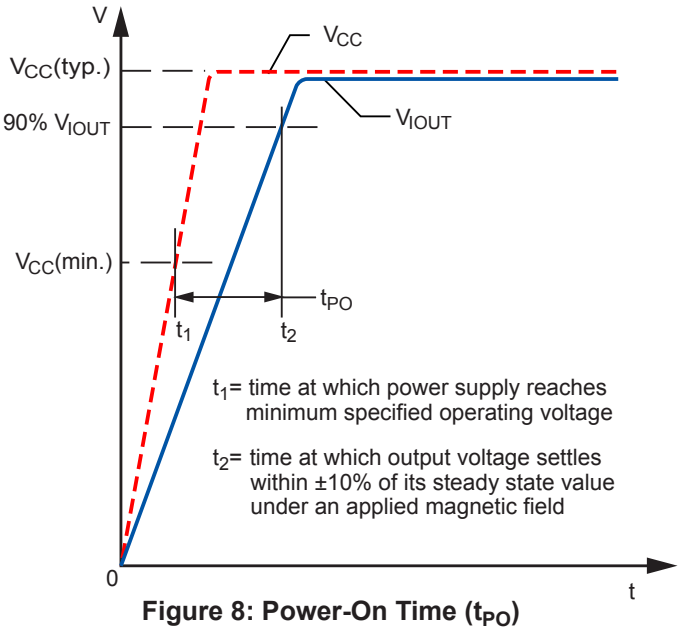

Figure 8: Power-On Time (t_{PO})

Rise Time (t_r). The time interval between a) when the sensor reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value.

Propagation Delay (t_{pd}). The time interval between a) when the sensed input current reaches 20% of its full-scale value, and b) when the sensor output reaches 20% of its full-scale value.

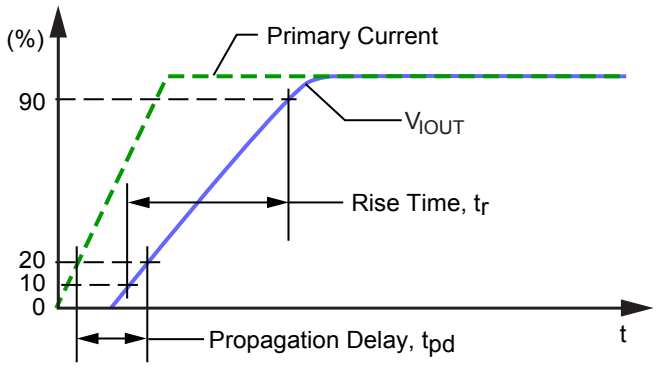

Figure 9: Rise Time (t_r) and Propagation Delay (t_{pd})

Response Time ($t_{RESPONSE}$). The time interval between a) when the sensed input current reaches 90% of its final value, and b) when the sensor output reaches 90% of its full-scale value.

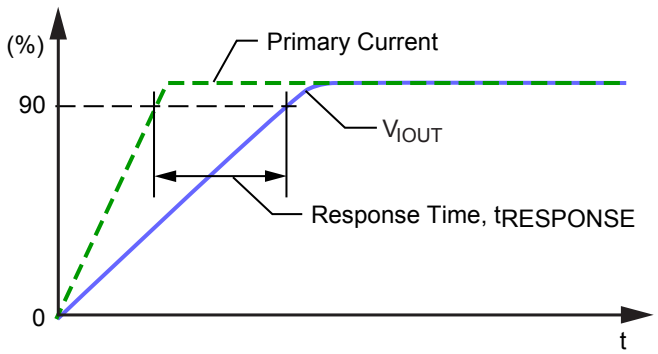

Figure 10: Response Time ($t_{RESPONSE}$)

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Common-Mode Field Rejection

The ACS71240 features two Hall-effect sensors used differentially in order to eliminate stray field. The two sensors are placed on opposite sides of the current loop. This allows the common magnetic field to be determined and removed before the signal is sent to the end user. Despite this common field rejection, it is always best practice to reduce the amount of stray fields around the current sensor as much as possible. See the Allegro Applications note on reducing common mode field for more details.

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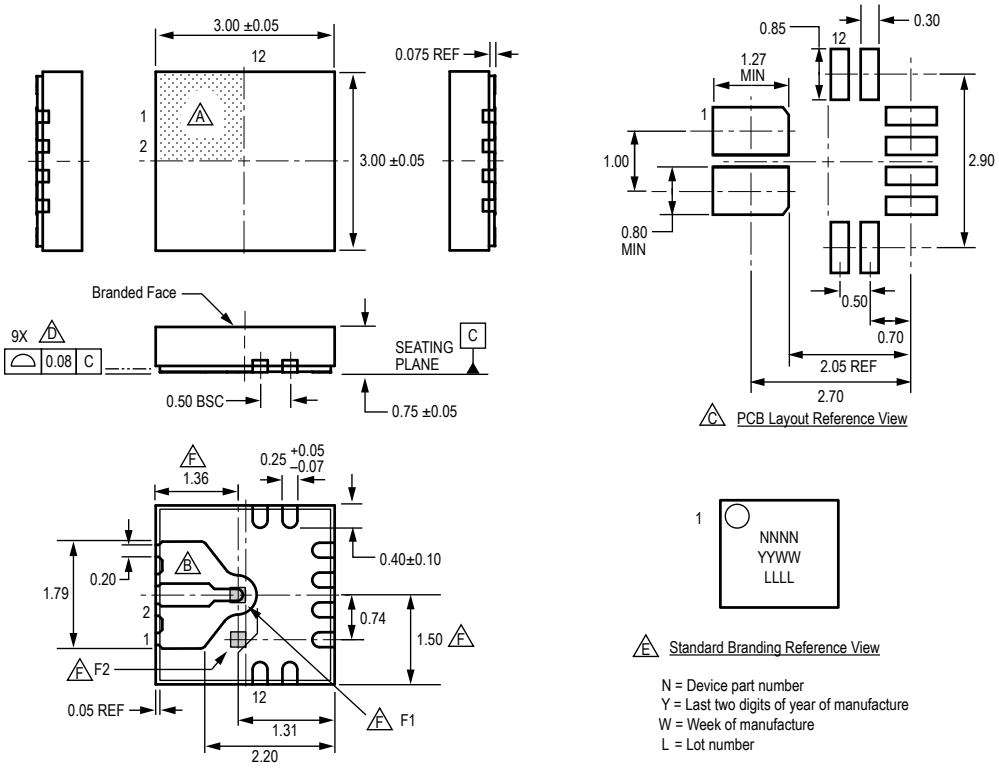
PACKAGE OUTLINE DRAWINGS



For reference only, not for tooling use (reference JEDEC MO-220WEED except for fused current path and wettable flank)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Fused sensed current path

C Reference land pattern layout (reference IPC7351 QFN50P300X300X80-17W4M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed current path and terminals

E Branding scale and appearance at supplier discretion

F Hall elements (F1 and F2); not to scale

Figure 11: Package EXB, 12-Contact QFN with Fused Sensed Current Loop and Wettable Flank

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(Reference MS-012AA)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

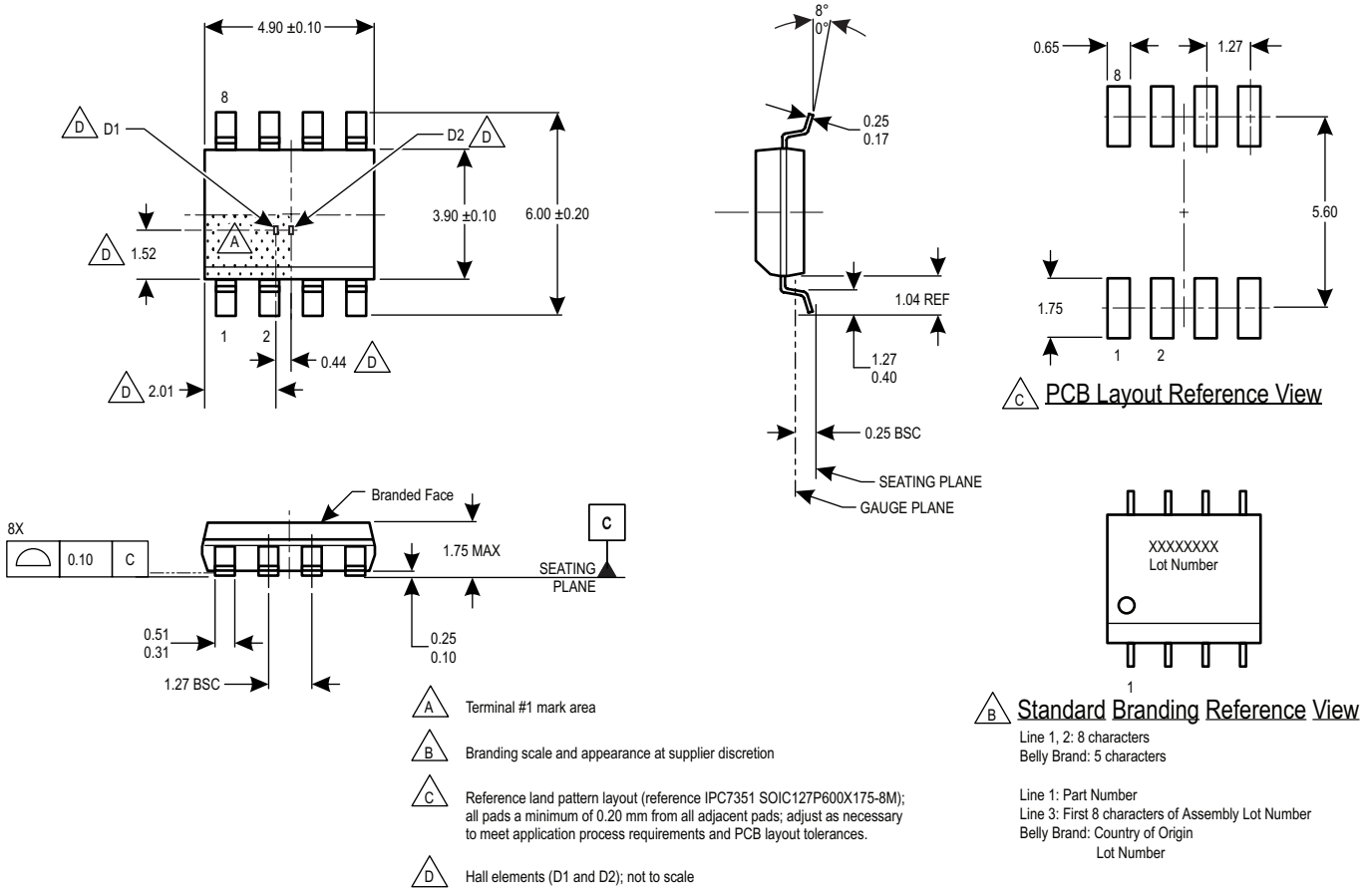

Figure 12: Package LCB, 8-Pin SOIC

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Revision History

Number	Date	Description
–	March 7, 2019	Initial release
1	May 31, 2019	Updated TUV certificate mark
2	July 24, 2019	Added Hall elements to LC package drawing (page 20)

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