NXP Semiconductors
Data Sheet: Technical Data

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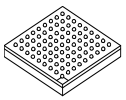
MCIMX6V2CVM08AB

i.MX 6SLL Applications Processors for Industrial Products



Package Information
Plastic Package
14 x 14 mm, 0.65 mm pitch BGA

Ordering Information
See Table 1 on page 2

1 Introduction

The i.MX 6SLL processor represents NXP's latest achievement in integrated multimedia applications processors, which are part of a growing family of multimedia-focused products that offer high performance processing and are optimized for lowest power consumption.

The processor features NXP's advanced implementation of a single Arm® Cortex®-A9, which operates at speeds up to 800 MHz. The processor provides a 32-bit DDR interface that supports LPDDR2 and LPDDR3. In addition, there are a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

The i.MX 6SLL processor is specifically useful for applications, such as:

- Color and monochrome eReaders
- Barcode scanners
- Connectivity
- IoT devices

The i.MX 6SLL processor features:

- Applications processor—The i.MX 6SLL incorporates a 1 GHz Cortex A9 with the NEON SIMD engine and a floating point engine that is optimized for low power consumption and includes hardware that allows dynamic voltage and frequency scaling (DVFS). This optimizes the voltage to the processor as the frequency changes with the demands of the application.
- Multilevel memory system—The multilevel memory system for the processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processor supports many types of external memory devices, including LPDDR2, LPDDR3, and eMMC.
- Powerful graphics acceleration—The processor has a 2D graphics processor called the pixel processor (PXP) that can support CSC, dithering, rotation, resize, and overlay.
- Interface flexibility—The processor supports connections to a variety of interfaces: high-speed USB on-the-go with PHY, high-speed USB host PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), and a variety of other popular interfaces (such as UART, I^2C, and I^2S).
- Electronic Paper Display Controller—The processor integrates EPD controller that supports E-INK color and monochrome with up to 2332 x 1650 resolution and 5-bit grayscale.
- Advanced security—The processor delivers hardware-enabled security features that enable secure information encryption, secure boot, and secure software downloads. The security features are discussed in the *i.MX 6SLL Security Reference Manual* (IMX6SLLSRM). Contact your local NXP representative for more information.
- GPIO with interrupt capabilities—The GPIO pad design supports configurable dual voltage rails at 1.8 V and 3.3 V supplies. The pad is configurable to interface at either voltage level.

1.1 Ordering Information

Table 1 shows the orderable part numbers covered by this data sheet.

Table 1. Example Orderable Part Numbers

Part Number	Feature	Temperature (Tj)	Package
MCIMX6V2CVM08AB	Features supports: • 800 MHz, industrial grade for general purpose • Basic security • With LCD/CSI • PXP • No EPDC • eMMC 5.0/SD 3.0 x3 • USB OTG x2 • UART x5 • SSI x3 • Timer x3 • PWM x4 • I2C x4 • SPI x4	-40 to +105 °C	14x14 mm, 0.65 mm pitch BGA

Figure 1 describes the part number nomenclature so that characteristics of a specific part number can be identified (for example, Cores, Frequency, Temperature Grade, Fuse options, Silicon revision).

- The i.MX 6SLL Applications Processors for Industrial Products Data Sheet (IMX6SLLIEC) covers parts listed with a “C (Industrial temp)”

Ensure to have the right data sheet for specific part by checking the Temperature Grade (Junction) field and matching it to the right data sheet. If there are any questions, visit the web page NXP.com/imx6series or contact a NXP representative.

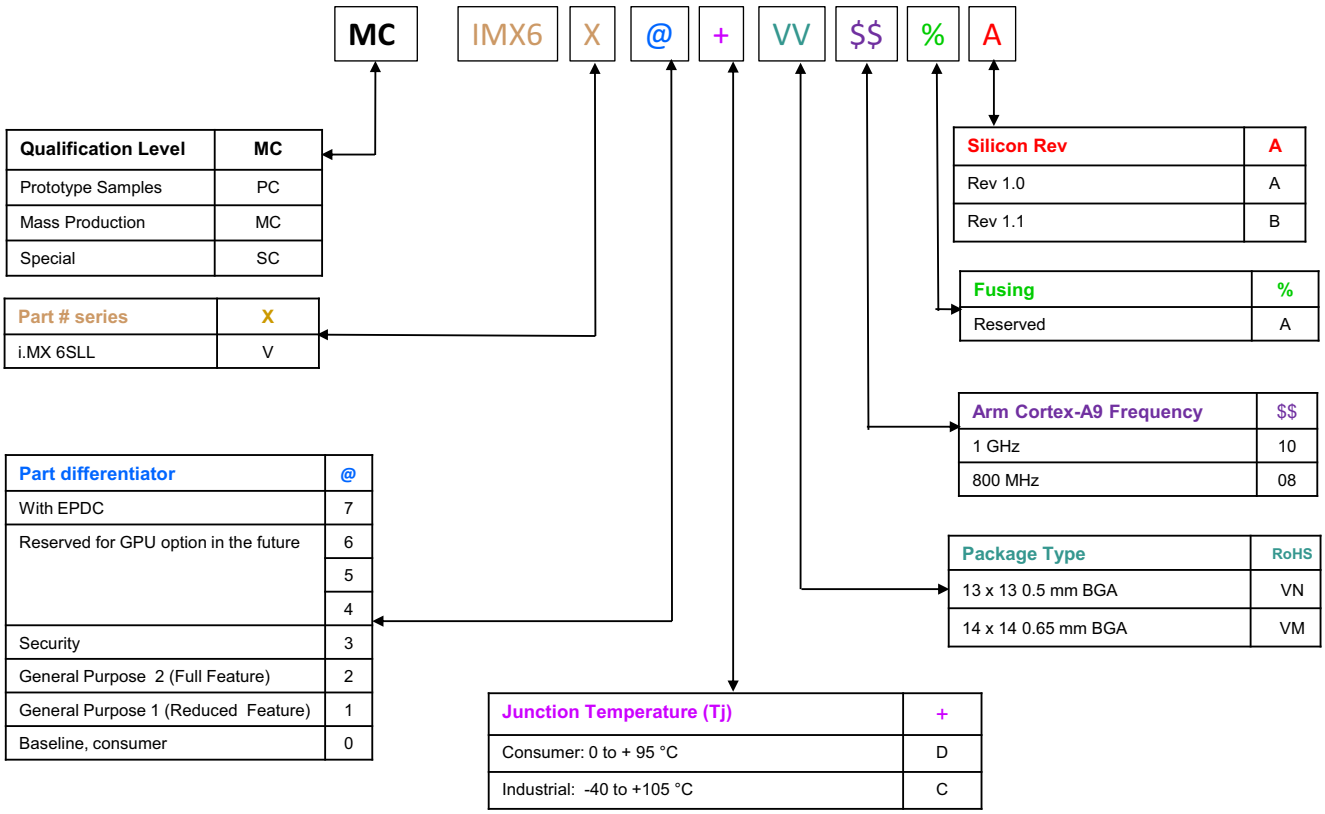


Figure 1. Part Number Nomenclature—i.MX 6SLL

1.2 Features

The i.MX 6SLL processor is based on Arm Cortex-A9 processor, which has the following features:

- Arm Cortex-A9 MPCore CPU processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) co-processor

The Arm Cortex-A9 includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- 256 KB unified I/D L2 cache
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including NEON and L1 cache) as per Table 9, "Operating Ranges," on page 19
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The SoC-level memory system consists of the following additional components:

  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 128 KB)
- External memory interfaces:
  - 32-bit LPDDR2/LPDDR3

Each i.MX 6SLL processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Display:
  - EPDC, color, and monochrome E-INK, up to 2332x1650 resolution and 5-bit grayscale
  - 24-bit parallel LCD
- Expansion cards:
  - Three MMC/SD/SDIO card ports all supporting:
    - SD 3.0 support
    - eMMC 5.0 support in HS400 mode
- USB:
  - Two High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB PHY
- Miscellaneous IPs and interfaces:
  - SSI block—capable of supporting audio sample frequencies up to 192 kHz stereo inputs and outputs with I^2S mode
  - Five UARTs, up to 5.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode
    - One of the five UARTs supports 8-wire, while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.

— Four eCSPI (Enhanced CSPI)
— Three I^2C, supporting 400 kbps
— Four Pulse Width Modulators (PWM)
— System JTAG Controller (SJC)
— GPIO with interrupt capabilities
— Sony Philips Digital Interface (SPDIF), Rx and Tx
— Two Watchdog timers (WDOG)
— Audio MUX (AUDMUX)

The i.MX 6SLL processor integrates power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use Software State Retention and Power Gating for Arm and NEON
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6SLL processor uses dedicated hardware accelerators to meet needs of E-INK Displays. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6SLL processor incorporates the following hardware accelerators:

- PXP—PiXel Processing Pipeline. Off loading key pixel processing operations are required to support the EPD display applications.

Security functions are enabled and accelerated by the following hardware:

- Arm TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock.
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements.

The actual feature set depends on the part numbers as described in Table 1, "Example Orderable Part Numbers," on page 2. Functions, such as 2D hardware graphics acceleration or E-Ink may not be enabled for specific part numbers.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6SLL processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6SLL processor system.

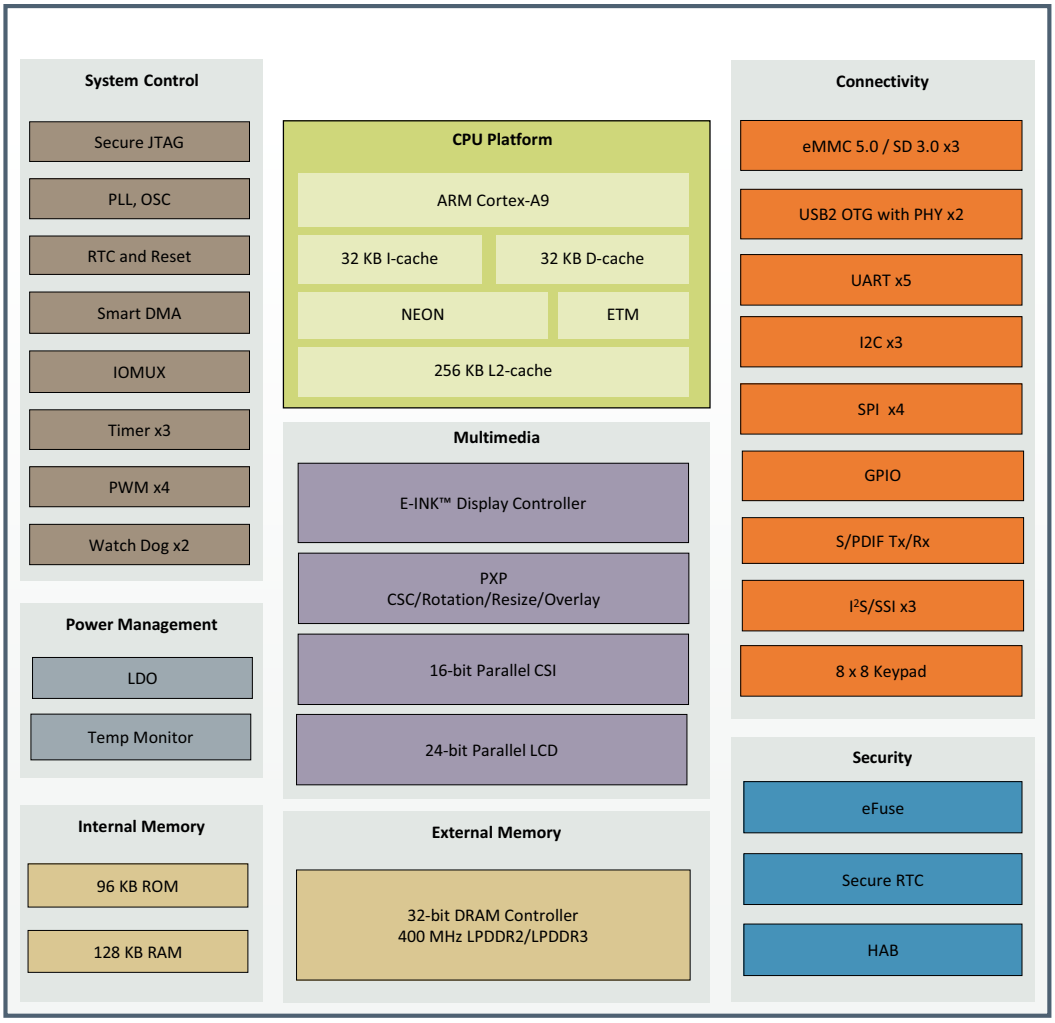


Figure 2. i.MX 6SLL System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (x4) indicates four separate PWM peripherals.

3 Modules List

The i.MX 6SLL processor contains a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6SLL Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters.
Arm	Arm Platform	Arm	The Arm Cortex-A9 platform consists of a Cortex-A9 core and associated sub-blocks, including level 2 cache controller, GIC (General Interrupt Controller), private timers, watchdog, and CoreSight debug modules.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The Digital Audio Multiplexer (AUDMUX) provides a programmable interconnect device for voice, audio, and synchronous data routing between Synchronous Serial Interface Controller (SSI) and audio/voice codec's (also known as coder-decoders) peripheral serial interfaces.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	Parallel CSI	Multimedia Peripherals	The CSI IP provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/16-bit Bayer data input.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6SLL platform. The Security Control Registers (SCR) of the CSU are set during boot time by the HAB and are locked to prevent further writing.
CTI-1 CTI-2	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCP	Data co-processor	Security	This module provides support for general encryption and hashing functions typically used for security functions. Because its basic job is moving data from memory to memory, it also incorporates a memory-copy (memcopy) function for both debugging and as a more efficient method of copying data between memory blocks than the DMA-based approach.

Table 2. i.MX 6SLL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eCSPI-1 eCSPI-2 eCSPI-3 eCSPI-4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EPDC	Electrophoretic Display Controller	Peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive E-INK™ EPD panels, supporting a wide variety of TFT backplanes.
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. GPIO module (1 - 5) supports 32 bits of I/O and GPIO6 supports 5 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
LCDIF	LCD interface	Connectivity peripherals	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Support 32-bit LPDDR2/LPDDR3 • Supports up to 2 GByte DDR memory space

Table 2. i.MX 6SLL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
OCOTP_ CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory Controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6SLL processor, the OCRAM is used for controlling the 128 KB multimedia RAM through a 64-bit AXI bus.
OCRAM_L 2	On-Chip Memory Controller for L2 Cache	Data Path	The On-Chip Memory controller for L2 cache (OCRAM_L2) module is designed as an interface between system's AXI bus and internal (on-chip) L2 cache memory module during boot mode.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from external crystal.
PMU	Power-Management functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
PXP	PiXel Processing Pipeline	Display Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with either of the integrated EPD controllers.
RAM 128 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controller.
RNGB	Random Number Generator	Security	Random number generating module.
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection.
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing.

Table 2. i.MX 6SLL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6SLL processor uses JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6SLL SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Phillips Digital Interface	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the AP to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options.
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP, for detecting high temperature conditions. The Temperature sensor IP for detecting die temperature. The temperature read out does not reflect case or ambient temperature, but the proximity of the temperature sensor location on the die. Temperature distribution may not be uniformly distributed, therefore the read out value may not be the reflection of the temperature value of the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by Arm) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 Mbps. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Only one can operate as 8-pins full UART, DCE, or DTE
USBO2	2x USB 2.0 High Speed OTG	Connectivity Peripherals	USBO2 contains: • Two high-speed OTG module with integrated HS USB PHY

Table 2. i.MX 6SLL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-3	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6SLL specific SoC characteristics: All three MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v5.0 including high-capacity (size > 2 GB) cards HC MMC. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB and SDXC cards up to 2 TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10. • Conforms to the SD Host Controller Standard Specification version 3.0.
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

3.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 6SLL processor. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, Package Information and Contact Assignments." Signal descriptions are provided in the *i.MX 6SLL Reference Manual*.

Table 3. Special Signal Considerations

Signal Name	Remarks
CLK1_P/ CLK1_N	One general purpose differential high speed clock Input/output is provided. It could be used to: • To feed external reference clock to the PLLs and further to the modules inside SoC, for example as alternate reference clock for Audio interfaces, etc. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. See the *i.MX 6SLL Reference Manual* for details on the respective clock trees. The clock inputs/outputs are LVDS differential pairs compatible with TIA/EIA-644 standard. The corresponding CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. See LVDS pad electrical specification for further details. After initialization, the CLK1 input/output could be disabled (if not used). If unused, the CLK1_N/P pair may remain unconnected.
DRAM_VREF	When using DRAM_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DRAM_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DRAM_VREF tolerance (per the DDR3 specification) is maintained when four DDR3 ICs plus the i.MX 6SLL are drawing current on the resistor divider. It is recommended to use regulated power supply for “big” memory configurations (more that eight devices).
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the non-connected condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MODE must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MODE set to high configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MODE set to low configures the JTAG interface for common Software debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and should be disconnected by the user.
ONOFF	In normal mode may be connected to ONOFF button (de-bouncing provided at this input). Internally this pad is pulled up. A short duration (<5s) connection to GND in OFF mode causes the internal power management state machine to change the state to ON. In ON mode, a short duration connection to GND generates interrupt (intended to initiate a software controllable power down). A long duration (above ~5s) connection to GND causes “forced” OFF.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low)

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
RTC_XTALI/ RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In the case when a high accuracy real time clock is not required, the system may use an internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO unconnected.
TEST_MODE	TEST_MODE is for NXP factory use. This signal is internally connected to an on-chip pull-down device. The user must either disconnect this signal or tie it to GND.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO. level and the frequency should be <32 MHz under typical conditions. The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typically 80 Ω is recommended. NXP BSP (board support package) software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALI must be directly driven by the external oscillator and XTALO is disconnected. The XTALI signal level must swing from ~0.8 x NVCC_PLL to ~0.2 V. This clock is used as a reference for USB, so there are strict frequency tolerance and jitter requirements. See the XTALOSC chapter and relevant interface specifications chapters of the *i.MX 6SLL Reference Manual* for details.
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-Chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRST_B	Input	47 kΩ pull-up
JTAG_MODE	Input	100 kΩ pull-up

3.2 Recommended Connections for Unused Analog Interfaces

Table 5 shows the recommended connections for unused analog interfaces.

Table 5. Recommended Connections for Unused Analog Interfaces

Module	Pad Name	Recommendations if Unused
XTALOSC	CLK1_N, CLK1_P	Not connected
USB	USB_OTGx_DN, USB_OTGx_DP, USB_OTGx_VBUS, USB_OTG_CHD_B	Not connected

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6SLL.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6SLL Chip-Level Conditions

For these characteristics …	Topic appears …
Absolute Maximum Ratings	on page 15
Thermal Resistance	on page 17
Operating Ranges	on page 19
External Clock Sources	on page 20
Maximum Supply Currents	on page 21
Low Power Mode Supply Currents	on page 22
USB PHY Current Consumption	on page 23

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7 shows the absolute maximum operating ratings.

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max[1]	Unit
Core supply voltages	VDD_ARM_IN VDD_SOC_IN	-0.3	1.4	V
GPIO supply voltage	Supplies denoted as I/O supply	-0.5	3.6	V
DDR I/O supply voltage	Supplies denoted as I/O supply	-0.4	1.975 (see note 2)	V
VDD_HIGH_IN supply voltage	VDD_HIGH_IN	-0.3	3.6	V
USB_OTG1_VBUS, USB_OTG2_VBUS	USB_OTG1_VBUS USB_OTG2_VBUS	—	5.5	V

Table 7. Absolute Maximum Ratings (continued)

Parameter Description	Symbol	Min	Max[1]	Unit
Input voltage on USB signals (non-VBUS)	USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN, USB_OTG_CHD_B	-0.3	3.63	V
Input/Output Voltage range (Non-DDR pins)	V_{in}/V_{out}	-0.5	OVDD + 0.3 (See note 3)	V
Input/Output Voltage range (DDR Pins)	V_{in}/V_{out}	-0.5	OVDD + 0.4 (See note 2, 3)	V
ESD Immunity (HBM) All pins except VDD_SNVS_CAP and VDD_ARM_IN pins	Vesd_HBM	—	2000	V
ESD Immunity (HBM) VDD_SNVS_CAP and VDD_ARM_IN pins	Vesd_HBM	—	1000	V
ESD Immunity (CDM)	Vesd_CDM	—	500	V
Storage temperature range	$T_{STORAGE}$	-40	150	°C

1 Exceeding maximum may result in breakdown, or reduction in IC life time, performance, and/or reliability.

2 The absolute maximum voltage includes an allowance for 400 mV of overshoot on the IO pins. Per JEDEC standards, the allowed signal overshoot must be de-rated if NVCC_DRAM exceeds 1.575 V.

3 OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

NOTE

Per JEDEC JESD51-2, the intent of thermal resistance measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

4.1.2.1 14 x 14 mm (VM) Package Thermal Resistance

Table 8 provides the 14 x 14 mm package thermal resistance data.

Table 8. Package Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to Ambient[1,2] (natural convection)	Single layer board (1s)	$R_{\theta JA}$	50.6	°C/W
Junction to Ambient[1,2,3] (natural convection)	Four layer board (2s2p)	$R_{\theta JA}$	31.7	°C/W
Junction to Ambient[1,3] (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	39.4	°C/W
	Four layer board (2s2p)	$R_{\theta JMA}$	27.5	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	16.7	°C/W
Junction to Case[5]	—	$R_{\theta JC}$	12.0	°C/W
Junction to Package Top[6]	Natural Convection	Ψ_{JT}	0.2	°C/W
Junction to Package Bottom[7]	Natural Convection	$R_{\theta JB\_CSB}$	13.9	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 The thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7 Thermal resistance between the die and the central solder balls on the bottom of the package based on simulation.

4.1.3 Operating Ranges

Figure 3 shows major power systems blocks and internal/external connections for the i.MX 6SLL processor.

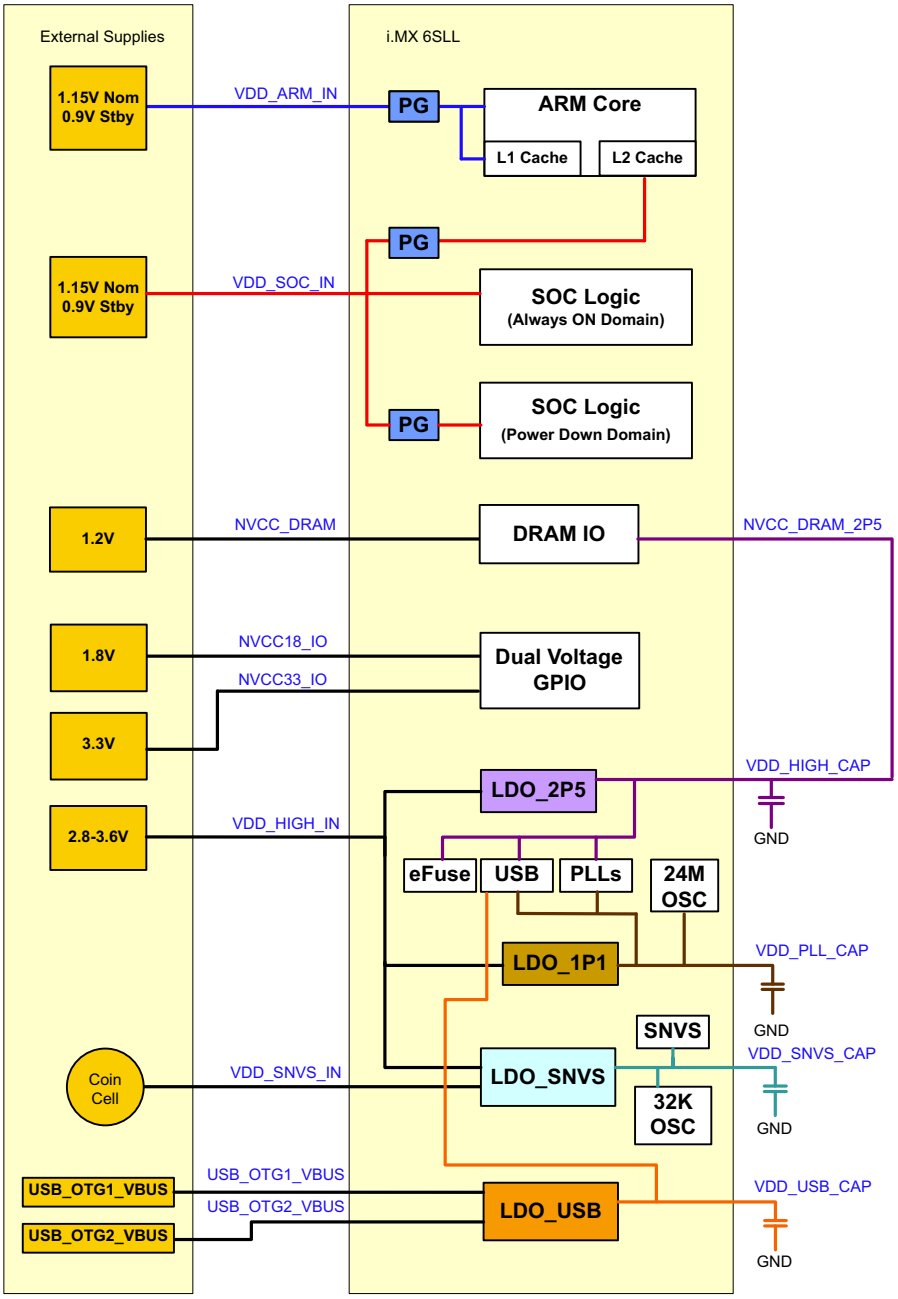


Figure 3. i.MX 6SLL SoC Power Block Diagram

Table 9 provides the operating ranges of the i.MX 6SLL processor.

Table 9. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Run Mode	VDD_ARM_IN	1.150	—	1.26	V	For operation up to 792 MHz.
		1.05	—	1.26	V	For operation up to 396 MHz.
		0.950	—	1.26	V	For operation up to 198 MHz
		0.925	—	1.26	V	For operation up to 24 MHz
	VDD_SOC_IN	1.15	—	1.26	V	—
Low Power Run Mode	VDD_ARM_IN	0.925	—	1.26	V	All PLL bypassed, all clocks running at 24 MHz or below.
	VDD_SOC_IN	0.925	—	1.26	V	
Standby/DSM Mode	VDD_ARM_IN	0.9	—	1.26	V	See Table 12, "Low Power Mode Current and Power Consumption," on page 22.
VDDHIGH internal Regulator	VDD_HIGH_IN[2]	2.8	—	3.6	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[2]	2.4	—	3.6	V	Should be supplied from the same supply as VDD_HIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG1_VBUS USB_OTG2_VBUS	4.4	—	5.5	V	—
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.26	V	LPDDR2, LPDDR3
	NVCC_DRAM_2P5	2.25	2.5	2.75	V	—
GPIO supplies[3]	NVCC33_IO[2]	3.0	3.3	3.6	V	Worst case, assuming all SOC I/O operating at 1.8V. NVCC33_IO must always be greater than NVCC18_IO.
	NVCC18_IO[2]	1.65	1.8	1.95	V	—
Junction temperature	T_J	-40	—	105	—	Industrial See *i.MX 6SLL Product Lifetime Usage Estimates Application Note* for information on product lifetime (power-on years) for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

2 Applying the maximum voltage results in shorten lifetime. 3.6 V usage limited to < 1% of the use profile. Rest of profile limited to below 3.49 V.

3 All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to have a pull-up or pull-down resistor applied to limit any non-connected gate current.

4.1.4 External Clock Sources

Each i.MX 6SLL processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can substitute the RTC_XTALI, in case accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier.

NOTE

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

Table 10 shows the interface frequency requirements.

Table 10. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1, 2]	f_{ckil}	—	32.768 (see 3) / 32.0	—	kHz
XTALI Oscillator[4, 2]	f_{xtal}	—	24	—	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent.

3 Recommended nominal frequency 32.768 kHz.

4 External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 10 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
  - Approximately 25 μA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision to choose a clock source should be taken based on real-time clock use and precision time-out.

4.1.5 Maximum Supply Currents

The numbers shown in Table 11 represent the maximum current consumption possible.

See the i.MX 6SLL Power Consumption Measurement Application Note for more details on typical power consumption under various use case definitions.

Table 11. Maximum Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_ARM_IN	800 MHz Arm clock based on Power Virus operation	1100	mA
VDD_SOC_IN	800 MHz Arm clock	650	mA
VDD_HIGH_IN	—	100[1]	mA
VDD_SNVS_IN	—	250[2]	μA
USB_OTG1_VBUS USB_OTG2_VBUS	—	25[3]	mA
Primary Interface (IO) Supplies			
NVCC_DRAM	—	(see[4])	
NVCC33_IO	N=156	Use maximum IO Equation[5]	
NVCC18_IO	N=156	Use maximum IO Equation[5]	mA
MISC			
DRAM_VREF	—	1	mA

1 The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_DRAM_2P5 supplies).

2 The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination.
See the i.MX 6SLL Power Consumption Measurement Application Note or examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximum power consumption of an IO power supply:

Imax = N x C x V x (0.5 x F)

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Low Power Mode Supply Currents

Table 12 shows the current core consumption (not including I/O) of i.MX 6SLL processor in selected low power modes.

Table 12. Low Power Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Unit
System Idle (WAIT)	• CPU is in WFI state, CPU clock is gated • DDR enters self refresh automatically when no access • High-speed peripherals are clock gated, but remain powered • LDO-2P5 set to 2.5 V, LDO_1P1 set to 1.1 V • 24 MHz XTAL is ON • 528 PLL active, other PLLs are power down	VDD_ARM_IN (1.15 V)	5.00	mA
		VDD_SOC_IN (1.15 V)	8.00	
		VDD_HIGH_IN (3.0 V)	7.00	
		VDD_SNVS_IN(3.0 V)	0.05	
		Total	36.1	mW
Low Power Idle (STANDBY)	• CPU is power gated • DDR is put in self refresh by SW, DDR IO is disabled • High-speed peripherals are clock gated, but remain powered • LDO_2P5 and LDO_1P1 are set to weak mode • 24 MHz XTAL is off, 24 MHz Hz RCOSC used as clock source • All PLL are power down	VDD_ARM_IN (0.9 V)	—	mA
		VDD_SOC_IN (0.9 V)	1.60	
		VDD_HIGH_IN (3.0 V)	0.30	
		VDD_SNVS_IN (3.0 V)	0.04	
		Total	2.46	mW
Suspend (DSM)	• CPU is power gated • DDR is put in self refresh by SW, DDR IO is disabled • High-speed peripherals are power gated • LDO_2P5 and LDO_1P1 are shut off • 24 MHz XTAL is off, 24 MHz RCOSC is off • All PLL are power down • All clocks are shut off, only except 32 kHz RTC	VDD_ARM_IN (0 V)	—	mA
		VDD_SoC_IN (0.9 V)	0.20	
		VDD_HIGH_IN (3.0 V)	0.03	
		VDD_SNVS_IN (3.0 V)	0.02	
		Total	0.33	mW
SNVS (RTC)	• CPU is power down • All SOC digital logic is power down • All analog circuit is power down except 32K RTC	VDD_ARM_IN (0 V)	—	mA
		VDD_SOC_IN (0 V)	—	
		VDD_HIGH_IN (0 V)	—	
		VDD_SNVS_IN (3.0 V)	0.02	
		Total	0.06	mW

[1] The typical values shown here are for information only and are not guaranteed. These values are average values measured on a typical process wafer at 25°C.

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the USB_OTGx_VBUS valid detectors, typical condition. Table 13 shows the USB interface current consumption in power down mode.

Table 13. USB PHY Current Consumption in Power Down Mode

	VDD_USB_CAP (3.0 V)	VDDHIGH_CAP (2.5 V)	NVCC_PLL (1.1 V)
Current	5.1 μA	1.7 μA	<0.5 μA

NOTE

The currents on the VDD_HIGH_CAP and VDD_USB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1 Power-Up Sequence

For power-up sequence, the restrictions are as follows:

- VDD_SNVS_IN supply must be turned ON before any other power supply. It may be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure it is connected before any other supply is switched on.
- VDD_SOC_IN must be turned on before any other digital IO power supply.
- POR_B signal must be immediately asserted at power-up and remain asserted after the last power rail reaches its working voltage.
- VDD_ARM_IN may be applied with no restrictions.
- NVCC33_IO must be applied before NVCC18_IO.

NOTE

See the *i.MX 6SLL Reference Manual* (IMX6SLLRM) for further details and to ensure that all necessary requirements are being met.

NOTE

Ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG1_VBUS and USB_OTG2_VBUS are not part of the power supply sequence and can be powered at any time.

4.2.2 Power-Down Sequence

For power-down sequence, the restrictions are as follows:

- VDD_SNVS_IN supply must be turned off after all other power supply. It may be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is removed after all other supply are switched off.

4.2.3 Power Supplies Usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC33_IO and NVCC18_IO) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Group” column of Table 64, "14 x 14 mm Functional Contact Assignments," on page 72.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX 6SLL Reference Manual* for details on the power tree scheme recommended operation.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Regulators for Analog Modules

4.3.1.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 9 for min and max input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. LDO_1P1 supplies the USB Phy and the PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For information on external capacitor requirements for this regulator, see the *Hardware Development Guide for i.MX 6SLL Applications Processors* (IMX6SLLHDG). For additional information, see the *i.MX 6SLL Reference Manual*.

4.3.1.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 9 for min and max input requirements). Typical programming operating range is 2.25 V to 2.75 V

with the nominal default setting as 2.5 V. LDO_2P5 supplies the USB Phy, LVDS Phy and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω.

For information on external capacitor requirements for this regulator, see the *Hardware Development Guide for i.MX 6SLL Applications Processors* (IMX6SLLHDG).

For additional information, see the *i.MX 6SLL Reference Manual* (IMX6SLLRM).

4.3.1.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG1_VBUS and USB_OTG2_VBUS voltages (4.4 V–5.5 V) to produce a nominal 3.0 V output voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either VBUS supply, when both are present. If only one of the VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets. If no VBUS voltage is present, then the VBUSVALID threshold setting will prevent the regulator from being enabled.

For information on external capacitor requirements for this regulator, see the *Hardware Development Guide for i.MX 6SLL Applications Processors* (IMX6SLLHDG).

For additional information, see the *i.MX 6SLL Reference Manual* (IMX6SLLRM).

4.4 PLL's Electrical Characteristics

4.4.1 Audio/Video PLL's Electrical Parameters

Table 14. Audio/Video PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles (450 μs)

4.4.2 528 MHz PLL

Table 15. 528 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles (15 μs)

4.4.3 480 MHz PLL

Table 16. 480 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles (15 μs)

4.4.4 Arm PLL

Table 17. Arm PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz~1.3 GHz
Reference clock	24 MHz
Lock time	<2250 reference cycles (50 μs)

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. It also implements a power mux such that the oscillator can be powered from VDD_SOC. If the oscillator is required to run in *stop mode* then it is necessary to run from VDD_SOC, which is 0.9 V in *stop mode*.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the back up battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 kHz clock will automatically switch to the internal ring oscillator.

CAUTION

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

Table 18. OSC32K Main Characteristics

Parameter	Min	Typ	Max	Comments
Fosc	—	32.768 kHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption	—	4 μA	—	The typical value shown is only for the oscillator, driven by an external crystal. If the internal ring oscillator is used instead of an external crystal, then approximately 25 μA should be added to this value.
Bias resistor	—	14 MΩ	—	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	—	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- Dual Voltage General Purpose I/O cell set (DVGPIO)
- Single Voltage General Purpose I/O cell set (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and LPDDR3 modes

NOTE

The term OVDD in this section refers to the associated supply rail of an input or output.

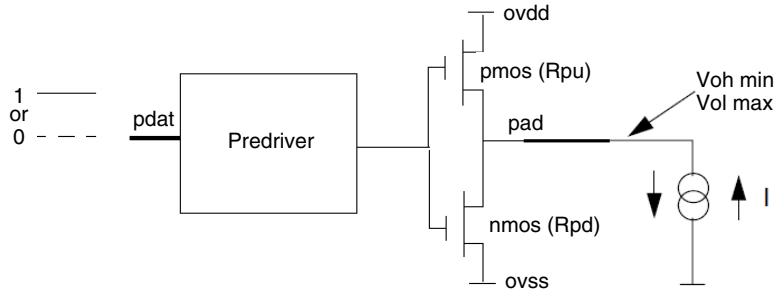


Figure 4. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 19 shows the DC parameters for the clock inputs.

Table 19. XTALI and RTC_XTALI DC Parameters [1]

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL	—	NVCC_PLL	V
XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	—	1.1[2]	V
RTC_XTALI low-level DC input voltage	Vil	—	0	—	0.2	V
Input Capacitance	C_{IN}	Simulated data	—	5	—	pF
Startup current	$I_{XTALI\_STARTUP}$	Power-on startup for 0.15 msec with a driven 24 MHz clock at 1.1 V. This current draw is present even if an external clock source directly drives XTALI	—	—	600	µA
DC input current	I_{XTALI_DC}	—	—	—	2.5	µA

1 The DC parameters are for external clock input only.

2 This voltage specification must not be exceeded and, as such, is an absolute maximum specification.

NOTE

The Vil and Vih specifications only apply when an external clock source is used. If a crystal is used, Vil and Vih do not apply.

4.6.2 Dual Voltage General Purpose IO cell set (DVGPIO) DC Parameters

Table 20 shows DC parameters for GPIO pads. The parameters in Table 21 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 20. DVGPIO I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage[1]	Voh	Ioh = -0.1 mA (DSE[2] = 001, 010) Ioh = -1 mA (DSE = 011, 100, 101, 110, 111)	OVDD – 0.15	—	V
Low-level output voltage[1]	Vol	Iol = 0.1 mA (DSE[2] = 001, 010) Iol = 1mA (DSE = 011, 100, 101, 110, 111)	—	0.15	V
High-Level DC input voltage[1, 3]	Vih	—	0.7 × OVDD	OVDD	V
Low-Level DC input voltage[1, 3]	Vil	—	0	0.3 × OVDD	V
Input Hysteresis	Vhys	OVDD = 1.8 V OVDD = 3.3 V	0.25	—	V
Schmitt trigger VT+[3, 4]	VT+	—	0.5 × OVDD	—	V
Schmitt trigger VT–[3, 4]	VT–	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	-1.25	1.25	μA
Input current (22 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	212 1	μA
Input current (47 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	100 1	μA
Input current (100 kΩ pull-up)	Iin	Vin = 0 V Vin= OVDD	—	48 1	μA
Input current (100 kΩ pull-down)	Iin	Vin = 0 V Vin = OVDD	—	1 48	μA
Keeper circuit resistance	Rkeep	Vin = 0.3 x OVDD Vin = 0.7 x OVDD	105	205	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 DSE is the Drive Strength Field setting in the associated IOMUX control register.

3 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

4 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.3 Single Voltage General Purpose I/O (GPIO) DC Parameters

Table 21 shows DC parameters for GPIO pads. The parameters in Table 21 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 21. GPIO I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage[1]	Voh	Ioh = -0.1 mA (DSE[2] = 001, 010) Ioh = -1 mA (DSE = 011, 100, 101, 110, 111)	OVDD – 0.15	—	V
Low-level output voltage[1]	Vol	Iol = 0.1 mA (DSE[2] = 001, 010) Iol = 1mA (DSE = 011, 100, 101, 110, 111)	—	0.15	V
High-Level DC input voltage[1, 3]	Vih	—	0.7 × OVDD	OVDD	V
Low-Level DC input voltage[1, 3]	Vil	—	0	0.3 × OVDD	V
Input Hysteresis	Vhys	OVDD = 3.3 V	0.25	—	V
Schmitt trigger VT+[3, 4]	VT+	—	0.5 × OVDD	—	V
Schmitt trigger VT–[3, 4]	VT–	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	-1.25	1.25	μA
Input current (22 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	212 1	μA
Input current (47 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	100 1	μA
Input current (100 kΩ pull-up)	Iin	Vin = 0 V Vin= OVDD	—	48 1	μA
Input current (100 kΩ pull-down)	Iin	Vin = 0 V Vin = OVDD	—	1 48	μA
Keeper circuit resistance	Rkeep	Vin = 0.3 x OVDD Vin = 0.7 x OVDD	105	205	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 DSE is the Drive Strength Field setting in the associated IOMUX control register.

3 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

4 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.4 DDR I/O DC Parameters

The DDR I/O pads support LPDDR2 and LPDDR3 operational modes. The Multi-mode DDR Controller (MMDC) is compatible with JEDEC-compliant SDRAMs.

The i.MX 6SLL MMDC supports the following memory types:

- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- LPDDR3 SDRAM compliant to JESD209-3B LPDDR3 JEDEC standard release August, 2013

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for the i.MX 6SLL Applications Processor* (IMX6SLLHDG).

4.6.4.1 LPDDR2/LPDDR3 I/O DC Parameters

Table 22 shows the DC parameters for DDR I/O operating in LPDDR2 and LPDDR3 mode.

Table 22. LPDDR2/LPDDR3 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	Voh	Ioh = -0.1 mA	0.9 × OVDD	—	V
Low-level output voltage	Vol	Iol = 0.1 mA	—	0.1 × OVDD	V
Input reference voltage	Vref	—	0.49 × OVDD	0.51 × OVDD	
DC input High Voltage	Vih(dc)	—	Vref+0.13V	OVDD	V
DC input Low Voltage	Vil(dc)	—	OVSS	Vref-0.13V	V
Differential Input Logic High	Vih(diff)	—	0.26	See Note [2]	
Differential Input Logic Low	Vil(diff)	—	See Note [2]	-0.26	
Input current (no pull-up/down)	Iin	Vin = 0 or OVDD	-2.5	2.5	μA
Pull-up/pull-down impedance Mismatch	MMpupd	—	-15	+15	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper circuit resistance	Rkeep	—	110	175	kΩ

1 Note that the JEDEC LPDDR2 and LPDDR3 specification (JESD209_2B and JESD209-3) supersedes any specification in this document.

2 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot (see Table 25).

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Dual Voltage General Purpose I/O (DVGPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and LPDDR3 modes

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 5 and Figure 6.

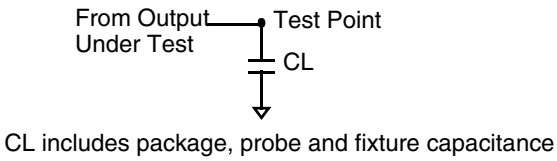


Figure 5. Load Circuit for Output

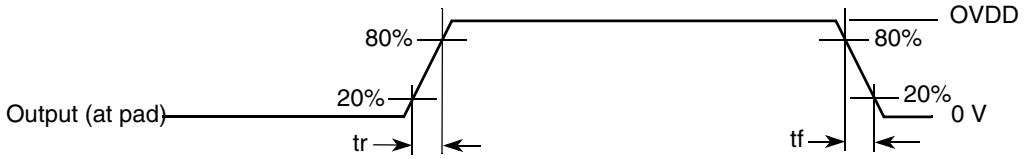


Figure 6. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 23 and Table 24, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 23. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 24. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC Parameters

The Multi-mode DDR Controller (MMDC) is compatible with JEDEC-compliant SDRAMs.

The i.MX 6SLL MMDC supports the following memory types:

- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- LPDDR3 SDRAM compliant to JESD209-3B LPDDR3 JEDEC standard release August, 2013

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for the i.MX 6SLL Applications Processor* (IMX6SLLHDG).

Table 25 shows the AC parameters for DDR I/O operating in LPDDR2 and LPDDR3 mode.

Table 25. DDR I/O AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	—	V
AC differential input low voltage	Vidl(ac)	—	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	—	0.12	V
Over/undershoot peak	Vpeak	—	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.3	V-ns
Single output slew rate, measured between Vol (ac) and Voh (ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 4 0 Ω ±30%	1.5	—	3.5	V/ns
		50 Ω to Vref. 5pF load. Drive impedance = 60 Ω ±30%	1	—	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC LPDDR2 and LPDDR3 specification (JESD209_2B and JESD209-3B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr – Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 × OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6SLL processor for the following I/O types:

- Dual Voltage General Purpose I/O cell set (DVGPIO)
- Single Voltage General Purpose I/O cell set (GPIO)

- Double Data Rate I/O (DDR)

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 7).

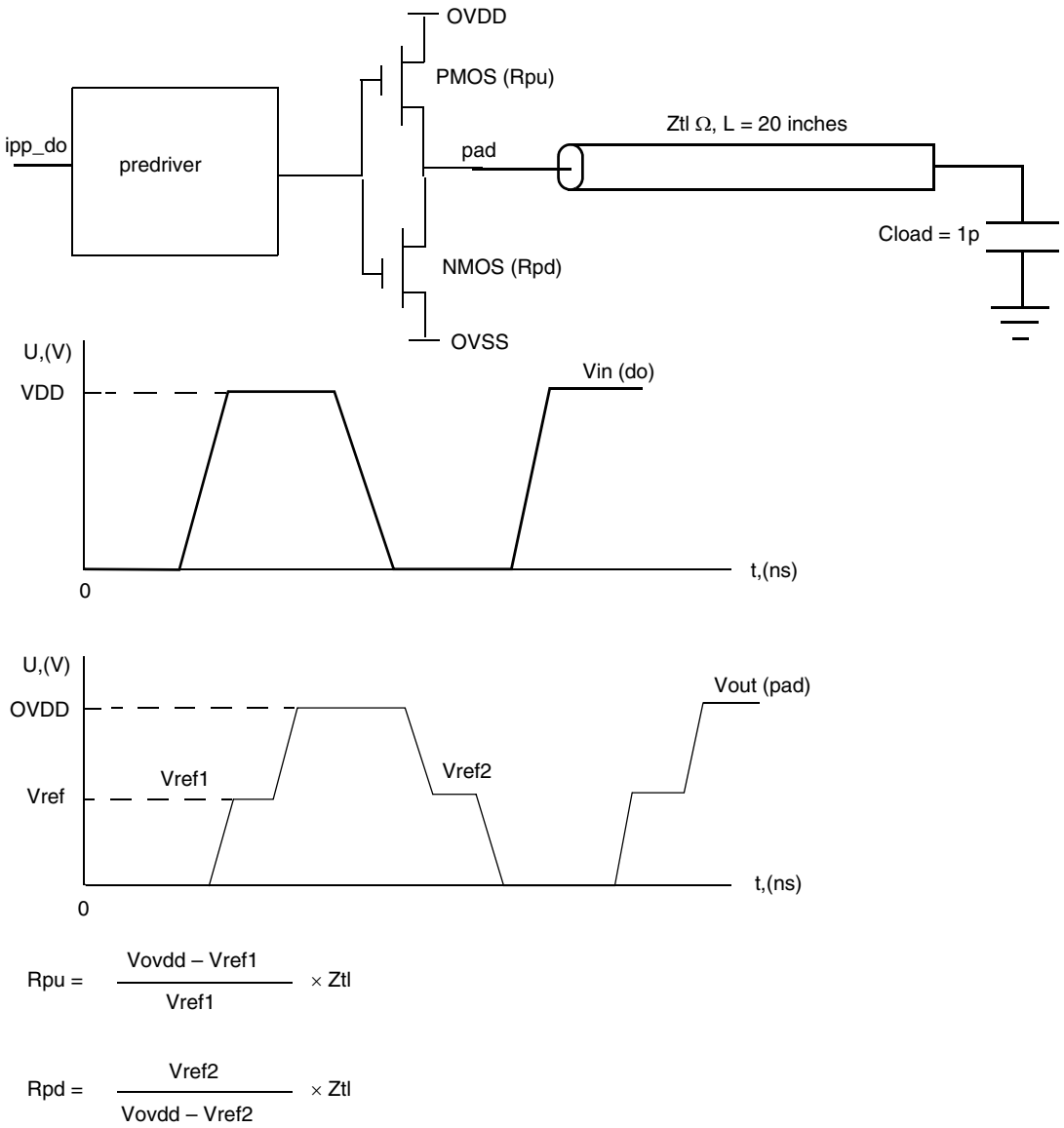


Figure 7. Impedance Matching Load for Measurement

4.8.1 Dual Voltage GPIO Output Buffer Impedance

Table 26 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 26. DVGPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 90 60 50 40 33	Ω

Table 27 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 27. DVGPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	150 75 50 37 30 25 20	Ω

4.8.2 Single Voltage GPIO Output Buffer Impedance

Table 28 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 28. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	150 75 50 37 30 25 20	Ω

4.8.3 DDR I/O Output Buffer Impedance

Table 29 shows DDR I/O output buffer impedance of i.MX 6SLL processor.

Table 29. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions	Typical	Unit
			NVCC_DRAM=1.2 V (LPDDR2/LPDDR3) DDR_SEL=10	
Output Driver Impedance	Rdrv	Drive Strength (DSE) =		Ω
		000	Hi-Z	
		001	240	
		010	120	
		011	80	
		100	60	
		101	48	
		110	40	
		111	34	

Note:
1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6SLL processor.

4.9.1 Reset Timings Parameters

Figure 8 shows the reset timing and Table 30 lists the timing parameters.

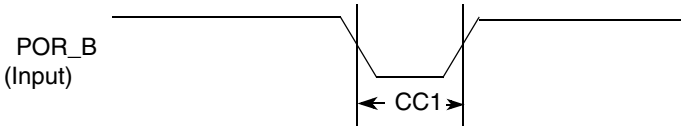


Figure 8. Reset Timing Diagram

Table 30. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid.	1	—	XTALOSC_RTC_XTALI cycle

4.9.2 WDOG Reset Timing Parameters

Figure 9 shows the WDOG reset timing and Table 31 lists the timing parameters.

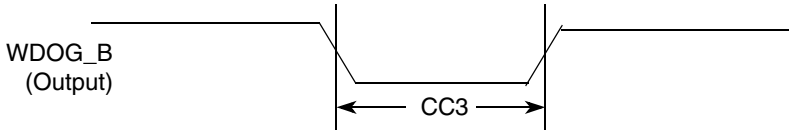


Figure 9. WDOG_B Timing Diagram

Table 31. WDOG_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG_B Assertion	1	—	XTALOSC_RTC_XTALI cycle

NOTE

XTALOSC_RTC_XTALI is approximately 32 kHz.
XTALOSC_RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG_B output signals (for each one of the Watchdog modules) do not have dedicated bins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.9.3 DDR SDRAM Specific Parameters (LPDDR2 and LPDDR3)

4.9.3.1 LPDDR2 and LPDDR3 Parameters

Figure 10 shows the LPDDR2 and LPDDR3 basic timing diagram. The timing parameters for this diagram appear in Table 32.

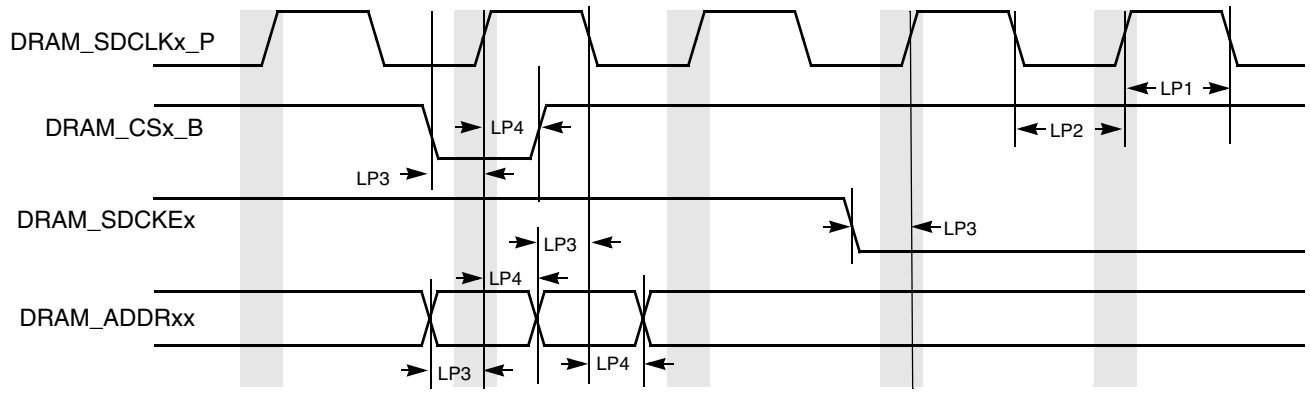


Figure 10. LPDDR2 and LPDDR3 Command and Address Timing Diagram

Table 32. LPDDR2 and LPDDR3 Timing Parameters

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
LP2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
LP3	DRAM_CSx_B, DRAM_SDCKEx setup time	t_{IS}	380	—	ps
LP4	DRAM_CSx_B, DRAM_SDCKEx hold time	t_{IH}	380	—	ps

[1] All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to DRAM_VREF.

Figure 11 shows the LPDDR2 and LPDDR3 write timing diagram. The timing parameters for this diagram appear in Table 33.

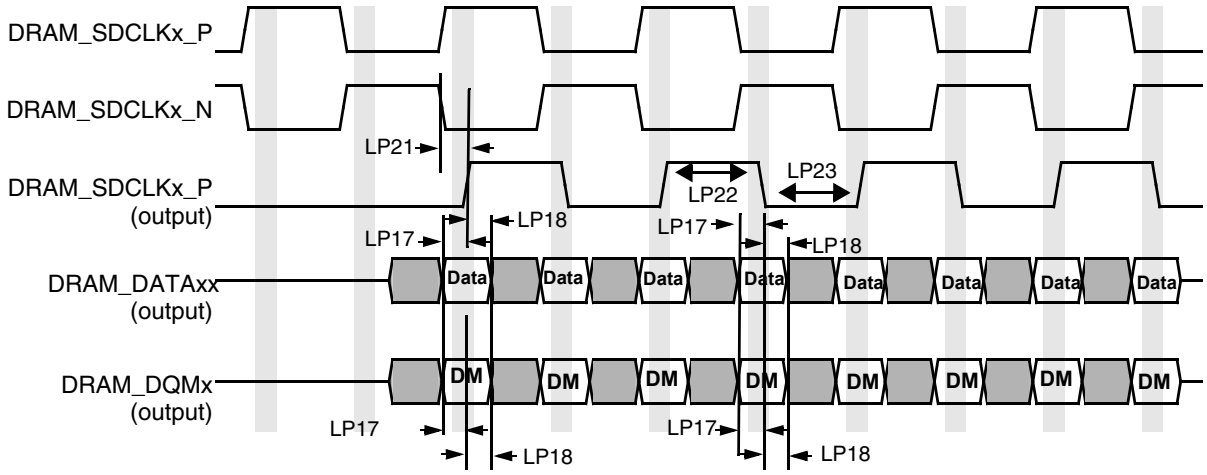


Figure 11. LPDDR2 and LPDDR3 Write Cycle

Table 33. LPDDR2 and LPDDR3 Write Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP17	DRAM_DATAxx and DRAM_DQMx setup time to DRAM_SDQSx_P (differential strobe)	t_{DS}	375	—	ps
LP18	DRAM_DATAxx and DRAM_DQMx hold time to DRAM_SDQSx_P (differential strobe)	t_{DH}	375	—	ps
LP21	DRAM_SDQSx_P latching rising transitions to associated clock edges	t_{DQSS}	-0.25	+0.25	tCK
LP22	DRAM_SDQSx_P high level width	t_{DQSH}	0.4	—	tCK
LP23	DRAM_SDQSx_P low level width	t_{DQSL}	0.4	—	tCK

1 To receive the reported setup and hold values, write calibration should be performed in order to locate the DRAM_SDQS in the middle of DRAM_DATAxx window.

2 All measurements are in reference to Vref level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to DRAM_VREF.

Figure 12 shows the LPDDR2 and LPDDR3 read timing diagram. The timing parameters for this diagram appear in Table 34.

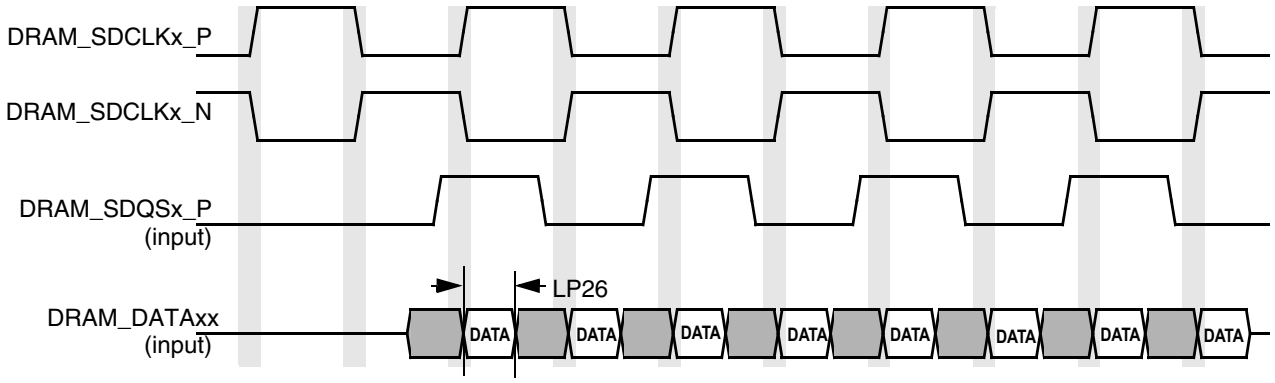


Figure 12. LPDDR2 and LPDDR3 Read Cycle

Table 34. LPDDR2 and LPDDR3 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP26	Minimum required DRAM_DATAxx valid window width for LPDDR2 and LPDDR3	—	270	—	ps

1 To receive the reported setup and hold values, read calibration should be performed in order to locate the DRAM_SDQSx_P in the middle of DRAM_DATA_xx window.

2 All measurements are in reference to Vref level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to DRAM_VREF.

4.10 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.10.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.10.2 CMOS Sensor Interface (CSI) Timing Parameters

4.10.2.1 Gated Clock Mode Timing

Figure 13 and Figure 14 shows the gated clock mode timings for CSI, and Table 35 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on CSI_VSYNC

(VSYNC), then CSI_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.

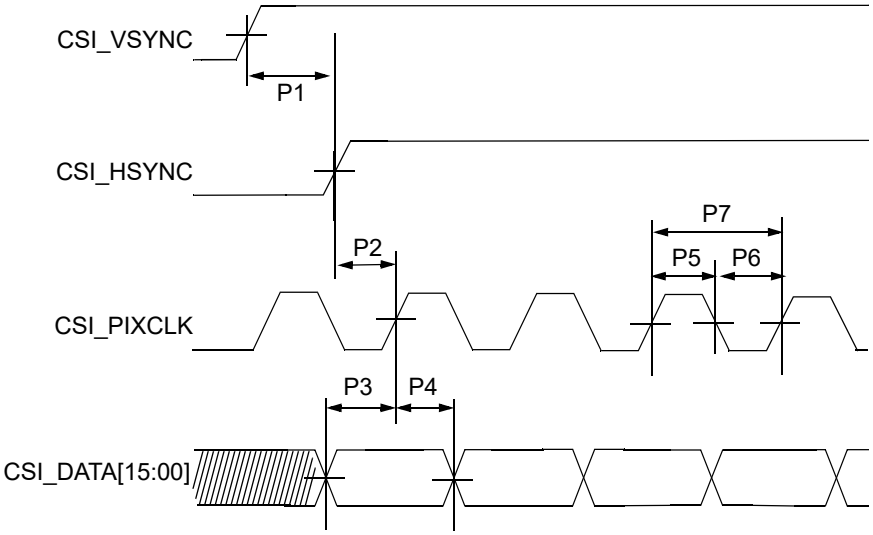


Figure 13. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

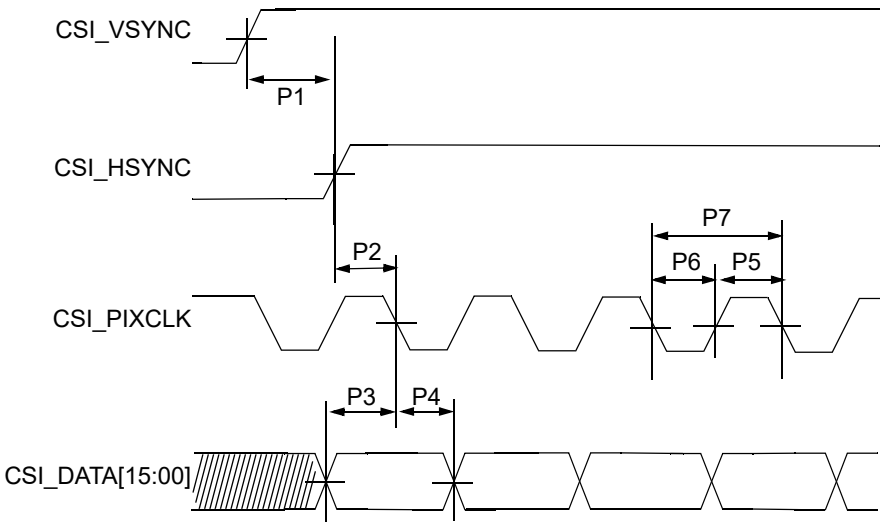


Figure 14. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 35. CSI Gated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to CSI_HSYNC time	tV2H	33.5	—	ns
P2	CSI_HSYNC setup time	tHsu	1	—	ns
P3	CSI DATA setup time	tDsu	1	—	ns
P4	CSI DATA hold time	tDh	1	—	ns
P5	CSI pixel clock high time	tCLKh	3.75	—	ns

Table 35. CSI Gated Clock Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min.	Max.	Units
P6	CSI pixel clock low time	tCLKl	3.75	—	ns
P7	CSI pixel clock frequency	fCLK	—	133.3	MHz

4.10.2.2 Ungated Clock Mode Timing

Figure 15 shows the ungated clock mode timings of CSI, and Table 36 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the CSI_VSYNC and CSI_PIXCLK signals are used, and the CSI_HSYNC signal is ignored.

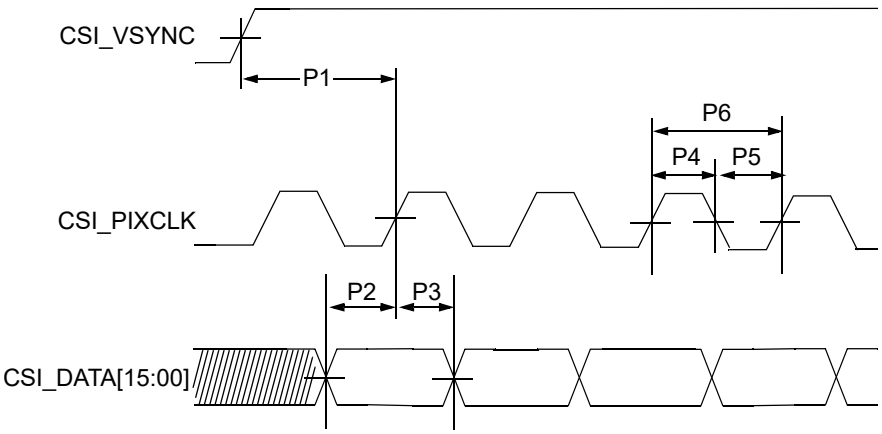


Figure 15. CSI Ungated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

Table 36. CSI Ungated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI_VSYNC to pixel clock time	tVSYNC	33.5	—	ns
P2	CSI DATA setup time	tDsu	1	—	ns
P3	CSI DATA hold time	tDh	1	—	ns
P4	CSI pixel clock high time	tCLKh	3.75	—	ns
P5	CSI pixel clock low time	tCLKl	3.75	—	ns
P6	CSI pixel clock frequency	fCLK	—	133.3	MHz

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

4.10.3 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI block. The ECSPI has separate timing parameters for master and slave modes.

4.10.3.1 ECSPI Master Mode Timing

Figure 16 depicts the timing of ECSPI in master mode and Table 37 lists the ECSPI master mode timing characteristics.

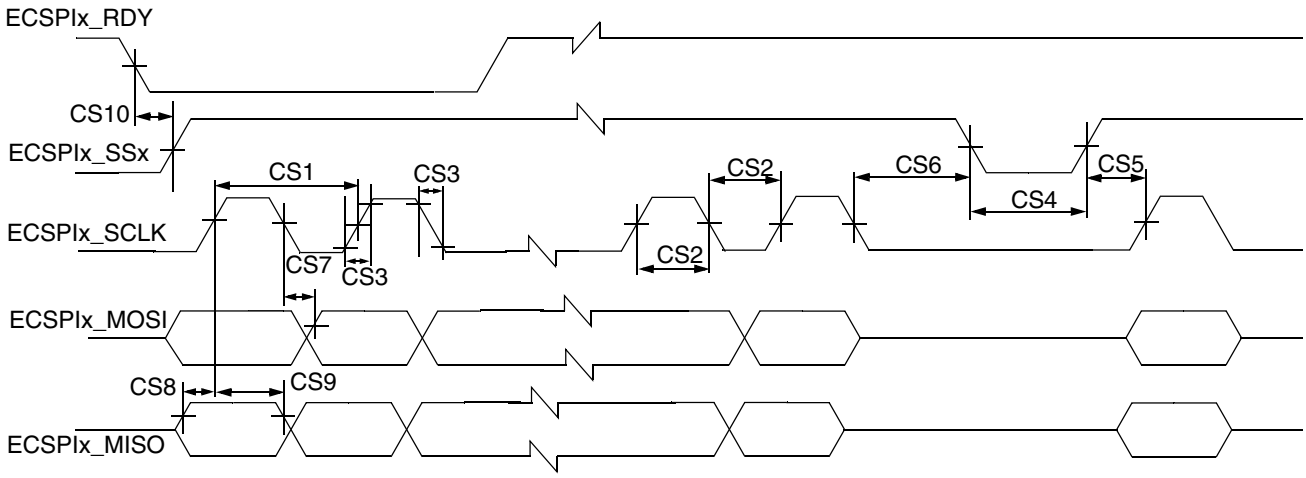


Figure 16. ECSPI Master Mode Timing Diagram

Table 37. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK Cycle Time–Write	t_{clk}	 46 40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK High or Low Time–Write	t_{SW}	 22 20 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[3]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half ECSPIx period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	Half ECSPI_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-0.5	2	ns
CS8	ECSPIx_MISO Setup Time • Slow group[1] • Fast group[2]	t_{Smiso}	— 14 12	—	ns

Table 37. ECSPI Master Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	ECSPIx_RDY to ECSPIx_SSx Time[4]	t_{SDRY}	5	—	ns

1 ECSPI slow group includes:
ECSPI2/EPDC_SDLE, ECSPI3/EPDC_D9, ECSPI4/EPDC_D1

2 ECSPI fast group includes:
ECSPI1/LCD_DATA01, ECSPI1/ECSPI1_MISO, ECSPI2/LCD_DATA10, ECSPI2/ECSPI2_MISO, ECSPI3/AUDx_TXC, ECSPI3/SD2_DAT1, ECSPI4/KEY_ROW1, ECSPI4

3 See specific I/O AC parameters Section 4.7, I/O AC Parameters."

4 ECSPIx_RDY is sampled internally by ipg_clk and is asynchronous to all other eCSPI signals.

4.10.3.2 ECSPI Slave Mode Timing

Figure 17 depicts the timing of ECSPI in slave mode and Table 38 lists the ECSPI slave mode timing characteristics.

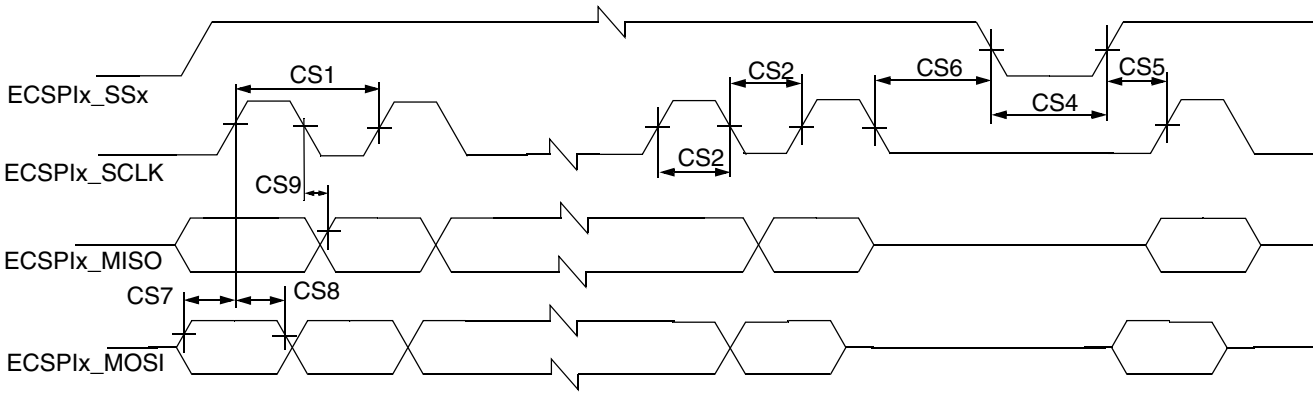


Figure 17. ECSPI Slave Mode Timing Diagram

Table 38. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	20 7	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	17	ns

4.10.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4/4.41/5.0 (Dual Date Rate) timing.

4.10.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 18 depicts the timing of SD/eMMC4.3, and Table 39 lists the SD/eMMC4.3 timing characteristics.

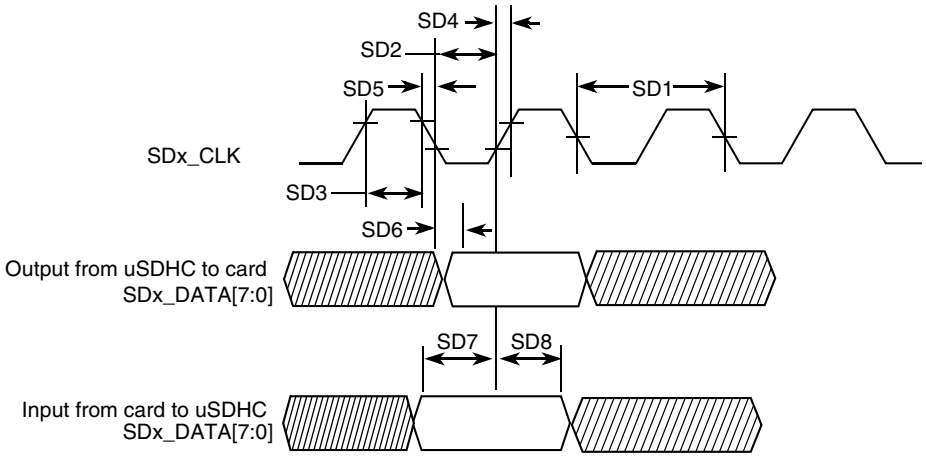


Figure 18. SD/eMMC4.3 Timing

Table 39. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock frequency (low speed)	f_{PP}[1]	0	400	kHz
	Clock frequency (sd/sdio full speed/high speed)	f_{PP}[2]	0	25/50	MHz
	Clock frequency (mmc full speed/high speed)	f_{PP}[3]	0	20/52[4]	MHz
	Clock frequency (identification mode)	f_{OD}	100	400	kHz
SD2	Clock low time	t_{WL}	7	—	ns
SD3	Clock high time	t_{WH}	7	—	ns
SD4	Clock rise time	t_{TLH}	—	3	ns
SD5	Clock fall time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs SDx_CMD, SDx_DATAx (Reference to CLK)					
SD6	eSDHC output delay	t_{OD}	–6.6	3.6	ns
eSDHC Input/Card Outputs SDx_CMD, SDx_DATAx (Reference to CLK)					

Table 39. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD7	eSDHC input setup time	t_{ISU}	2.5	—	ns
SD8	eSDHC input hold time[5]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 uSDHC3 dat4 ~ dat7 have two pad groups. The first group use SD2 pad and run at 52 MHz for output. The second group use KEY pad and only run at 50 MHz for output.

5 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.10.4.2 eMMC4.4/4.41 (Dual Data Rate) eSDHCv3 AC Timing

Figure 19 depicts the timing of eMMC4.4/4.41. Table 40 lists the eMMC4.4/4.41 timing characteristics. Be aware that only SDx_DATAx is sampled on both edges of the clock (not applicable to SDx_CMD).

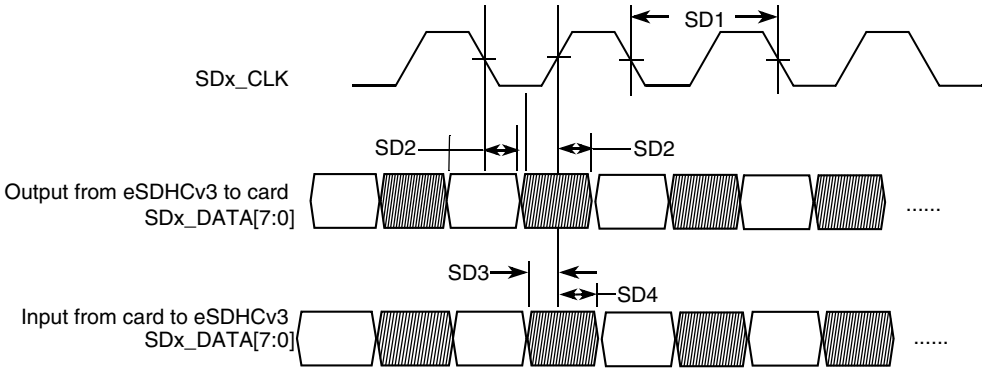


Figure 19. eMMC4.4/4.41 Timing

Table 40. eMMC4.4/4.41 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SD_DATAx (Reference to CLK)					
SD2	uSDHC output delay	t_{OD}	2.8	6.8	ns
uSDHC Input / Card Outputs SD_CMD, SD_DATAx (Reference to CLK)					
SD3	uSDHC input setup time	t_{ISU}	1.7	—	ns
SD4	uSDHC input hold time	t_{IH}	1.5	—	ns

4.10.4.3 SDR50/SDR104 AC Timing

Figure 20 depicts the timing of SDR50/SDR104, and Table 39 lists the SDR50/SDR104 timing characteristics.

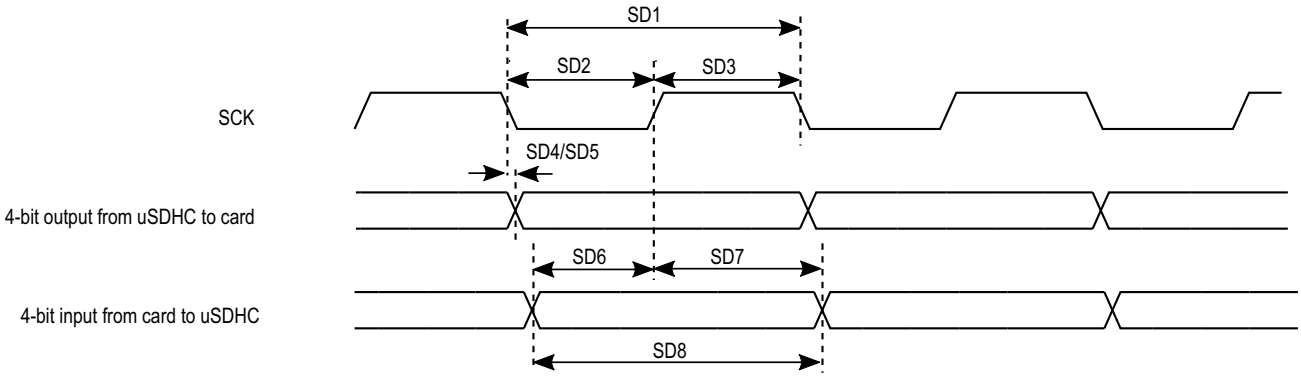


Figure 20. SDR50/SDR104 Timing

Table 41. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1]Data window in SDR104 mode is variable.

4.10.4.4 HS200 Mode Timing

Figure 21 depicts the timing of HS200 mode, and Table 42 lists the HS200 timing characteristics.

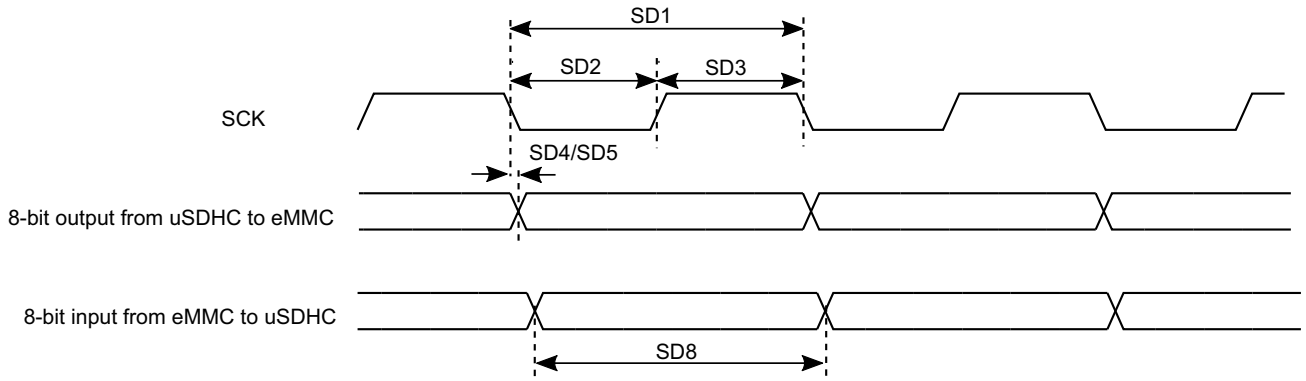


Figure 21. HS200 Mode Timing

Table 42. HS200 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock frequency period	t_{CLK}	5.0	—	ns
SD2	Clock low time	t_{CL}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
SD3	Clock high time	t_{CH}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC output delay[1]	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[2]					
SD8	Card output data window	t_{ODW}	0.5 × t_{CLK}	—	ns

1 If using KEY_COL1, KEY_ROW1, KEY_COL2 and KEY_ROW2 for SD3_DATA4–SD3_DATA7, note the difference in timing: t_{od} minimum is -1.8 and t_{od} maximum is 0.5.

2 HS200 is for 8 bits while SDR104 is for 4 bits.

4.10.4.5 HS400 DDR AC Timing—eMMC5.0 only

Figure 22 depicts the timing of HS400 mode, and Table 43 lists the HS400 timing characteristics. Be aware that only data is sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for SDR104 mode. Check

SD5, SD6, and SD7 parameters in Table 41 SDR50/SDR104 Interface Timing Specification for CMD input/output timing for HS400 mode.

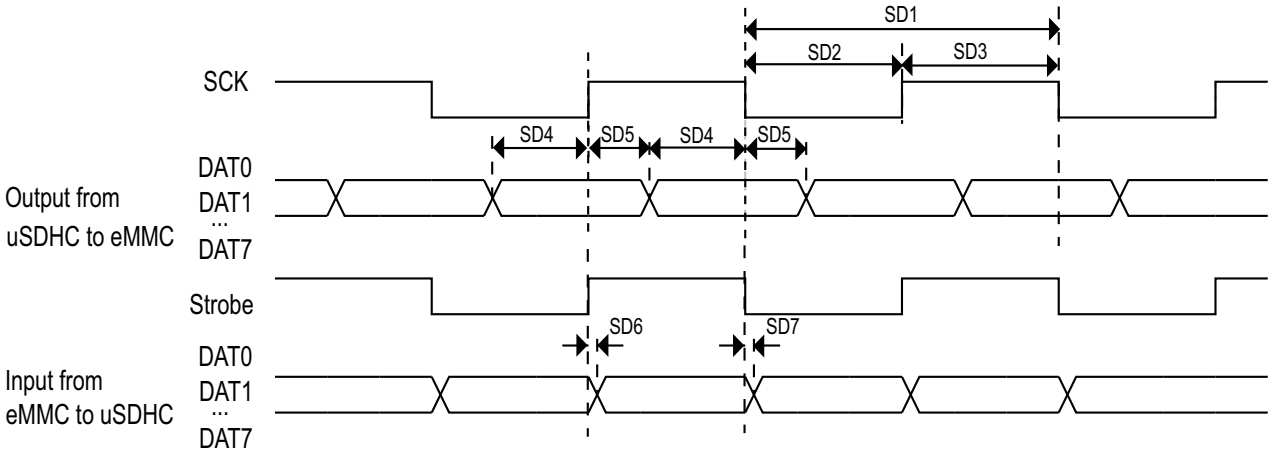


Figure 22. HS400 Mode Timing

Table 43. HS400 Interface Timing Specification[1]

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock frequency	f_{PP}	0	150	MHz
SD2	Clock low time	t_{CL}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
SD3	Clock high time	t_{CH}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
uSDHC Output/Card Inputs DAT (Reference to SCK)					
SD4	Output skew from data of edge of SCK	t_{OSkew1}	0.45		ns
SD5	Output skew from edge of SCk to data	t_{OSkew2}	0.45		ns
uSDHC Input/Card Outputs DAT (Reference to Strobe)					
SD6	uSDHC input skew	t_{RQ}		0.45	ns
SD7	uSDHC hold skew	t_{RQH}		0.45	ns

1 Do not support HS400 mode if using KEY pad for SD3_DATA4 ~ SD3DATA7.

4.10.5 I²C Bus Characteristics

The Inter-Integrated Circuit (I^2C) provides functionality of a standard I^2C slave and master. The I^2C is designed to be compatible with the I^2C Bus Specification, Version 2.1, by Philips Semiconductor.

4.10.6 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMn_OUT) external pin (see external signals table in the *i.MX 6SLL Reference Manual* for PWM pin assignments).

Figure 23 depicts the timing of the PWM, and Table 44 lists the PWM timing parameters.

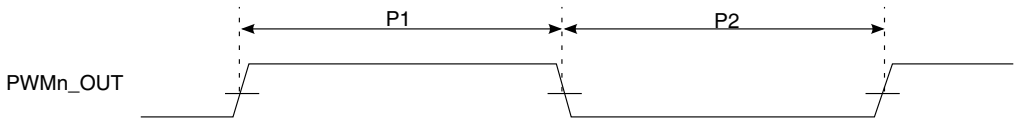


Figure 23. PWM Timing

Table 44. PWM Output Timing Parameters

Reference Number	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	66	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	9.1591	—	ns

4.10.7 LCD Controller (LCDIF) Parameters

Figure 24 shows the LCDIF timing and Table 45 lists the timing parameters.

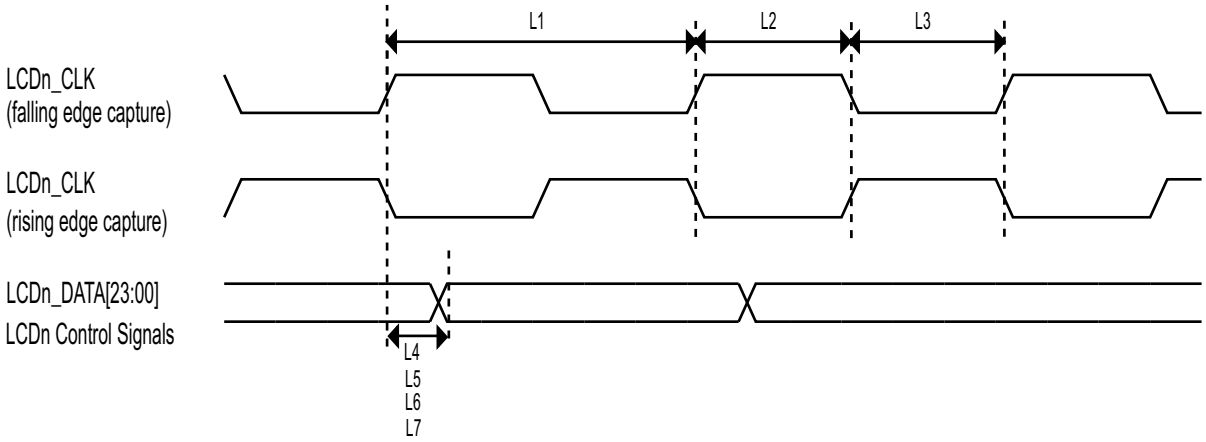


Figure 24. LCD Timing

Table 45. LCD Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
L1	LCD pixel clock frequency	tCLK(LCD)	—	150	MHz
L2	LCD pixel clock high (falling edge capture)	tCLKH(LCD)	3	—	ns
L3	LCD pixel clock low (rising edge capture)	tCLKL(LCD)	3	—	ns
L4	LCD pixel clock high to data valid (falling edge capture)	td(CLKH-DV)	-1	1	ns
L5	LCD pixel clock low to data valid (rising edge capture)	td(CLKL-DV)	-1	1	ns
L6	LCD pixel clock high to control signal valid (falling edge capture)	td(CLKH-CTRLV)	-1	1	ns
L7	LCD pixel clock low to control signal valid (rising edge capture)	td(CLKL-CTRLV)	-1	1	ns

4.10.7.1 LCDIF signal mapping

Table 46 lists the details about the mapping signals.

Table 46. LCD Signal Parameters

Pin name	8-bit DOTCLK LCD IF	16-bit DOTCLK LCD IF	18-bit DOTCLK LCD IF	24-bit DOTCLK LCD IF	8-bit DVI LCD IF
LCD_RS	—	—	—	—	CCIR_CLK
LCD_VSYNC* (Two options)	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	—
LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	—
LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	—
LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	—
LCD_D23	—	—	—	R[7]	—
LCD_D22	—	—	—	R[6]	—
LCD_D21	—	—	—	R[5]	—
LCD_D20	—	—	—	R[4]	—
LCD_D19	—	—	—	R[3]	—
LCD_D18	—	—	—	R[2]	—
LCD_D17	—	—	R[5]	R[1]	—
LCD_D16	—	—	R[4]	R[0]	—
LCD_D15 / VSYNC*	—	R[4]	R[3]	G[7]	—
LCD_D14 / HSYNC**	—	R[3]	R[2]	G[6]	—
LCD_D13 / LCD_DOTCLK **	—	R21]	R[1]	G[5]	—

Table 46. LCD Signal Parameters (continued)

LCD_D12 / ENABLE**	—	R[1]	R[0]	G[4]	—
LCD_D11	—	R[0]	G[5]	G[3]	—
LCD_D10	—	G[5]	G[4]	G[2]	—
LCD_D9	—	G[4]	G[3]	G[1]	—
LCD_D8	—	G[3]	G[2]	G[0]	—
LCD_D8	—	G[3]	G[2]	G[0]	—
LCD_D7	R[2]	G[2]	G[1]	B[7]	Y/C[7]
LCD_D6	R[1]	G[1]	G[0]	B[6]	Y/C[6]
LCD_D5	R[0]	G[0]	B[5]	B[5]	Y/C[5]
LCD_D4	G[2]	B[4]	B[4]	B[4]	Y/C[4]
LCD_D3	G[1]	B[3]	B[3]	B[3]	Y/C[3]
LCD_D2	G[0]	B[2]	B[2]	B[2]	Y/C[2]
LCD_D1	B[1]	B[1]	B[1]	B[1]	Y/C[1]
LCD_D0	B[0]	B[0]	B[0]	B[0]	Y/C[0]
LCD_RESET	LCD_RESET	LCD_RESET	LCD_RESET	LCD_RESET	—
LCD_BUSY / LCD_VSYNC	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	LCD_BUSY (or optional LCD_VSYNC)	—

4.10.8 SCAN JTAG Controller (SJC) Timing Parameters

Figure 25 depicts the SJC test clock input timing. Figure 26 depicts the SJC boundary scan timing. Figure 27 depicts the SJC test access port. Signal parameters are listed in Table 47.

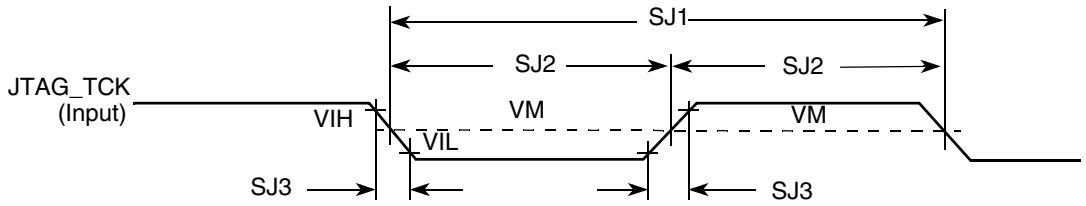


Figure 25. Test Clock Input Timing Diagram

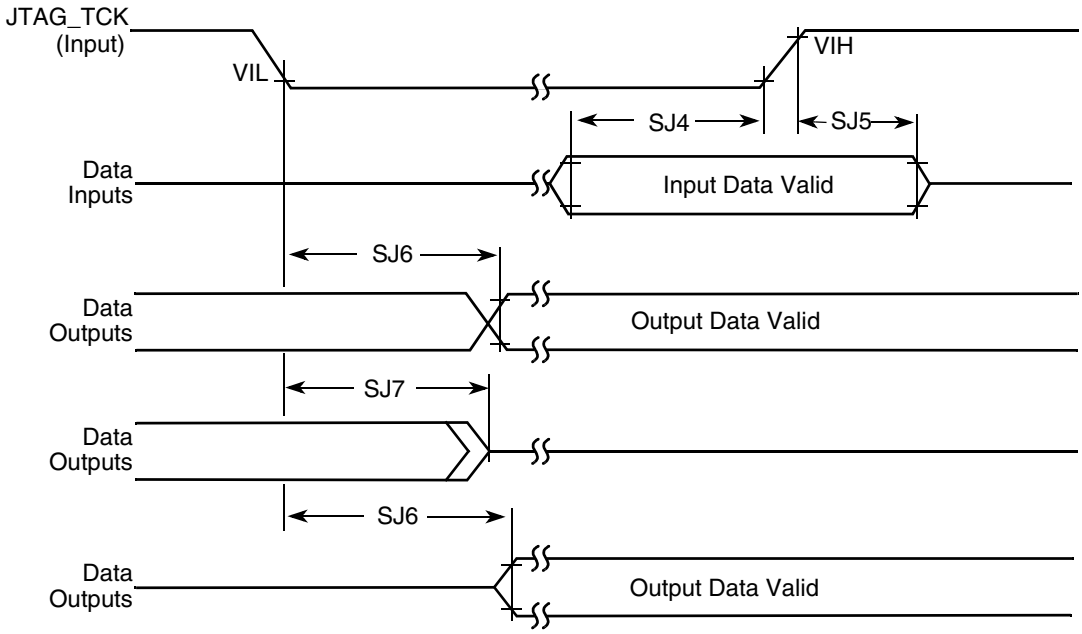


Figure 26. Boundary Scan (JTAG) Timing Diagram

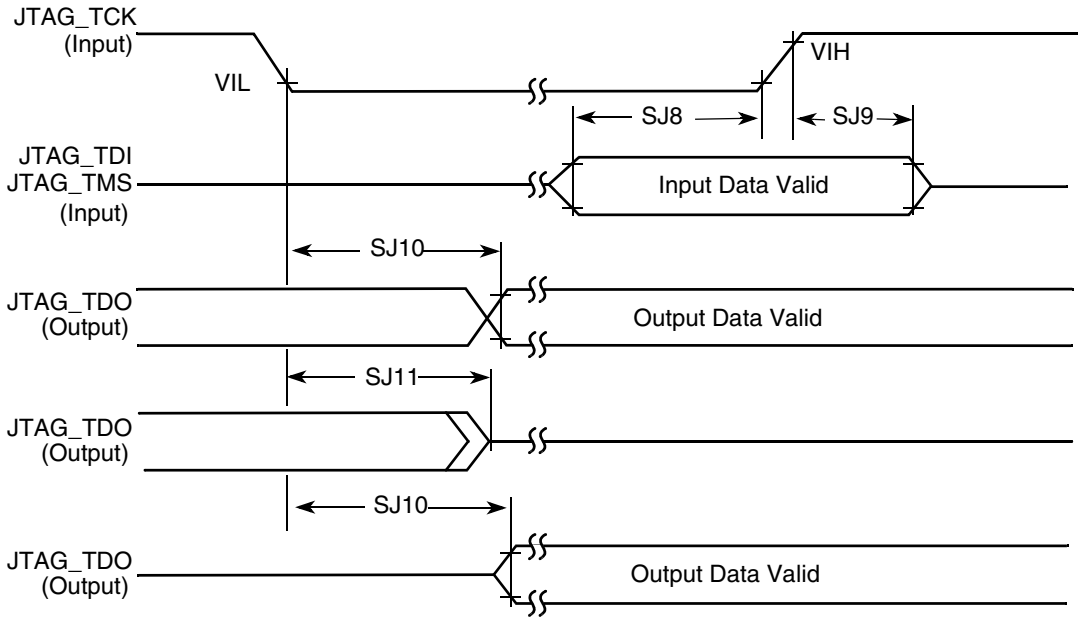


Figure 27. Test Access Port Timing Diagram

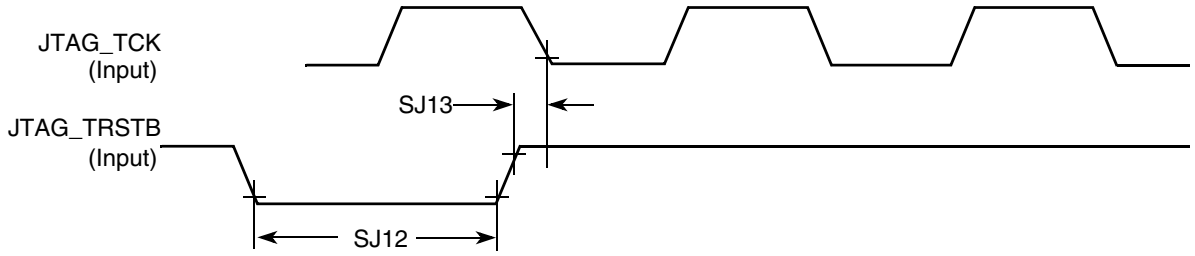


Figure 28. $\overline{\text{TRST}}$ Timing Diagram

Table 47. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRSTB assert time	100	—	ns
SJ13	JTAG_TRSTB set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.10.9 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 48 and Figure 29 and Figure 30 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 48. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

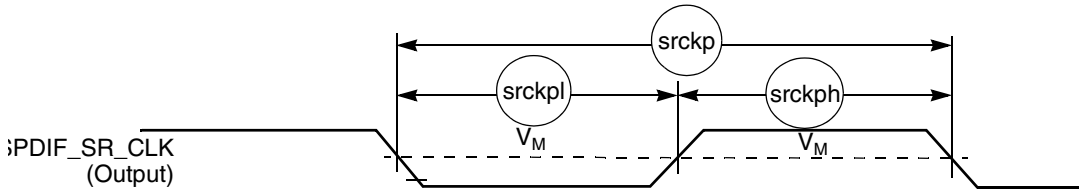


Figure 29. SRCK Timing Diagram

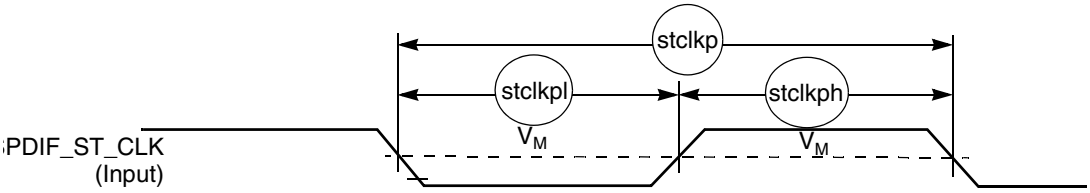


Figure 30. STCLK Timing Diagram

4.10.10 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in Table 49.

Table 49. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External – AUD3 I/O
AUDMUX port 4	AUD4	External – I2C2 and LCD, or ECSPI1, or SD2 I/O through IOMUXC
AUDMUX port 5	AUD5	External – EPDC or SD3 I/O through IOMUXC
AUDMUX port 6	AUD6	External – KEY_ROW and KEY_COL through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).

4.10.10.1 SSI Transmitter Timing with Internal Clock

Figure 31 depicts the SSI transmitter internal clock timing and Table 50 lists the timing parameters for the SSI transmitter internal clock.

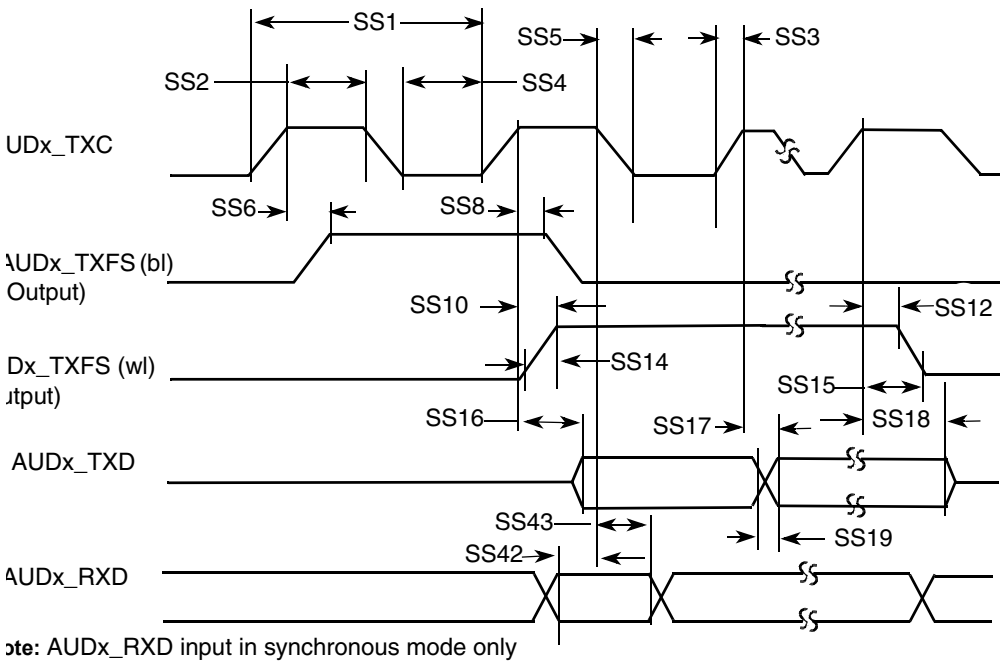


Figure 31. SSI Transmitter Internal Clock Timing Diagram

Table 50. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS6	AUDx_TXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS8	AUDx_TXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS10	AUDx_TXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS12	AUDx_TXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS14	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS rise time	—	6.0	ns
SS15	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS fall time	—	6.0	ns
SS16	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS17	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS18	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns
Synchronous Internal Clock Operation				
SS42	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS43	AUDx_RXD hold after AUDx_TXC falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TXC/RXC = 0) and a non-inverted frame sync (TXFS/RXFS = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal TXC/RXC and/or the frame sync TXFS/RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is used for data transfer.
- The terms, WL and BL, refer to Word Length(WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of TXD (for example, during AC97 mode of operation).

4.10.10.2 SSI Receiver Timing with Internal Clock

Figure 32 depicts the SSI receiver internal clock timing and Table 51 lists the timing parameters for the receiver timing with the internal clock.

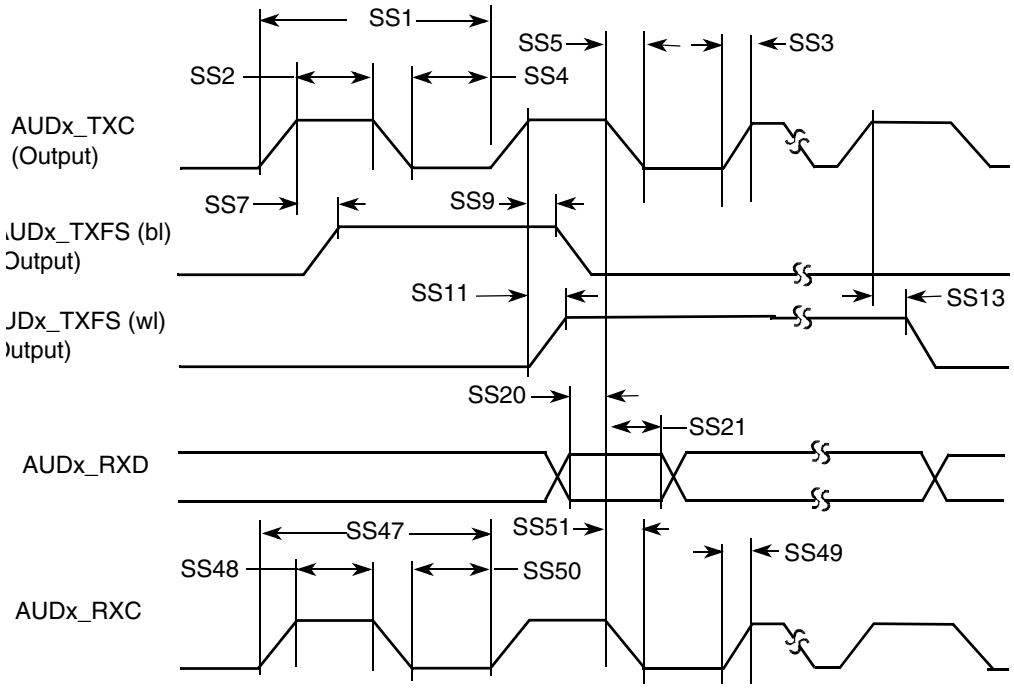


Figure 32. SSI Receiver Internal Clock Timing Diagram

Table 51. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS3	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS5	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS7	AUDx_RXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS9	AUDx_RXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS11	AUDx_RXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS13	AUDx_RXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS20	AUDx_RXD setup time before AUDx_RXC low	10.0	—	ns
SS21	AUDx_RXD hold time after AUDx_RXC low	0.0	—	ns

Table 51. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TXC/RXC = 0) and a non-inverted frame sync (TXFS/RXFS = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal TXC/RXC and/or the frame sync TXFS/RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length(WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of TXD (for example, during AC97 mode of operation).

4.10.10.3 SSI Transmitter Timing with External Clock

Figure 33 depicts the SSI transmitter external clock timing and Table 52 lists the timing parameters for the transmitter timing with the external clock.

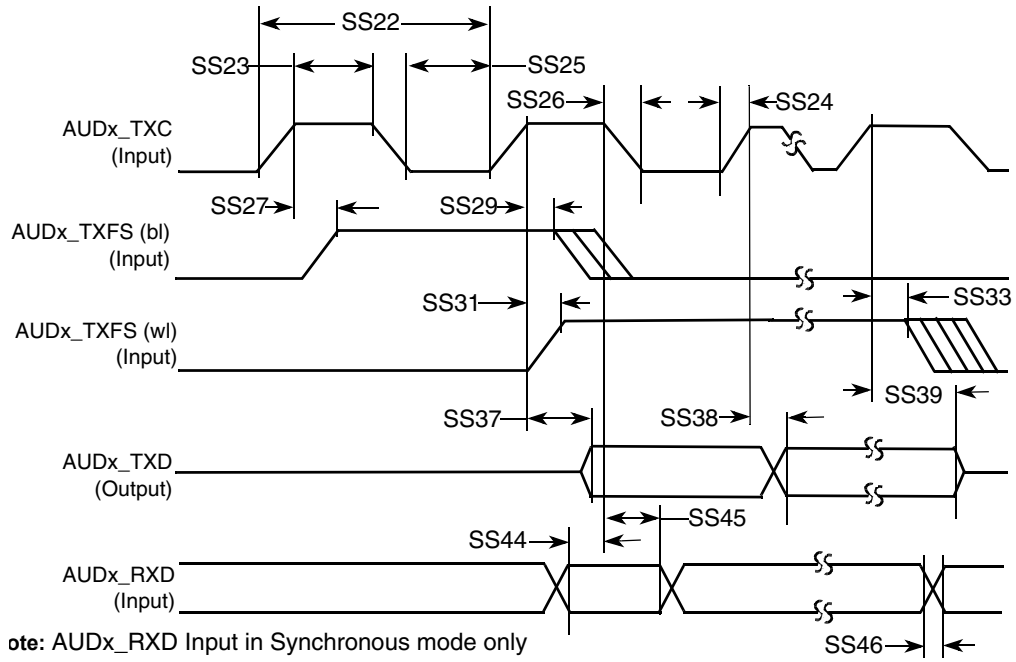


Figure 33. SSI Transmitter External Clock Timing Diagram

Table 52. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS27	AUDx_TXC high to AUDx_TXFS (bl) high	–10.0	15.0	ns
SS29	AUDx_TXC high to AUDx_TXFS (bl) low	10.0	—	ns
SS31	AUDx_TXC high to AUDx_TXFS (wl) high	–10.0	15.0	ns
SS33	AUDx_TXC high to AUDx_TXFS (wl) low	10.0	—	ns
SS37	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS38	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS39	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS45	AUDx_RXD hold after AUDx_TXC falling	2.0	—	ns
SS46	AUDx_RXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TXC/RXC = 0) and a non-inverted frame sync (TXFS/RXFS = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal TXC/RXC and/or the frame sync TXFS/RXFS shown in the tables and in the figures.
- All timings are on AUDMUX Pads when SSI is used for data transfer.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of TXD (for example, during AC97 mode of operation).

4.10.10.4 SSI Receiver Timing with External Clock

Figure 34 depicts the SSI receiver external clock timing and Table 53 lists the timing parameters for the receiver timing with the external clock.

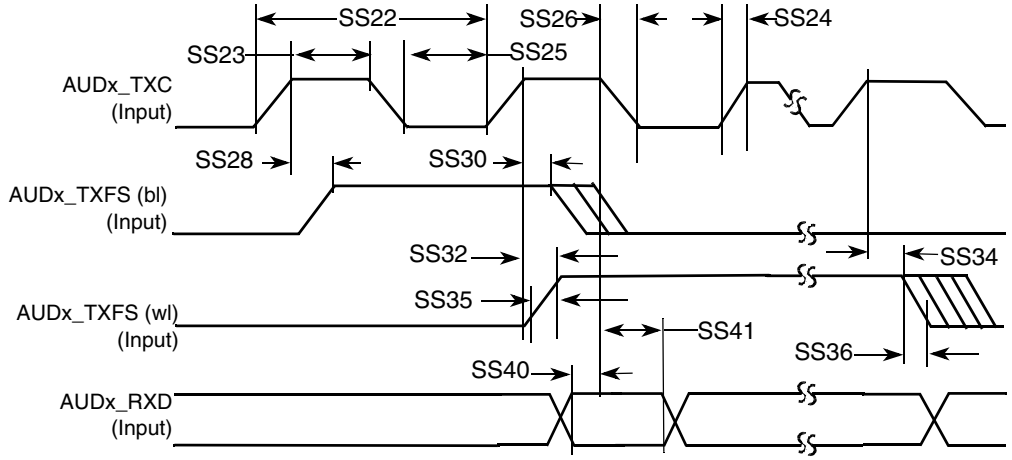


Figure 34. SSI Receiver External Clock Timing Diagram

Table 53. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS28	AUDx_RXC high to AUDx_TXFS (bl) high	–10	15.0	ns
SS30	AUDx_RXC high to AUDx_TXFS (bl) low	10	—	ns

Table 53. SSI Receiver Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS32	AUDx_RXC high to AUDx_TXFS (wl) high	–10	15.0	ns
SS34	AUDx_RXC high to AUDx_TXFS (wl) low	10	—	ns
SS35	AUDx_TXC/AUDx_RXC External AUDx_TXFS rise time	—	6.0	ns
SS36	AUDx_TXC/AUDx_RXC External AUDx_TXFS fall time	—	6.0	ns
SS40	AUDx_RXD setup time before AUDx_RXC low	10	—	ns
SS41	AUDx_RXD hold time after AUDx_RXC low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TXC/RXC=0) and a non-inverted frame sync (TXFS/RXFS=0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal TXC/RXC and/or the frame sync TXFS/RXFS shown in the tables and in the figures.
- All timings are on AUDMUX Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length(WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of TXD (for example, during AC97 mode of operation).

4.10.11 UART I/O Configuration and Timing Parameters

4.10.11.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6SLL UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 – DCE mode). Table 54 shows the UART I/O configuration based on the enabled mode.

Table 54. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UART_RTS_B	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
UART_CTS_B	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
UART_DTR_B	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
UART_DSR_B	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
UART_DCD_B	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
UART_RI_B	Input	RING from DCE to DTE	Output	RING from DCE to DTE

Table 54. UART I/O Configuration vs. Mode (continued)

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UART_TX_DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UART_RX_DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.10.11.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.10.11.2.1 UART Transmitter

Figure 35 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 55 lists the UART RS-232 serial mode transmit timing characteristics.

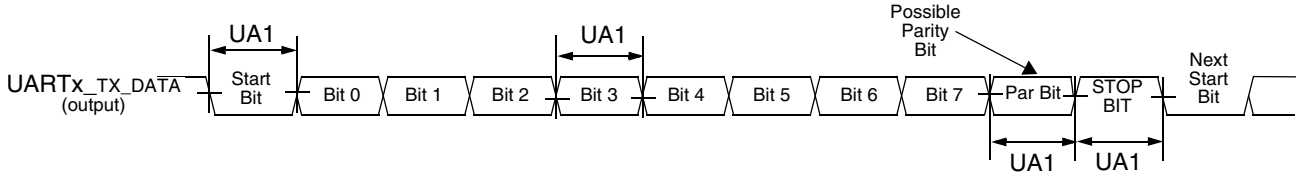


Figure 35. UART RS-232 Serial Mode Transmit Timing Diagram

Table 55. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART Receiver

Figure 36 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 56 lists serial mode receive timing characteristics.

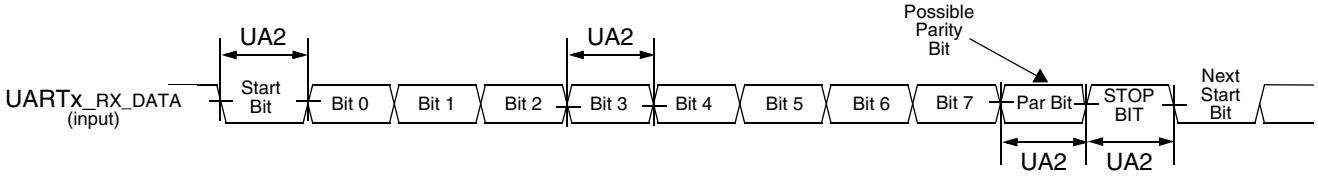


Figure 36. UART RS-232 Serial Mode Receive Timing Diagram

Table 56. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.10.11.2.2 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 37 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 57 lists the transmit timing characteristics.

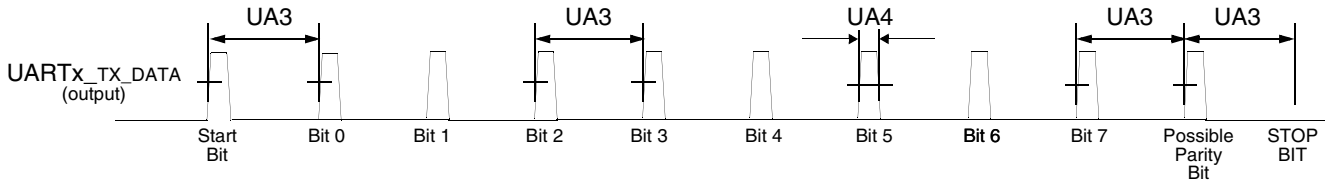


Figure 37. UART IrDA Mode Transmit Timing Diagram

Table 57. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 38 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 58 lists the receive timing characteristics.

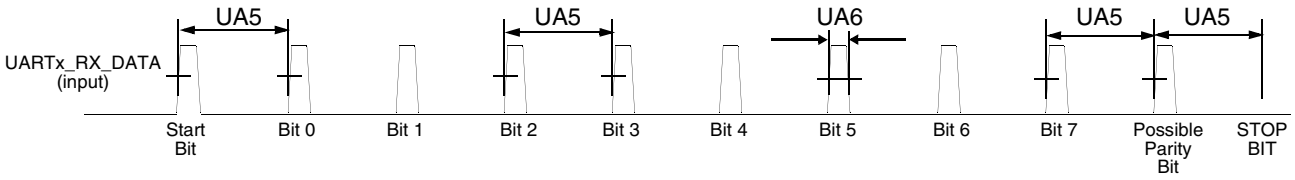


Figure 38. UART IrDA Mode Receive Timing Diagram

Table 58. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.10.12 USB PHY Parameters

This section describes the USB-OTG PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG.

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 59 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6SLL Fuse Map document and the System Boot chapter of the *i.MX 6SLL Reference Manual*.

Table 59. Fuses and Associated Pins Used for Boot

Ball Name	Direction at Reset	eFuse Name
Boot Mode Selection		
BOOT_MODE1	Input	Boot Mode Selection
BOOT_MODE0	Input	Boot Mode Selection
Boot Options[1]		
LCD_DAT0	Input	BOOT_CFG1[0]
LCD_DAT1	Input	BOOT_CFG1[1]
LCD_DAT2	Input	BOOT_CFG1[2]
LCD_DAT3	Input	BOOT_CFG1[3]
LCD_DAT4	Input	BOOT_CFG1[4]
LCD_DAT5	Input	BOOT_CFG1[5]
LCD_DAT6	Input	BOOT_CFG1[6]
LCD_DAT7	Input	BOOT_CFG1[7]
LCD_DAT8	Input	BOOT_CFG2[0]
LCD_DAT09	Input	BOOT_CFG2[1]
LCD_DAT10	Input	BOOT_CFG2[2]
LCD_DAT11	Input	BOOT_CFG2[3]
LCD_DAT12	Input	BOOT_CFG2[4]
LCD_DAT13	Input	BOOT_CFG2[5]
LCD_DAT14	Input	BOOT_CFG2[6]
LCD_DAT15	Input	BOOT_CFG2[7]
LCD_DAT16	Input	BOOT_CFG4[0]
LCD_DAT17	Input	BOOT_CFG4[1]
LCD_DAT18	Input	BOOT_CFG4[2]

Table 59. Fuses and Associated Pins Used for Boot (continued)

Ball Name	Direction at Reset	eFuse Name
LCD_DAT19	Input	BOOT_CFG4[3]
LCD_DAT20	Input	BOOT_CFG4[4]
LCD_DAT21	Input	BOOT_CFG4[5]
LCD_DAT22	Input	BOOT_CFG4[6]
LCD_DAT23	Input	BOOT_CFG4[7]

[1] Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.

5.2 Boot Devices Interfaces Allocation

Table 60 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 60. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Ball Names During Boot	Comment
SPI	ECSPI-1	ECSPI1_MISO, ECSPI1_MOSI, ECSPI1_SCLK, ECSPI1_SS0, I2C1_SCL, I2C1_SDA, ECSPI2_SS0	—
SPI	ECSPI-2	ECSPI2_MISO, ECSPI2_MOSI, ECSPI2_SCLK, ECSPI2_SS0, EPDC_SDCE0, EPDC_GDCLK, EPDC_GDOE	—
SPI	ECSPI-3	EPDC_D9, EPDC_D8, EPDC_D11, EPDC_D10, EPDC_D12, EPDC_D13, EPDC_D14	—
SPI	ECSPI-4	EPDC_D1, EPDC_D0, EPDC_D3, EPDC_D2, EPDC_D2, EPDC_D5, EPDC_D6	—
SD/MMC	USDHC-1	SD1_CLK, SD1_CMD,SD1_DAT0, SD1_DAT1, SD1_DAT2, SD1_DAT3, SD1_DAT4, SD1_DAT5, SD1_DAT6, SD1_DAT7, GPIO3_IO30, GPIO4_IO7, ECSPI2_MOSI	1, 4, or 8 bit Fastboot
SD/MMC	USDHC-2	SD2_CLK, SD2_CMD, SD2_DAT0, SD2_DAT1, SD2_DAT2, SD2_DAT3, SD2_DAT4, SD2_DAT5, SD2_DAT6, SD2_DAT7, SD2_RST, ECSPI1_MOSI	1, 4, or 8 bit Fastboot
SD/MMC	USDHC-3	SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, GPIO3_IO26, GPIO3_IO27, GPIO3_IO28, GPIO3_IO29, GPIO4_IO4, GPIO4_IO5	1, 4, or 8 bit Fastboot
USB	USB_OTG1_PHY	USB_OTG1_DP USB_OTG1_DN USB_OTG1_VBUS USB_OTG1_CHD_B	—

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 14 x 14 mm Package Information

6.1.1 14 x 14 mm, 0.65 mm Pitch, 24 x 24 Ball Matrix

Figure 39 shows the top, bottom, and side views of the 14 × 14 mm BGA package.

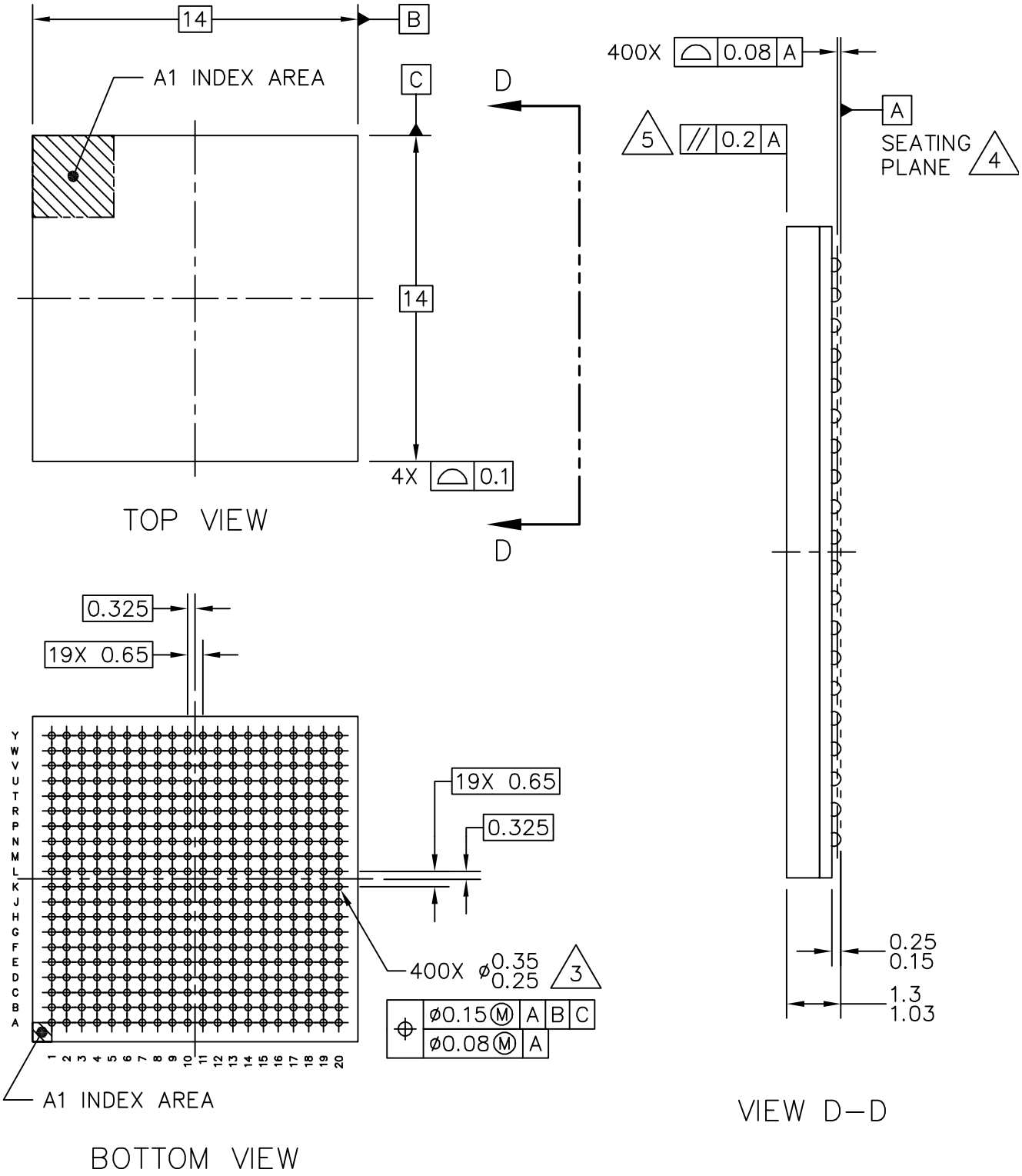


Figure 39. 14 x 14, 0.65 mm BGA Package Top, Bottom, and Side Views

Table 62 shows the 14 x 14 mm BGA package details.

Table 62. 14 x 14, 0.65 mm BGA Package Details

Parameter	Symbol	Common Dimensions		
		Minimum	Normal	Maximum
Total Thickness	A	1.03	—	1.30
Stand Off	A1	0.15	—	0.25
Substrate Thickness	A2		0.25	
Mold Thickness	A3		0.7	
Body Size	D		14	
	E		14	
Ball Diameter	—		0.3	
Ball Opening	—		0.3	
Ball Width	b	0.25	—	0.35
Ball Pitch	e		0.65	
Ball Count	n	400	—	—
Edge Ball Center to Center	D1		—	
	E1		—	
Body Center to Contact Ball	SD		0.65	
	SE		0.65	
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.2	
Coplanarity	ddd		0.08	
Ball Offset (Package)	eee		0.15	
Ball Offset (Ball)	fff		0.08	

6.1.2 14 x 14 mm Ground, Power, Sense, Not Connected and Reference Contact Assignments

Table 63 shows the device connection list for ground, power, sense, and reference contact signals.

Table 63. 14 x 14 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
DRAM_VREF	K4	—
GND	A1, A7, A13, A20, B3, D4, D17, E5, E6, E9, E12, E15, E16, F5, F16, G1, G7, G8, G9, G10, G11, G12, G13, G14, G20, H3, H5, H7, H14, J5, J7, J14, J16, K7, K9, K10, K11, k12, K14, L5, L7, L9, L10, L11, L12, L14, M5, M7, M14, N3, N7, N14, P1, P5, P7, P8, P9, P10, P11, P12, P13, P14, P16, P20, R5, R16, T4, T6, T7, T15, V3, V12, Y1, Y4, Y7, Y11, Y15, Y20	—
GPANAIO	T16	Analog output for NXP only. This output must always be left unconnected.
NGND_KEL0	T14	—
NVCC_1V8	E7, E8, E13, E14, G16, H16, M16, N16, R7, R8	—
NVCC_3V3	F7, F8, F9, F10, F11, F12, F13, F14, F15, G15, H15, J15, K15, L15, M15, N15, P15, R9, R10, R11, R12, R13, R14, R15	—
NVCC_DRAM	G5, G6, H6, J6, K5, L6, M6, N5, N6, P6	Supply of the DDR interface
NVCC_DRAM_2P5	F6, K6, R6	—
NVCC_PLL	V17	—
VDD_ARM_IN	H11, H12, H13, J11, J12, J13, K13, L13	Primary Supply for the Arm Core
VDD_HIGH_CAP	U16, V16	Secondary Supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDD_HIGH_IN	W17, Y17	Primary Supply for the 2.5 V Regulator
VDD_SNVS_CAP	U14	Secondary Supply for the SNVS (internal regulator output—requires capacitor if internal regulator is used)
VDD_SNVS_IN	V14	Primary Supply for the SNVS Regulator
VDD_SOC_IN	H8, H9, H10, J8, J9, J10, K8, L8, M8, M9, M10, M11, M12, M13, N8, N9, N10, N11, N12, N13	Primary Supply for the SoC
VDD_USB_CAP	T13	Secondary Supply for the 3V Domain (USBPHY, MLPBPHY, eFuse), internal regulator output, requires capacitor if internal regulator is used.
ZQPAD	G3	—

Table 64 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 64. 14 x 14 mm Functional Contact Assignments

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
AUD_MCLK	F17	GPIO	GPIO	ALT5	GPIO1_GPIO[6]	Not connected	Hi-Z	Hi-Z
AUD_RXC	H17	GPIO	GPIO	ALT5	GPIO1_GPIO[1]	Not connected	Hi-Z	Hi-Z
AUD_RXD	H18	GPIO	GPIO	ALT5	GPIO1_GPIO[2]	Not connected	Hi-Z	Hi-Z
AUD_RXFS	F18	GPIO	GPIO	ALT5	GPIO1_GPIO[0]	Not connected	Hi-Z	Hi-Z
AUD_TXC	G17	GPIO	GPIO	ALT5	GPIO1_GPIO[3]	Not connected	Hi-Z	Hi-Z
AUD_TXD	G18	GPIO	GPIO	ALT5	GPIO1_GPIO[5]	Not connected	Hi-Z	Hi-Z
AUD_TXFS	F19	GPIO	GPIO	ALT5	GPIO1_GPIO[4]	Not connected	Hi-Z	Hi-Z
BOOT_MODE0	W11	RESET	GPIO	ALT0	SRC.BOOT_MODE[0]	Input	PD (100K)	PD (100K)
BOOT_MODE1	T11	RESET	GPIO	ALT0	SRC.BOOT_MODE[1]	Input	PD (100K)	PD (100K)
CLK1_N	U15	ANATOP	—	—	—	—	—	—
CLK1_P	V15	ANATOP	—	—	—	—	—	—
DRAM_A0	P4	DRAM	DDR	ALT0	DRAM_A[0]	Output	0	PU (100K)
DRAM_A1	N4	DRAM	DDR	ALT0	DRAM_A[1]	Output	0	PU (100K)
DRAM_A2	M3	DRAM	DDR	ALT0	DRAM_A[2]	Output	0	PU (100K)
DRAM_A3	M4	DRAM	DDR	ALT0	DRAM_A[3]	Output	0	PU (100K)
DRAM_A4	L4	DRAM	DDR	ALT0	DRAM_A[4]	Output	0	PU (100K)
DRAM_A5	L1	DRAM	DDR	ALT0	DRAM_A[5]	Output	0	PU (100K)
DRAM_A6	L3	DRAM	DDR	ALT0	DRAM_A[6]	Output	0	PU (100K)
DRAM_A7	F4	DRAM	DDR	ALT0	DRAM_A[7]	Output	0	PU (100K)

Table 64. 14 x 14 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
DRAM_A8	H4	DRAM	DDR	ALT0	DRAM_A[8]	Output	0	PU (100K)
DRAM_A9	G4	DRAM	DDR	ALT0	DRAM_A[9]	Output	0	PU (100K)
DRAM_CS0_B	L2	DRAM	DDR	ALT0	DRAM_CS0_B	Output	0	PU (100K)
DRAM_CS1_B	K2	DRAM	DDR	ALT0	DRAM_CS1_B	Output	0	PU (100K)
DRAM_D0	T2	DRAM	DDR	ALT0	DRAM_D[0]	Input	PU (100K)	PU (100K)
DRAM_D1	T1	DRAM	DDR	ALT0	DRAM_D[1]	Input	PU (100K)	PU (100K)
DRAM_D10	K1	DRAM	DDR	ALT0	DRAM_D[10]	Input	PU (100K)	PU (100K)
DRAM_D11	J1	DRAM	DDR	ALT0	DRAM_D[11]	Input	PU (100K)	PU (100K)
DRAM_D12	H2	DRAM	DDR	ALT0	DRAM_D[12]	Input	PU (100K)	PU (100K)
DRAM_D13	F2	DRAM	DDR	ALT0	DRAM_D[13]	Input	PU (100K)	PU (100K)
DRAM_D14	F1	DRAM	DDR	ALT0	DRAM_D[14]	Input	PU (100K)	PU (100K)
DRAM_D15	G2	DRAM	DDR	ALT0	DRAM_D[15]	Input	PU (100K)	PU (100K)
DRAM_D16	W3	DRAM	DDR	ALT0	DRAM_D[16]	Input	PU (100K)	PU (100K)
DRAM_D17	Y3	DRAM	DDR	ALT0	DRAM_D[17]	Input	PU (100K)	PU (100K)
DRAM_D18	W2	DRAM	DDR	ALT0	DRAM_D[18]	Input	PU (100K)	PU (100K)
DRAM_D19	Y2	DRAM	DDR	ALT0	DRAM_D[19]	Input	PU (100K)	PU (100K)
DRAM_D2	R2	DRAM	DDR	ALT0	DRAM_D[2]	Input	PU (100K)	PU (100K)
DRAM_D20	V2	DRAM	DDR	ALT0	DRAM_D[20]	Input	PU (100K)	PU (100K)

Table 64. 14 x 14 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
DRAM_D21	W1	DRAM	DDR	ALT0	DRAM_D[21]	Input	PU (100K)	PU (100K)
DRAM_D22	U1	DRAM	DDR	ALT0	DRAM_D[22]	Input	PU (100K)	PU (100K)
DRAM_D23	V1	DRAM	DDR	ALT0	DRAM_D[23]	Input	PU (100K)	PU (100K)
DRAM_D24	E2	DRAM	DDR	ALT0	DRAM_D[24]	Input	PU (100K)	PU (100K)
DRAM_D25	E1	DRAM	DDR	ALT0	DRAM_D[25]	Input	PU (100K)	PU (100K)
DRAM_D26	D1	DRAM	DDR	ALT0	DRAM_D[26]	Input	PU (100K)	PU (100K)
DRAM_D27	C2	DRAM	DDR	ALT0	DRAM_D[27]	Input	PU (100K)	PU (100K)
DRAM_D28	B1	DRAM	DDR	ALT0	DRAM_D[28]	Input	PU (100K)	PU (100K)
DRAM_D29	C1	DRAM	DDR	ALT0	DRAM_D[29]	Input	PU (100K)	PU (100K)
DRAM_D3	R1	DRAM	DDR	ALT0	DRAM_D[3]	Input	PU (100K)	PU (100K)
DRAM_D30	B2	DRAM	DDR	ALT0	DRAM_D[30]	Input	PU (100K)	PU (100K)
DRAM_D31	A2	DRAM	DDR	ALT0	DRAM_D[31]	Input	PU (100K)	PU (100K)
DRAM_D4	P2	DRAM	DDR	ALT0	DRAM_D[4]	Input	PU (100K)	PU (100K)
DRAM_D5	N2	DRAM	DDR	ALT0	DRAM_D[5]	Input	PU (100K)	PU (100K)
DRAM_D6	M2	DRAM	DDR	ALT0	DRAM_D[6]	Input	PU (100K)	PU (100K)
DRAM_D7	N1	DRAM	DDR	ALT0	DRAM_D[7]	Input	PU (100K)	PU (100K)
DRAM_D8	J2	DRAM	DDR	ALT0	DRAM_D[8]	Input	PU (100K)	PU (100K)
DRAM_D9	H1	DRAM	DDR	ALT0	DRAM_D[9]	Input	PU (100K)	PU (100K)

Table 64. 14 x 14 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
DRAM_DQM0	P3	DRAM	DDR	ALT0	DRAM_DQM[0]	Output	0	PU (100K)
DRAM_DQM1	F3	DRAM	DDR	ALT0	DRAM_DQM[1]	Output	0	PU (100K)
DRAM_DQM2	T3	DRAM	DDR	ALT0	DRAM_DQM[2]	Output	0	PU (100K)
DRAM_DQM3	C3	DRAM	DDR	ALT0	DRAM_DQM[3]	Output	0	PU (100K)
DRAM_SDCKE0	M1	DRAM	DDR	ALT0	DRAM_SDCKE[0]	Output	0	PD (100K)
DRAM_SDCKE1	K3	DRAM	DDR	ALT0	DRAM_SDCKE[1]	Output	0	PD (100K)
DRAM_SDCLK_0	J4	DRAM	DDRCLK	ALT0	DRAM_SDCLK[0]	Output	0	Low
DRAM_SDCLK_0_B	J3	DRAM	—	—	—	—	—	—
DRAM_SDQS0	R3	DRAM	DDRCLK	ALT0	DRAM_SDQS[0]	Input	Hi-Z	Not connected
DRAM_SDQS0_B	R4	DRAM	—	—	—	—	—	—
DRAM_SDQS1	E4	DRAM	DDRCLK	ALT0	DRAM_SDQS[1]	Input	Hi-Z	Not connected
DRAM_SDQS1_B	E3	DRAM	—	—	—	—	—	—
DRAM_SDQS2	U2	DRAM	DDRCLK	ALT0	DRAM_SDQS[2]	Input	Hi-Z	Not connected
DRAM_SDQS2_B	U3	DRAM	—	—	—	—	—	—
DRAM_SDQS3	D2	DRAM	DDRCLK	ALT0	DRAM_SDQS[3]	Input	Hi-Z	Not connected
DRAM_SDQS3_B	D3	DRAM	—	—	—	—	—	—
ECSPI1_MISO	L18	GPIO	GPIO	ALT5	GPIO4_GPIO[10]	Not connected	Hi-Z	Hi-Z
ECSPI1_MOSI	M18	GPIO	GPIO	ALT5	GPIO4_GPIO[9]	Not connected	Hi-Z	Hi-Z
ECSPI1_SCLK	M17	GPIO	GPIO	ALT5	GPIO4_GPIO[8]	Not connected	Hi-Z	Hi-Z
ECSPI1_SS0	L17	GPIO	GPIO	ALT5	GPIO4_GPIO[11]	Not connected	Hi-Z	Hi-Z

Table 64. 14 x 14 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
ECSPI2_MISO	N18	GPIO	GPIO	ALT5	GPIO4_GPIO[14]	Not connected	Hi-Z	Hi-Z
ECSPI2_MOSI	P18	GPIO	GPIO	ALT5	GPIO4_GPIO[13]	Not connected	Hi-Z	Hi-Z
ECSPI2_SCLK	P17	GPIO	GPIO	ALT5	GPIO4_GPIO[12]	Not connected	Hi-Z	Hi-Z
ECSPI2_SS0	N17	GPIO	GPIO	ALT5	GPIO4_GPIO[15]	Not connected	Hi-Z	Hi-Z
EPDC_BDR0	B13	GPIO	GPIO	ALT5	GPIO2_GPIO[5]	Not connected	Hi-Z	Hi-Z
EPDC_BDR1	C13	GPIO	GPIO	ALT5	GPIO2_GPIO[6]	Not connected	Hi-Z	Hi-Z
EPDC_D0	C12	GPIO	GPIO	ALT5	GPIO1_GPIO[7]	Not connected	Hi-Z	Hi-Z
EPDC_D1	B12	GPIO	GPIO	ALT5	GPIO1_GPIO[8]	Not connected	Hi-Z	Hi-Z
EPDC_D10	D13	GPIO	GPIO	ALT5	GPIO1_GPIO[17]	Not connected	Hi-Z	Hi-Z
EPDC_D11	C11	GPIO	GPIO	ALT5	GPIO1_GPIO[18]	Not connected	Hi-Z	Hi-Z
EPDC_D12	C10	GPIO	GPIO	ALT5	GPIO1_GPIO[19]	Not connected	Hi-Z	Hi-Z
EPDC_D13	B9	GPIO	GPIO	ALT5	GPIO1_GPIO[20]	Not connected	Hi-Z	Hi-Z
EPDC_D14	A9	GPIO	GPIO	ALT5	GPIO1_GPIO[21]	Not connected	Hi-Z	Hi-Z
EPDC_D15	C9	GPIO	GPIO	ALT5	GPIO1_GPIO[22]	Not connected	Hi-Z	Hi-Z
EPDC_D2	A12	GPIO	GPIO	ALT5	GPIO1_GPIO[9]	Not connected	Hi-Z	Hi-Z
EPDC_D3	A11	GPIO	GPIO	ALT5	GPIO1_GPIO[10]	Not connected	Hi-Z	Hi-Z
EPDC_D4	B11	GPIO	GPIO	ALT5	GPIO1_GPIO[11]	Not connected	Hi-Z	Hi-Z
EPDC_D5	B10	GPIO	GPIO	ALT5	GPIO1_GPIO[12]	Not connected	Hi-Z	Hi-Z

Table 64. 14 x 14 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
EPDC_D6	A10	GPIO	GPIO	ALT5	GPIO1_GPIO[13]	Not connected	Hi-Z	Hi-Z
EPDC_D7	E11	GPIO	GPIO	ALT5	GPIO1_GPIO[14]	Not connected	Hi-Z	Hi-Z
EPDC_D8	D11	GPIO	GPIO	ALT5	GPIO1_GPIO[15]	Not connected	Hi-Z	Hi-Z
EPDC_D9	D12	GPIO	GPIO	ALT5	GPIO1_GPIO[16]	Not connected	Hi-Z	Hi-Z
EPDC_GDCLK	C8	GPIO	GPIO	ALT5	GPIO1_GPIO[31]	Not connected	Hi-Z	Hi-Z
EPDC_GDOE	A8	GPIO	GPIO	ALT5	GPIO2_GPIO[0]	Not connected	Hi-Z	Hi-Z
EPDC_GDRL	D10	GPIO	GPIO	ALT5	GPIO2_GPIO[1]	Not connected	Hi-Z	Hi-Z
EPDC_GDSP	A6	GPIO	GPIO	ALT5	GPIO2_GPIO[2]	Not connected	Hi-Z	Hi-Z
EPDC_PWRCOM	B7	GPIO	GPIO	ALT5	GPIO2_GPIO[11]	Not connected	Hi-Z	Hi-Z
EPDC_PWRCTRL0	C7	GPIO	GPIO	ALT5	GPIO2_GPIO[7]	Not connected	Hi-Z	Hi-Z
EPDC_PWRCTRL1	D9	GPIO	GPIO	ALT5	GPIO2_GPIO[8]	Not connected	Hi-Z	Hi-Z
EPDC_PWRCTRL2	B8	GPIO	GPIO	ALT5	GPIO2_GPIO[9]	Not connected	Hi-Z	Hi-Z
EPDC_PWRCTRL3	E10	GPIO	GPIO	ALT5	GPIO2_GPIO[10]	Not connected	Hi-Z	Hi-Z
EPDC_PWRINT	D8	GPIO	GPIO	ALT5	GPIO2_GPIO[12]	Not connected	Hi-Z	Hi-Z
EPDC_PWRSTAT	C6	GPIO	GPIO	ALT5	GPIO2_GPIO[13]	Not connected	Hi-Z	Hi-Z
EPDC_PWRWAKEUP	B5	GPIO	GPIO	ALT5	GPIO2_GPIO[14]	Not connected	Hi-Z	Hi-Z
EPDC_SDCE0	B6	GPIO	GPIO	ALT5	GPIO1_GPIO[27]	Not connected	Hi-Z	Hi-Z
EPDC_SDCE1	D7	GPIO	GPIO	ALT5	GPIO1_GPIO[28]	Not connected	Hi-Z	Hi-Z

Table 64. 14 x 14 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
EPDC_SDCE2	D6	GPIO	GPIO	ALT5	GPIO1_GPIO[29]	Not connected	Hi-Z	Hi-Z
EPDC_SDCE3	D5	GPIO	GPIO	ALT5	GPIO1_GPIO[30]	Not connected	Hi-Z	Hi-Z
EPDC_SDCLK	A5	GPIO	GPIO	ALT5	GPIO1_GPIO[23]	Not connected	Hi-Z	Hi-Z
EPDC_SDLE	C5	GPIO	GPIO	ALT5	GPIO1_GPIO[24]	Not connected	Hi-Z	Hi-Z
EPDC_SDOE	C4	GPIO	GPIO	ALT5	GPIO1_GPIO[25]	Not connected	Hi-Z	Hi-Z
EPDC_SDSHR	B4	GPIO	GPIO	ALT5	GPIO1_GPIO[26]	Not connected	Hi-Z	Hi-Z
EPDC_VCOM0	A4	GPIO	GPIO	ALT5	GPIO2_GPIO[3]	Not connected	Hi-Z	Hi-Z
EPDC_VCOM1	A3	GPIO	GPIO	ALT5	GPIO2_GPIO[4]	Not connected	Hi-Z	Hi-Z
GPIO4_IO16	U6	GPIO	GPIO	ALT5	GPIO4_GPIO[16]	Not connected	Hi-Z	Hi-Z
GPIO4_IO17	W4	GPIO	GPIO	ALT5	GPIO4_GPIO[17]	Not connected	Hi-Z	Hi-Z
GPIO4_IO18	Y5	GPIO	GPIO	ALT5	GPIO4_GPIO[18]	Not connected	Hi-Z	Hi-Z
GPIO4_IO19	V4	GPIO	GPIO	ALT5	GPIO4_GPIO[19]	Not connected	Hi-Z	Hi-Z
GPIO4_IO20	U5	GPIO	GPIO	ALT5	GPIO4_GPIO[20]	Not connected	Hi-Z	Hi-Z
GPIO4_IO21	U4	GPIO	GPIO	ALT5	GPIO4_GPIO[21]	Not connected	Hi-Z	Hi-Z
GPIO4_IO22	W6	GPIO	GPIO	ALT5	GPIO4_GPIO[22]	Not connected	Hi-Z	Hi-Z
GPIO4_IO23	W5	GPIO	GPIO	ALT5	GPIO4_GPIO[23]	Not connected	Hi-Z	Hi-Z
GPIO4_IO24	Y6	GPIO	GPIO	ALT5	GPIO4_GPIO[24]	Not connected	Hi-Z	Hi-Z
GPIO4_IO25	V5	GPIO	GPIO	ALT5	GPIO4_GPIO[25]	Not connected	Hi-Z	Hi-Z

Table 64. 14 x 14 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
GPIO4_IO26	V6	GPIO	GPIO	ALT5	GPIO4_GPIO[26]	Not connected	Hi-Z	Hi-Z
I2C1_SCL	Y9	GPIO	GPIO	ALT5	GPIO3_GPIO[12]	Not connected	Hi-Z	Hi-Z
I2C1_SDA	W9	GPIO	GPIO	ALT5	GPIO3_GPIO[13]	Not connected	Hi-Z	Hi-Z
I2C2_SCL	B14	GPIO	GPIO	ALT5	GPIO3_GPIO[14]	Not connected	Hi-Z	Hi-Z
I2C2_SDA	A14	GPIO	GPIO	ALT5	GPIO3_GPIO[15]	Not connected	Hi-Z	Hi-Z
JTAG_MOD	T9	GPIO	GPIO	ALT0	SJC.MOD	Input	PU (100K)	PU (100K)
JTAG_TCK	V9	GPIO	GPIO	ALT0	SJC.TCK	Input	PU (47K)	PU (47K)
JTAG_TDI	U8	GPIO	GPIO	ALT0	SJC.TDI	Input	PU (47K)	PU (47K)
JTAG_TDO	V10	GPIO	GPIO	ALT0	SJC.TDO	Input	0	Input keeper
JTAG_TMS	U9	GPIO	GPIO	ALT0	SJC.TMS	Input	PU (47K)	PU (47K)
JTAG_TRSTB	U10	GPIO	GPIO	ALT0	SJC.TRSTB	Input	PU (47K)	PU (47K)
KEY_COL0	D18	GPIO	GPIO	ALT5	GPIO3_GPIO[24]	Not connected	Hi-Z	Hi-Z
KEY_COL1	E18	GPIO	GPIO	ALT5	GPIO3_GPIO[26]	Not connected	Hi-Z	Hi-Z
KEY_COL2	D20	GPIO	GPIO	ALT5	GPIO3_GPIO[28]	Not connected	Hi-Z	Hi-Z
KEY_COL3	E19	GPIO	GPIO	ALT5	GPIO3_GPIO[30]	Not connected	Hi-Z	Hi-Z
KEY_COL4	C19	GPIO	GPIO	ALT5	GPIO4_GPIO[0]	Not connected	Hi-Z	Hi-Z
KEY_COL5	D19	GPIO	GPIO	ALT5	GPIO4_GPIO[2]	Not connected	Hi-Z	Hi-Z
KEY_COL6	C17	GPIO	GPIO	ALT5	GPIO4_GPIO[4]	Not connected	Hi-Z	Hi-Z

Table 64. 14 x 14 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
KEY_COL7	A19	GPIO	GPIO	ALT5	GPIO4_GPIO[6]	Not connected	Hi-Z	Hi-Z
KEY_ROW0	F20	GPIO	GPIO	ALT5	GPIO3_GPIO[25]	Not connected	Hi-Z	Hi-Z
KEY_ROW1	E17	GPIO	GPIO	ALT5	GPIO3_GPIO[27]	Not connected	Hi-Z	Hi-Z
KEY_ROW2	E20	GPIO	GPIO	ALT5	GPIO3_GPIO[29]	Not connected	Hi-Z	Hi-Z
KEY_ROW3	C20	GPIO	GPIO	ALT5	GPIO3_GPIO[31]	Not connected	Hi-Z	Hi-Z
KEY_ROW4	B18	GPIO	GPIO	ALT5	GPIO4_GPIO[1]	Not connected	Hi-Z	Hi-Z
KEY_ROW5	C18	GPIO	GPIO	ALT5	GPIO4_GPIO[3]	Not connected	Hi-Z	Hi-Z
KEY_ROW6	B20	GPIO	GPIO	ALT5	GPIO4_GPIO[5]	Not connected	Hi-Z	Hi-Z
KEY_ROW7	B19	GPIO	GPIO	ALT5	GPIO4_GPIO[7]	Not connected	Hi-Z	Hi-Z
LCD_CLK	R18	GPIO	GPIO	ALT5	GPIO2_GPIO[15]	Not connected	Hi-Z	Hi-Z
LCD_DAT0	U20	GPIO	GPIO	ALT5	GPIO2_GPIO[20]	Input	PD (100K)	PD (100K)
LCD_DAT1	T20	GPIO	GPIO	ALT5	GPIO2_GPIO[21]	Input	PD (100K)	PD (100K)
LCD_DAT10	M19	GPIO	GPIO	ALT5	GPIO2_GPIO[30]	Input	PD (100K)	PD (100K)
LCD_DAT11	N20	GPIO	GPIO	ALT5	GPIO2_GPIO[31]	Input	PD (100K)	PD (100K)
LCD_DAT12	M20	GPIO	GPIO	ALT5	GPIO3_GPIO[0]	Input	PD (100K)	PD (100K)
LCD_DAT13	L20	GPIO	GPIO	ALT5	GPIO3_GPIO[1]	Input	PD (100K)	PD (100K)
LCD_DAT14	L16	GPIO	GPIO	ALT5	GPIO3_GPIO[2]	Input	PD (100K)	PD (100K)
LCD_DAT15	K20	GPIO	GPIO	ALT5	GPIO3_GPIO[3]	Input	PD (100K)	PD (100K)

Table 64. 14 x 14 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
LCD_DAT16	L19	GPIO	GPIO	ALT5	GPIO3_GPIO[4]	Input	PD (100K)	PD (100K)
LCD_DAT17	K16	GPIO	GPIO	ALT5	GPIO3_GPIO[5]	Input	PD (100K)	PD (100K)
LCD_DAT18	K19	GPIO	GPIO	ALT5	GPIO3_GPIO[6]	Input	PD (100K)	PD (100K)
LCD_DAT19	J19	GPIO	GPIO	ALT5	GPIO3_GPIO[7]	Input	PD (100K)	PD (100K)
LCD_DAT2	T19	GPIO	GPIO	ALT5	GPIO2_GPIO[22]	Input	PD (100K)	PD (100K)
LCD_DAT20	K17	GPIO	GPIO	ALT5	GPIO3_GPIO[8]	Input	PD (100K)	PD (100K)
LCD_DAT21	K18	GPIO	GPIO	ALT5	GPIO3_GPIO[9]	Input	PD (100K)	PD (100K)
LCD_DAT22	J20	GPIO	GPIO	ALT5	GPIO3_GPIO[10]	Input	PD (100K)	PD (100K)
LCD_DAT23	J17	GPIO	GPIO	ALT5	GPIO3_GPIO[11]	Input	PD (100K)	PD (100K)
LCD_DAT3	T18	GPIO	GPIO	ALT5	GPIO2_GPIO[23]	Input	PD (100K)	PD (100K)
LCD_DAT4	R20	GPIO	GPIO	ALT5	GPIO2_GPIO[24]	Input	PD (100K)	PD (100K)
LCD_DAT5	T17	GPIO	GPIO	ALT5	GPIO2_GPIO[25]	Input	PD (100K)	PD (100K)
LCD_DAT6	R17	GPIO	GPIO	ALT5	GPIO2_GPIO[26]	Input	PD (100K)	PD (100K)
LCD_DAT7	R19	GPIO	GPIO	ALT5	GPIO2_GPIO[27]	Input	PD (100K)	PD (100K)
LCD_DAT8	P19	GPIO	GPIO	ALT5	GPIO2_GPIO[28]	Input	PD (100K)	PD (100K)
LCD_DAT9	N19	GPIO	GPIO	ALT5	GPIO2_GPIO[29]	Input	PD (100K)	PD (100K)
LCD_ENABLE	J18	GPIO	GPIO	ALT5	GPIO2_GPIO[16]	Not connected	Hi-Z	Hi-Z
LCD_HSYNC	G19	GPIO	GPIO	ALT5	GPIO2_GPIO[17]	Not connected	Hi-Z	Hi-Z

Table 64. 14 x 14 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
LCD_RESET	H19	GPIO	GPIO	ALT5	GPIO2_GPIO[19]	Not connected	Hi-Z	Hi-Z
LCD_VSYNC	H20	GPIO	GPIO	ALT5	GPIO2_GPIO[18]	Not connected	Hi-Z	Hi-Z
ONOFF	U12	RESET	GPIO	ALT0	SRC.RESET_B	Input	PU (100K)	PU (100K)
PMIC_ON_REQ	Y10	RESET	GPIO	ALT0	SNVS_LP_WRAPPER.SNVS_WAKEUP_ALARM	Output	Open Drain with PU (100K)	PU (100K)
PMIC_STBY_REQ	W10	RESET	GPIO	ALT0	CCM.PMIC_VSTBY_REQ	Output	0	Not connected
POR_B	V11	RESET	GPIO	ALT0	SRC.POR_B	Input	PU (100K)	PU (100K)
PWM1	T5	GPIO	GPIO	ALT5	GPIO3_GPIO[23]	Not connected	Hi-Z	Hi-Z
REF_CLK_24M	T8	GPIO	GPIO	ALT5	GPIO3_GPIO[21]	Not connected	Hi-Z	Hi-Z
REF_CLK_32K	T10	GPIO	GPIO	ALT5	GPIO3_GPIO[22]	Not connected	Hi-Z	Hi-Z
RTC_XTALI	Y16	ANATOP	—	—	—	—	—	—
RTC_XTALO	W16	ANATOP	—	—	—	—	—	—
SD1_CLK	D15	GPIO	GPIO	ALT5	GPIO5_GPIO[15]	Not connected	Hi-Z	Hi-Z
SD1_CMD	C15	GPIO	GPIO	ALT5	GPIO5_GPIO[14]	Not connected	Hi-Z	Hi-Z
SD1_DAT0	A18	GPIO	GPIO	ALT5	GPIO5_GPIO[11]	Not connected	Hi-Z	Hi-Z
SD1_DAT1	C16	GPIO	GPIO	ALT5	GPIO5_GPIO[8]	Not connected	Hi-Z	Hi-Z
SD1_DAT2	B17	GPIO	GPIO	ALT5	GPIO5_GPIO[13]	Not connected	Hi-Z	Hi-Z
SD1_DAT3	B16	GPIO	GPIO	ALT5	GPIO5_GPIO[6]	Not connected	Hi-Z	Hi-Z
SD1_DAT4	D16	GPIO	GPIO	ALT5	GPIO5_GPIO[12]	Not connected	Hi-Z	Hi-Z

Table 64. 14 x 14 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
SD1_DAT5	A17	GPIO	GPIO	ALT5	GPIO5_GPIO[9]	Not connected	Hi-Z	Hi-Z
SD1_DAT6	A16	GPIO	GPIO	ALT5	GPIO5_GPIO[7]	Not connected	Hi-Z	Hi-Z
SD1_DAT7	D14	GPIO	GPIO	ALT5	GPIO5_GPIO[10]	Not connected	Hi-Z	Hi-Z
SD2_CLK	Y19	GPIO	GPIO	ALT5	GPIO5_GPIO[5]	Not connected	Hi-Z	Hi-Z
SD2_CMD	W20	GPIO	GPIO	ALT5	GPIO5_GPIO[4]	Not connected	Hi-Z	Hi-Z
SD2_DAT0	Y18	GPIO	GPIO	ALT5	GPIO5_GPIO[1]	Not connected	Hi-Z	Hi-Z
SD2_DAT1	W18	GPIO	GPIO	ALT5	GPIO4_GPIO[30]	Not connected	Hi-Z	Hi-Z
SD2_DAT2	V18	GPIO	GPIO	ALT5	GPIO5_GPIO[3]	Not connected	Hi-Z	Hi-Z
SD2_DAT3	W19	GPIO	GPIO	ALT5	GPIO4_GPIO[28]	Not connected	Hi-Z	Hi-Z
SD2_DAT4	V20	GPIO	GPIO	ALT5	GPIO5_GPIO[2]	Not connected	Hi-Z	Hi-Z
SD2_DAT5	U17	GPIO	GPIO	ALT5	GPIO4_GPIO[31]	Not connected	Hi-Z	Hi-Z
SD2_DAT6	U18	GPIO	GPIO	ALT5	GPIO4_GPIO[29]	Not connected	Hi-Z	Hi-Z
SD2_DAT7	V19	GPIO	GPIO	ALT5	GPIO5_GPIO[0]	Not connected	Hi-Z	Hi-Z
SD2_RST	U19	GPIO	GPIO	ALT5	GPIO4_GPIO[27]	Not connected	Hi-Z	Hi-Z
SD3_CLK	U7	GPIO	GPIO	ALT5	GPIO5_GPIO[18]	Not connected	Hi-Z	Hi-Z
SD3_CMD	W7	GPIO	GPIO	ALT5	GPIO5_GPIO[21]	Not connected	Hi-Z	Hi-Z
SD3_DAT0	Y8	GPIO	GPIO	ALT5	GPIO5_GPIO[19]	Not connected	Hi-Z	Hi-Z
SD3_DAT1	W8	GPIO	GPIO	ALT5	GPIO5_GPIO[20]	Not connected	Hi-Z	Hi-Z

Table 64. 14 x 14 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]				During Reset Condition
				Default Mode (Reset Mode)	Default Function	Input / Output	Value[3]	
SD3_DAT2	V7	GPIO	GPIO	ALT5	GPIO5_GPIO[16]	Not connected	Hi-Z	Hi-Z
SD3_DAT3	V8	GPIO	GPIO	ALT5	GPIO5_GPIO[17]	Not connected	Hi-Z	Hi-Z
TAMPER	T12	RESET	GPIO	ALT0	SNVS_LP_WRAPPER.SNVS_TD1	Input	—	PD (100K)
TEST_MODE	U11	RESET	GPIO	ALT0	TCU.TEST_MODE	Input	—	PD (100K)
UART1_RXD	A15	GPIO	GPIO	ALT5	GPIO3_GPIO[16]	Not connected	Hi-Z	Hi-Z
UART1_TXD	B15	GPIO	GPIO	ALT5	GPIO3_GPIO[17]	Not connected	Hi-Z	Hi-Z
USB_OTG1_CHD_B	W15	ANATOP	—	—	—	—	—	—
USB_OTG1_DN	Y14	ANATOP	—	—	—	—	—	—
USB_OTG1_DP	W14	ANATOP	—	—	—	—	—	—
USB_OTG2_DN	Y12	ANATOP	—	—	—	—	—	—
USB_OTG2_DP	W12	ANATOP	—	—	—	—	—	—
WDOG_B	C14	GPIO	GPIO	ALT5	GPIO3_GPIO[18]	Not connected	Hi-Z	Hi-Z
XTALI	V13	ANATOP	—	—	—	—	—	—
XTALO	U13	ANATOP	—	—	—	—	—	—
ZQPAD	G3	DRAM	—	—	—	Input	Hi-Z	Not connected

1 All balls marked Power Group NVCC33_IO or NVCC18_IO are dual-voltage IOs. The user supplies NVCC33_IO and NVCC18_IO. In the IOMUX for each ball, the user selects either 3.3 V or 1.8 V operation using the LVE field in the Pad Control Register for each ball.

2 The state immediately after reset and before ROM firmware or software has executed.

3 Variance of the pull-up and pull-down strengths are shown in the tables as follows:

- Table 20, "DVGPIO I/O DC Parameters," on page 29.
- Table 21, "GPIO I/O DC Parameters," on page 30
- Table 22, "LPDDR2/LPDDR3 I/O DC Electrical Parameters," on page 31

6.1.3 14 x 14 mm, 0.65 mm Pitch Ball Map

Table 65 shows the MAPBGA 14 x 14 mm, 0.65 mm pitch ball map.

Table 65. 14 x 14 mm, 0.65 mm Pitch Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	DRAM_D31	EPDC_VCOM1	EPDC_VCOM0	EPDC_SDCLK	EPDC_GDSP	GND	EPDC_GDOE	EPDC_D14	EPDC_D6	EPDC_D3	EPDC-D2	GND	I2C2_SDA	UART1_RXD	SD1_DAT6	SD1_DAT5	SD1_DAT0	KEY_COL7	GND
B	DRAM_D28	DRAM_D30	GND	EPDC_SDSHR	EPDC_PWRWAKEUP	EPDC_SDCE0	EPDC_PWRCOM	EPDC_PWRCTRL2	EPDC_D13	EPDC_D5	EPDC_D4	EPDC_D1	EPDC_BDR0	I2C2_SCL	UART1_TXD	SD1_DAT3	SD1_DAT2	KEY_ROW4	KEY_ROW7	KEY_ROW6
C	DRAM_D29	DRAM_D27	DRAM_DQM3	EPDC_SDOE	EPDC_SDLE	EPDC_PWRSTAT	EPDC_PWRCTRL0	EPDC_GDCLK	EPDC_D15	EPDC_D12	EPDC_D11	EPDC_D0	EPDC_BDR1	WDOG_B	SD1_CMD	SD1_DAT1	KEY_COL6	KEY_ROW5	KEY_COL4	KEY_ROW3
D	DRAM_D26	DRAM_SDQS3	DRAM_SDQS3_B	GND	EPDC_SDCE3	EPDC_SDCE2	EPDC_SDCE1	EPDC_PWRINT	EPDC_PWRCTRL1	EPDC_GDRL	EPDC_D8	EPDC_D9	EPDC_D10	SD1_DAT7	SD1_CLK	SD1_DAT4	GND	KEY_COL0	KEY_COL5	KEY_COL2
E	DRAM_D25	DRAM_D24	DRAM_SDQS1_B	DRAM_SDQS1	GND	GND	NVCC_1V8	NVCC_1V8	GND	EPDC_PWRCTRL3	EPDC_D7	GND	NVCC_1V8	NVCC_1V8	GND	GND	KEY_ROW1	KEY_COL1	KEY_COL3	KEY_ROW2
F	DRAM_D14	DRAM_D13	DRAM_DQM1	DRAM_A7	GND	NVCC_DRAM_2P5	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	GND	AUD_MCLK	AUD_RXFS	AUD_TXFS	KEY_ROW0

Table 65. 14 x 14 mm, 0.65 mm Pitch Ball Map (continued)

	P	N	M	L	K	J	H	G	
1	GND	DRAM_D7	DRAM_SDCKE0	DRAM_A5	DRAM_D10	DRAM_D11	DRAM_D9	GND	1
2	DRAM_D4	DRAM_D5	DRAM_D6	DRAM_CS0_B	DRAM_CS1_B	DRAM_D8	DRAM_D12	DRAM_D15	2
3	DRAM_DQM0	GND	DRAM_A2	DRAM_A6	DRAM_SDCKE1	DRAM_SDCLK_0_B	GND	ZQPAD	3
4	DRAM_A0	DRAM_A1	DRAM_A3	DRAM_A4	DRAM_VREF	DRAM_SDCLK_0	DRAM_A8	DRAM_A9	4
5	GND	NVCC_DRAM	GND	GND	NVCC_DRAM	GND	GND	NVCC_DRAM	5
6	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM_2P5	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	6
7	GND	GND	GND	GND	GND	GND	GND	GND	7
8	GND	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	GND	8
9	GND	VDD_SOC_IN	VDD_SOC_IN	GND	GND	VDD_SOC_IN	VDD_SOC_IN	GND	9
10	GND	VDD_SOC_IN	VDD_SOC_IN	GND	GND	VDD_SOC_IN	VDD_SOC_IN	GND	10
11	GND	VDD_SOC_IN	VDD_SOC_IN	GND	GND	VDD_ARM_IN	VDD_ARM_IN	GND	11
12	GND	VDD_SOC_IN	VDD_SOC_IN	GND	GND	VDD_ARM_IN	VDD_ARM_IN	GND	12
13	GND	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN	GND	13
14	GND	GND	GND	GND	GND	GND	GND	GND	14
15	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	15
16	GND	NVCC_1V8	NVCC_1V8	LCD_DAT14	LCD_DAT17	GND	NVCC_1V8	NVCC_1V8_2	16
17	ECSPI2_SCLK	ECSPI2_SS0	ECSPI1_SCLK	ECSPI1_SS0	LCD_DAT20	LCD_DAT23	AUD_RXC	AUD_TXC	17
18	ECSPI2_MOSI	ECSPI2_MISO	ECSPI1_MOSI	ECSPI1_MISO	LCD_DAT21	LCD_ENABLE	AUD_RXD	AUD_TXD	18
19	LCD_DAT8	LCD_DAT9	LCD_DAT10	LCD_DAT16	LCD_DAT18	LCD_DAT19	LCD_RESET	LCD_HSYNC	19
20	GND	LCD_DAT11	LCD_DAT12	LCD_DAT13	LCD_DAT15	LCD_DAT22	LCD_VSYNC	GND	20

Table 65. 14 x 14 mm, 0.65 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
R	DRAM_D3	DRAM_D2	DRAM_SDQS0	DRAM_SDQS0_B	GND	NVCC_DRAM_2P5	NVCC_1V8	NVCC_1V8	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	NVCC_3V3	GND	LCD_DAT6	LCD_CLK	LCD_DAT7	LCD_DAT4
T	DRAM_D1	DRAM_D0	DRAM_DQM2	GND	PWM1	GND	GND	REF_CLK_24M	JTAG_MOD	REF_CLK_32K	BOOT_MODE1	TAMPER	VDD_USB_CAP	NGND_KEL0	GND	GPANAIO	LCD_DAT5	LCD_DAT3	LCD_DAT2	LCD_DAT1
U	DRAM_D22	DRAM_SDQS2	DRAM_SDQS2_B	GPIO4_IO21	GPIO4_IO20	GPIO4_IO16	SD3_CLK	JTAG_TDI	JTAG_TMS	JTAG_TRSTB	TEST_MODE	ONOFF	XTALO	VDD_SNVS_CAP	CLK1_N	VDD_HIGH_CAP	SD2_DAT5	SD2_DAT6	SD2_RST	LCD_DAT0
V	DRAM_D23	DRAM_D20	GND	GPIO4_IO19	GPIO4_IO25	GPIO4_IO226	SD3_DAT2	SD3_DAT3	JTAG_TCK	JTAG_TDO	POR_B	GND	XTALI	VDD_SNVS_IN	CLK1_P	VDD_HIGH_CAP	NVCC_PLL	SD2_DAT2	SD2_DAT7	SD2_DAT4
W	DRAM_D21	DRAM_D18	DRAM_D16	GPIO4_IO17	GPIO4_IO23	GPIO4_IO22	SD3_CMD	SD3_DAT1	I2C1_SDA	PMC_STBY_REQ	BOOT_MODE0	USB_OTG2_DP	USB_OTG1_VBUS	USB_OTG1_DP	USB_OTG1_CHD_B	RTC_XTALO	VDD_HIGH_IN	SD2_DAT1	SD2_DAT3	SD2_CMD
Y	GND	DRAM_D19	DRAM_D17	GND	GPIO4_IO18	GPIO4_IO24	GND	SD3_DAT0	I2C1_SCL	PMIC_ON_REQ	GND	USB_OTG2_DN	USB_OTG2_VBUS	USB_OTG1_DN	GND	RTC_XTALI	VDD_HIGH_IN	SD2_DAT0	SD2_CLK	GND

7 Revision History

Table 66 provides a history for this data sheet.

Table 66. i.MX 6SLL Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 1	01/2019	• Added the SD Host Controller information in the Table 2, "i.MX 6SLL Modules List" • Updated the input voltages for non-VBUS USB signals in the Table 7, "Absolute Maximum Ratings" • Added Vin/Vout for non-DDR pins in the Table 7, "Absolute Maximum Ratings" • Added a note in the Section 4.1.2, Thermal Resistance • Updated the Table 19, "XTALI and RTC_XTALI DC Parameters" • Updated the SD2 min and max values in the Table 40, "eMMC4.4/4.41 Interface Timing Specification" • Updated the remark of GPANAIO in the Table 63, "14 x 14 mm Supplies Contact Assignment" • Changed K5 to K6 for NVCC_DRAM and K6 to K5 for NVCC_DRAM_2P5 in the Table 63, "14 x 14 mm Supplies Contact Assignment" • Updated the IO and value of DRAM_SDCLK_0 in the Table 64, "14 x 14 mm Functional Contact Assignments"
Rev. 0.2	11/2017	• Removed the HBM note in the Table 7, "Absolute Maximum Ratings and updated the ESD HBM values • Added a note in the Table 7, "Absolute Maximum Ratings
Rev. 0.1	09/2017	• Added a note for HBM in the Table 7, "Absolute Maximum Ratings
Rev. 0	04/2017	• Initial version

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