MIC58P42

8-Bit Serial-Input Protected Latched Driver

General Description

The MIC58P42 serial-input latched driver is a high-voltage (80V), high-current (500mA) integrated circuit comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common STROBE, CLOCK, SERIAL DATA INPUT, and OUTPUT ENABLE functions. Similar to the MIC5842, additional protection circuitry supplied on this device includes thermal shutdown, under voltage lockout (UVLO), and overcurrent shutdown.

The bipolar/CMOS combination provides an extremely low-power latch with maximum interface flexibility. The MIC58P42 has open-collector outputs capable of sinking 500 mA and integral diodes for inductive load transient suppression with a minimum output breakdown voltage rating of 80V (50V sustaining). The drivers can be operated with a split supply, where the negative supply is down to –20V and may be paralleled for higher load current capability.

With a 5V logic supply, the MIC58P42 will typically operate at better than 5MHz. With a 12V logic supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL circuits may require pull-up resistors. By using the serial data output, drivers may be cascaded for interface applications requiring additional drive lines.

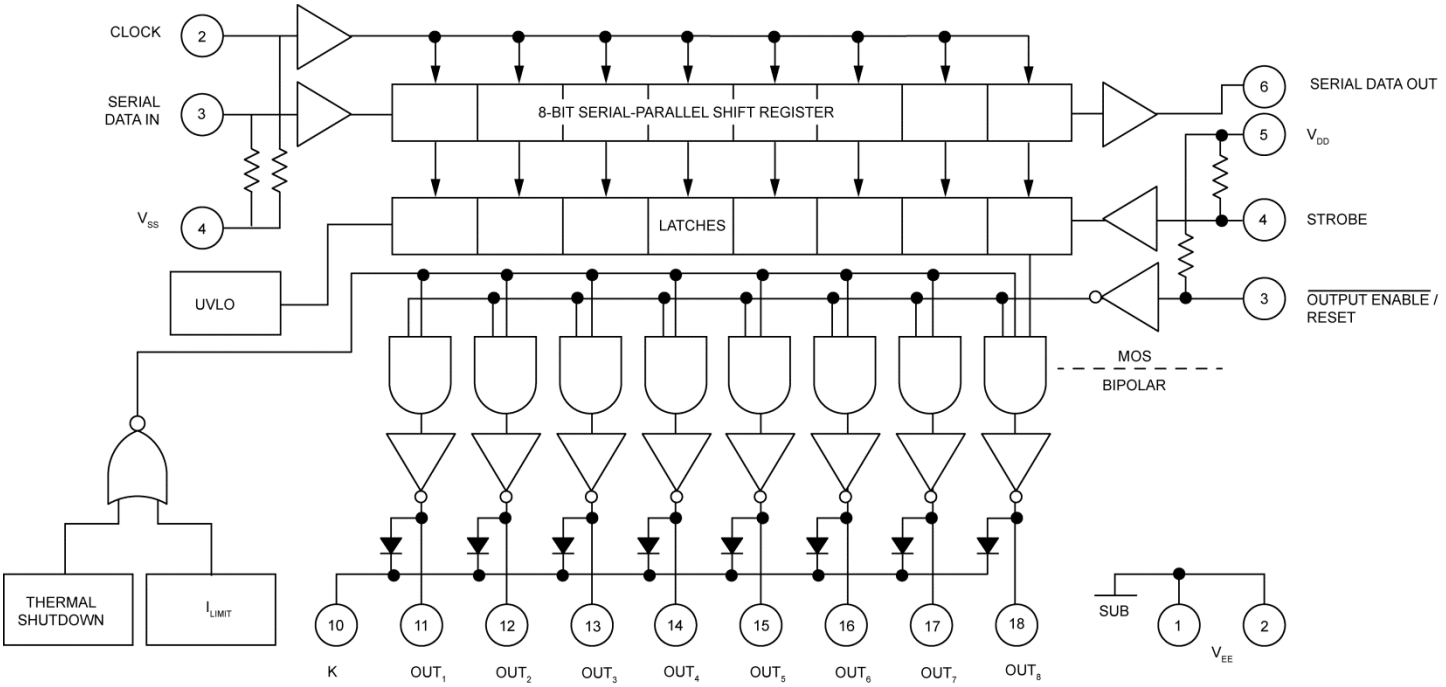
Each of these eight outputs has an independent over current shutdown of 500 mA. Upon over-current detection, the affected channel will turn OFF until V_{DD} is cycled or the ENABLE/RESET pin is pulsed high. Current pulses less than 2μs will not activate current shutdown. Temperatures above 165°C will shut down the device. The UVLO circuit prevents operation at low V_{DD}; hysteresis of 0.5V is provided. See the MIC59P60 for a similar device that additionally provides an error flag output.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Features

- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, and TTL Compatible
- Internal Pull-Up/Pull-Down Resistors
- Low Power CMOS Logic and Latches
- High Voltage (80V) Current-Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation
- Thermal Shutdown
- Under-Voltage Lockout
- Per-Output Over-Current Shutdown (500mA typical)

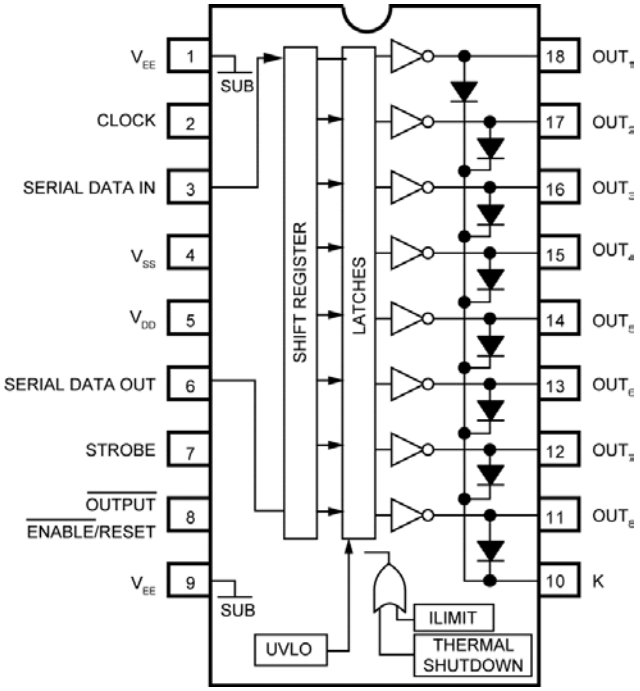
Functional Diagram



Ordering Information

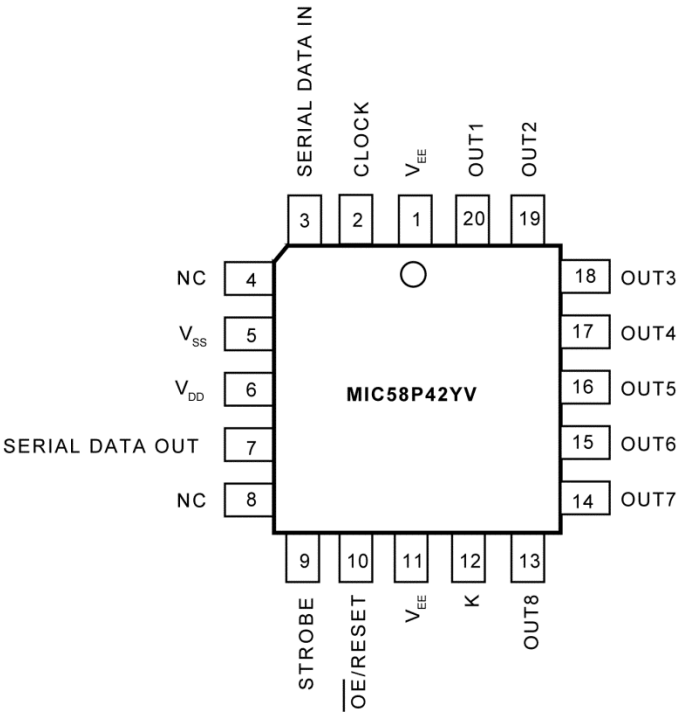
Part Number	Junction Temperature Range	Package	Pb-Free
MIC58P42YN	–40°C to +85°C	18-Pin Plastic DIP	√
MIC58P42YV	–40°C to +85°C	20-Pin PLCC	√
MIC58P42YWM	–40°C to +85°C	18-Pin Wide SOIC	√

Pin Configuration



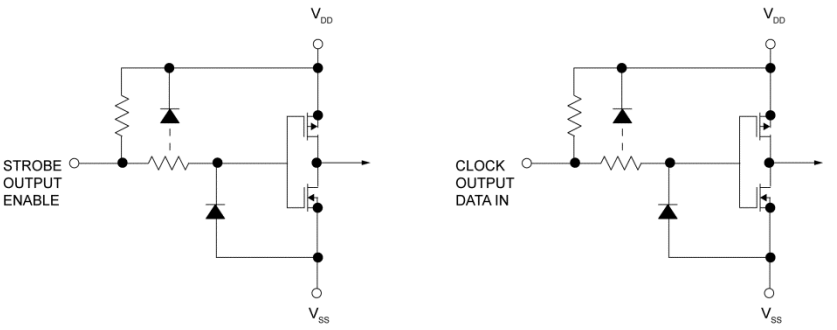
18-pin DIP (N) and 18-pin Wide SOIC (WM)

(Top View)

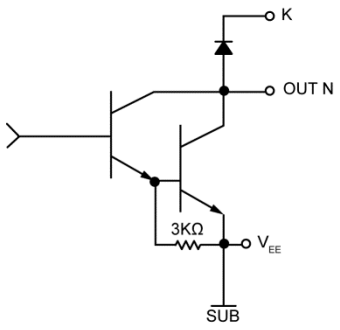


20-pin PLCC (V)

(Top View)



Typical Input Circuits



Typical Output Driver

Pin Description

Pin Number DIP & SOIC	Pin Number PLCC	Pin Name	Pin Function
1, 9	1, 11	V_{EE}	Substrate. Most Negative voltage in the system connects here.
2	2	CLOCK	Serial Data Clock. A CLEAR input must also be clocked into the latches.
3	3	SERIAL DATA IN	Serial Data Input pin.
4	5	V_{SS}	Logic reference (Ground) pin.
5	6	V_{DD}	Logic Positive Supply voltage.
6	7	SERIAL DATA OUT	Serial Data Output pin. (Flow–through).
7	9	STROBE	Output Strobe pin. Loads output latches when high. Strobe is needed to clear latch.
8	10	$\overline{\text{OUTPUT}}$ ENABLE/RESET	When Low, Outputs are active. When High, device is reset from a fault condition.
10	12	K	Transient suppression diode's cathode common pin.
11 – 18	13 – 20	OUT_N	Open Collector outputs 8 through 1.

Absolute Maximum Ratings[1]

Output Voltage ..... +80V
Output Voltage, $V_{CE(SUS)}$[3] ..... +50V
Logic Supply Voltage Range (V_{DD}) ..... 4.5V to 15V
V_{DD} with reference to V_{EE} 25V
Emitter Supply Voltage (Substrate) (V_{EE}) ..... –20V
Input Voltage Range (V_{IN}) ..... –0.3V to V_{DD} +0.3V
Operating Temperature Range (T_A) ..... –65°C to +125°C
Storage Temperature Range (T_S) ..... –60°C to +150°C
ESD Rating[4] ..... ESD Sensitive

Operating Ratings[2]

Package Power Dissipation, P_D
MIC58P42YN 1.82W
Derate above T_A = +25°C ..... 18mW/°C
MIC58P42YV 1.4W
Derate above T_A = +25°C ..... 14mW/°C
MIC58P42YWM 1.2W
Derate above T_A = +25°C ..... 12mW/°C
Operating Temperature Range (T_A) ..... –40°C to +85°C

Electrical Characteristics[5]

T_A = 25°C, V_{DD} = 5V; V_{SS} = V_{EE} = 0V, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CEX}	Output Leakage Current	V_{OUT} = 80V			50	µA
		V_{OUT} = 80V, T_A = +70°C			100	
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	I_{OUT} = 100mA I_{OUT} = 200mA I_{OUT} = 350mA		0.9 1.1 1.3	1.1 1.3 1.6	V
$V_{CE(SUS)}$	Collector-Emitter Sustaining Voltage	I_{OUT} = 350mA, L = 2mH	50			V
$V_{IN(0)}$	Input Voltage (Low)				1.0	V
$V_{IN(1)}$	Input Voltage (High)	V_{DD} = 12V V_{DD} = 10V V_{DD} = 5.0V, Note 6		10.5 8.5 3.5		
R_{IN}	Input Resistance	V_{DD} = 12V V_{DD} = 10V V_{DD} = 5.0V	50 50 50	200 300 600		kΩ
$I_{DD(ON)}$	Supply Current	All Drivers ON, V_{DD} = 12V All Drivers ON, V_{DD} = 10V All Drivers ON, V_{DD} = 5.0V		6.4 6.0 4.6	10.0 9.0 7.5	mA
$I_{DD(1\ ON)}$		One Driver ON, All others OFF, V_{DD} = 12V One Driver ON, All others OFF, V_{DD} = 10V One Driver ON, All others OFF, V_{DD} = 5.0V		3.1 2.9 2.3	4.5 4.5 3.6	
$I_{DD(OFF)}$		All Drivers OFF, V_{DD} = 12V All Drivers OFF, V_{DD} = 10V All Drivers OFF, V_{DD} = 5.0V		2.6 2.4 1.9	4.2 3.6 3.0	

Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. For inductive load applications.
4. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
5. Specification for packaged product only.
6. Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic “1”.

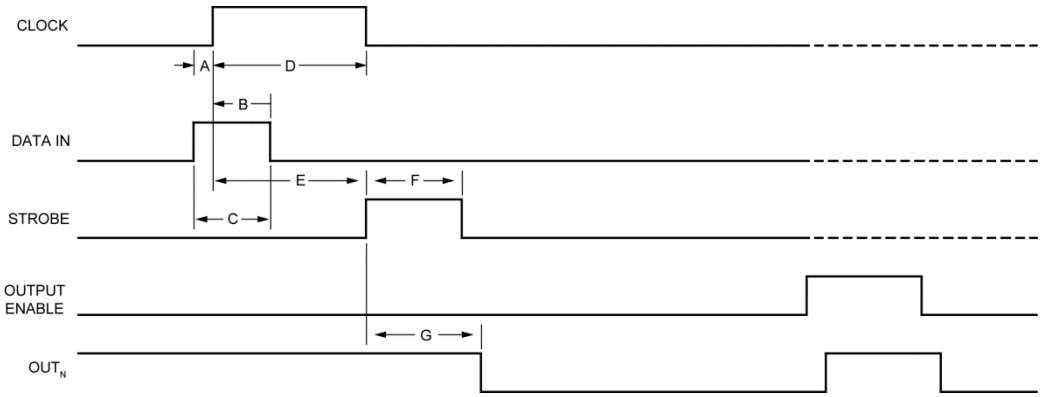
Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_R	Clamp Diode Leakage Current	V_R = 80V			50	µA
V_F	Clamp Diode Forward Voltage	I_F = 350mA		1.7	2.0	V
I_{LIM}	Output Current Shutdown Threshold			500		mA
V_{SU}	Start Up Voltage	Note 7	3.5	4.0	4.5	V
$V_{DD\ MIN}$	Minimum Supply (V_{DD})		3.0	3.5	4.0	V
	Thermal Shutdown			165		°C
	Thermal Shutdown Hysteresis			10		°C

Note:

7. Undervoltage Lockout is guaranteed to release device at no more than 4.5V, and disable the device at no less than 3.0V.

Timing Diagram



Timing Conditions

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS}), V_{DD} = 5V

A. Typical Data Active Time Before Clock Pulse (Data Set-Up Time)..... 75ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time). 75ns
C. Minimum Data Pulse Width 150ns
D. Minimum Clock Pulse Width..... 150ns
E. Minimum Time Between Clock Activation and Strobe..... 300ns
F. Minimum Strobe Pulse Width 100ns
G. Typical Time Between Strobe Activation and Output Transition 500ns

SERIAL DATA present at the input is transferred to the shift register on the logic “0” to logic “1” transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high to prevent invalid output states.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches. A positive OUTPUT ENABLE/ RESET pulse resets the output after a current shutdown fault. Thermal limit faults are not latched and require no reset pulse.

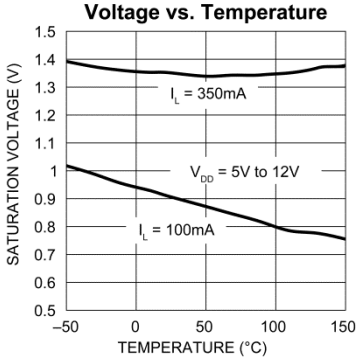
MIC58P42 Truth Table

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Enable	Output Contents
		I_1 I_2 I_3 ..... I_8			I_1 I_2 I_3 ..... I_8		I_1 I_2 I_3 ..... I_8
H	⌐‾	H R_1 R_2 ..... R_7	R_7				
L	⌐‾	L R_1 R_2 ..... R_7	R_7				
X	‾⌐	R_1 R_2 R_3 ..... R_8	R_8				
	⌐‾	O O O ..... O	L				
		X X X X	X	L	R_1 R_2 R_3 ..... R_8		
		P_1 P_2 P_3 ..... P_8	P_8	H	P_1 P_2 P_3 ..... P_8	L	P_1 P_2 P_3 ..... P_8
					X X X X	H	H H H ..... H

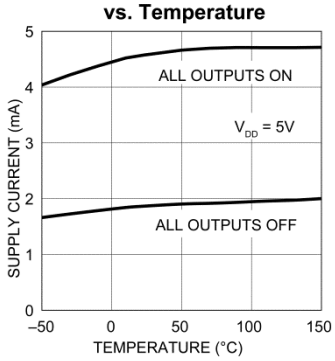
L = Low Level Logic
H = High Level Logic
X = Irrelevant
P = Present State
R = Previous State
O = Output OFF

Typical Characteristics

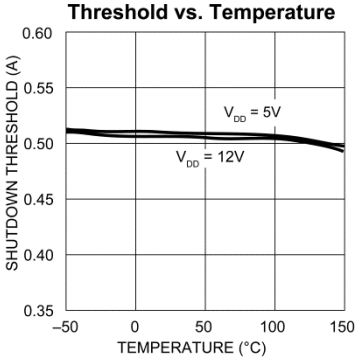
Output Saturation Voltage vs. Temperature



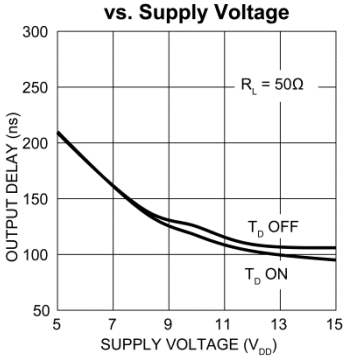
Supply Current vs. Temperature



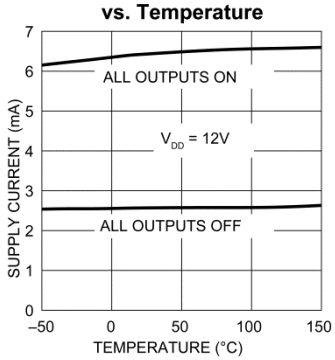
Current Shutdown Threshold vs. Temperature



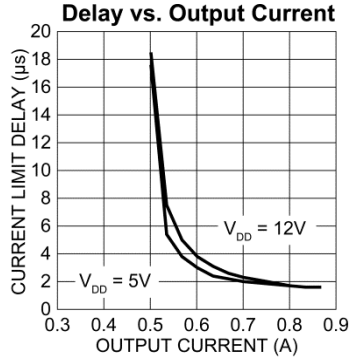
Output Delay vs. Supply Voltage



Supply Current vs. Temperature



Current Shutdown Delay vs. Output Current



Maximum Allowable Duty Cycle, Plastic DIP

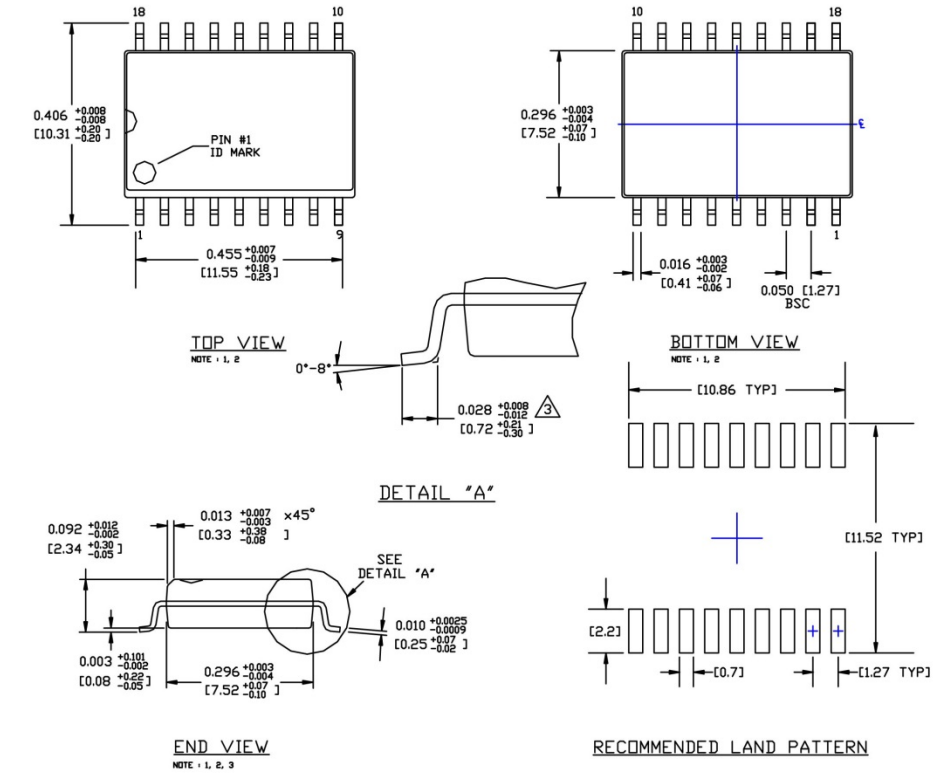
V_{DD} = 5.0V

Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 5.0V)	Max. Allowable Duty Cycle at Ambient Temperatures				
	25°C	40°C	50°C	60°C	70°C
8	85%	72%	64%	55%	46%
7	97%	82%	73%	63%	53%
6	100%	96%	85%	73%	62%
5	100%	100%	100%	88%	75%
4	100%	100%	100%	100%	93%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

V_{DD} = 12V

Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 12V)	Max. Allowable Duty Cycle at Ambient Temperatures				
	25°C	40°C	50°C	60°C	70°C
8	80%	68%	60%	52%	44%
7	91%	77%	68%	59%	50%
6	100%	90%	79%	69%	58%
5	100%	100%	95%	82%	69%
4	100%	100%	100%	100%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

Package Information and Recommended Landing Pattern[8]

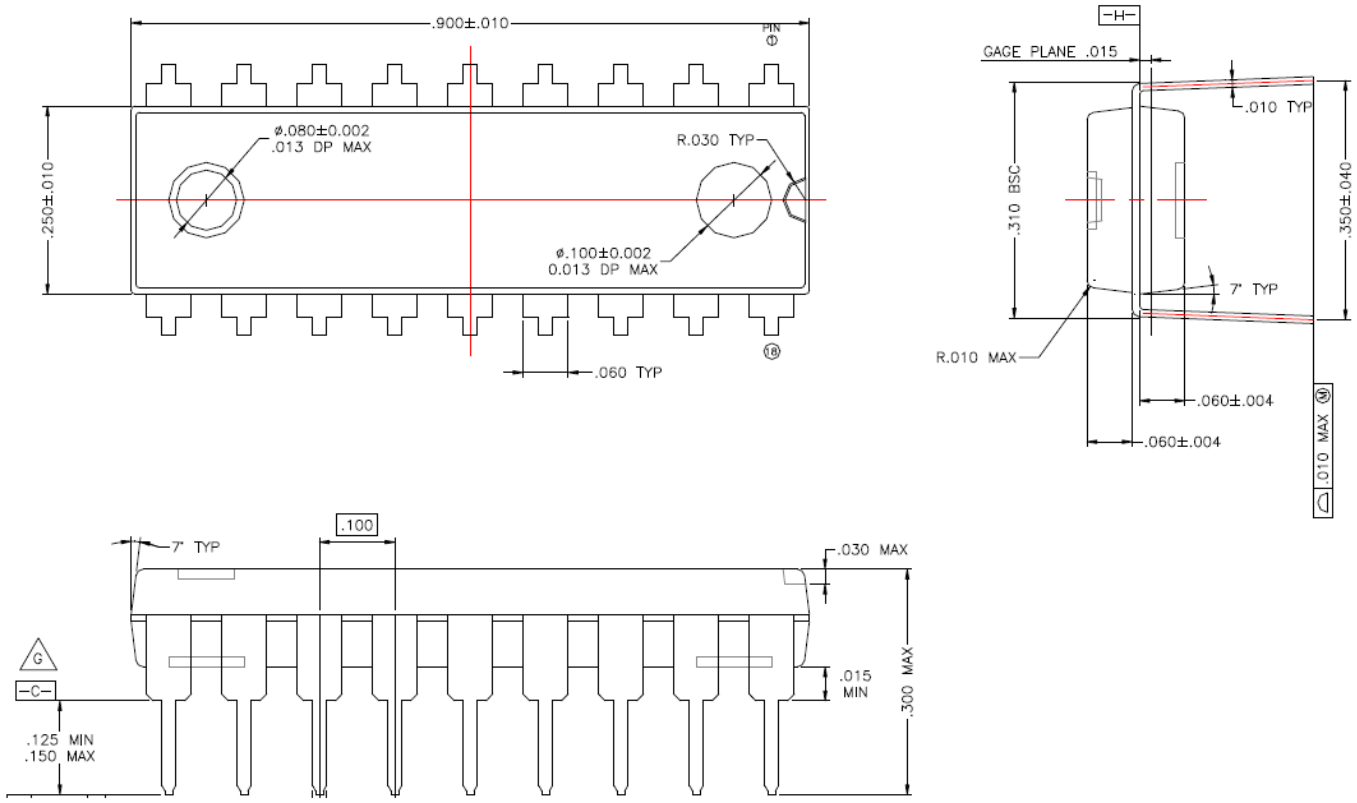


18-Pin Wide SOIC (WM)

Note:

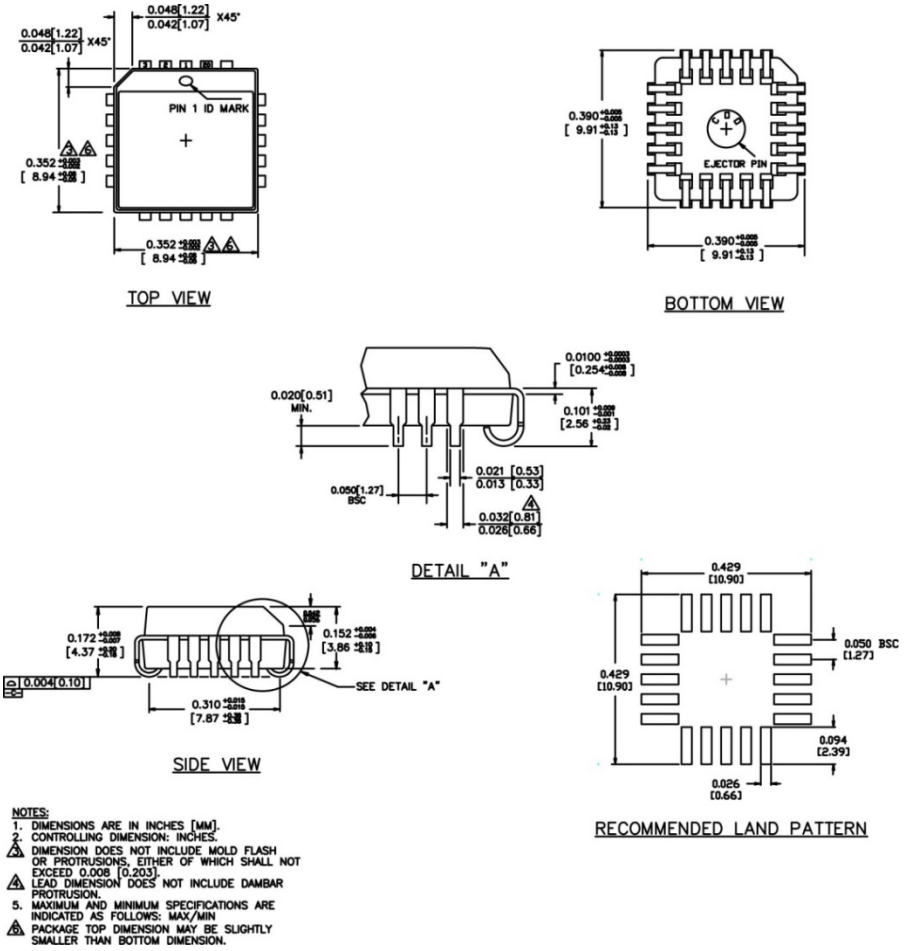
8. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Package Information and Recommended Landing Pattern[8] Continued



18-Pin DIP (N)

Package Information and Recommended Landing Pattern[8] Continued



20-Pin PLCC (V)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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