High Linearity Broadband SP2T 5MHz to 10GHz

Description

The F2976 is a single-pole double-throw (SP2T) reflective RF switch featuring high linearity and wide bandwidth. This device is optimized from 5MHz to 1.8GHz to support downstream cable modem future migration for DOCSIS 3.1 applications, and operates at up to 10GHz to support a multitude of wireless RF applications. Superb performance is achieved when used in either 50Ω or 75Ω terminating impedance applications.

The F2976 uses a single positive supply voltage of either +3.3V or +5.0V and is compatible with either 1.8V or 3.3V control logic.

Competitive Advantage

The F2976 provides extremely low insertion loss across the entire bandwidth while providing superb distortion performance.

- Optimized for DOCSIS 3.1 applications up to 1.8GHz
- Optimized for Wi-Fi applications up to 5.9GHz
- Low insertion loss
- High isolation
- Fast switching
- No external matching required

Typical Applications

- Broadband Cable DOCSIS 3.0 / 3.1
- Set top box
- CATV filter bank switching
- Wi-Fi
- Cellular BTS
- General purpose

General Features

- Supply voltage: +2.5V to +5.25V
- 1.8V and 3.3V compatible control logic
- 2mm x 2mm, 12-pin TQFN package
- -40°C to +105°C operating temperature range

Features (75Ω)

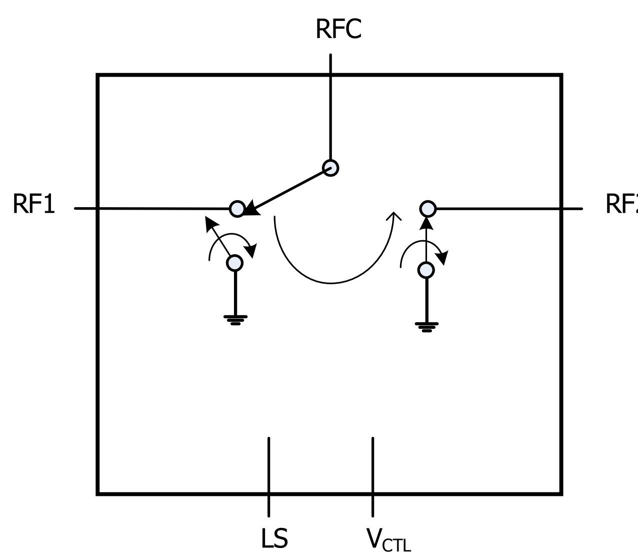
- Low insertion loss:
  - 0.23dB at 204MHz
  - 0.34dB at 1.8GHz
- High Isolation: 40dB at 1.8GHz
- P0.1dB compression of +37dBm at 204MHz
- Second Harmonic: -100dBc at 204MHz
- Third Harmonic: -120dBc at 204MHz
- Composite Second Order Distortion > 100dBc
- Composite Triple Beat Distortion > 100dBc

Features (50Ω)

- Low insertion loss:
  - 0.40dB at 2.4GHz
  - 0.55dB at 8GHz
- High Isolation:
  - 34dB at 2.4GHz
- High Linearity:
  - IIP2 +125dBm at 2.4GHz
  - IIP3 +77dBm at 2.4GHz
- P0.1dB compression of +40dBm at 2.4GHz
- Second Harmonic: -100dBc at 2.4GHz
- Third Harmonic: -110dBc at 2.4GHz

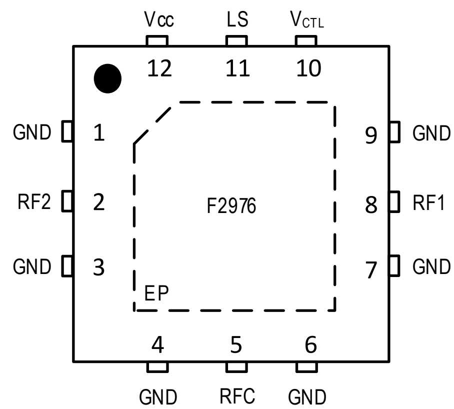
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 2mm x 2mm x 0.5mm 12-pin TQFN, NEG12 – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
2	RF2	RF2 Port. If this pin is not 0V DC, then an external coupling capacitor must be used.
3	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
4	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
5	RFC	RF Common Port. If this pin is not 0V DC, then an external coupling capacitor must be used.
6	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
7	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
8	RF1	RF1 Port. If this pin is not 0V DC, then an external coupling capacitor must be used.
9	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
10	V_{CTL}	Logic control pin (see Table 9).
11	LS	Truth Table select pin. Defines V_{CTL} logic for RF switching (see Table 9). Pin is internally pulled up to 2.5V through a 500kΩ resistor.
12	V_{CC}	Power supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
	EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Symbol	Minimum	Maximum	Units
V_{CC} to GND		V_{CC}	-0.3	+5.5	V
V_{CTL}, LS		V_{LOGIC}	-0.3	Lower of (V_{CC} + 0.3, 3.9)	V
RF1, RF2, RFC		V_{RF}	-0.3	+0.3	V
Maximum Input CW Power, 50Ω, T_{EP} = 25°C, Vcc = 5.25V (any port, insertion loss state) [a,b]	5MHz ≤ f_{RF} ≤ 10MHz	P_{ABSCW1}		30	dBm
	10MHz < f_{RF} ≤ 25MHz	P_{ABSCW2}		32	
	25MHz < f_{RF} ≤ 200MHz	P_{ABSCW3}		33	
	200MHz < f_{RF} ≤ 6000MHz	P_{ABSCW4}		34	
	f_{RF} > 6000MHz	P_{ABSCW5}		33	
Maximum Peak Power, 50Ω, T_{EP} = 25°C, Vcc = 5.25V (any port, insertion loss state) [a, b, c]	5MHz ≤ f_{RF} ≤ 10MHz	P_{ABSPK1}		35	dBm
	10MHz < f_{RF} ≤ 25MHz	P_{ABSPK2}		37	
	25MHz < f_{RF} ≤ 200MHz	P_{ABSPK3}		38	
	200MHz < f_{RF} ≤ 6000MHz	P_{ABSPK4}		39	
	f_{RF} > 6000MHz	P_{ABSPK5}		38	
Maximum Junction Temperature		T_{JMAX}		+140	°C
Storage Temperature Range		T_{ST}	-65	+150	°C
Lead Temperature (soldering, 10s)		T_{LEAD}		+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)		V_{ESDHBM}		2500 (Class 2)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)		V_{ESDCDM}		1000 (Class C3)	V

a. In a 50Ω system, dBmV = dBm [50Ω] + 47.
In a 75Ω system, dBmV = dBm [75Ω] + 48.75.

b. T_{EP} = Temperature of the exposed paddle.

c. 5 % duty cycle of a 4.6ms period.

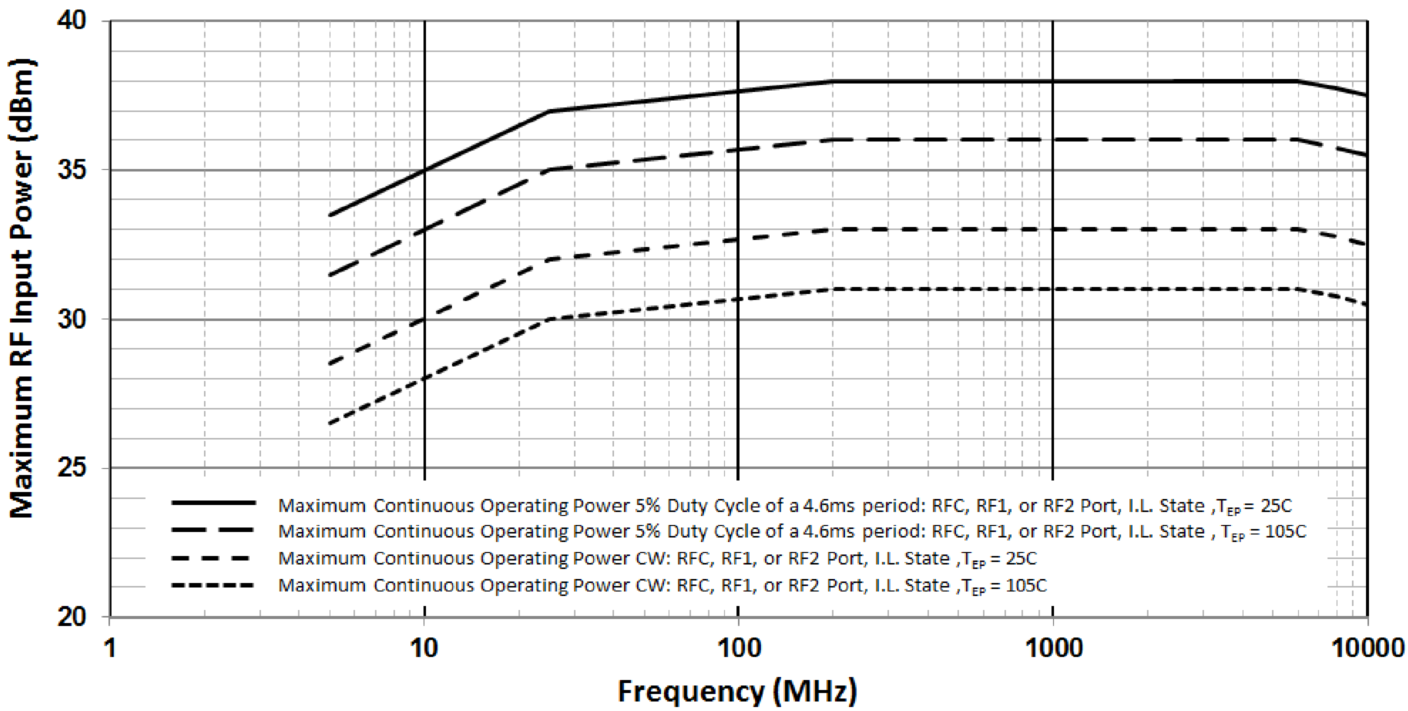
Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Supply Voltage	V_{CC}		2.5	3.3	5.25	V
Operating Temperature Range	T_{EP}	Exposed Paddle	-40		+105	°C
RF Frequency Range	f_{RF}	75Ω	0.005		1.8	GHz
		50Ω	0.005		10	
Maximum Operating Input Power	P_{MAX}	Insertion Loss State $Z_S = Z_L = 50\Omega$			See Figure 3 [a]	dBm
Port Impedance (RFC, RF1, RF2)	Z_{RF}	75Ω System		75		Ω
		50Ω System		50		

a. In a 50Ω system, dBmV = dBm [50Ω] + 47. In a 75Ω system, dBmV = dBm [75Ω] + 48.75.

Figure 3. Maximum Operating RF Input Power ($Z_S = Z_L = 50\Omega$)



General Specifications

Table 4. General Specifications

See F2976 Typical Application Circuit. Specifications apply when operated with V_{CC} = +3.3V, T_{EP} = +25°C, LS = HIGH, single tone signal applied at RF1 or RF2 and measured at RFC, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High Threshold	V_{IH}	V_{CTL}, LS pins	1.17 [b]		Lower of (V_{CC}, 3.6)	V
Logic Input Low Threshold	V_{IL}	V_{CTL}, LS pins	-0.3		0.6	V
Logic Current	I_{IH}, I_{IL}	V_{CTL}, LS pins (each pin)	***-10*** [a]		***+10***	µA
DC Current (V_{CC})	I_{CC}			80	***150***	µA
Switching Rate	SW_{RATE}				25	kHz
Maximum Video Feed-Through, RFC Port	VID_{FT}	Peak transient during switching. Z_S = Z_L = 75Ω. Measured with 20ns rise time, 0V to 3.3V (3.3V to 0V) control pulse applied to V_{CTL}.		5		mVp-p
Switching Time [c]	SW_{TIME}	50% V_{CTL} to 90% or 10% RF		1.5	3	µs

a. Items in min/max columns in ***bold italics*** are guaranteed by test.

b. Items in min/max columns that are not bold italics are guaranteed by design characterization.

c. Measured at f_{RF} = 1GHz.

Electrical Characteristics

Table 5. Electrical Characteristics - 75Ω SPECIFICATION

See F2976 75Ω Application Circuit. Specifications apply when operated with V_{CC} = +3.3V, T_{EP} = +25°C. Z_S = Z_L = 75Ω, LS = HIGH, single tone signal applied at RF1 or RF2 and measured at RFC, EVKit trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Insertion Loss (RFC to RF1, RF2)	IL	f_{RF} = 5MHz		0.20		dB
		5MHz < f_{RF} ≤ 204MHz		0.23	0.43 [b]	
		204MHz < f_{RF} ≤ 1.2GHz		0.32	0.52	
		1.2GHz < f_{RF} ≤ 1.8GHz		0.34	0.54	
Isolation (All Paths)	ISO1	f_{RF} = 5MHz		77		dB
		5MHz < f_{RF} ≤ 204MHz		60		
		204MHz < f_{RF} ≤ 1.2GHz		44		
		1.2GHz < f_{RF} ≤ 1.8GHz		40		
Return Loss (RFC, RF1, RF2) (Insertion Loss States)	RL	f_{RF} = 5MHz		35		dB
		5MHz < f_{RF} ≤ 204MHz		30		
		204MHz < f_{RF} ≤ 1.2GHz		17		
		1.2GHz < f_{RF} ≤ 1.8GHz		16		
2nd Harmonic	H2	f_{IN} = 27MHz P_{OUT} = 20dBm [c]		-80	-70	dBc
		f_{IN} = 204MHz P_{OUT} = 20dBm		-100	-90	
		f_{IN} = 800MHz P_{OUT} = 20dBm		-120	-110	
3rd Harmonic	H3	f_{IN} = 17MHz P_{OUT} = 20dBm		-95	-80	dBc
		f_{IN} = 204MHz P_{OUT} = 20dBm		-120	-105	
		f_{IN} = 800MHz P_{OUT} = 20dBm		-115	-100	
Input 0.1dB Compression Point [d] (RFC to RF1, RF2)	P0.1dB	f_{RF} = 5MHz		37		dBm
		f_{RF} = 204MHz		37		
		f_{RF} = 1.8GHz		38		
Composite Second Order	CSO	41dBmV / channel 137 channels [e]		>100		dBc
Composite Triple Beat	CTB			>100		

a. Items in min/max columns in ***bold italics*** are guaranteed by test.
b. Items in min/max columns that are not bold italics are guaranteed by design characterization.
c. dBmV = dBm [75Ω] + 48.75.
d. The input 0.1dB compression point is a linearity figure of merit. Refer to Figure 3 for the maximum operating RF input power levels.
e. Total power = -7.75 dBm [75Ω] + 10*log (137) = +13.62 dBm [75Ω].

Electrical Characteristics

Table 6. Electrical Characteristics - 50Ω SPECIFICATION

See F2976 50Ω Application Circuit. Specifications apply when operated with V_{CC} = +3.3V, T_{EP} = +25°C. Z_S = Z_L = 50Ω, LS = HIGH, single tone signal applied at RF1 or RF2 and measured at RFC, EVKit trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Insertion Loss (RFC to RF1, RF2)	IL	f_{RF} = 5MHz		0.25	0.45 [b]	dB
		5MHz < f_{RF} ≤ 1GHz		0.33	0.53	
		1GHz < f_{RF} ≤ 2GHz [c]		0.36	***0.56*** [a]	
		2GHz < f_{RF} ≤ 3GHz		0.40		
		3GHz < f_{RF} ≤ 6GHz		0.45		
		6GHz < f_{RF} ≤ 8GHz		0.55		
		8GHz < f_{RF} ≤ 9GHz		0.65		
		9GHz < f_{RF} ≤ 10GHz		0.80		
Isolation (RFC to RF1, RF2)	ISO1	5MHz < f_{RF} ≤ 1GHz	43	48		dB
		1GHz < f_{RF} ≤ 2GHz	36	42		
		2GHz < f_{RF} ≤ 3GHz	31	37		
		3GHz < f_{RF} ≤ 6GHz		27		
		6GHz < f_{RF} ≤ 8GHz		22		
		8GHz < f_{RF} ≤ 10GHz		18		
Isolation (RF1 to RF2, RF2 to RF1)	ISO2	5MHz < f_{RF} ≤ 1GHz	40	45		dB
		1GHz < f_{RF} ≤ 2GHz	33	38		
		2GHz < f_{RF} ≤ 3GHz	29	34		
		3GHz < f_{RF} ≤ 6GHz		26		
		6GHz < f_{RF} ≤ 8GHz		21		
		8GHz < f_{RF} ≤ 10GHz		18		
Return Loss (RFC, RF1, RF2) (Insertion loss states)	RL	5MHz < f_{RF} ≤ 1GHz		28		dB
		1GHz < f_{RF} ≤ 2GHz		26		
		2GHz < f_{RF} ≤ 3GHz		26		
		3GHz < f_{RF} ≤ 6GHz		25		
		6GHz < f_{RF} ≤ 8GHz		23		
		8GHz < f_{RF} ≤ 9GHz		18		
		9GHz < f_{RF} ≤ 10GHz		16		

a. Items in min/max columns in ***bold italics*** are guaranteed by test.
b. Items in min/max columns that are not bold italics are guaranteed by design characterization.
c. Minimum or maximum specification guaranteed by test at 2GHz and by design characterization over the whole frequency range.

Electrical Characteristics

Table 7. Electrical Characteristics - 50Ω SPECIFICATION

See F2976 50Ω Application Circuit. Specifications apply when operated with V_{CC} = +3.3V, T_{EP} = +25°C. Z_S = Z_L = 50Ω, LS = HIGH, single tone signal applied at RF1 or RF2 and measured at RFC, EVKit trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Input 0.1dB Compression [c]	P0.1dB	f_{RF} = 2.4GHz		40		dBm
		f_{RF} = 6.0GHz		40		
		f_{RF} = 8.0GHz		40		
Input IP3 (RF1, RF2 to RFC)	IIP3	f_{RF} = 2.4GHz P_{IN} = +24dBm/tone 100MHz spacing		77		dBm
Input IP2 (RF1, RF2 to RFC)	IIP2	f_1 = 700MHz f_2 = 1.7GHz P_{IN} = +24dBm/tone Measure 2.4GHz product		125		dBm
		f_1 = 2.4GHz f_2 = 3.5GHz P_{IN} = +24dBm/tone Measure 5.9GHz product		120		
Second Harmonic (RF1, RF2 to RFC)	H2	f_{IN} = 2.4GHz, P_{IN} = +24dBm		-100	-90 [b]	dBc
		f_{IN} = 5.9GHz, P_{IN} = +24dBm		-90	-80	
Third Harmonic (RF1, RF2 to RFC)	H3	f_{IN} = 2.4GHz, P_{IN} = +24dBm		-110	-95	dBc
		f_{IN} = 5.9GHz, P_{IN} = +24dBm		-100	-85	
Spurious Output (No RF Applied)	P_{SPUR1}	f_{OUT} ≥ 5MHz All unused ports terminated		-133		dBm
	P_{SPUR2}	f_{OUT} < 5 MHz All unused ports terminated		-120		

a. Items in min/max columns in ***bold italics*** are guaranteed by test.
b. Items in min/max columns that are not bold italics are guaranteed by design characterization.
c. The input 0.1dB compression point is a linearity figure of merit. Refer to Figure 3 for the maximum RF operating input power levels.

Thermal Characteristics

Table 8. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	θ_{JA}	102	°C/W
Junction to Case Thermal Resistance (Case is defined as the exposed paddle)	θ_{JC_BOT}	56	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions (TOCs)

Unless otherwise noted:

- V_{CC} = +3.3V
- LS = HIGH
- $Z_L = Z_S = 75\Omega$
- $Z_L = Z_S = 50\Omega$
- All temperatures are referenced to the exposed paddle
- Evaluation Kit traces and connector losses are de-embedded

Typical Performance Characteristics - 75Ω Performance

Figure 4. RF1 to RFC Insertion Loss

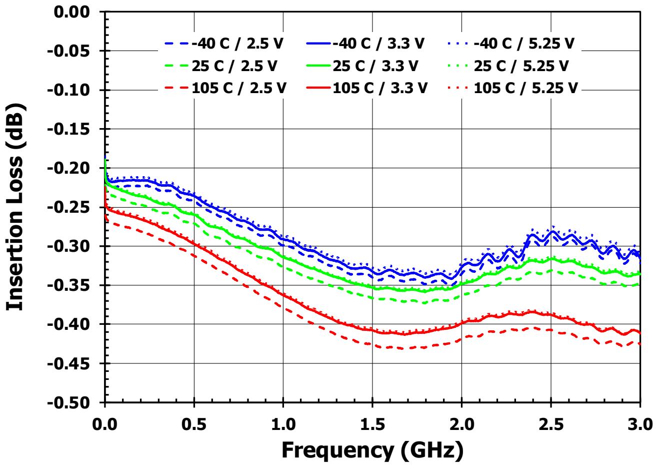


Figure 5. RF2 to RFC Insertion Loss

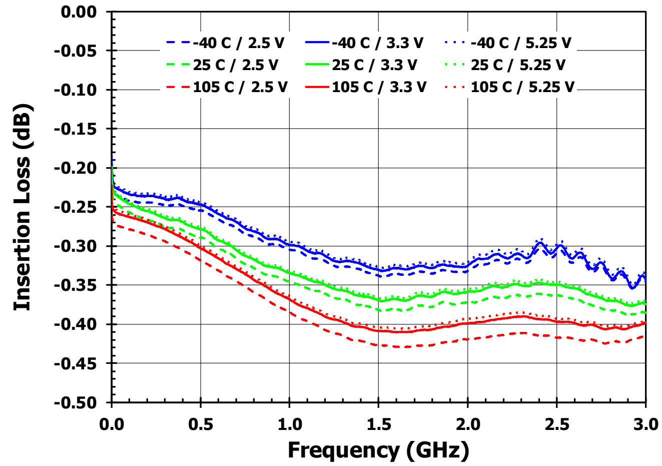


Figure 6. RF1 to RFC Isolation [RF2 On State]

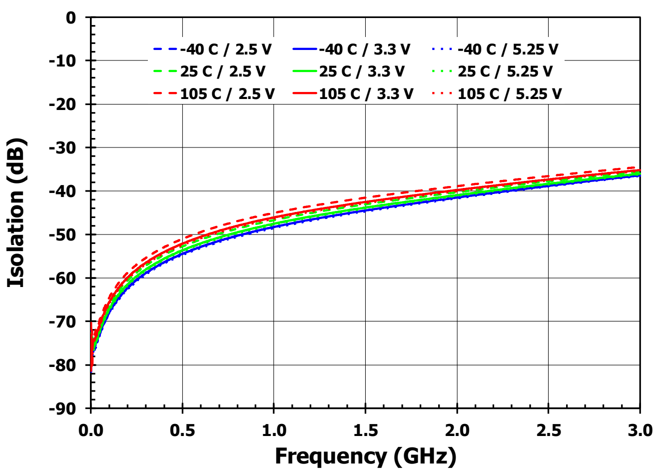


Figure 7. RF2 to RFC Isolation [RF1 On State]

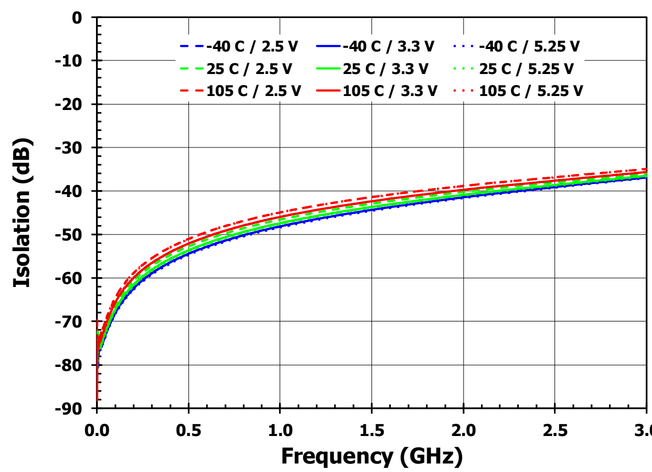


Figure 8. RF1 to RF2 Isolation [RF1 On State]

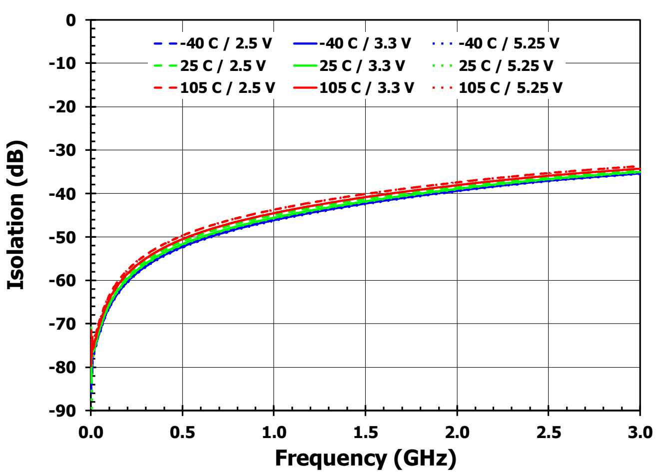
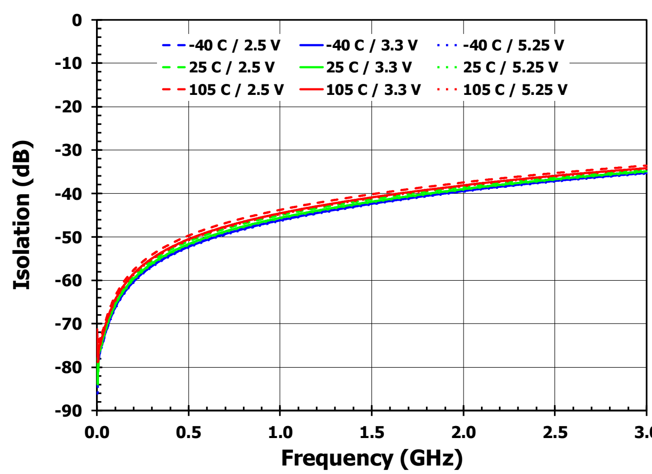


Figure 9. RF1 to RF2 Isolation [RF2 On State]



Typical Performance Characteristics - 75Ω Performance

Figure 10. RFC Return Loss [RF1 On State]

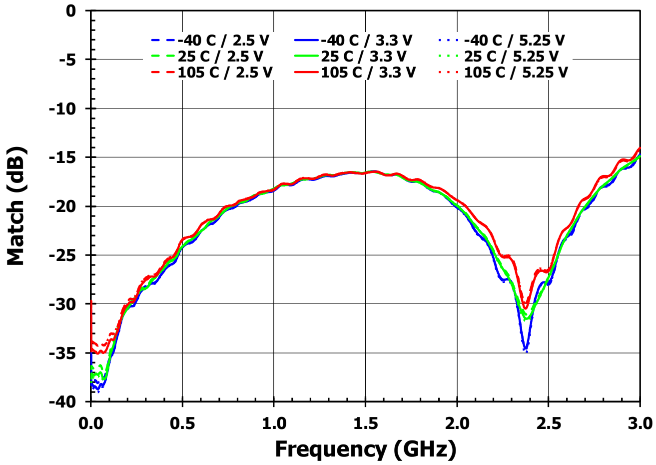


Figure 11. RFC Return Loss [RF2 On State]

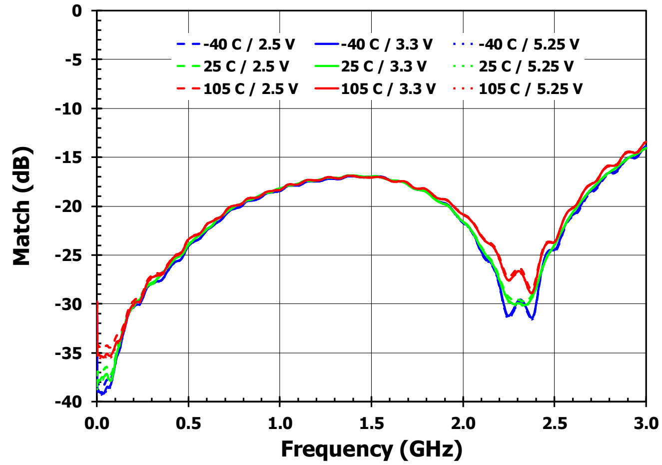


Figure 12. RF1 Return Loss [RF1 On State]

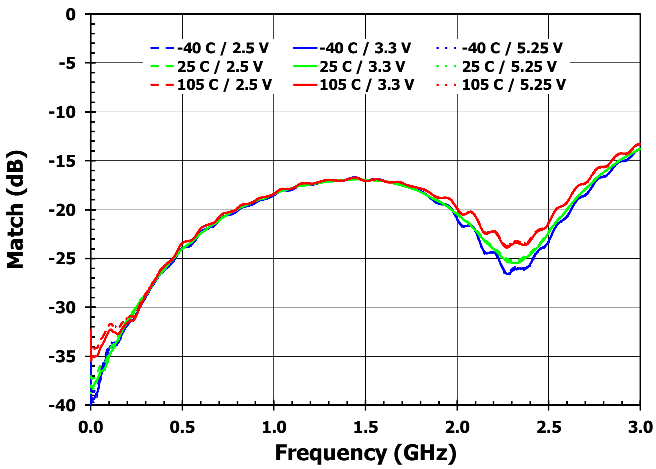
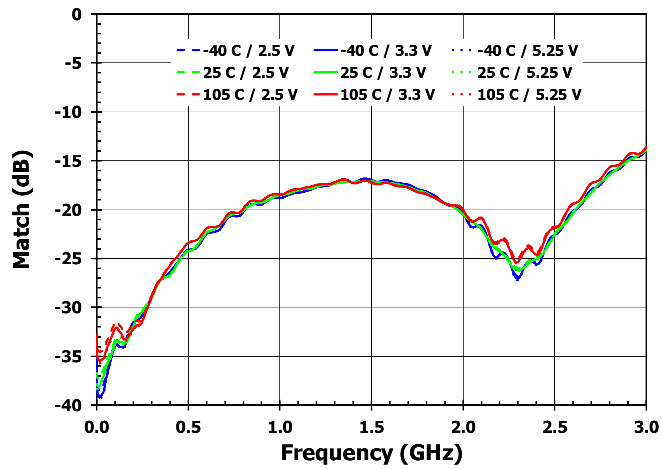


Figure 13. RF2 Return Loss [RF2 On State]



Typical Performance Characteristics - 50Ω Performance

Figure 14. RF1 to RFC Insertion Loss

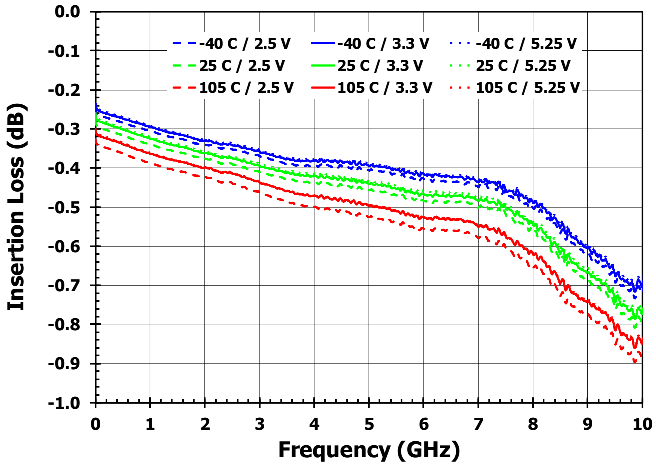


Figure 15. RF2 to RFC Insertion Loss

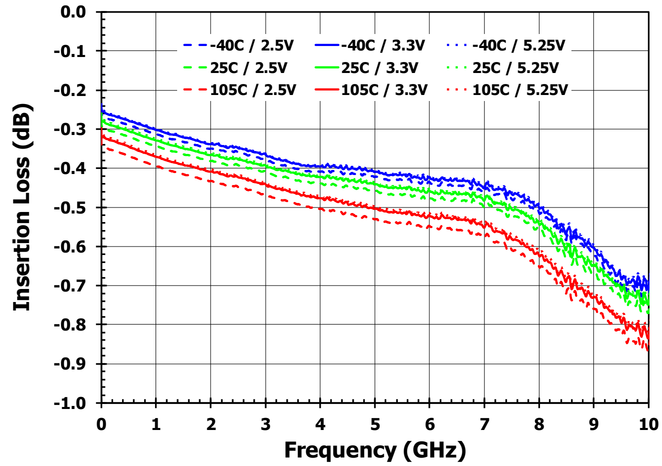


Figure 16. RF1 to RFC Isolation [RF2 On State]

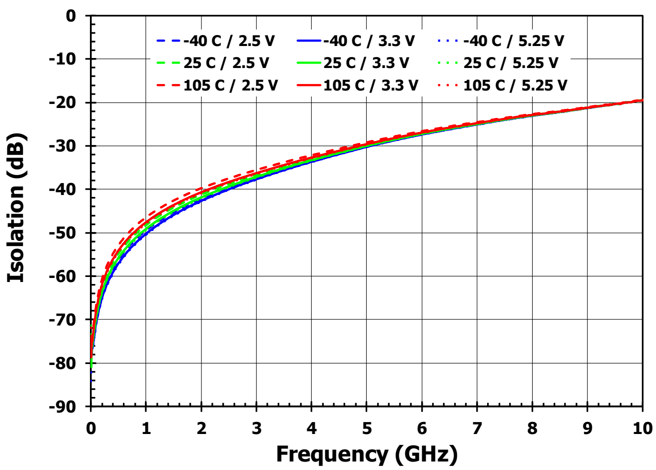


Figure 17. RF2 to RFC Isolation [RF1 On State]

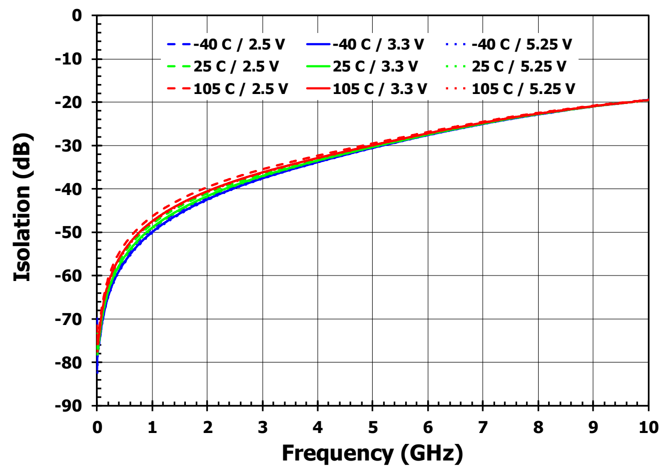


Figure 18. RF1 to RF2 Isolation [RF1 On State]

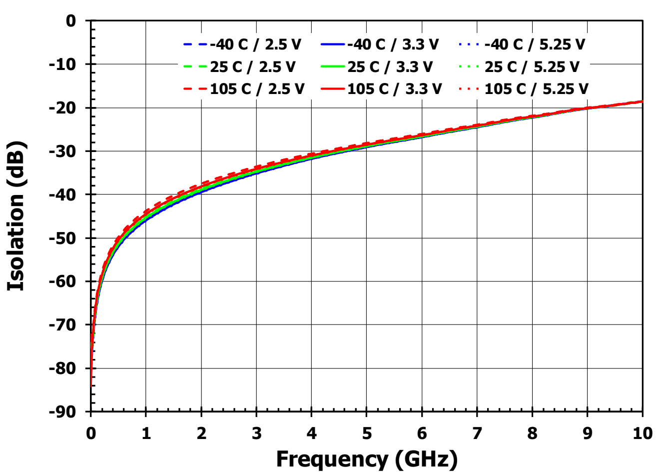
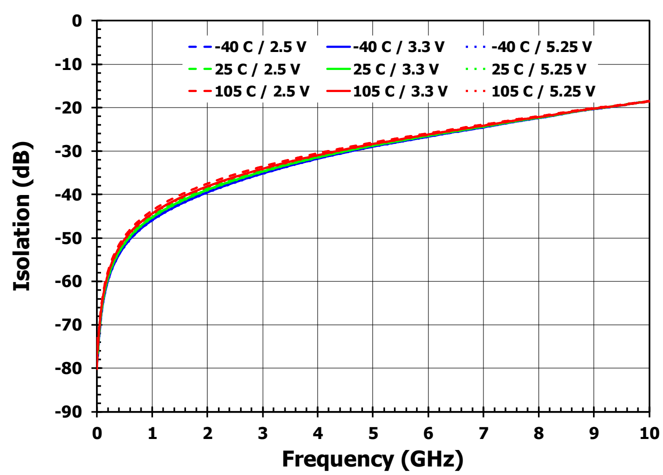


Figure 19. RF1 to RF2 Isolation [RF2 On State]



Typical Performance Characteristics - 50Ω Performance

Figure 20. RFC Return Loss [RF1 On State]

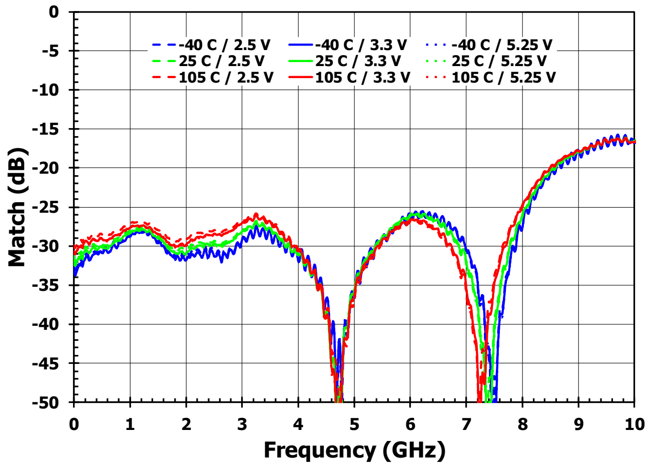


Figure 21. RFC Return Loss [RF2 On State]

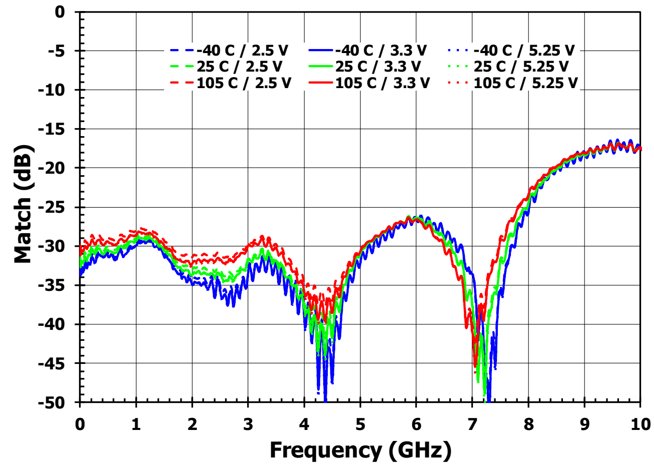


Figure 22. RF1 Return Loss [RF1 On State]

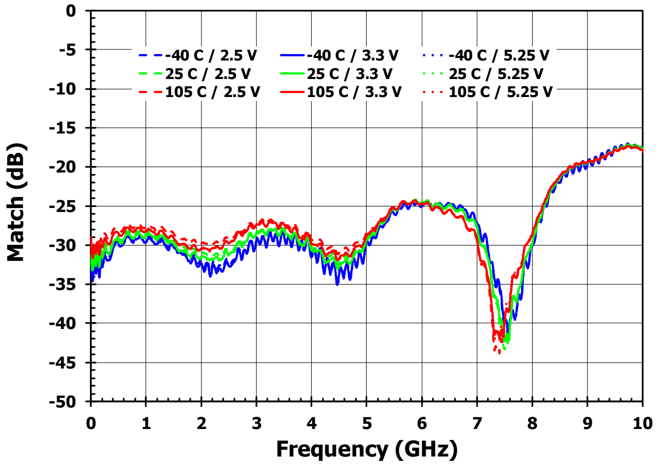


Figure 23. RF2 Return Loss [RF2 On State]

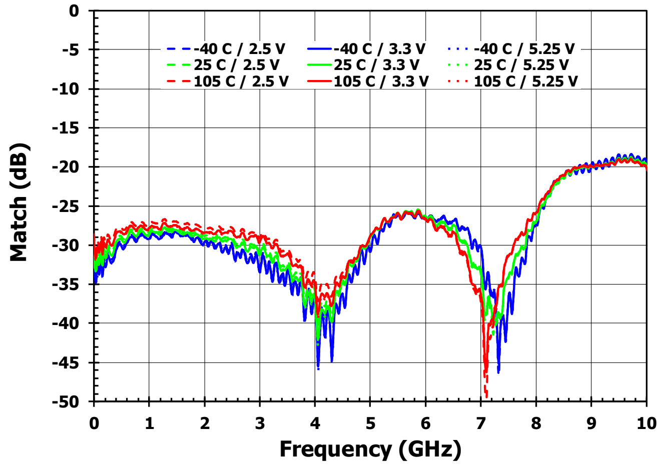


Figure 24. Switching Time [Isolation to Insertion Loss State]

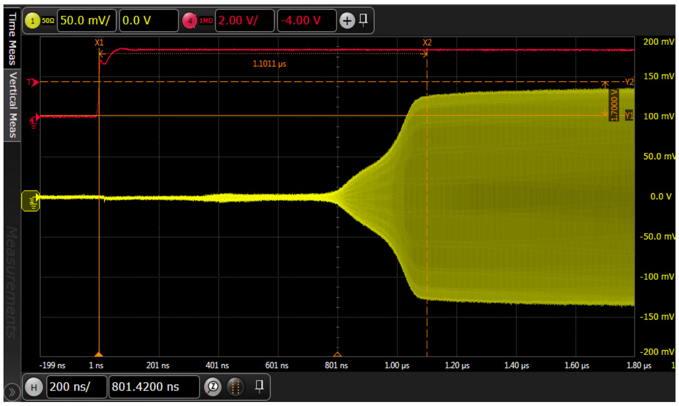


Figure 25. Switching Time [Insertion Loss to Isolation State]

Control Mode

Table 9. Switch Control Truth Table

V_{CTL} (pin 10)	LS (pin 11)	Switch State
HIGH	HIGH	RFC to RF2 Insertion Loss State
LOW	HIGH	RFC to RF1 Insertion Loss State
HIGH	LOW	RFC to RF1 Insertion Loss State
LOW	LOW	RFC to RF2 Insertion Loss State

Application Information

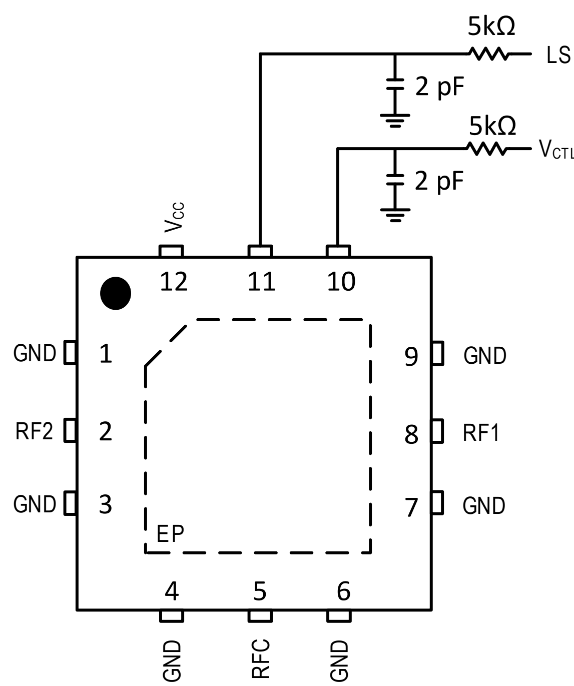
Power Supplies

A common V_{CC} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V / 20µs. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps up or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 7 and 8 as shown below.

Figure 26. Control Pin Interface Schematic



75Ω Evaluation Kit Picture

Figure 27. Top View (75Ω)

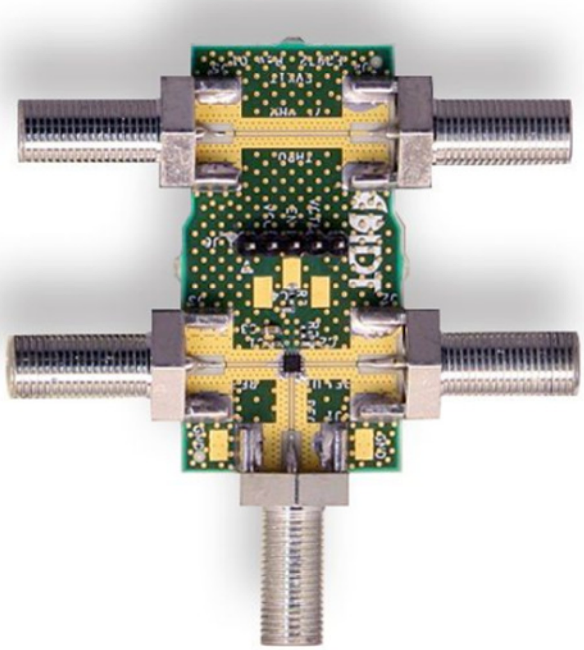
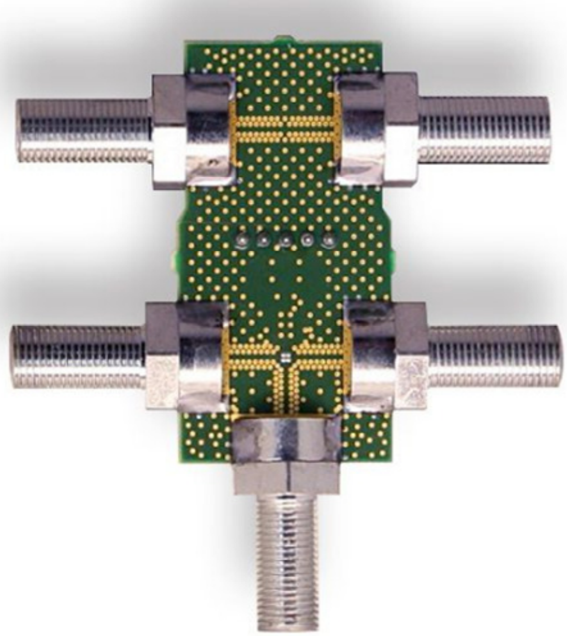


Figure 28. Bottom View (75Ω)



50Ω Evaluation Kit Picture

Figure 29. Top View (50Ω)

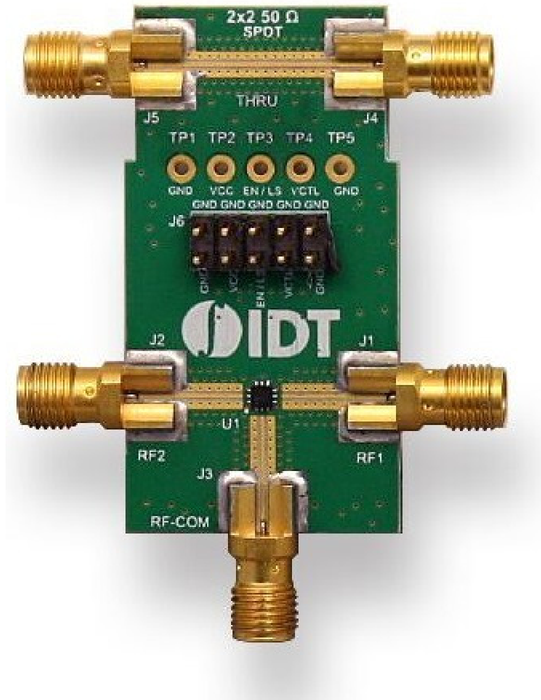
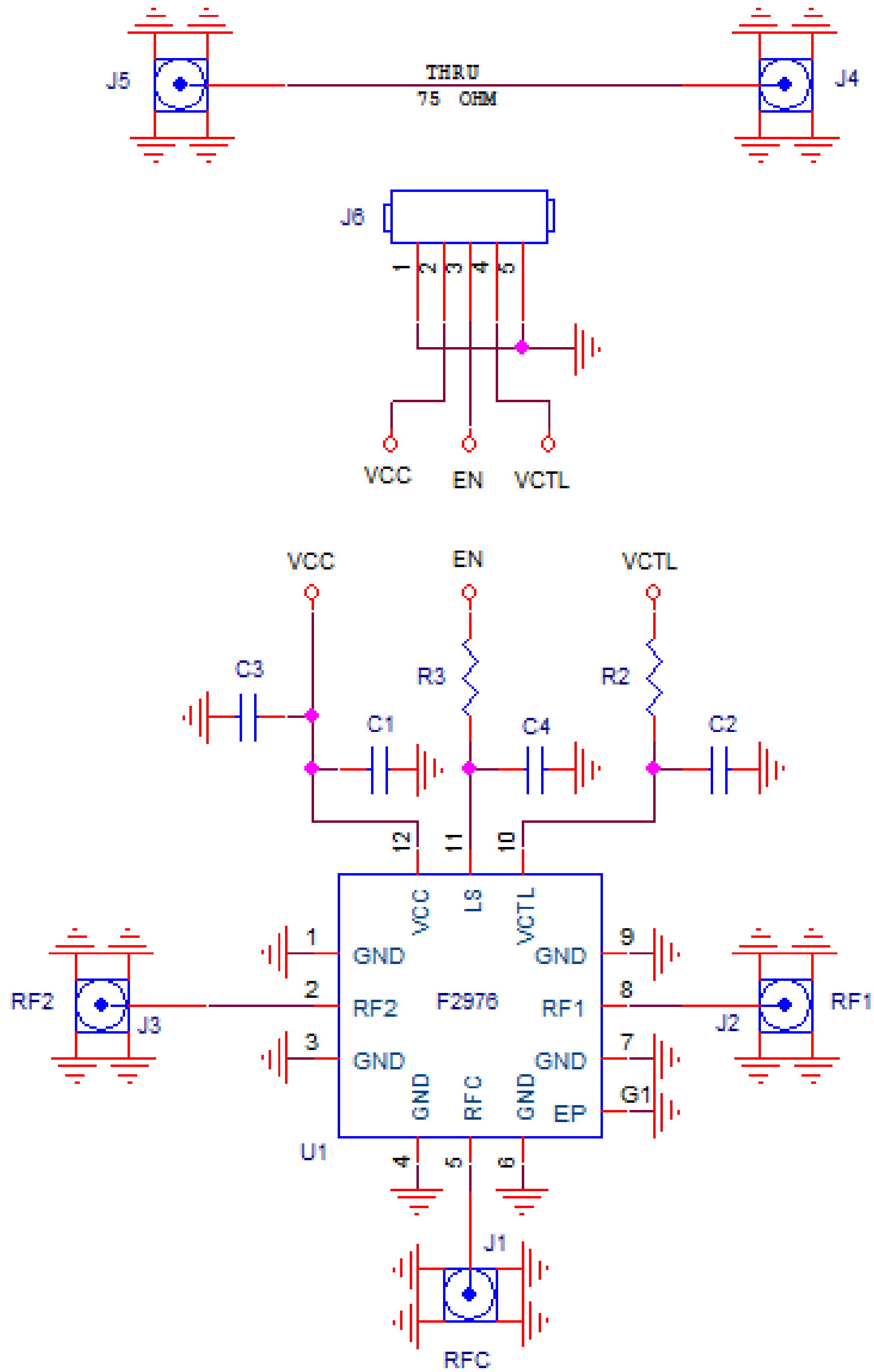


Figure 30. Bottom View (50Ω)

75Ω Evaluation Kit / Applications Circuit

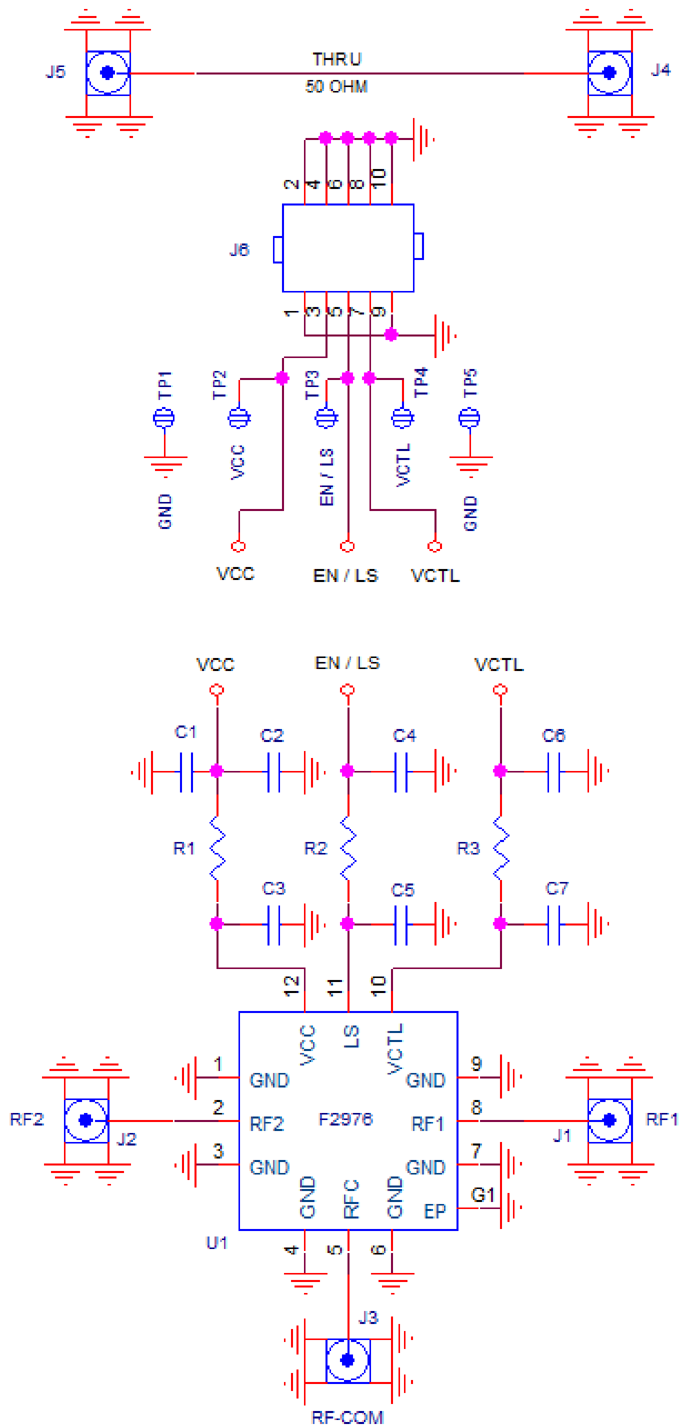
Figure 31. Electrical Schematic (75Ω)



Note: The F2976 75Ω EVKit reuses the 75Ω PCB from the F2972 and requires pin 1 of the F2976 to be rotated by 90 degrees clockwise from the F2972 PCB pin 1 marking, for proper assembly.

50Ω Evaluation Kit / Applications Circuit

Figure 32. Electrical Schematic (50Ω)



Note: The F2976 50Ω EVKit reuses the 50Ω PCB from the F2972 and requires pin 1 of the F2976 to be rotated by 90 degrees clockwise from the F2972 PCB pin 1 marking, for proper assembly.

Table 10. 75Ω Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1	1	0.1µF ±10%, 16V, X7R, Ceramic Capacitor (0402)	GRM155R71C104KA88D	Murata
C2, C4	2	100pF ±5% 50V, C0G, Ceramic Capacitor (0402)	GRM1555C1H101JA01D	Murata
C3	1	0.01µF ±5% 50V, X7R, Ceramic Capacitor (0603)	GRM188R71H103JA01D	Murata
R2, R3	2	100Ω 1/10W, Resistor (0402)	ERJ-2RKF1000X	Panasonic
J1 – J5	5	F-Type Edge Mount	222181	Amphenol RF
J6	1	Conn Header Vert 5x1 Pos Gold	68002-205HLF	Amphenol FCI
U1	1	SP2T Switch 2mm x 2mm 12-pin TQFN	F2976NEGK	IDT
	1	Printed Circuit Board [a]	F2972 75Ω PCB	IDT

a. The F2976 75Ω EVKit reuses the 75Ω PCB from the F2972 and requires pin 1 of the F2976 to be rotated by 90 degrees clockwise from the F2972 PCB pin 1 marking, for proper assembly.

Table 11. 50Ω Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1 – C7	0	Not Installed (0402)		
R1– R3	3	0Ω 1/10 W, Resistor (0402)	ERJ-2GE0R00X	Panasonic
J1 – J5	5	SMA Edge Mount	142-0761-881	Cinch Connectivity
J6	1	Conn Header 10 Pos 0.100” Str 15 Au	68602-210HLF	Amphenol FCI
TP1, TP2, TP3, TP4, TP5	0	Not Installed Test Point Loop		
U1	1	SP2T Switch 2mm x 2mm 12-pin TQFN	F2976NEGK	IDT
	1	Printed Circuit Board [a]	F2972 50Ω PCB	IDT

a. The F2976 50Ω EVKit reuses the 50Ω PCB from the F2972 and requires pin 1 of the F2976 to be rotated by 90 degrees clockwise from the F2972 PCB pin 1 marking, for proper assembly.

Evaluation Kit (EVKit) Operation

External Supply Setup

Set up a V_{CC} power supply in the voltage range of 2.5V to 5.25V with the power supply output disabled.

For the 75Ω EVKit, connect the disabled Vcc supply connection to J6 pin 2 and GND to J6 pins 1 or 5.

For the 50Ω EVKit, connect the disabled Vcc supply connection to J6 pin 3 and GND to J6 pin 1, 2, 4, 6, 8, 9, or 10.

Logic Control Setup

With the logic control lines disabled set the HIGH and LOW logic levels to satisfy the levels stated in the electrical specifications table.

For the 75Ω EVKit, connect the disabled logic control lines to J6 EN (pin 3) and V_{CTL} (pin 4).

For the 50Ω EVKit, connect the disabled logic control lines to J6 EN / LS (pin 5) and V_{CTL} (pin 7).

See Table 9 for the logic truth table.

Turn On Procedure

Setup the supplies and EVKit as noted in the External Supply Setup and Logic Control Setup sections above.

Enable the V_{CC} supply.

Enable the logic control signals.

Set the logic settings to achieve the desired Table 9 configuration. Note that external control logic should not be applied without V_{CC} being present.

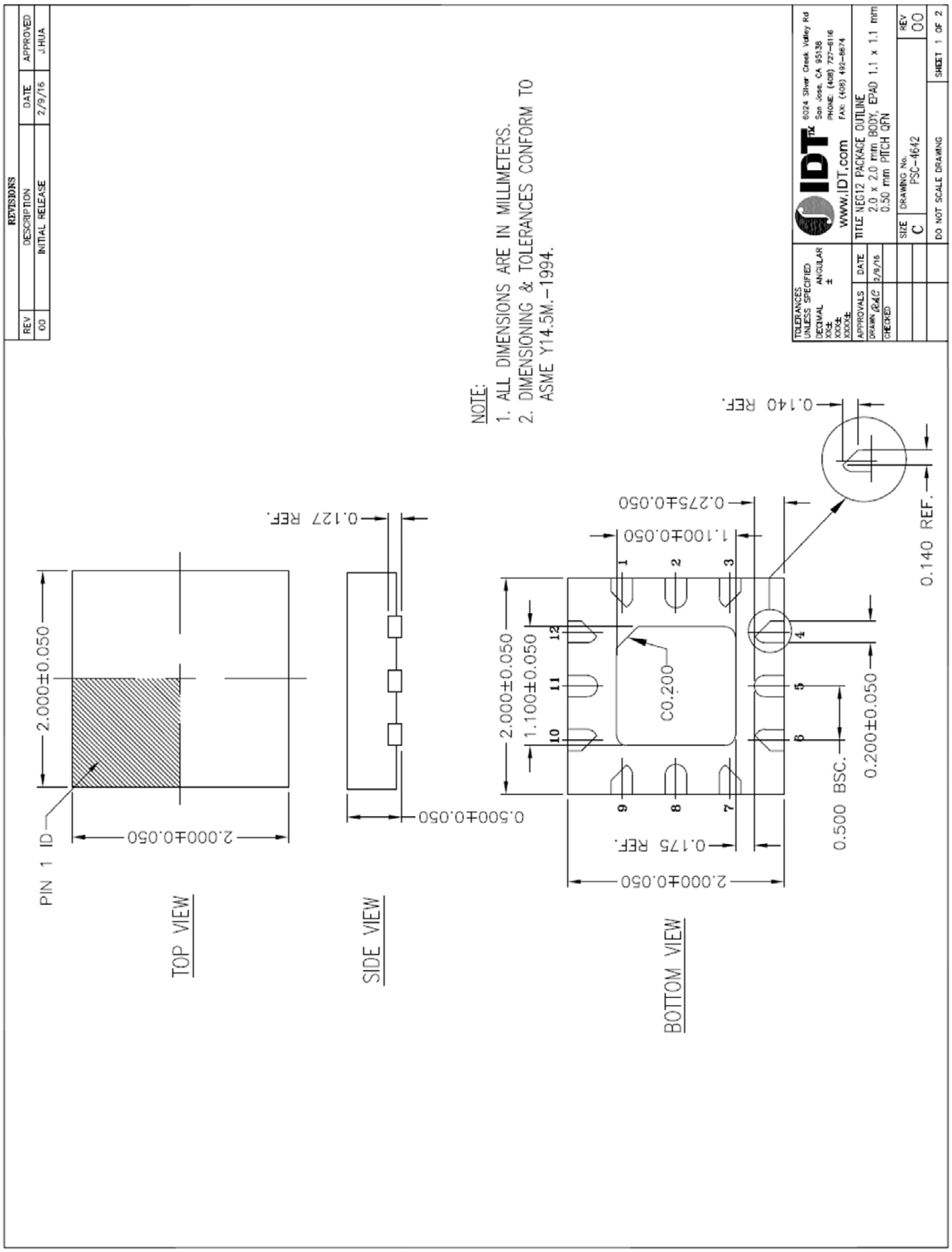
Turn Off Procedure

Set the logic control pins to a logic LOW.

Disable the V_{CC} supply.

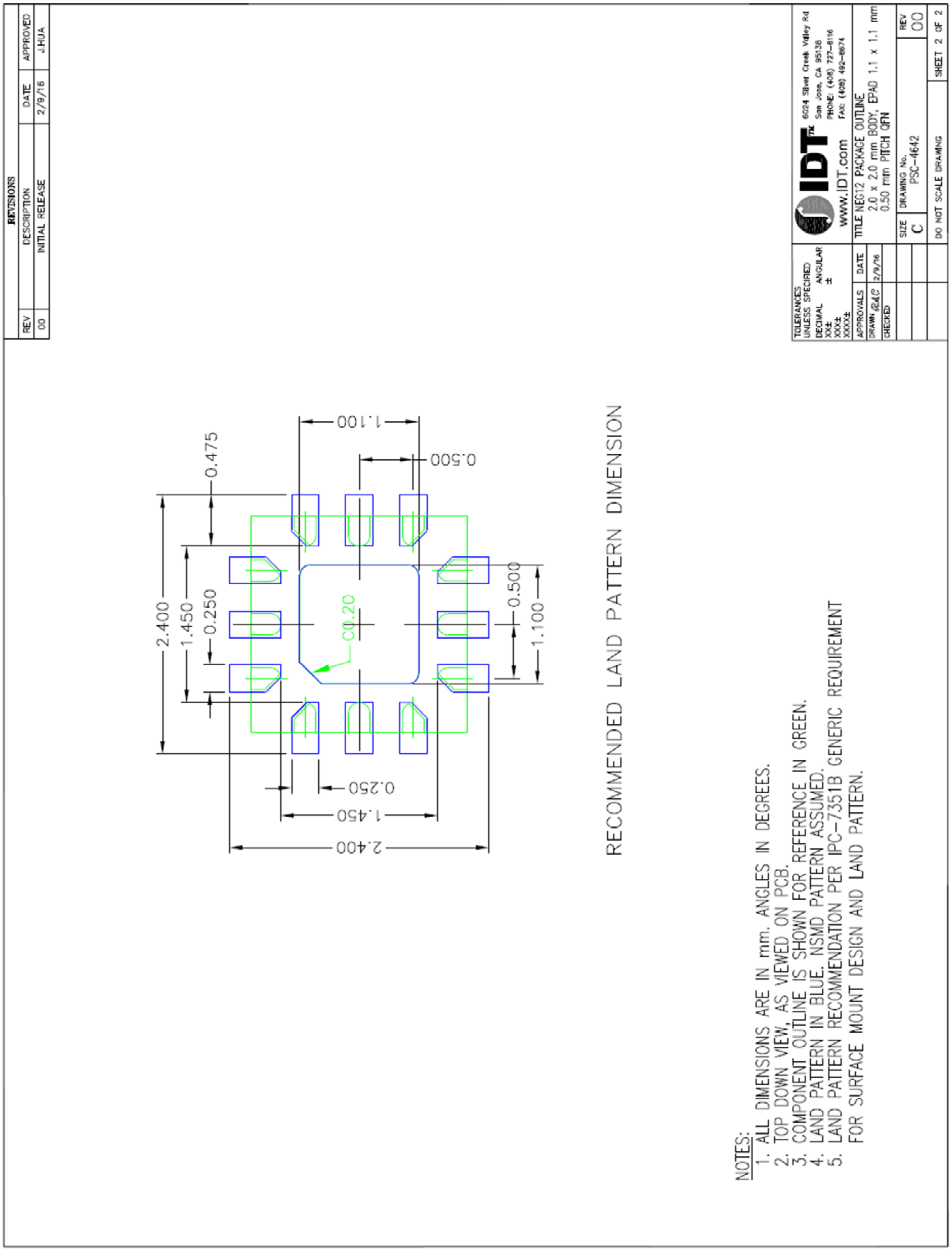
Package Drawings

Figure 33. Package Outline Drawing NEG12 PSC-4642

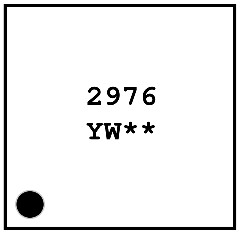


Recommended Land Pattern

Figure 34. Recommended Land Pattern NEG12 PSC-4642



Marking Diagram



Line 1 - 2976 = Abbreviated part number.
Line 2 - Y = Year code.
Line 2 - W = Work week code.
Line 2 - ** = Sequential alpha for lot traceability.

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F2976NEGK	2mm x 2mm x 0.5mm 12-VFQFP-N	MSL1	Cut Reel	-40°C to +105°C
F2976NEGK8	2mm x 2mm x 0.5mm 12-VFQFP-N	MSL1	Tape and Reel	-40°C to +105°C
F2976EVBI-75OHM	75Ω Evaluation Board			
F2976EVBI-50OHM	50Ω Evaluation Board			

Revision History

Revision	Revision Date	Description of Change
Rev O	2017-Apr-19	Initial Release

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www.renesas.com/contact/