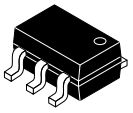
Low-Voltage SPDT Analog Switch or 2:1 Multiplexer / De-multiplexer Bus Switch

NC7SB3157, FSA3157

SIP6
CASE 127EB

SC−88 (SC−70 6 Lead)
CASE 419AD−01



Description

The NC7SB3157 / FSA3157 is a high−performance, single−pole / double−throw (SPDT) analog switch or 2:1 multiplexer / de−multiplexer bus switch.

The device is fabricated with advanced sub−micron CMOS technology to achieve high−speed enable and disable times and low on resistance. The break−before−make select circuitry prevents disruption of signals on the B Port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5 V V_{CC} operating range. The control input tolerates voltages up to 5.5 V, independent of the V_{CC} operating range.

Features

- Useful in Both Analog and Digital Applications
- Space−Saving, SC70 6−Lead Surface Mount Package
- Ultra−Small, MicroPak™ Leadless Package
- Low On Resistance: < 10 Ω on Typical at 3.3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Rail−to−Rail Signal Handling
- Power−Down, High−Impedance Control Input
- Over−Voltage Tolerance of Control Input to 7.0 V
- Break−Before−Make Enable Circuitry
- 250 MHz, 3 dB Bandwidth
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

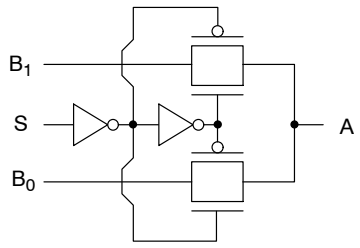
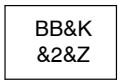


Figure 1. Logic Symbol

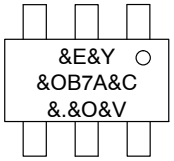
MARKING DIAGRAM

SIP6



BB	= Specific Device Code
&K	= Lot Code
&2	= Date Code (Year and Week)
&Z	= Assembly Location

SC−88



&E	= Designates Space
&Y	= Date Code (Year)
&O	= Plant Code
B7A	= Specific Device Code
&C	= Die Run Code
&.	= Pin 1 Dot
&V	= Date (Week)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

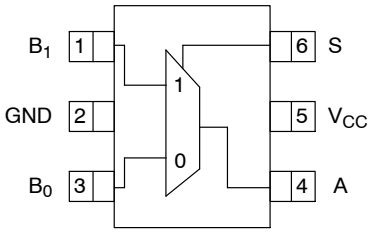


Figure 2. Pin Assignments SC70

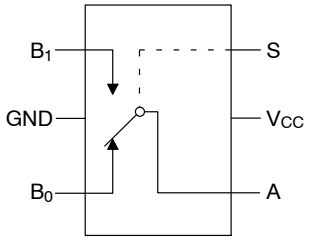


Figure 3. Analog Symbol

FUNCTION TABLE

Input (S)	Function
Logic Level Low	B_0 Connected to A
Logic Level High	B_1 Connected to A

PIN DESCRIPTIONS

Pin Names	Description
A, B_0, B_1	Data Ports
S	Control Input

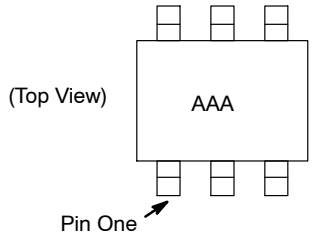


Figure 4. Pin One Orientation

NOTE: Orientation of top mark determines pin one location. Read the top product code mark left to right and pin one is the lower left pin (see Figure 4).

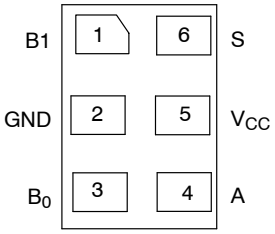


Figure 5. Pad Assignments for MicroPak

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	−0.5	+7.0	V
V_S	DC Switch Voltage (Note 1)	−0.5	V_{CC} +0.5	V
V_{IN}	DC Input Voltage (Note 1)	−0.5	+7.0	V
I_{IK}	DC Input Diode Current at V_{IN} < 0 V	–	−50	mA
I_{OUT}	DC Output Current	–	128	mA
I_{CC}/I_{GND}	DC V_{CC} or Ground Current	–	±100	mA
T_{STG}	Storage Temperature Range	−65	+150	°C
T_J	Junction Temperature Under Bias	–	+150	°C
T_L	Junction Lead Temperature (Soldering, 10 seconds)	–	+260	°C
MSL	Moisture Sensitivity Level (JEDEC J−STD−020A)	–	1	Level
P_D	Power Dissipation at +85°C	–	180	mW
ESD	Human Body Model, JESD22−A114	–	4000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage Operating		1.65	5.50	V
V_{IN}	Control Input Voltage (Note 2)		0	V_{CC}	V
V_{IN}	Switch Input Voltage (Note 2)		0	V_{CC}	V
V_{OUT}	Output Voltage (Note 2)		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
f_r, t_f	Input Rise and Fall Time	Control Input V_{CC} = 2.3 V – 3.6 V	0	10	ns/V
		Control Input V_{CC} = 4.5 V – 5.5 V	0	5	ns/V
θ_{JA}	Thermal Resistance, SC70		–	270	°C/W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Control input must be held HIGH or LOW; it must not float.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage		1.65–1.95	0.75 V_{CC}	–	–	0.75 V_{CC}	–	V
			2.3–5.5	0.7 V_{CC}	–	–	0.7 V_{CC}	–	V
V_{IL}	Low Level Input Voltage		1.65–1.95	–	–	0.25 V_{CC}	–	0.25 V_{CC}	V
			2.3–5.5	–	–	0.3 V_{CC}	–	0.3 V_{CC}	V
I_{IN}	Input Leakage Current	0 ≤ V_{IN} ≤ 5.5 V	0–5.5	–	±0.05	±0.1	–	±1	μA
I_{OFF}	Off State Leakage Current	0 ≤ A, B ≤ V_{CC}	1.65–5.5	–	±0.05	±0.1	–	±1	μA
R_{ON}	Switch On Resistance (Note 3)	V_{IN} = 0 V, I_O = 30 mA	4.5	–	3.0	7.0	–	7.0	Ω
		V_{IN} = 2.4 V, I_O = −30 mA	4.5	–	5.0	12.0	–	12.0	
		V_{IN} = 4.5 V, I_O = −30 mA	4.5	–	7.0	15.0	–	15.0	
		V_{IN} = 0 V, I_O = 24 mA	3.0	–	4.0	9.0	–	9.0	
		V_{IN} = 3 V, I_O = −24 mA	3.0	–	10.0	20.0	–	20.0	
		V_{IN} = 0 V, I_O = 8 mA	2.3	–	5.0	12.0	–	12.0	
		V_{IN} = 2.3 V, I_O = −8 mA	2.3	–	13.0	30.0	–	30.0	
		V_{IN} = 0 V, I_O = 4 mA	1.65	–	6.5	20.0	–	20.0	
		V_{IN} = 1.65 V, I_O = −4 mA	1.65	–	17.0	50.0	–	50.0	
I_{CC}	Quiescent Supply Current; All Channels On or Off	V_{IN} = V_{CC} or GND I_{OUT} = 0	5.5	–	–	1	–	10	μA
	Analog Signal Range		V_{CC}	0	–	V_{CC}	0	V_{CC}	V
R_{RANGE}	On Resistance Over Signal Range (Note 3, 7)	I_A = −30 mA, 0 ≤ V_{Bn} ≤ V_{CC}	4.5	–	–	–	–	25.0	Ω
		I_A = −24 mA, 0 ≤ V_{Bn} ≤ V_{CC}	3.0	–	–	–	–	50.0	
		I_A = −8 mA, 0 ≤ V_{Bn} ≤ V_{CC}	2.3	–	–	–	–	100	
		I_A = −4 mA, 0 ≤ V_{Bn} ≤ V_{CC}	1.65	–	–	–	–	300	
ΔR_{ON}	On Resistance Match Between−Channels (Note 3, 4, 5)	I_A = −30 mA, V_{Bn} = 3.15	4.5	–	0.15	–	–	–	Ω
		I_A = −24 mA, V_{Bn} 2.1	3.0	–	0.2	–	–	–	
		I_A = −8 mA, V_{Bn} = 1.6	2.3	–	0.5	–	–	–	
		I_A = −4 mA, V_{Bn} = 1.15	1.65	–	0.50	–	–	–	
R_{flat}	On Resistance Flatness (Note 3, 4, 6)	I_A = −30 mA, 0 ≤ V_{Bn} ≤ V_{CC}	5.0	–	6.0	–	–	–	Ω
		I_A = −24 mA, 0 ≤ V_{Bn} ≤ V_{CC}	3.3	–	12.0	–	–	–	
		I_A = −8 mA, 0 ≤ V_{Bn} ≤ V_{CC}	2.5	–	28.0	–	–	–	
		I_A = −4 mA, 0 ≤ V_{Bn} ≤ V_{CC}	1.8	–	125	–	–	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B Ports).
4. Parameter is characterized, but not tested in production.
5. ΔR_{ON} = R_{ON} max − R_{ON} minimum measured at identical V_{CC}, temperature, and voltage levels.
6. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.
7. Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Unit	Figure Number
				Min.	Typ.	Max.	Min.	Max.		
t_{PHL}, t_{PLH}	Propagation Delay Bus−to−Bus (Note 8)	V_I = OPEN	1.65–1.95	–	–	3.5	–	3.5	ns	Figure 12 Figure 13
			2.3–2.7	–	–	1.2	–	1.2		
			3.0–3.6	–	–	0.8	–	0.8		
			4.5–5.5	–	–	0.3	–	0.3		
t_{PZL}, t_{PZH}	Output Enable Time Turn−On Time (A to B_n)	V_I = 2 x V_{CC} for t_{PZL} V_I = 0 V for t_{PZH}	1.65–1.95	7.0	–	23.0	7.0	24.0	ns	Figure 12 Figure 13
			2.3–2.7	3.5	–	13.0	3.5	14.0		
			3.0–3.6	2.5	–	6.9	2.5	7.6		
			4.5–5.5	1.7	–	5.2	1.7	5.7		
t_{PLZ}, t_{PHZ}	Output Disable Time Turn−Off Time (A Port to B Port)	V_I = 2 x V_{CC} for t_{PLZ} V_I = 0 V for t_{PHZ}	1.65–1.95	3.0	–	12.5	3.0	13.0	ns	Figure 12 Figure 13
			2.3–2.7	2.0	–	7.0	2.0	7.5		
			3.0–3.6	1.5	–	5.0	1.5	5.3		
			4.5–5.5	0.8	–	3.5	0.8	3.8		
t_{B-M}	Break−Before−Make Time (Note 9)		1.65–1.95	0.5	–	–	0.5	–	ns	Figure 14
			2.3–2.7	0.5	–	–	0.5	–		
			3.0–3.6	0.5	–	–	0.5	–		
			4.5–5.5	0.5	–	–	0.5	–		
Q	Charge Injection (Note 9)	C_L = 0.1 nF, V_{GEN} = 0 V	5.0	–	7.0	–	–	–	pC	Figure 15
		R_{GEN} = 0 Ω	3.3		3.0					
OIRR	Off Isolation (Note 10)	R_L = 50 Ω, f = 10 MHz	1.65–5.5	–	–57.0	–	–	–	dB	Figure 16
Xtalk	Crosstalk	R_L = 50 Ω, f = 10 MHz	1.65–5.5	–	–54.0	–	–	–	dB	Figure 17
BW	−3dB Bandwidth	R_L = 50 Ω	1.65–5.5	–	250	–	–	–	MHz	Figure 20
THD	Total Harmonic Distortion (Note 9)	R_L = 600 Ω, 0.5 V_{PP}, f = 600 Hz to 20 KHz	5.0	–	.011	–	–	–	%	–

8. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).
9. Guaranteed by design.
10. Off Isolation = 20 $\log_{10}$ [V_A / V_{Bn}].

CAPATICANCE (T_A = 25°C, f = 1 MHz Capacitance is characterized, but not tested in production.)

Symbol	Parameter	Conditions	Typ.	Max.	Unit	Figure Number
C_{IN}	Control Pin Input Capacitance	V_{CC} = 0 V	2.3	–	pF	–
C_{IO-B}	B Port Off Capacitance	V_{CC} = 5.0 V	6.5	–	pF	Figure 18
C_{IOA-ON}	A Port Capacitance When Switch Is Enabled	V_{CC} = 5.0 V	18.5	–	pF	Figure 19

TYPICAL PERFORMANCE CHARACTERISTICS

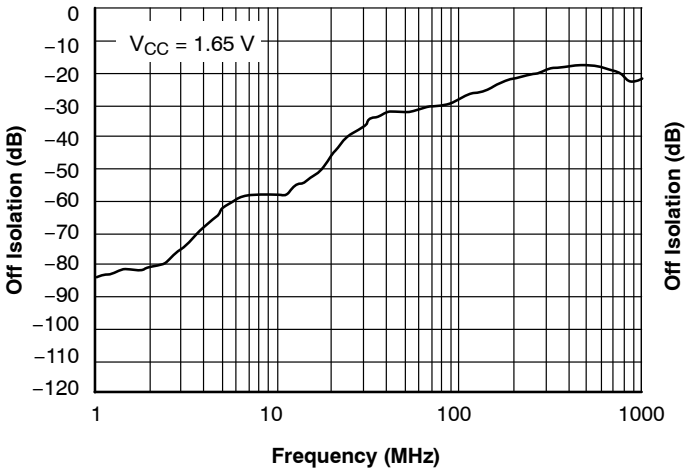


Figure 6. Off Isolation, V_{CC} = 1.65 V

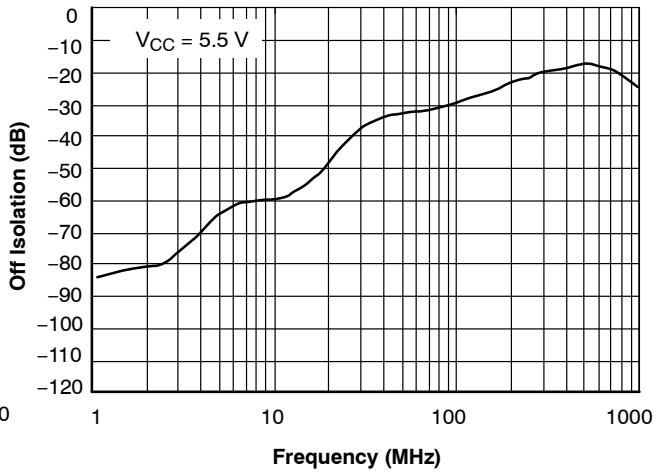


Figure 7. Off Isolation, V_{CC} = 5.5 V

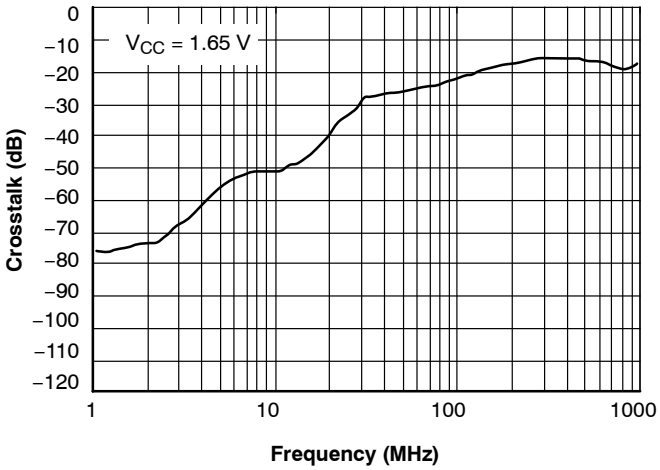


Figure 8. Crosstalk, V_{CC} = 1.65 V

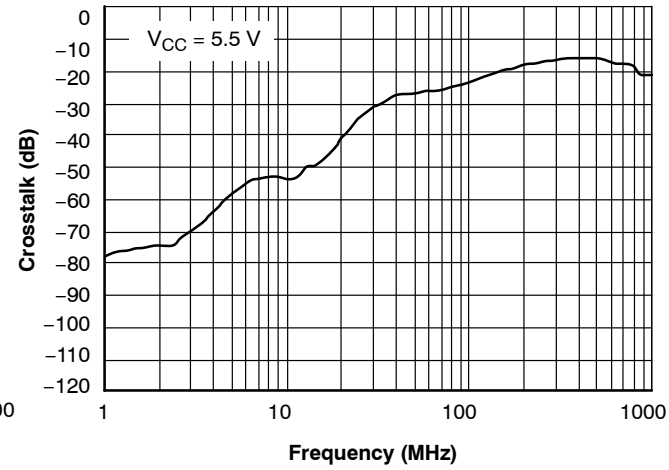


Figure 9. Crosstalk, V_{CC} = 5.5 V

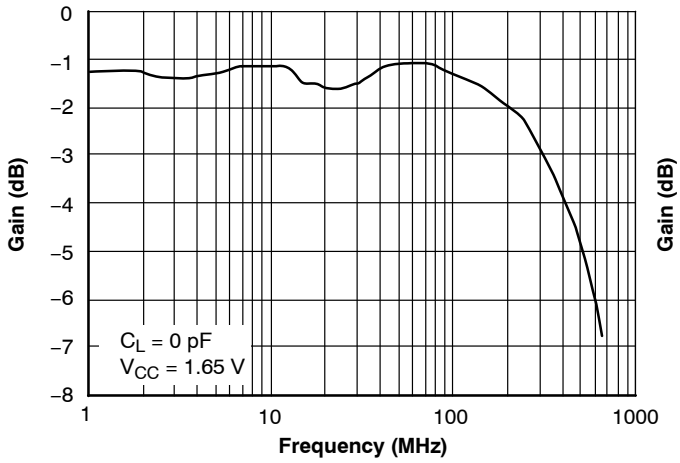


Figure 10. Bandwidth, V_{CC} = 1.65 V

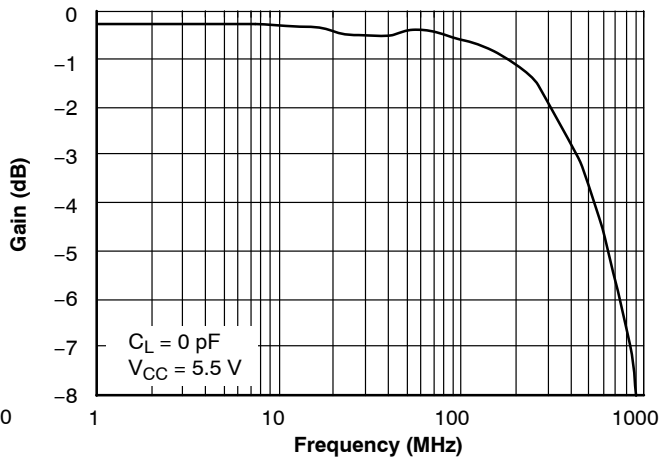
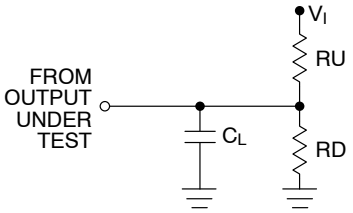


Figure 11. Bandwidth, V_{CC} = 5.5 V

AC LOADING AND WAVEFORMS



NOTE: Input driven by 50 Ω source terminated in 50 Ω C_L includes load and stray capacitance
Input PRR = 1.0 MHz, t_W = 500 ns.

Figure 12. AC Test Circuit

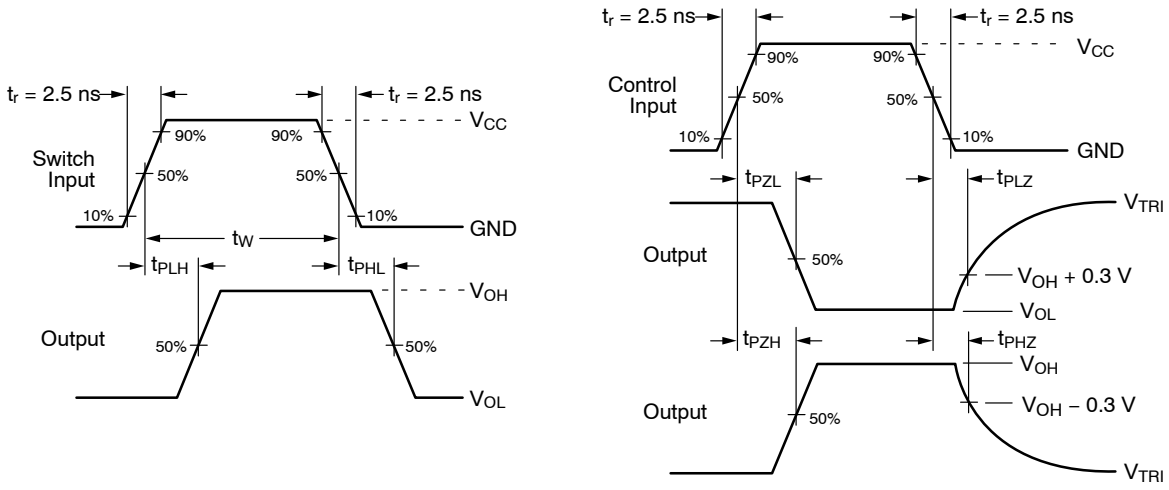


Figure 13. AC Waveforms

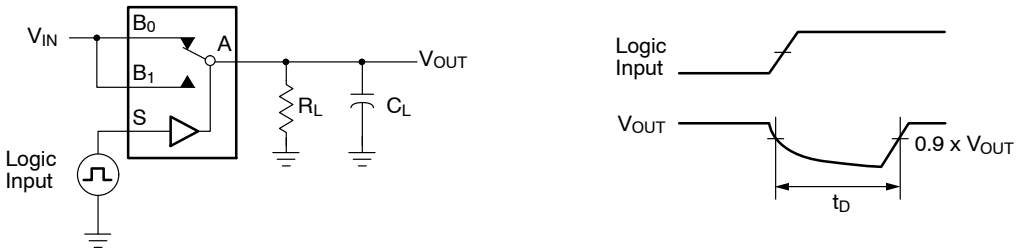


Figure 14. Break−Before−Make Interval Timing

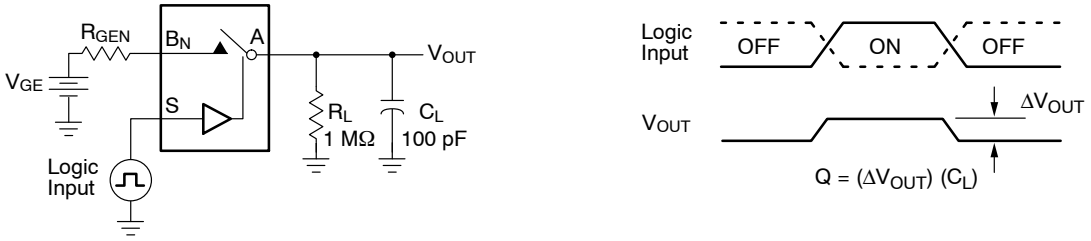


Figure 15. Charge Injection Test

AC LOADING AND WAVEFORMS (Continued)

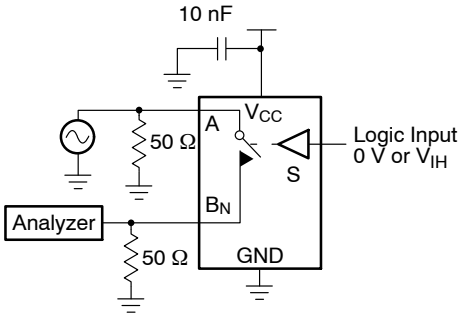


Figure 16. Off Isolation

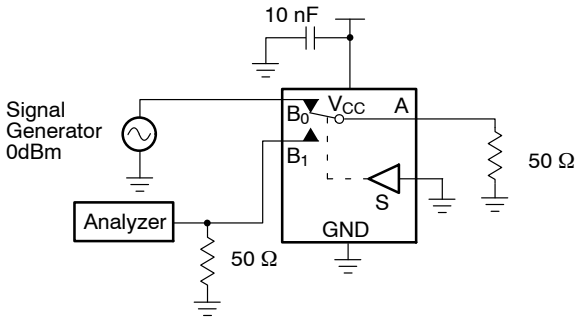


Figure 17. Crosstalk

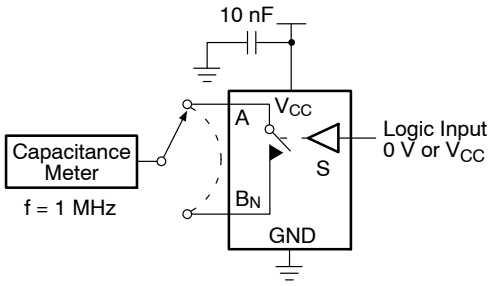


Figure 18. Channel Off Capacitance

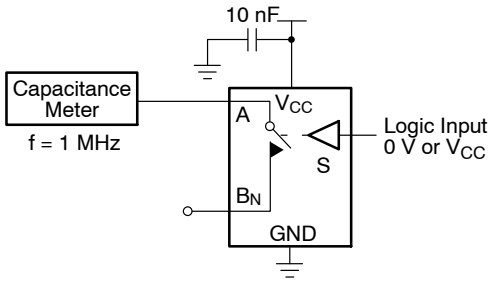


Figure 19. Channel On Capacitance

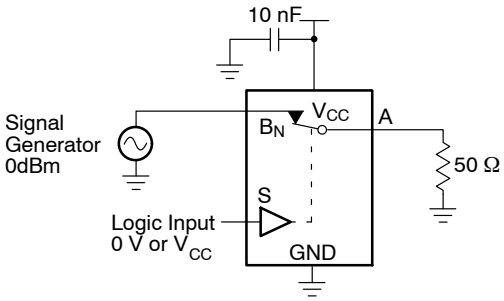


Figure 20. Bandwidth

ORDERING INFORMATION

Part Number	Top Mark	Eco Status	Package Description	Shipping†
NC7SB3157P6X	B7A	RoHS	6−Lead, SC70, EIAJ SC88, 1.25 mm Wide Package	3000 / Tape and Reel
NC7SB3157L6X	BB	RoHS	6−Lead, MicroPak 1.0 mm Wide Package	5000 / Tape and Reel
FSA3157P6X	B7A	RoHS	6−Lead, SC70, EIAJ SC88, 1.25 mm Wide Package	3000 / Tape and Reel
FSA3157L6X	BB	RoHS	6−Lead, MicroPak 1.0 mm Wide Package	5000 / Tape and Reel

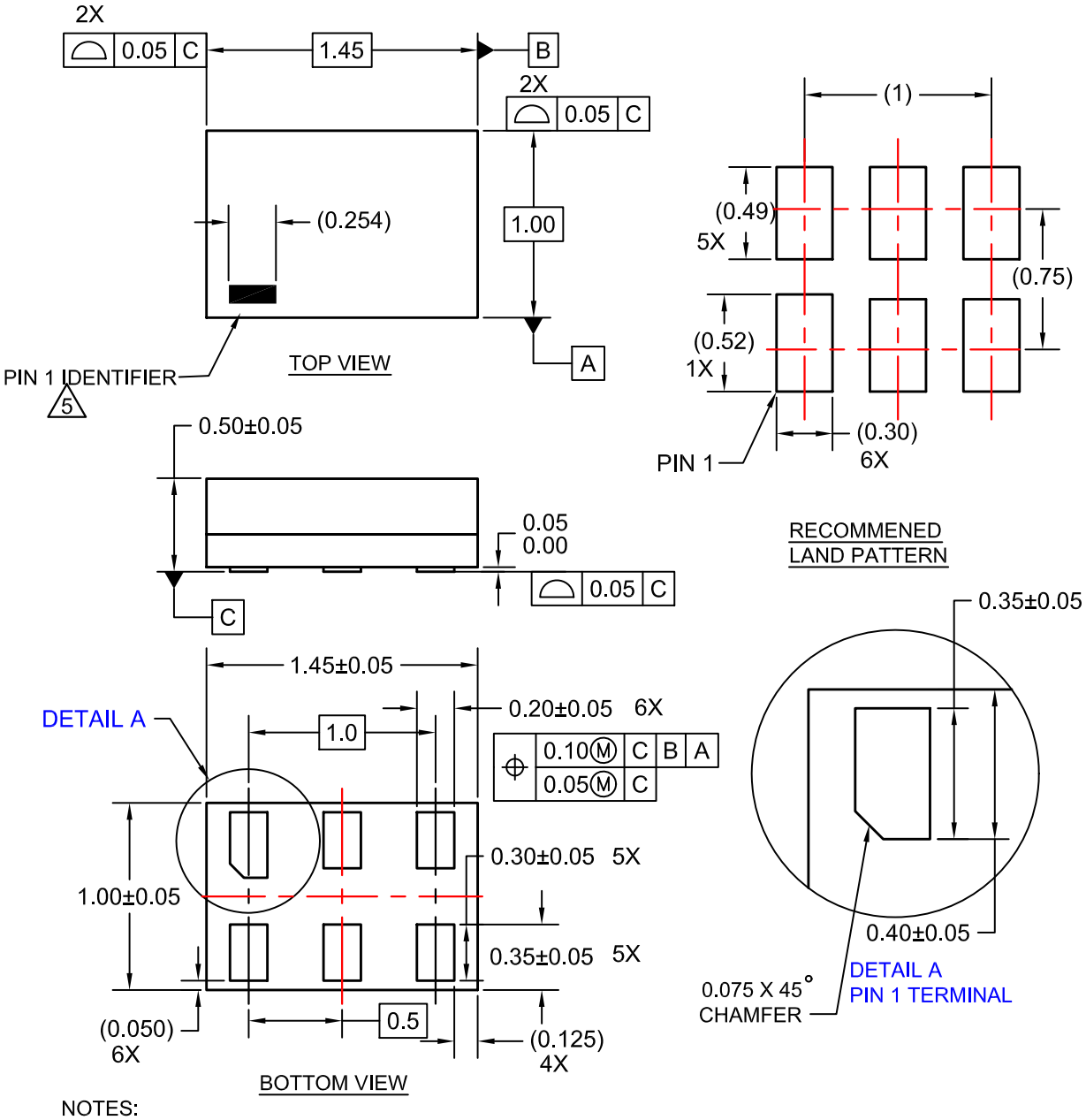
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SIP6 1.45X1.0
CASE 127EB
ISSUE O

DATE 31 AUG 2016



NOTES:

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

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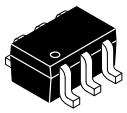
DESCRIPTION:	**SIP6 1.45X1.0**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



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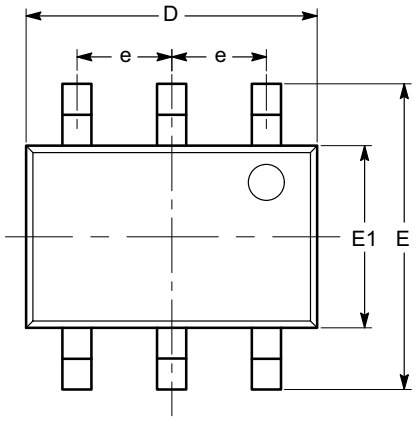
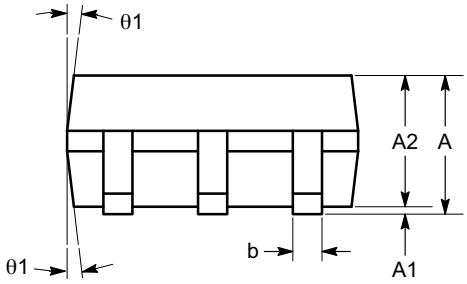
SC−88 (SC−70 6 Lead), 1.25x2
CASE 419AD
ISSUE A

DATE 07 JUL 2010

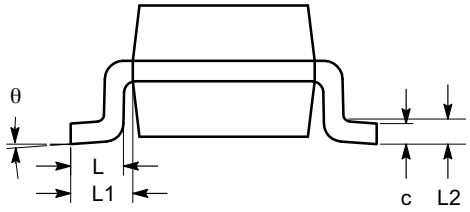


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e		0.65 BSC	
L	0.26	0.36	0.46
L1		0.42 REF	
L2		0.15 BSC	
θ	0°		8°
θ1	4°		10°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-203.

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