

RICOH

RP131x SERIES

LOW ON RESISTANCE / LOW VOLTAGE 1A LDO

NO.EA-174-200128

OUTLINE

The RP131x Series are voltage-regulators with a built-in low ON-resistance transistor and output current is 1A capability. These ICs are capable of the low input voltage (Min.1.6V) and also the minimum output voltage can be set from 0.8V. (The output voltage is fixed in the IC.)

Each of these ICs consists of a voltage reference unit, an error amplifier, a resistor net for setting output voltage, a chip enable circuit, current limit circuits for over-current and short, and a thermal-shutdown circuit.

A standby mode with ultra low supply current can be realized with the chip enable function.

The packages for these ICs are DFN1616-6B and DFN(PLP)1820-6 which are suitable for high density mounting of the ICs on boards. SOT-89-5, HSOP-6J and TO-252-5-P2 with high power dissipation are also available.

FEATURES

- Output Current Min. 1A
- Supply Current Typ. 65 μ A
- Standby Current Typ. 0.15 μ A
- Input Voltage Range 1.6V to 6.5V
- Output Voltage Range 0.8V to 5.5V ⁽¹⁾(0.1V steps)
- Dropout Voltage..... Typ. 0.5V ($V_{OUT}=2.8V$, $I_{OUT}=1A$)
- Ripple Rejection Typ. 70dB ($f=1kHz$, $V_{OUT}=2.8V$)
- Output Voltage Accuracy..... $\pm 1.0\%$
- Temperature-Drift Coefficient of Output Voltage Typ. $\pm 100ppm/^{\circ}C$
- Line Regulation Typ. 0.05%/V
- Load Regulation Typ. 20mV at $I_{OUT}=300mA$, Typ. 80mV at $I_{OUT}=1A$
- Packages DFN1616-6B, DFN(PLP)1820-6, SOT-89-5, HSOP-6J, TO-252-5-P2
- Built-in Inrush current limit circuit Typ. 500mA
- Built-in Fold-Back Protection Circuit Typ. 250mA (Current at short mode)
- Built-in Thermal Shutdown Circuit Thermal Shutdown Temperature ; Typ. 165 $^{\circ}C$
Released Temperature ; Typ. 135 $^{\circ}C$
- Built-in Auto Discharge Function D version
- Ceramic capacitors are recommended to be used with this IC 2.2 μ F or more ($V_{OUT}\leq 3.6V$)
4.7 μ F or more ($V_{OUT}> 3.6V$)

APPLICATIONS

- Power source for battery-powered equipment.
- Power source for portable communication equipment.
- Power source for electrical appliances such as cameras, VCRs and camcorders.
- Power source for Notebook PC.
- Power source for home appliances.

⁽¹⁾ For other voltages, please refer to MARK INFORMATIONS.

RP131x

NO.EA-174-200128

SELECTION GUIDE

The output voltage, auto discharge function, package for the ICs can be selected at the user's request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RP131Lxx1*-TR	DFN1616-6B	5,000 pcs	Yes	Yes
RP131Kxx1*-TR	DFN(PLP)1820-6	5,000 pcs	Yes	Yes
RP131Hxx1*-T1-FE	SOT-89-5	1,000 pcs	Yes	Yes
RP131Sxx1*-E2-FE	HSOP-6J	1,000 pcs	Yes	Yes
RP131Jxx1*-T1-FE	TO-252-5-P2	3,000 pcs	Yes	Yes

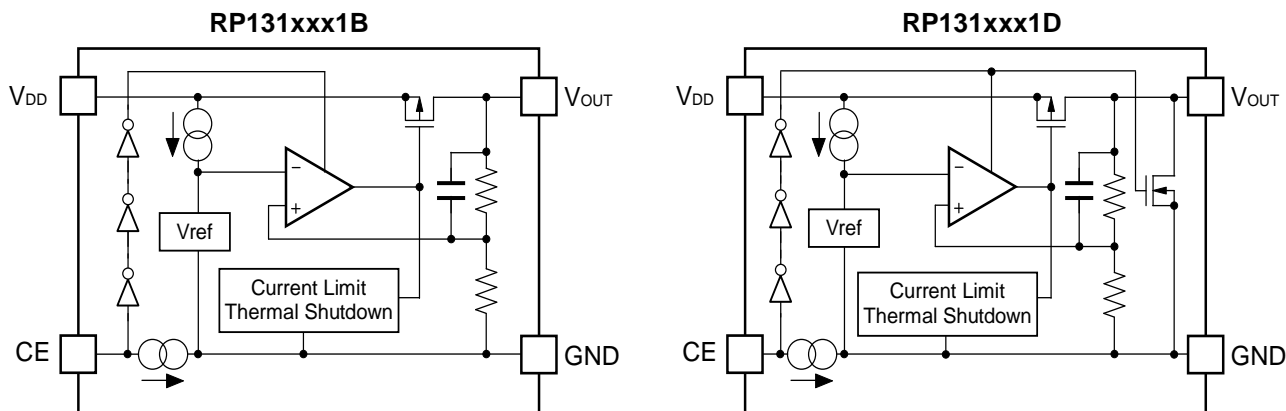
xx : The output voltage can be designated in the range from 0.8V(08) to 5.5V(55) in 0.1V steps.
(For other voltages, please refer to MARK INFORMATIONS.)

* : The auto discharge function at off state are options as follows.⁽¹⁾

(B) without auto discharge function at off state

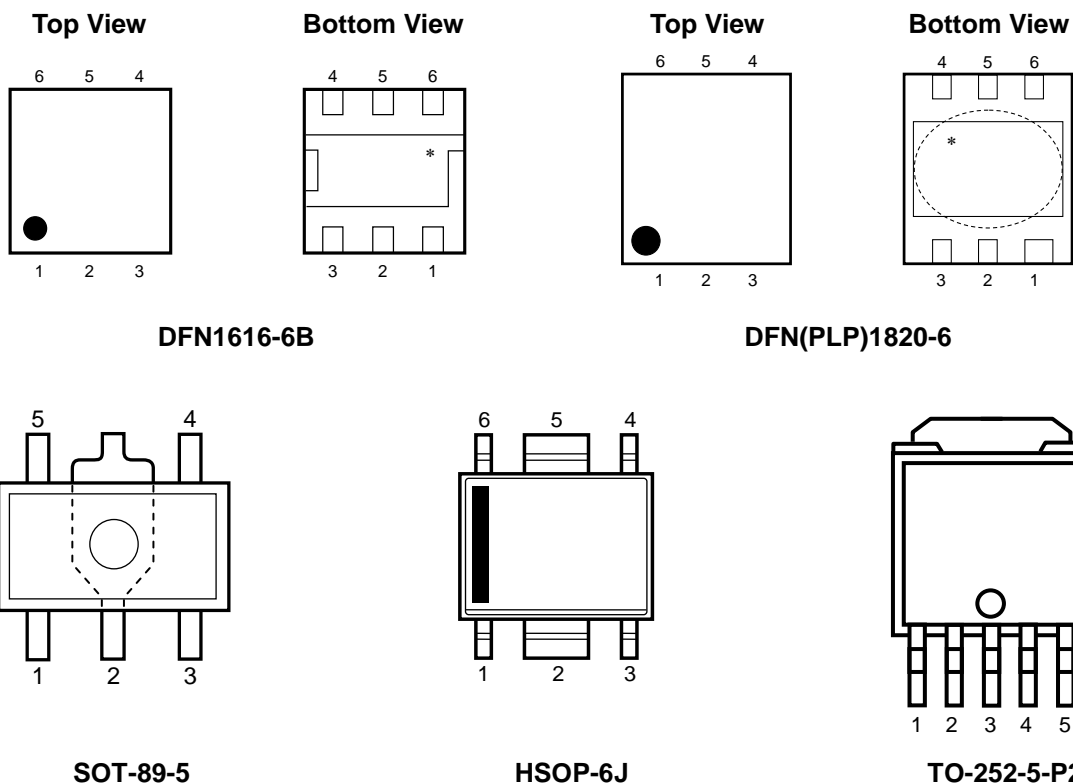
(D) with auto discharge function at off state

BLOCK DIAGRAMS



⁽¹⁾ Auto-discharge function quickly lowers the output voltage to 0V, when the chip enable signal is switched from the active mode to the standby mode, by releasing the electrical charge accumulated in the external capacitor.

PIN DESCRIPTIONS



*Tab is GND level. (They are connected to the reverse side of this IC.) The tab is better to be connected to the GND, but leaving it open is also acceptable.

RP131L (DFN1616-6B) Pin Description

Pin No.	Symbol	Pin Description
1	VOUT	Output Pin ⁽¹⁾
2	VOUt	Output Pin ⁽¹⁾
3	GND	Ground Pin
4	CE	Chip Enable Pin ("H" Active)
5	VDD	Input Pin ⁽¹⁾
6	VDD	Input Pin ⁽¹⁾

⁽¹⁾ When you use this IC, please make sure be wired with 1pin with 2pin and 5pin with 6pin.

*RP131L(DFN1616-6B) is the non-promotion product as of March 2020.

RP131x

NO.EA-174-200128

RP131K (DFN(PLP)1820-6) Pin Description

Pin No.	Symbol	Pin Description
1	VOUT	Output Pin ⁽¹⁾
2	VOUT	Output Pin ⁽¹⁾
3	GND	Ground Pin
4	CE	Chip Enable Pin ("H" Active)
5	VDD	Input Pin ⁽¹⁾
6	VDD	Input Pin ⁽¹⁾

RP131H (SOT-89-5) Pin Description

Pin No.	Symbol	Pin Description
1	NC	No Connection
2	GND	Ground Pin
3	CE	Chip Enable Pin ("H" Active)
4	VDD	Input Pin
5	VOUT	Output Pin

RP131S (HSOP-6J) Pin Description

Pin No.	Symbol	Pin Description
1	VOUT	Output Pin
2	GND	Ground Pin ⁽²⁾
3	NC	No Connection
4	CE	Chip Enable Pin ("H" Active)
5	GND	Ground Pin ⁽²⁾
6	VDD	Input Pin

RP131J (TO-252-5-P2) Pin Description

Pin No.	Symbol	Pin Description
1	V _{OUT}	Output Pin
2	GND	Ground Pin ⁽³⁾
3	GND	Ground Pin ⁽³⁾
4	CE	Chip Enable Pin ("H" Active)
5	V _{DD}	Input Pin

⁽¹⁾ When you use this IC, please make sure be wired with 1pin with 2pin and 5pin with 6pin.

⁽²⁾ When you use this IC, please make sure be wired with 2pin and 5pin.

⁽³⁾ When you use this IC, please make sure be wired with 2pin and 3pin.

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit	
V_{IN}	Input Voltage	7.0	V	
V_{CE}	Input Voltage (CE Pin)	-0.3 to 7.0	V	
V_{OUT}	Output Voltage	-0.3 to $V_{IN}+0.3$	V	
P_D	Power Dissipation ⁽¹⁾	DFN1616-6B, JEDEC STD.51-7	2400	mW
		DFN(PLP)1820-6, JEDEC STD.51-7	2200	
		SOT-89-5, JEDEC STD.51-7	2600	
		HSOP-6J, JEDEC STD.51-7	2700	
		TO-252-5-P2, JEDEC STD.51-7	3800	
T_j	Junction Temperature Range	-40 to 125	°C	
T_{stg}	Storage Temperature Range	-55 to 125	°C	

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	1.6 to 6.5	V
T_a	Operating Temperature Range	-40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

⁽¹⁾ Refer to POWER DISSIPATION for detailed information.

RP131x

NO.EA-174-200128

ELECTRICAL CHARACTERISTICS

$V_{IN} = \text{Set } V_{OUT} + 1V, I_{OUT} = 1mA$

The specification in is checked and guaranteed by design engineering at $-40^{\circ}C \leq T_a \leq 85^{\circ}C$, unless otherwise noted.

RP131xxx1B/D

($T_a = 25^{\circ}C$)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	
V_{OUT}	Output Voltage	$T_a = 25^{\circ}C$	$V_{OUT} > 1.5V$	$\times 0.99$		$\times 1.01$	V
			$V_{OUT} \leq 1.5V$	-15		15	mV
		$-40^{\circ}C \leq T_a \leq 85^{\circ}C$	$V_{OUT} > 1.5V$	×0.974		×1.018	V
			$V_{OUT} \leq 1.5V$	-40		27	mV
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$0.1mA \leq I_{OUT} \leq 300mA$		20	40	mV	
		$0.1mA \leq I_{OUT} \leq 1A$		80	120		
V_{DIF}	Dropout Voltage	Refer to the following table					
I_{SS}	Supply Current	$I_{OUT} = 0mA$ ($V_{IN} = 6.5V$)		65	90	μA	
$I_{standby}$	Standby Current	$V_{CE} = 0V, V_{IN} = 6.5V$		0.15	0.60	μA	
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	Set $V_{OUT} + 0.5V \leq V_{IN} \leq 6.5V$ *However, $V_{IN} \geq 1.6V$		0.05	0.1	%/V	
RR	Ripple Rejection	$f = 1kHz$ Ripple 0.2Vp-p $I_{OUT} = 100mA$	$V_{OUT} \leq 3.3V$		70	dB	
			$V_{OUT} > 3.3V$		60		
V_{IN}	Input Voltage		1.6		6.5	V	
I_{LIM}	Output Current Limit		1			A	
$\frac{\Delta V_{OUT}}{\Delta T_a}$	Output Voltage Temperature Coefficient	$-40^{\circ}C \leq T_a \leq 85^{\circ}C$		± 100		ppm/ $^{\circ}C$	
I_{SC}	Short Current Limit	$V_{OUT} = 0V$		250		mA	
I_{PD}	CE Pull-down Current			0.3		μA	
V_{CEH}	CE Input Voltage "H"		1.0			V	
V_{CEL}	CE Input Voltage "L"				0.4	V	
e_n	Output Noise	$BW = 10Hz \text{ to } 100kHz, I_{OUT} = 1mA$		45		μV_{rms}	
T_{TSD}	Thermal Shutdown Temperature	Junction Temperature		165		$^{\circ}C$	
T_{TSR}	Thermal Shutdown Released Temperature	Junction Temperature		135		$^{\circ}C$	
R_{LOW}	Low Output Nch Tr. ON Resistance (of D version)	$V_{IN} = 4.0V, V_{CE} = 0V$		30		Ω	

All test items listed under Electrical Characteristics are done under the pulse load condition ($T_j \approx T_a = 25^{\circ}C$) except for Output Noise, Ripple Rejection, Output Voltage Temperature Coefficient, Dropout Voltage at 1A Output Current and Thermal Shutdown items.

The specification in is checked and guaranteed by design engineering at $-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$, unless otherwise noted.

Dropout Voltage

($T_a = 25^{\circ}\text{C}$)

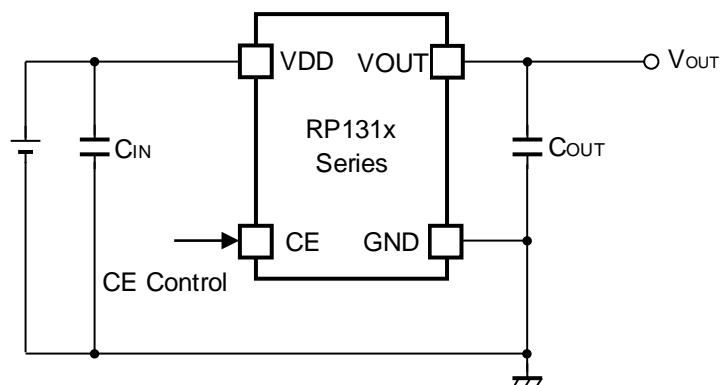
Output Voltage V_{OUT} (V)	Dropout Voltage V_{DIF} (V)					
	Condition	Typ.	Max.	Condition	Typ.	Max.
$0.8 \leq V_{\text{OUT}} < 0.9$	$I_{\text{OUT}}=300\text{mA}$	0.600	<input type="checkbox"/> 0.780	$I_{\text{OUT}}=1\text{A}$	1.100	<input type="checkbox"/> 1.650
$0.9 \leq V_{\text{OUT}} < 1.0$		0.550	<input type="checkbox"/> 0.690		1.050	<input type="checkbox"/> 1.500
$1.0 \leq V_{\text{OUT}} < 1.1$		0.450	<input type="checkbox"/> 0.610		1.000	<input type="checkbox"/> 1.450
$1.1 \leq V_{\text{OUT}} < 1.2$		0.340	<input type="checkbox"/> 0.540		0.930	<input type="checkbox"/> 1.420
$1.2 \leq V_{\text{OUT}} < 1.5$		0.290	<input type="checkbox"/> 0.500		0.900	<input type="checkbox"/> 1.380
$1.5 \leq V_{\text{OUT}} < 2.6$		0.230	<input type="checkbox"/> 0.310		0.700	<input type="checkbox"/> 1.100
$2.6 \leq V_{\text{OUT}} < 3.3$		0.150	<input type="checkbox"/> 0.180		0.500	<input type="checkbox"/> 0.750
$3.3 \leq V_{\text{OUT}} \leq 5.5$		0.140	<input type="checkbox"/> 0.170		0.450	<input type="checkbox"/> 0.650

RP131x

NO.EA-174-200128

APPLICATION INFORMATION

Typical Application Circuits



Recommendation value of the external capacitors

V_{OUT}	Capacitors	
$V_{OUT} \leq 3.6V$	C_{IN}	Kyocera 2.2 μ F (size:1005) [CM05X5R225M06AB]
	C_{OUT}	Kyocera 2.2 μ F (size:1608) [CM105X5R225K06AB]
$V_{OUT} > 3.6V$	C_{IN}	Kyocera 2.2 μ F (size:1608) [CM105X5R225K06AB]
	C_{OUT}	Kyocera 4.7 μ F (size:1608) [CM105X5R475M06AB]

Technical Notes on the External Components

When using this IC, consider following points:

Phase Compensation

In these ICs, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, use a capacitor C_{OUT} with good frequency characteristics and ESR (Equivalent Series Resistance).

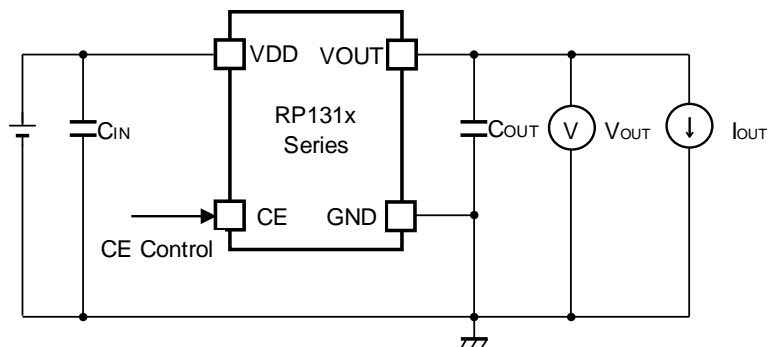
If a tantalum capacitor is used, and its ESR of C_{OUT} is large, the loop oscillation may result. Because of this, select C_{OUT} carefully considering its frequency characteristics.

PCB Layout

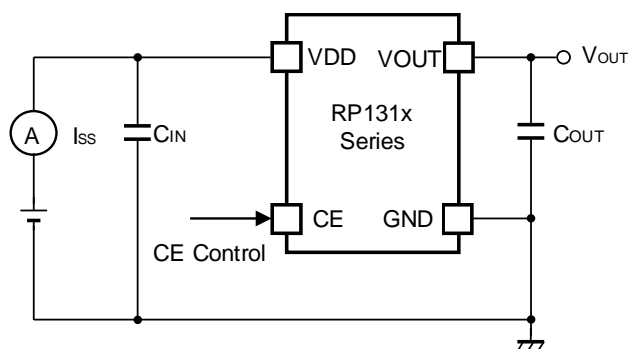
Make V_{DD} and GND lines sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect a capacitor C_{IN} between V_{DD} and GND pin with a capacitance value as "Recommendation value of the external capacitors" above or more, and as close as possible to the pins.

Set external components, especially the output capacitor C_{OUT} , as close as possible to the ICs, and make wiring as short as possible.

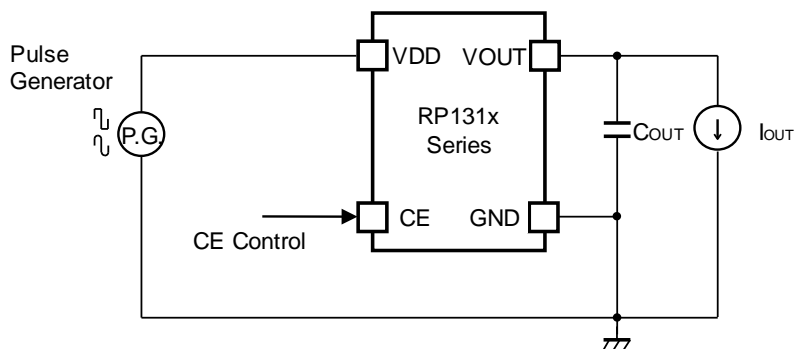
TEST CIRCUITS



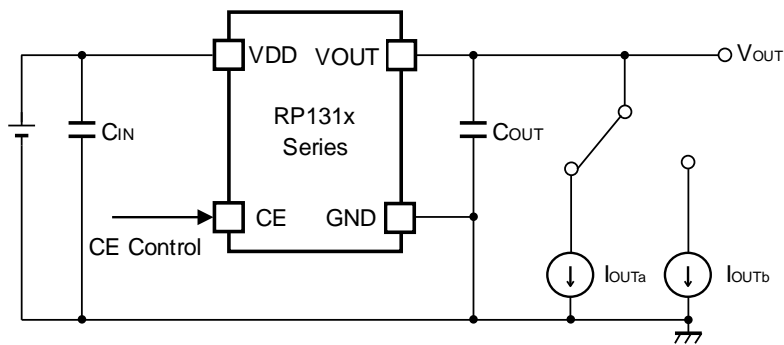
Basic Test Circuit



Test Circuit for Supply Current



Test Circuit for Ripple Rejection



Test Circuit for Load Transient Response

RP131x

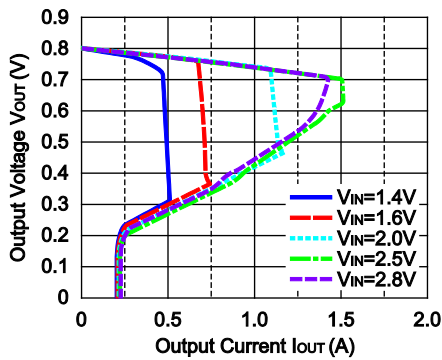
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TYPICAL CHARACTERISTICS

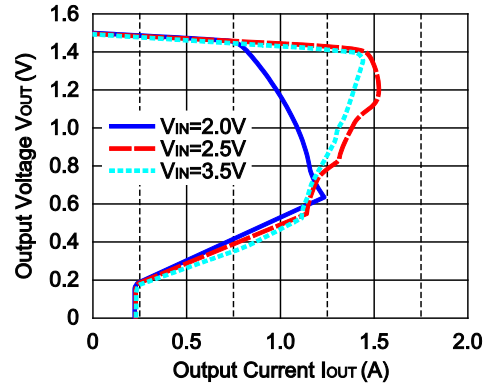
Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Output Voltage vs. Output Current ($T_a = 25^\circ\text{C}$)

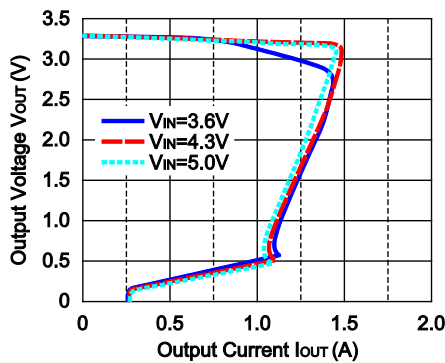
RP131x081x



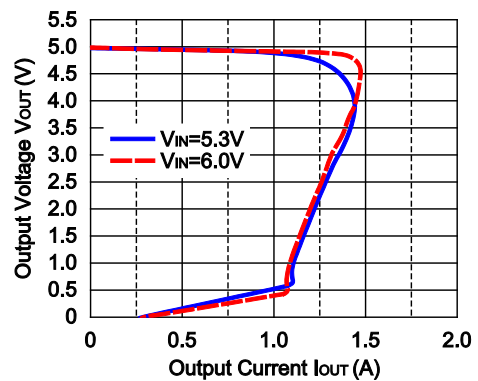
RP131x151x



RP131x331x

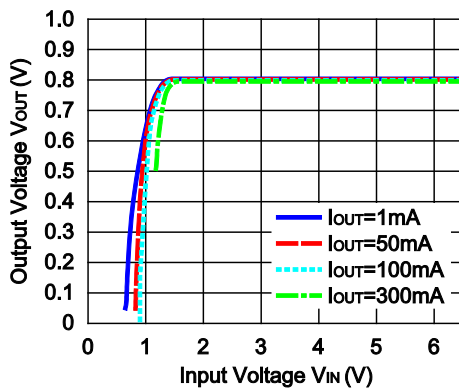


RP131x501x

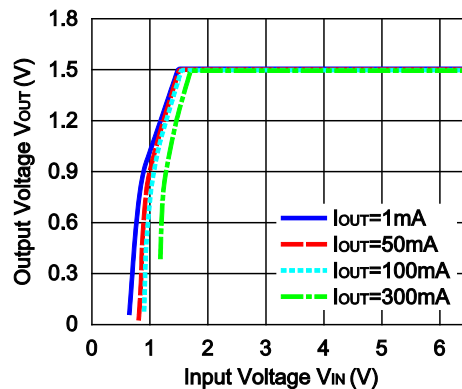


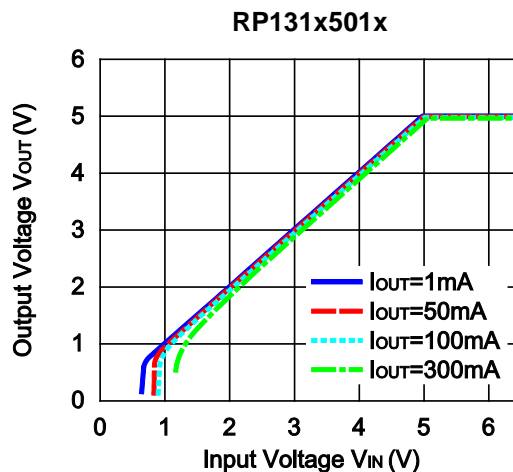
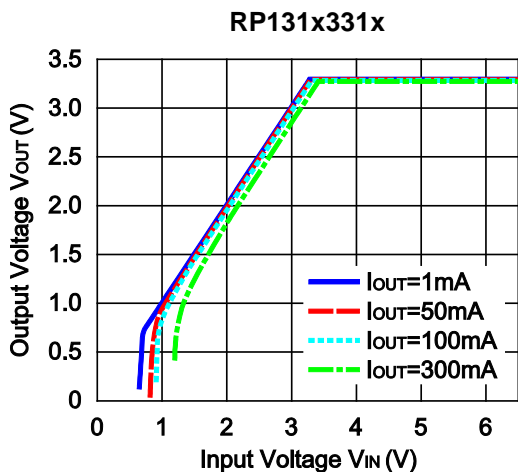
2) Output Voltage vs. Input Voltage ($T_a = 25^\circ\text{C}$)

RP131x081x

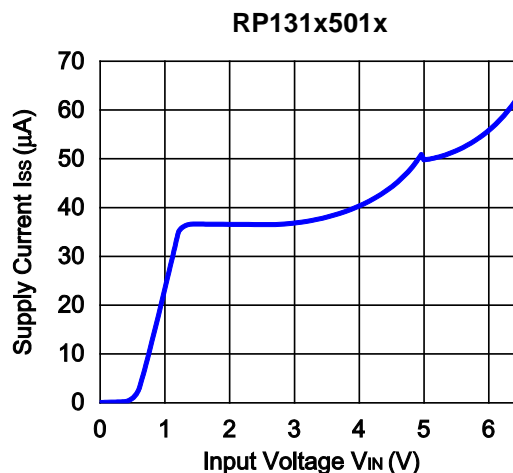
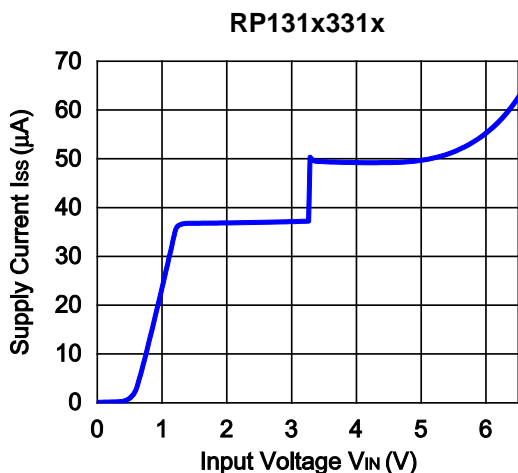
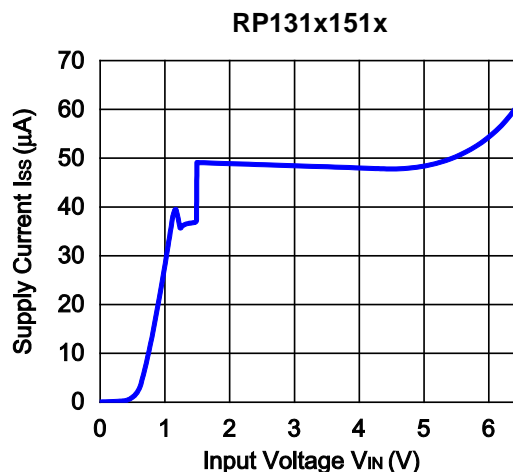
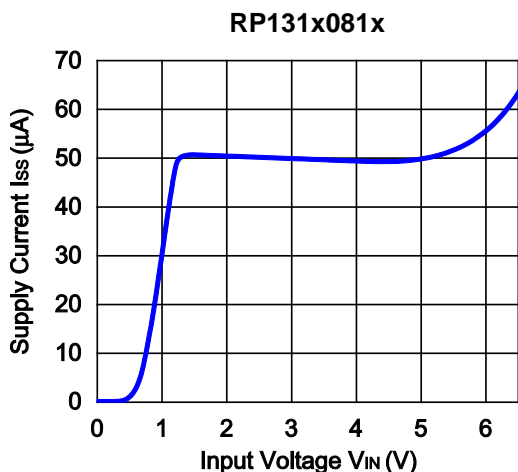


RP131x151x





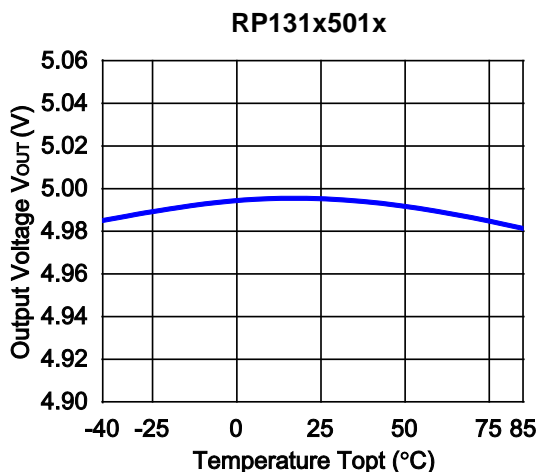
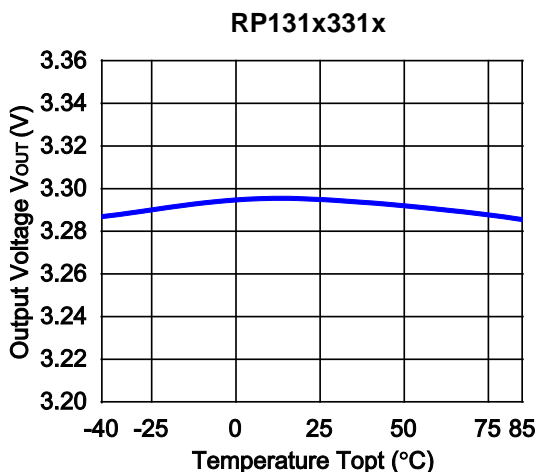
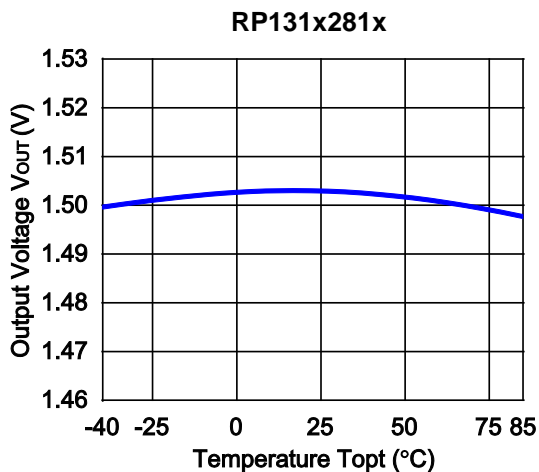
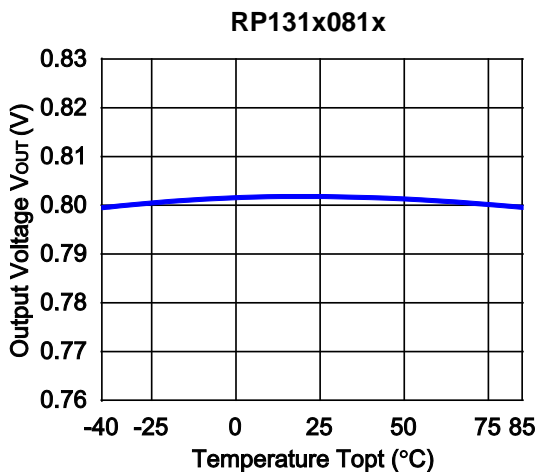
3) Supply Current vs. Input Voltage ($T_a=25^{\circ}\text{C}$)



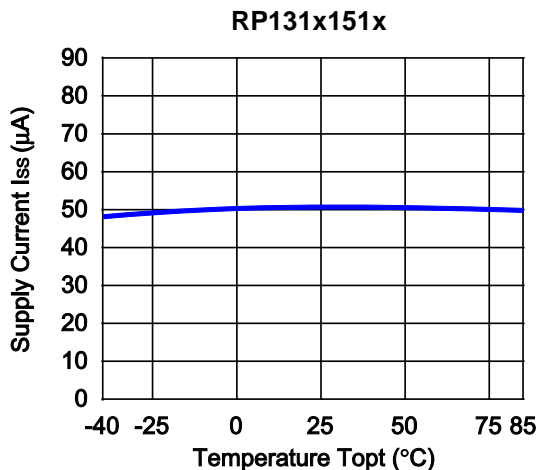
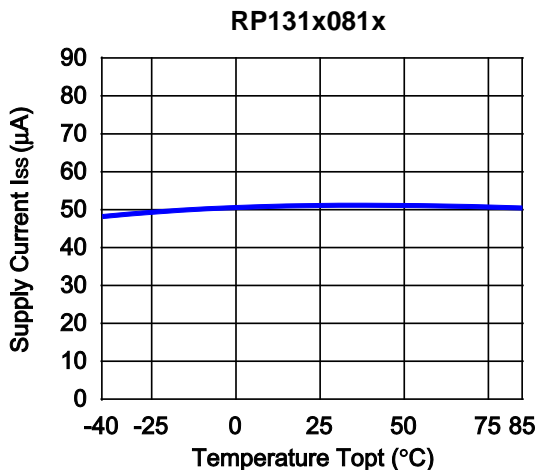
RP131x

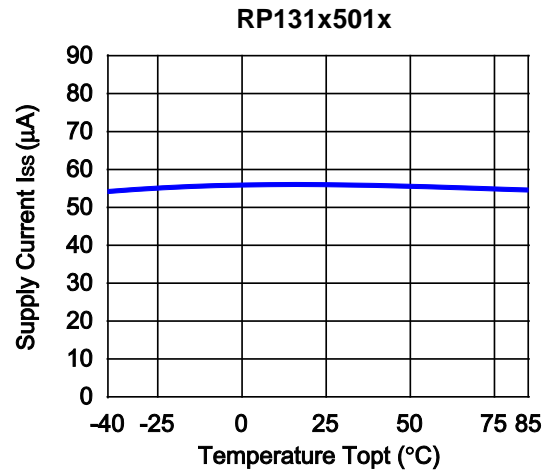
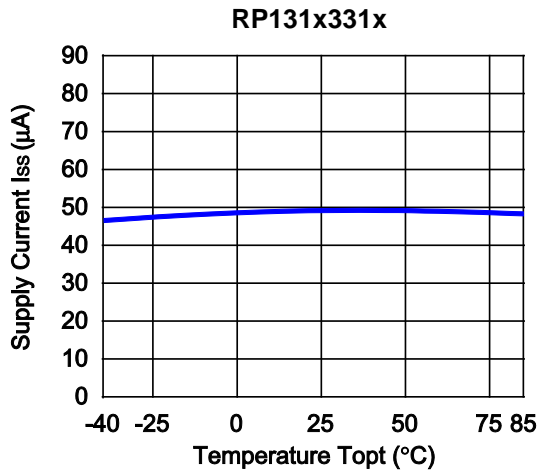
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4) Output Voltage vs. Temperature

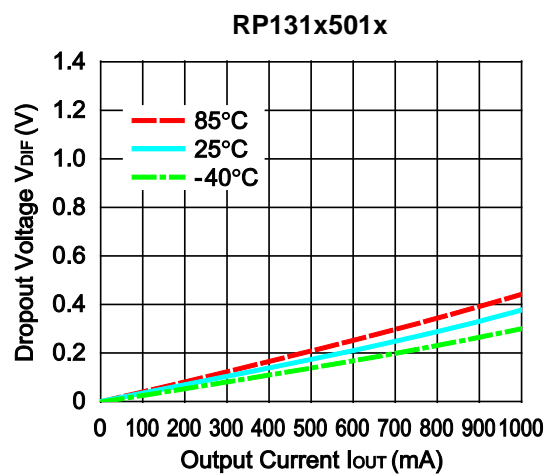
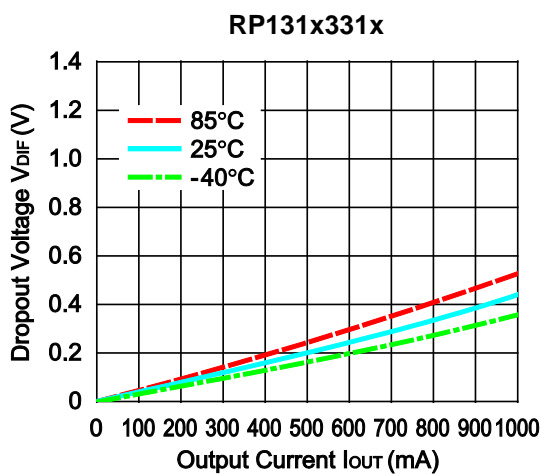
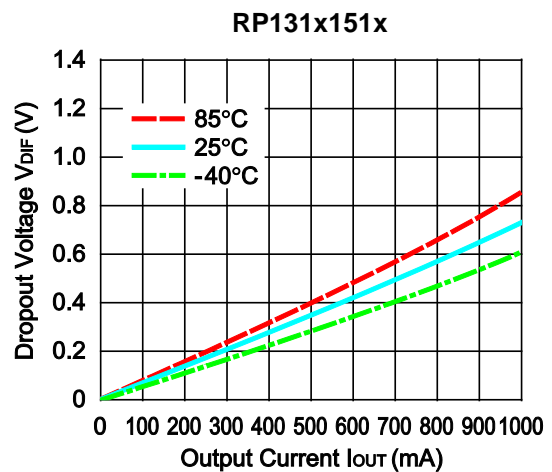
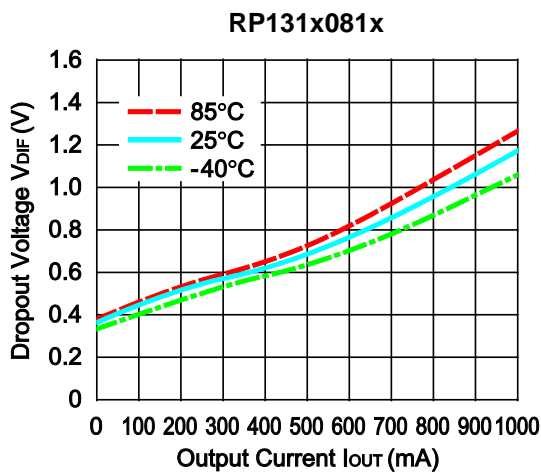


5) Supply Current vs. Temperature





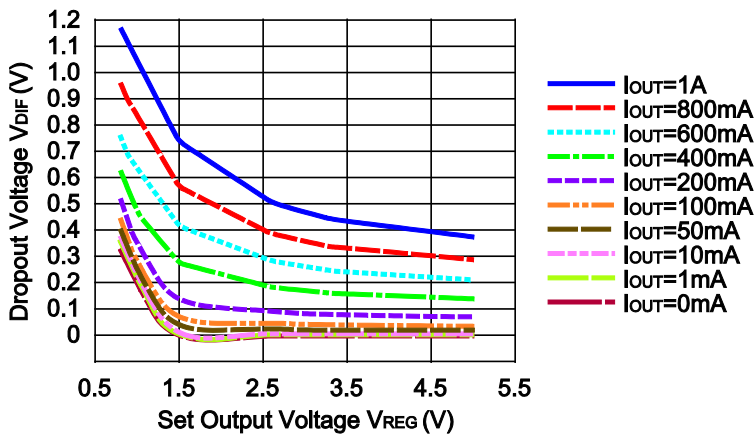
6) Dropout Voltage vs. Output Current



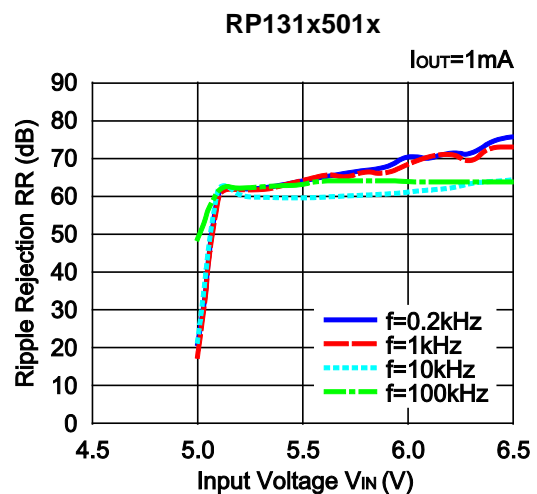
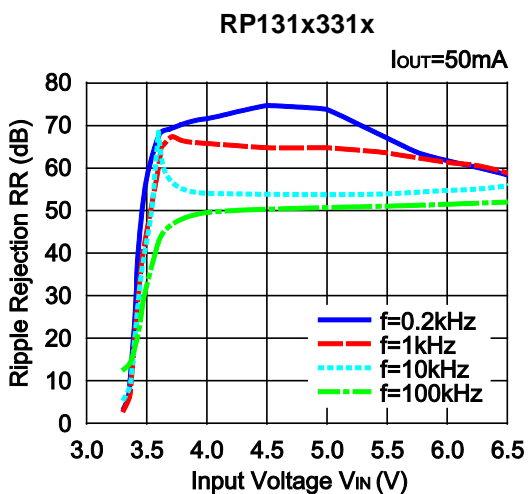
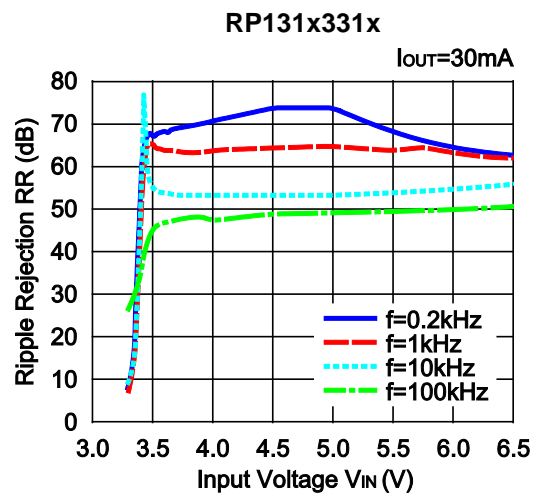
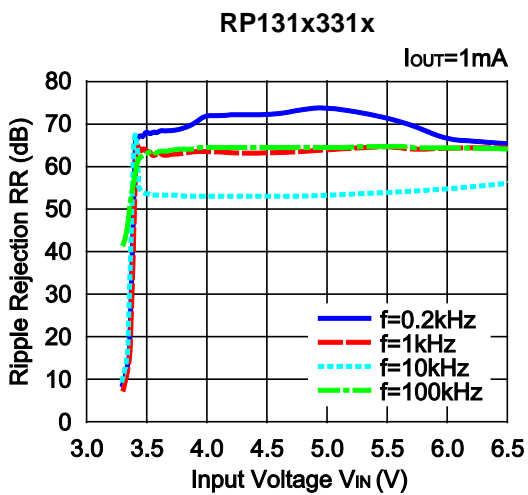
RP131x

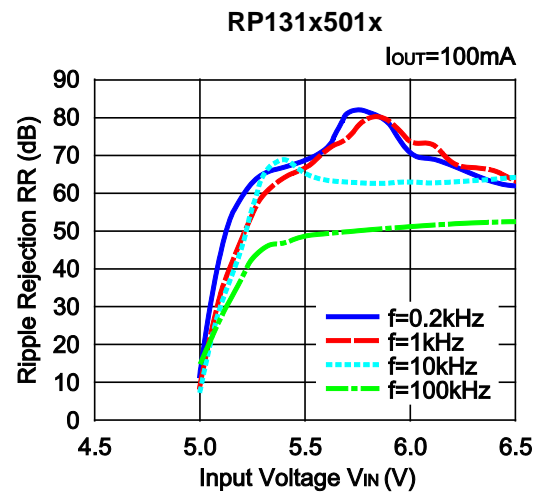
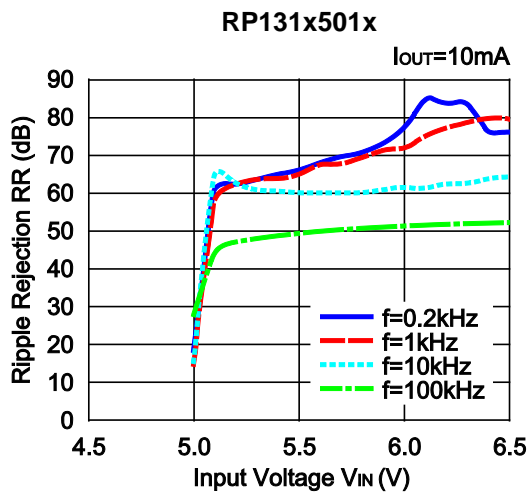
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7) Dropout Voltage vs. Set Output Voltage

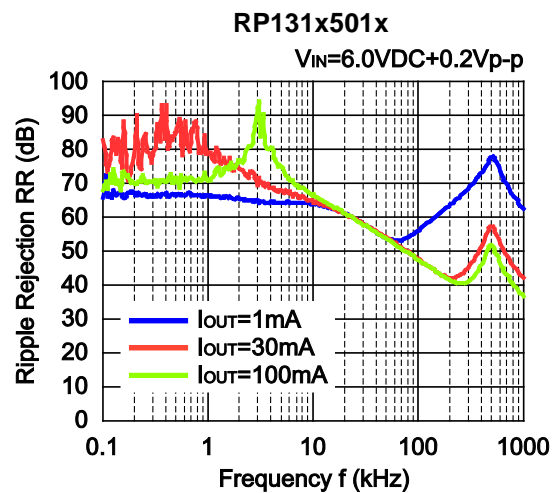
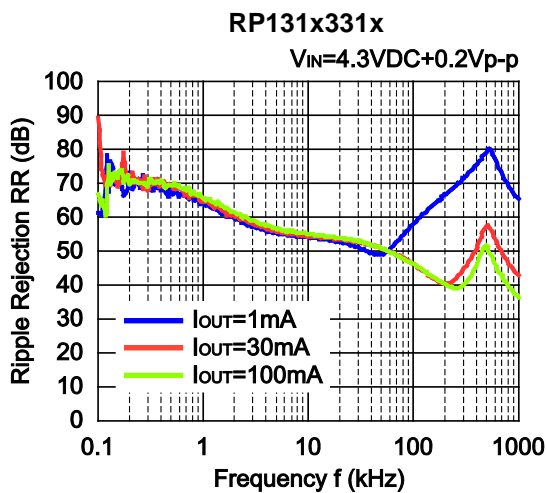
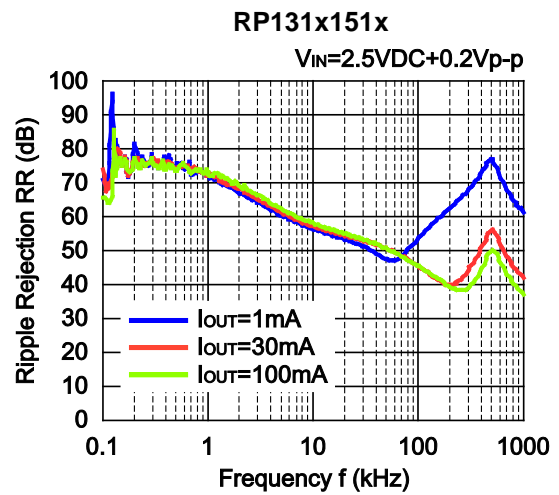
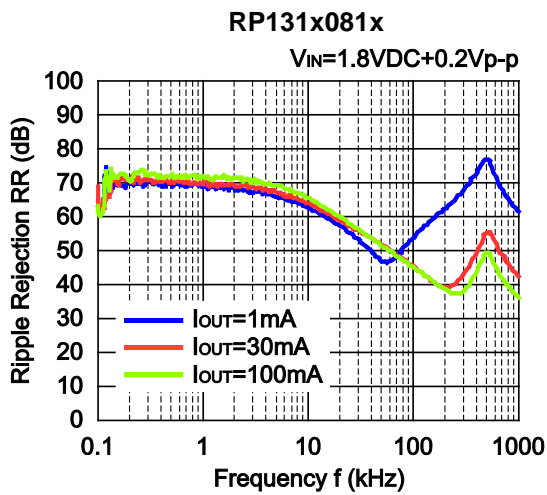


8) Ripple Rejection vs. Input Bias Voltage ($C1=none$, $C2=Ceramic\ 1.0\mu F$, Ripple= $0.2V_{pp}$, $T_a=25^\circ C$)





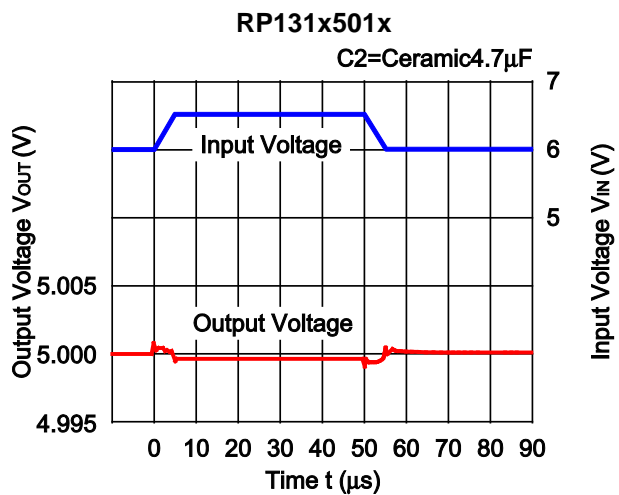
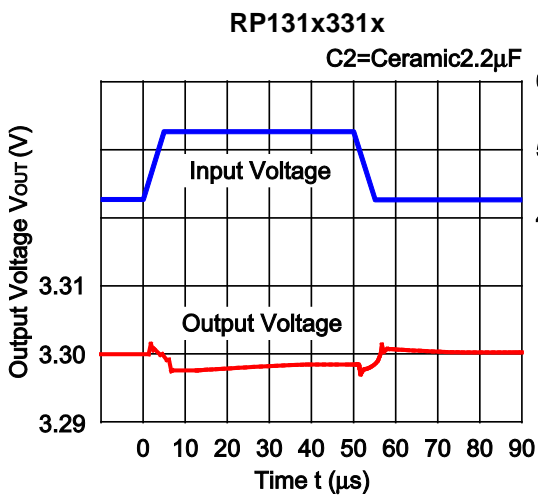
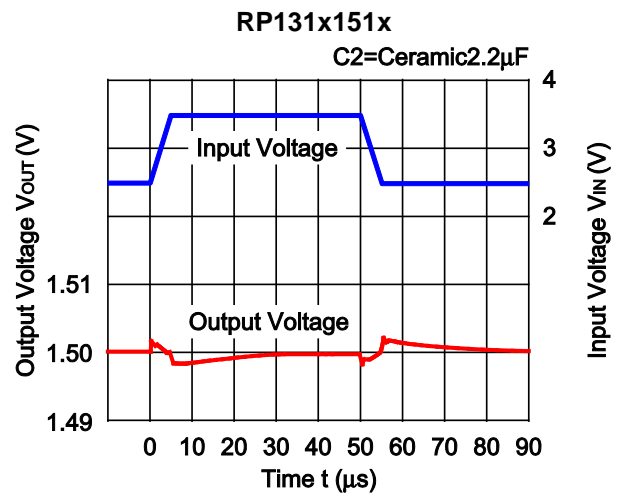
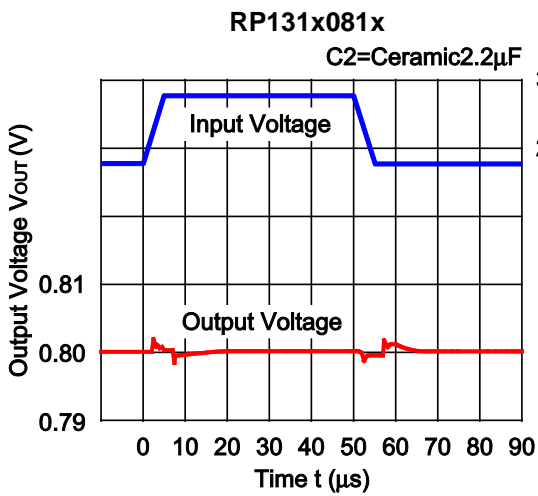
9) Ripple Rejection vs. Frequency ($C1=none$, $C2=Ceramic\ 4.7\mu F$, $T_a=25^{\circ}C$)



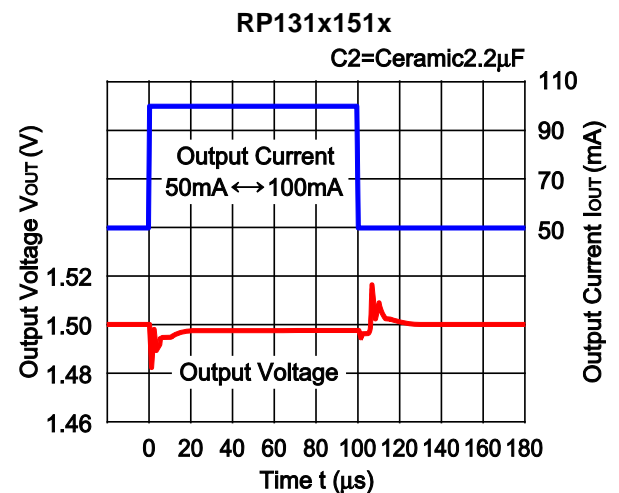
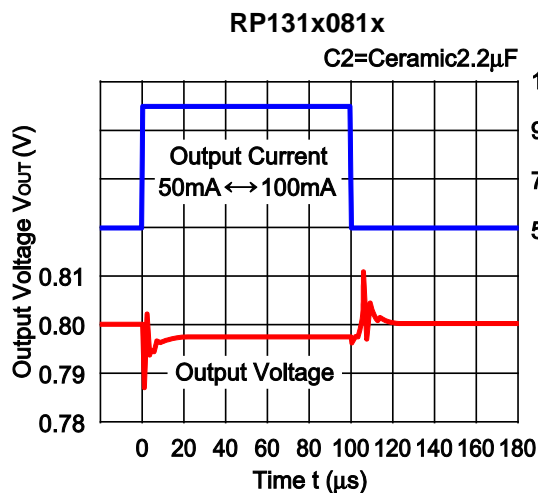
RP131x

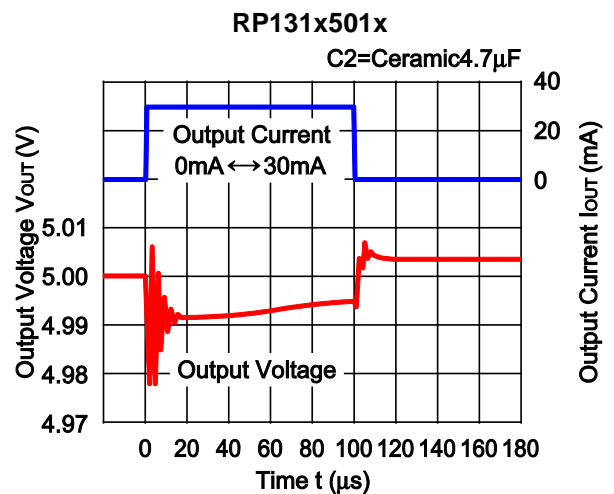
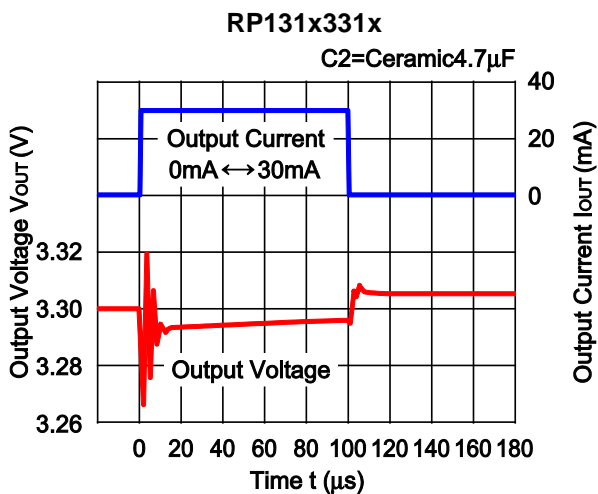
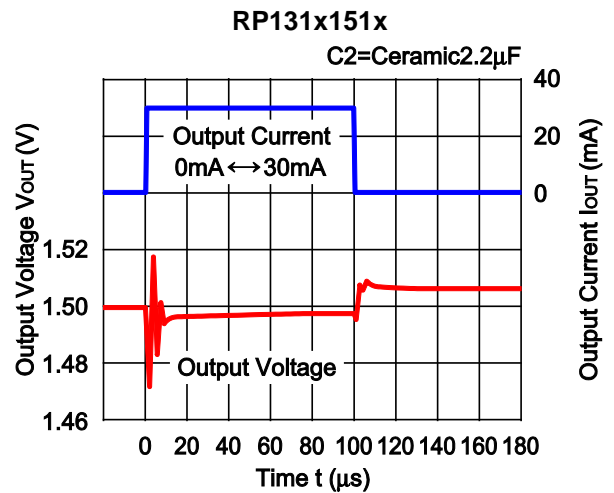
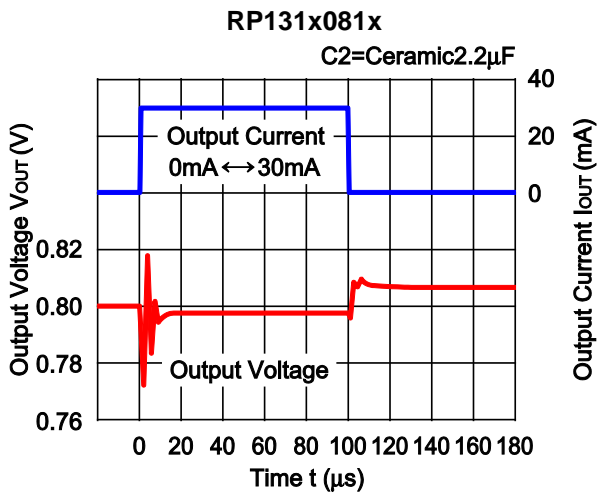
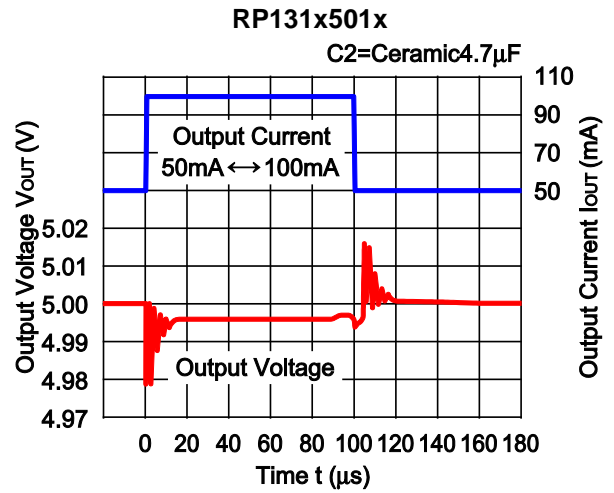
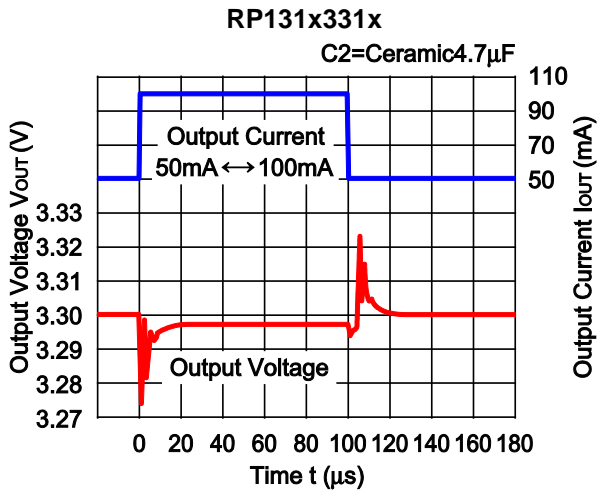
NO.EA-174-200128

10) Input Transient Response ($I_{OUT}=100mA$, $t_r=t_f=5\mu s$, $C1=none$, $T_a=25^\circ C$)



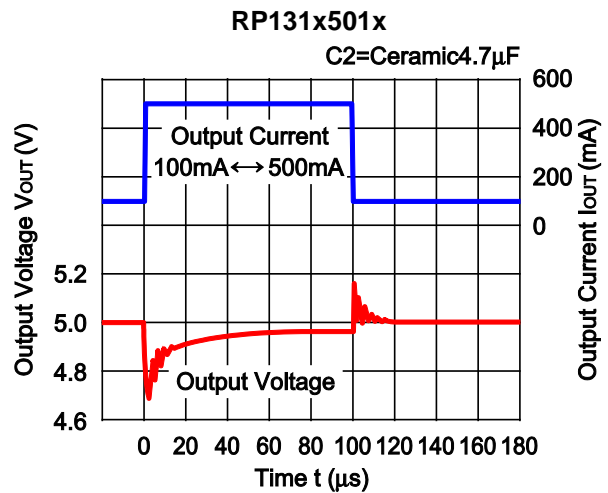
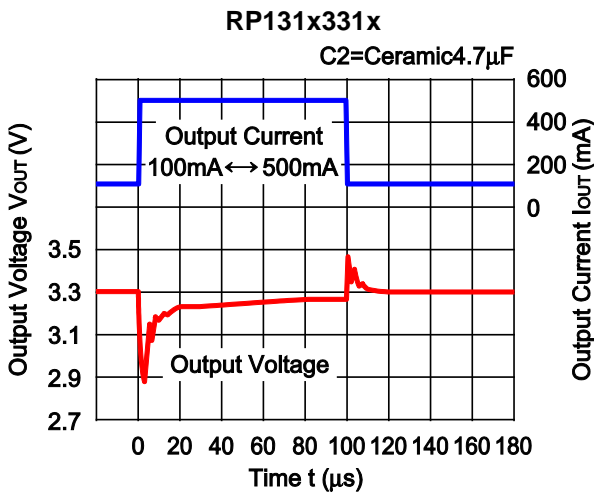
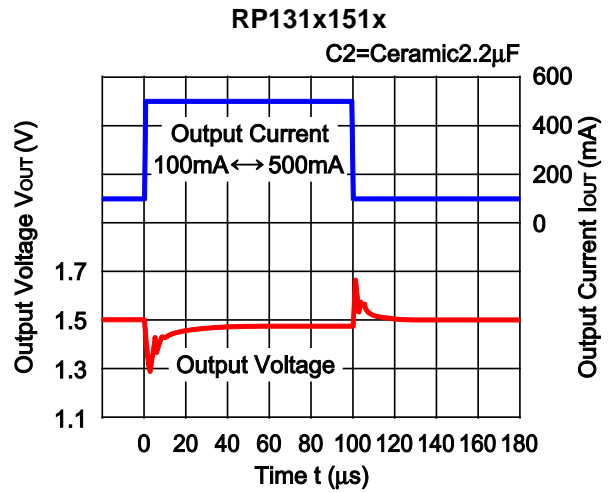
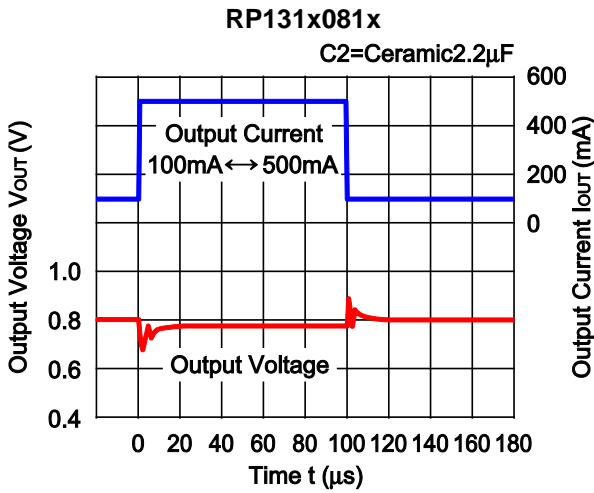
11) Load Transient Response ($t_r=t_f=0.5\mu s$, $C1=Ceramic\ 2.2\mu F$, $V_{IN}=V_{OUT}+1.0V$, $T_{opt}=25^\circ C$)



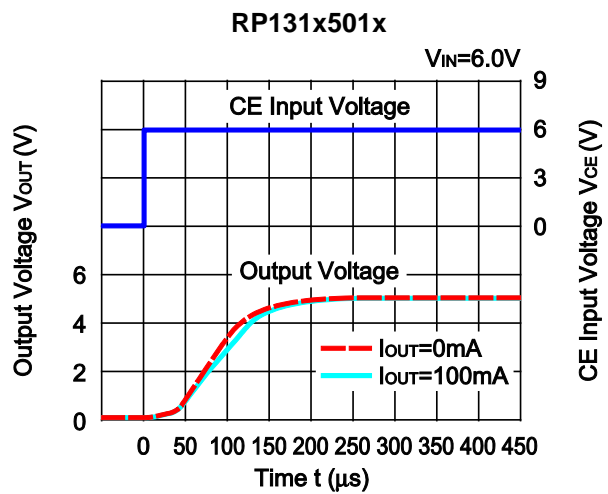
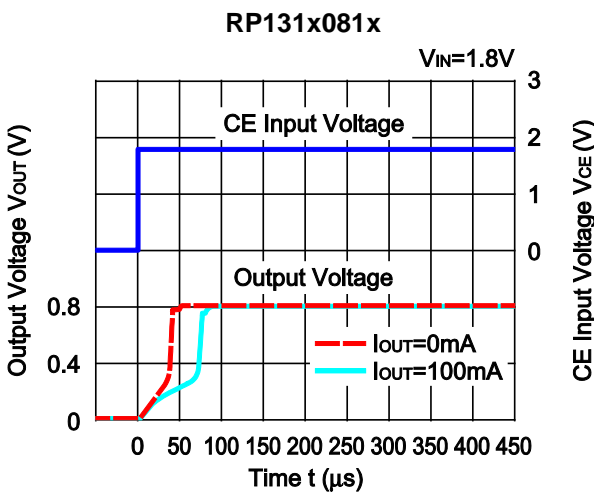


RP131x

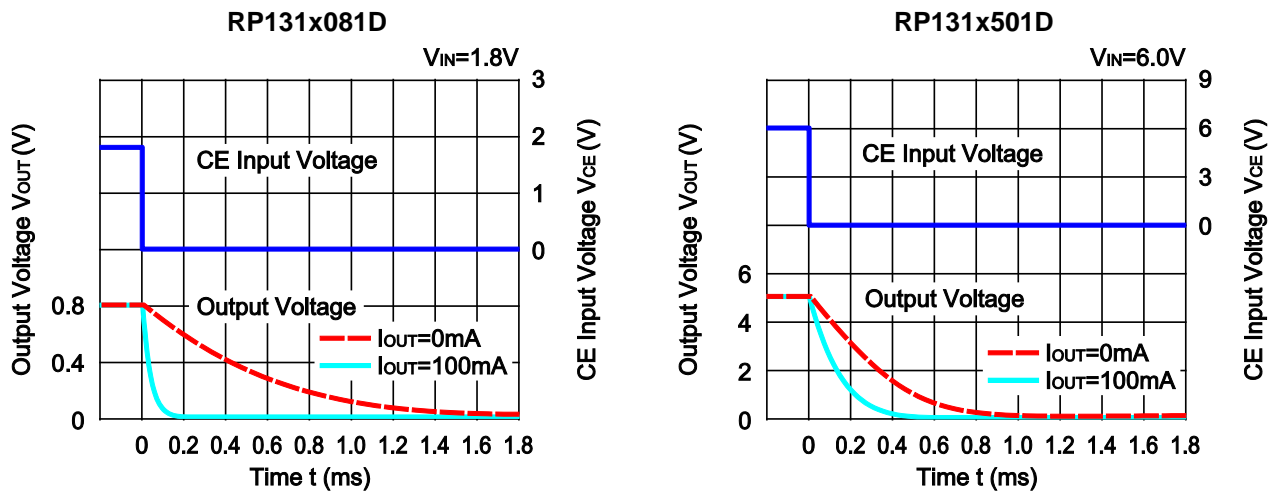
NO.EA-174-200128



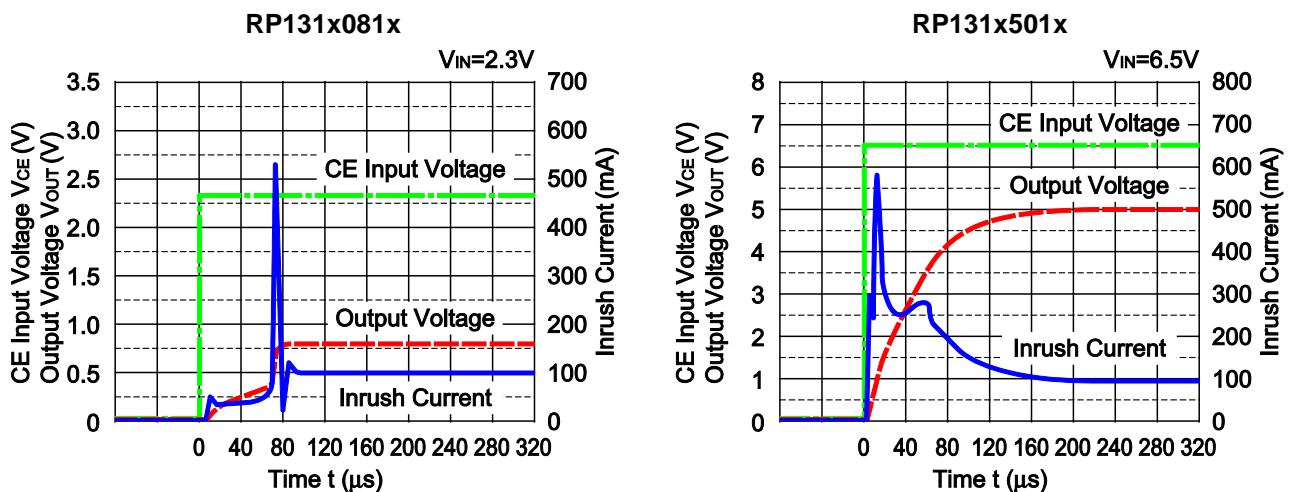
12) Turn On Speed with CE pin (C1=Ceramic 2.2 μ F, C2=Ceramic 4.7 μ F, T_{opt}=25°C)



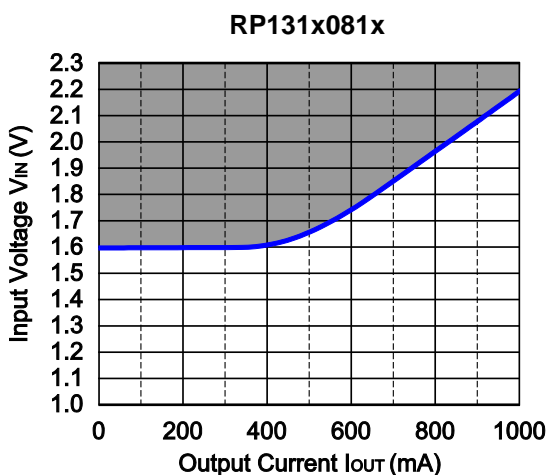
13) Turn Off Speed with CE pin (D Version) (C1=Ceramic 2.2 μ F, C2=Ceramic 4.7 μ F, T_a=25°C)



14) Inrush Current at turning on (C1=Ceramic 2.2 μ F, C2=Ceramic 4.7 μ F, T_{opt}=25°C)



15) Minimum Operating Voltage



Hatched area is available for 0.8V output.

RP131x

NO.EA-174-200128

ESR vs. Output Current

When using these ICs, consider the following points:

The relations between I_{OUT} (Output Current) and ESR of an output capacitor are shown below.

The conditions when the white noise level is under $40\mu\text{V}$ (Avg.) are marked as the hatched area in the graph.

Measurement conditions

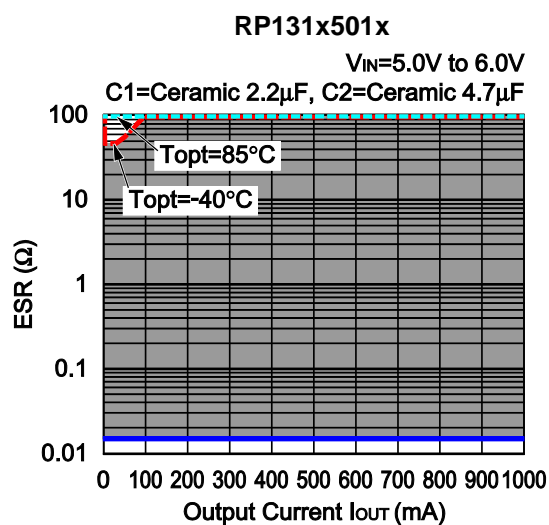
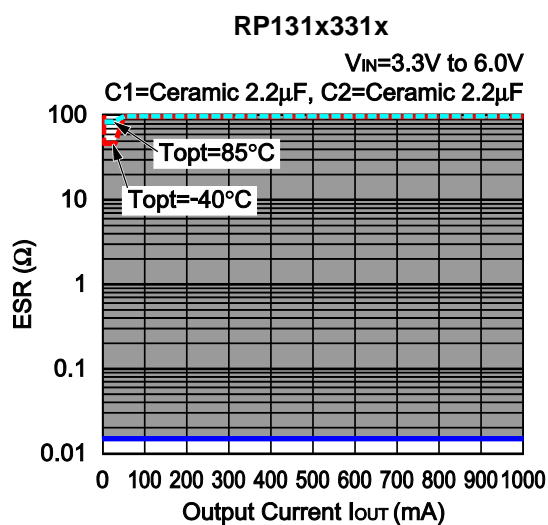
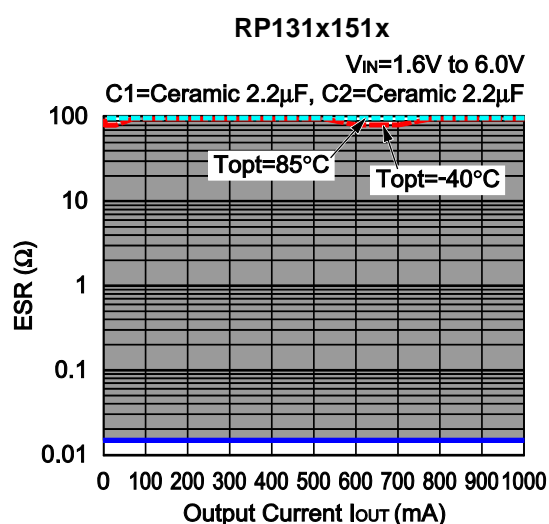
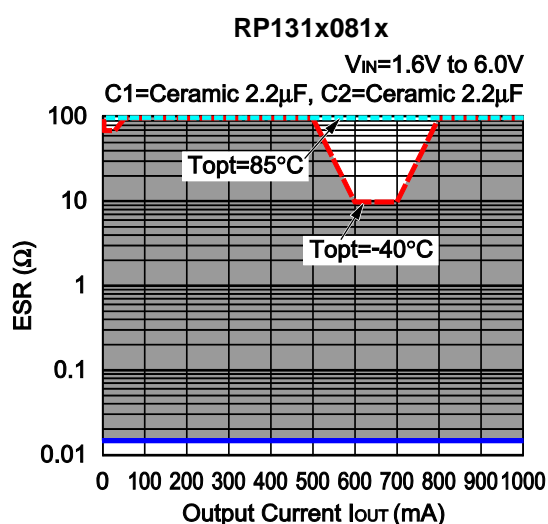
Frequency Band : 10Hz to 3MHz

Temperature : -40°C to 85°C

C1 : $2.2\mu\text{F}$ (Kyocera, CM05X5R225M04AD)

C2 : $2.2\mu\text{F}$ (Kyocera, CM105X5R225K06AE)

$4.7\mu\text{F}$ (Kyocera, CM105X5R475M06AB)



POWER DISSIPATION

DFN1616-6B

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.2 mm × 15 pcs

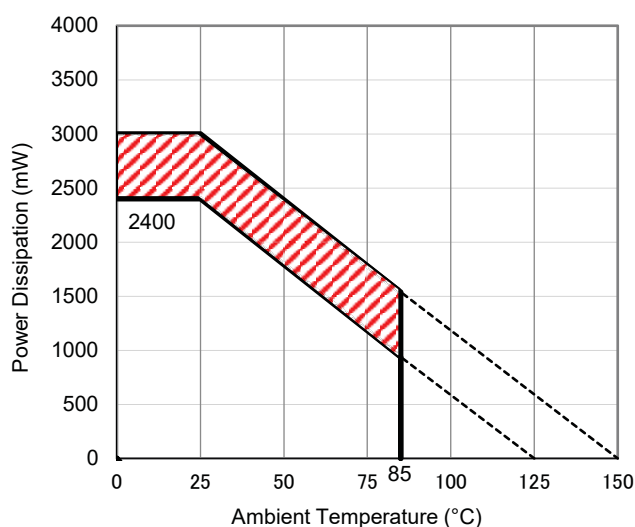
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

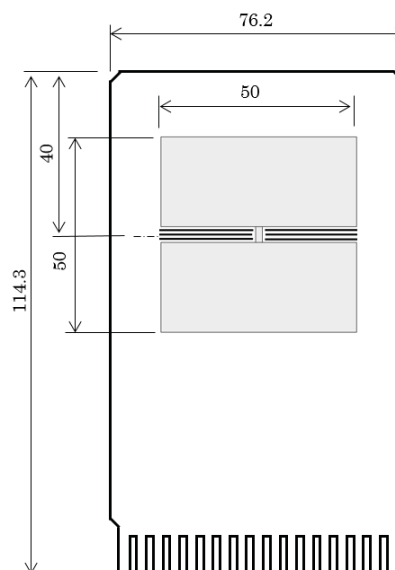
Item	Measurement Result
Power Dissipation	2400 mW
Thermal Resistance (θ_{ja})	$\theta_{ja} = 41^{\circ}\text{C/W}$
Thermal Characterization Parameter (ψ_{jt})	$\psi_{jt} = 11^{\circ}\text{C/W}$

θ_{ja} : Junction-to-Ambient Thermal Resistance

ψ_{jt} : Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

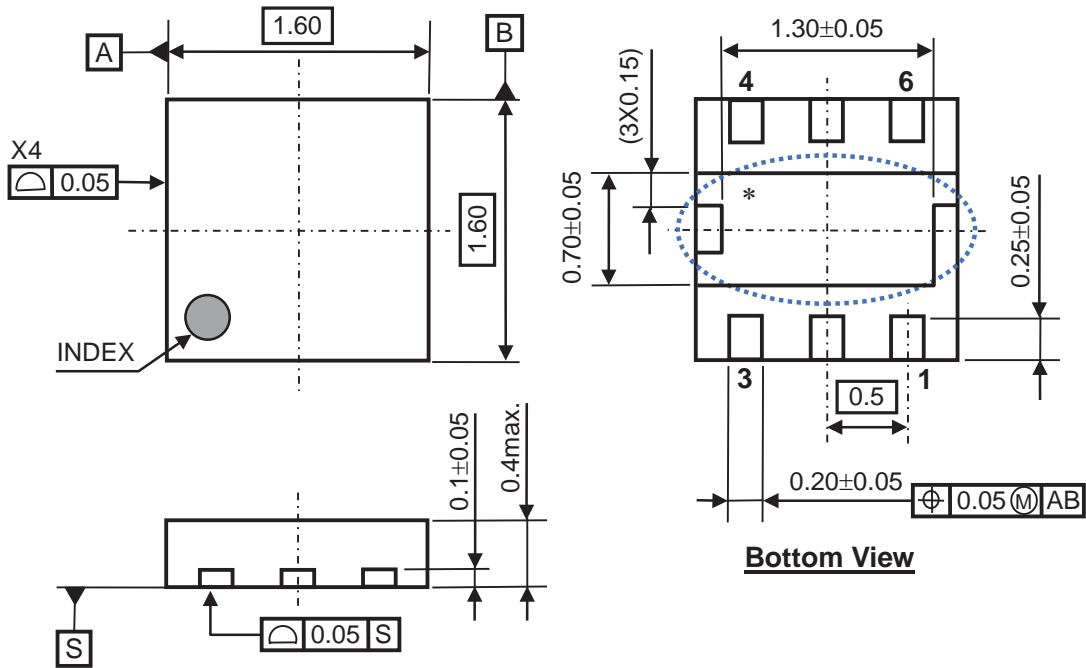
The above graph shows the power dissipation of the package at $T_{jmax} = 125^{\circ}\text{C}$ and $T_{jmax} = 150^{\circ}\text{C}$. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years

PACKAGE DIMENSIONS

DFN1616-6B

Ver. A



DFN1616-6B Package Dimensions (Unit: mm)

* The tab on the bottom of the package shown by blue circle is a substrate potential (GND). It is recommended that this tab be connected to the ground plane pin on the board but it is possible to leave the tab floating.

POWER DISSIPATION

DFN(PLP)1820-6

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.2 mm × 34 pcs

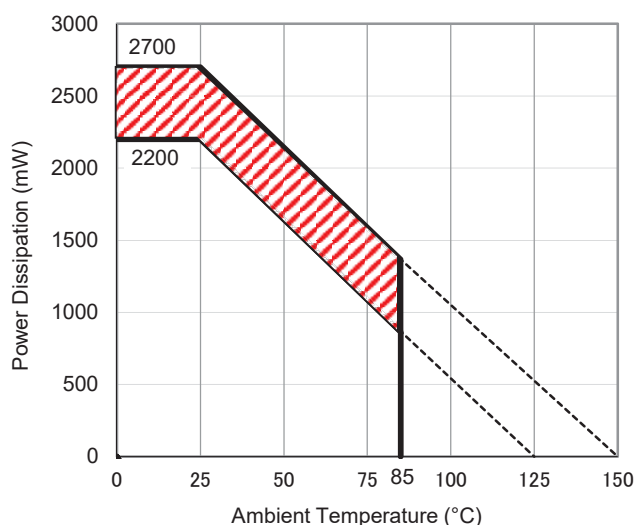
Measurement Result

($T_a = 25^\circ\text{C}$, $T_{j\text{max}} = 125^\circ\text{C}$)

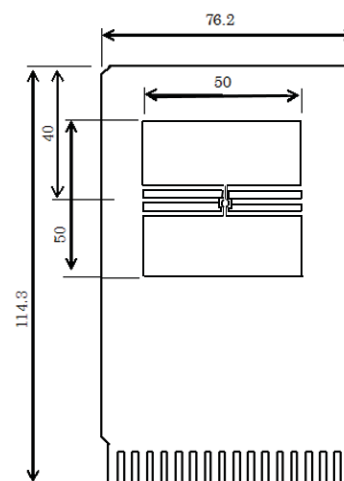
Item	Measurement Result
Power Dissipation	2200 mW
Thermal Resistance (θ_{ja})	$\theta_{ja} = 45^\circ\text{C/W}$
Thermal Characterization Parameter (ψ_{jt})	$\psi_{jt} = 18^\circ\text{C/W}$

θ_{ja} : Junction-to-Ambient Thermal Resistance

ψ_{jt} : Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

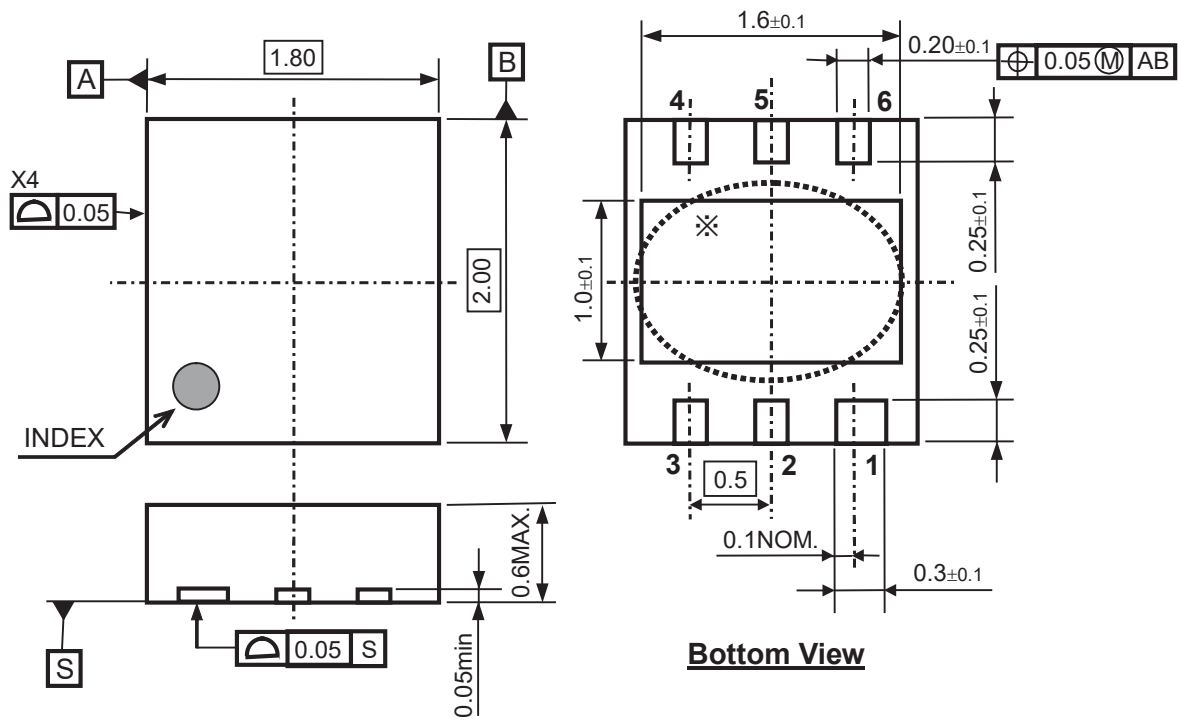
The above graph shows the power dissipation of the package at $T_{j\text{max}} = 125^\circ\text{C}$ and $T_{j\text{max}} = 150^\circ\text{C}$. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years

PACKAGE DIMENSIONS

DFN(PLP)1820-6

Ver. A



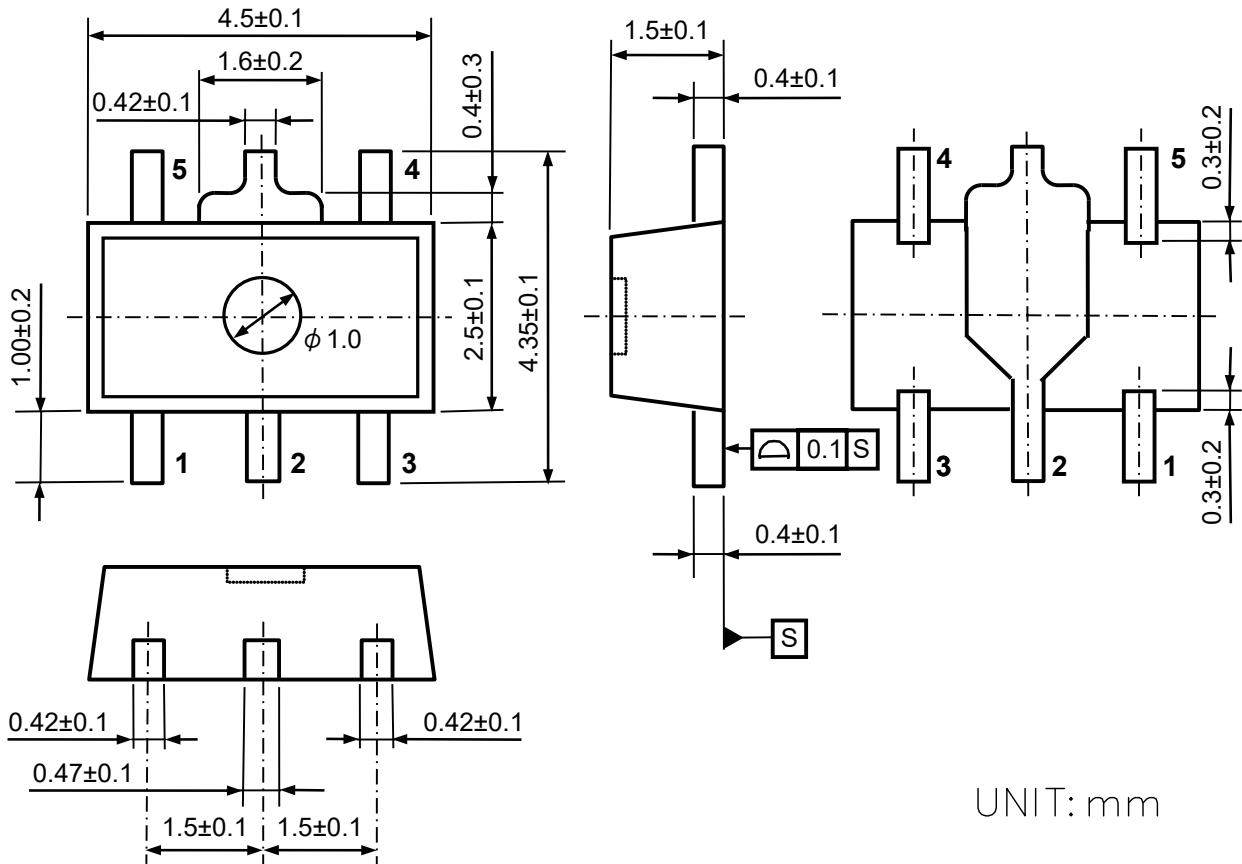
DFN(PLP)1820-6 Package Dimensions (Unit: mm)

* The tab on the bottom of the package is substrate level (GND). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

PACKAGE DIMENSIONS

SOT-89-5

Ver. A



UNIT: mm

SOT-89-5 Package Dimensions

POWER DISSIPATION

SOT-89-5

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 13 pcs

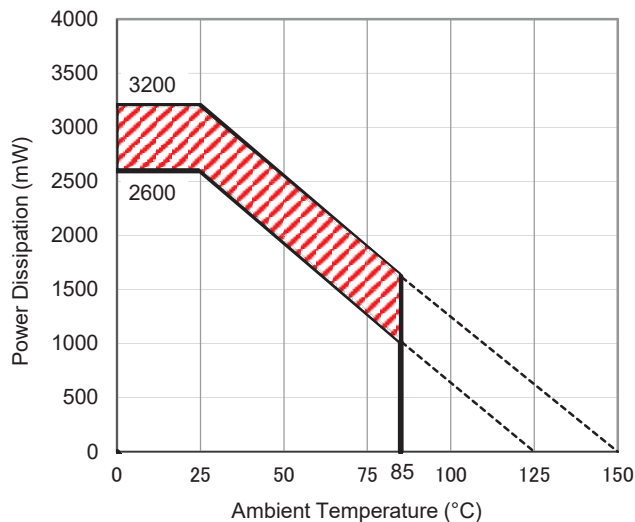
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

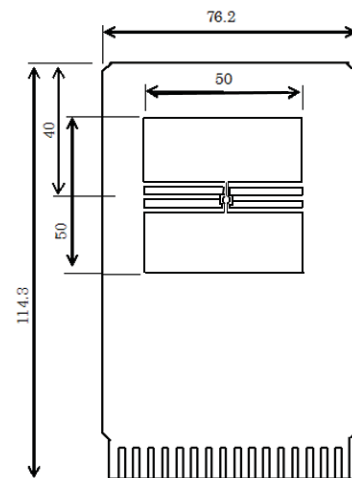
Item	Measurement Result
Power Dissipation	2600 mW
Thermal Resistance (θ_{ja})	$\theta_{ja} = 38^{\circ}\text{C/W}$
Thermal Characterization Parameter (ψ_{jt})	$\psi_{jt} = 13^{\circ}\text{C/W}$

θ_{ja} : Junction-to-Ambient Thermal Resistance

ψ_{jt} : Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

The above graph shows the power dissipation of the package at $T_{jmax} = 125^{\circ}\text{C}$ and $T_{jmax} = 150^{\circ}\text{C}$. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years

POWER DISSIPATION

HSOP-6J

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 28 pcs

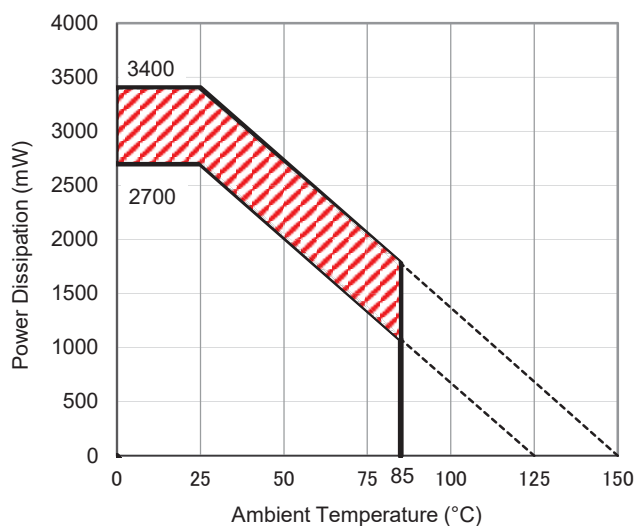
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

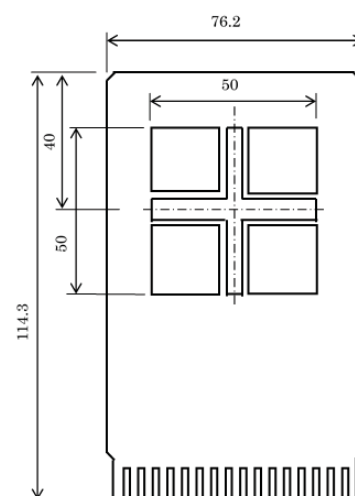
Item	Measurement Result
Power Dissipation	2700 mW
Thermal Resistance (θ_{ja})	$\theta_{ja} = 37^{\circ}\text{C/W}$
Thermal Characterization Parameter (ψ_{jt})	$\psi_{jt} = 7^{\circ}\text{C/W}$

θ_{ja} : Junction-to-Ambient Thermal Resistance

ψ_{jt} : Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

The above graph shows the power dissipation of the package at $T_{jmax} = 125^{\circ}\text{C}$ and $T_{jmax} = 150^{\circ}\text{C}$. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

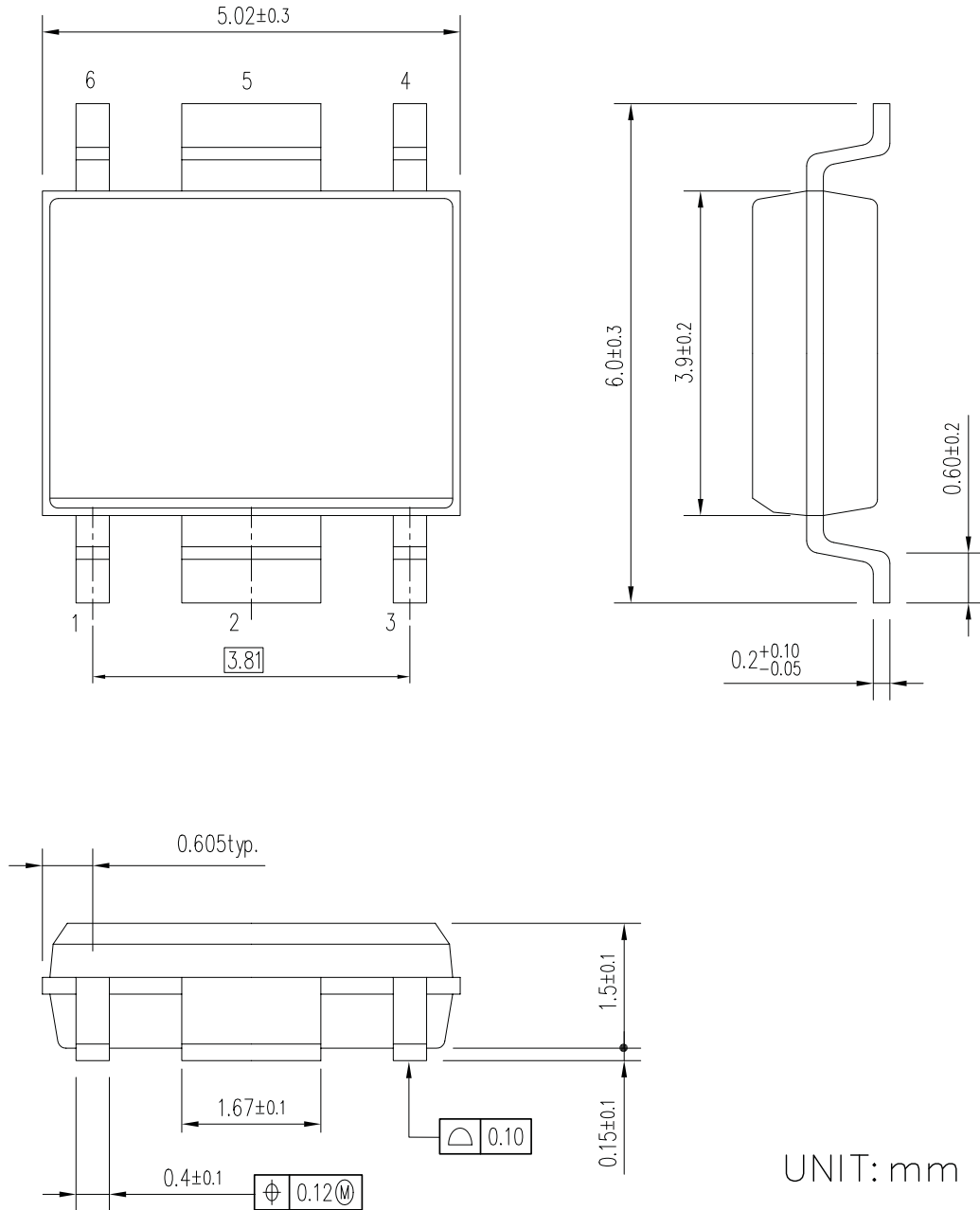
Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years

*RP131L(DFN1616-6B) is the non-promotion product as of March 2020.

PACKAGE DIMENSIONS

HSOP-6J

Ver. A



HSOP-6J Package Dimensions

UNIT: mm

POWER DISSIPATION

TO-252-5

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 21 pcs

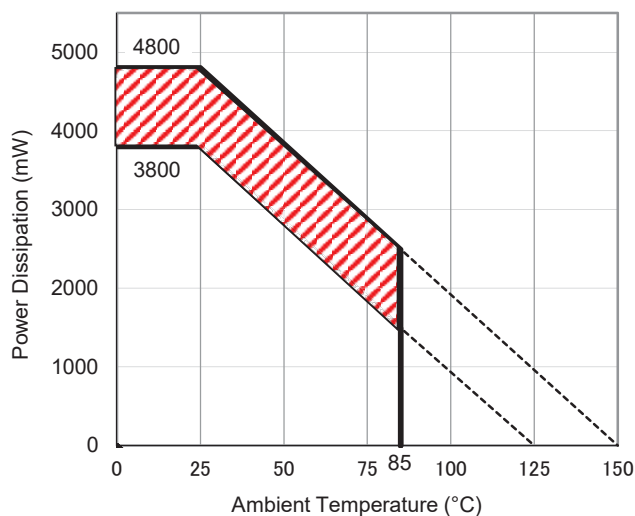
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

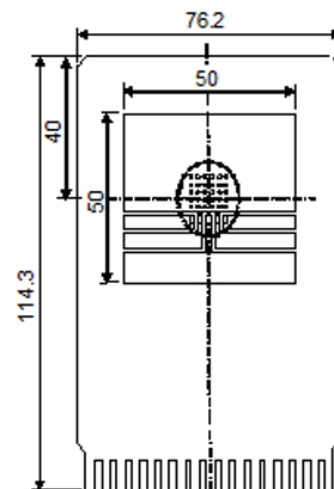
Item	Measurement Result
Power Dissipation	3800 mW
Thermal Resistance (θja)	θja = 26°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 7°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

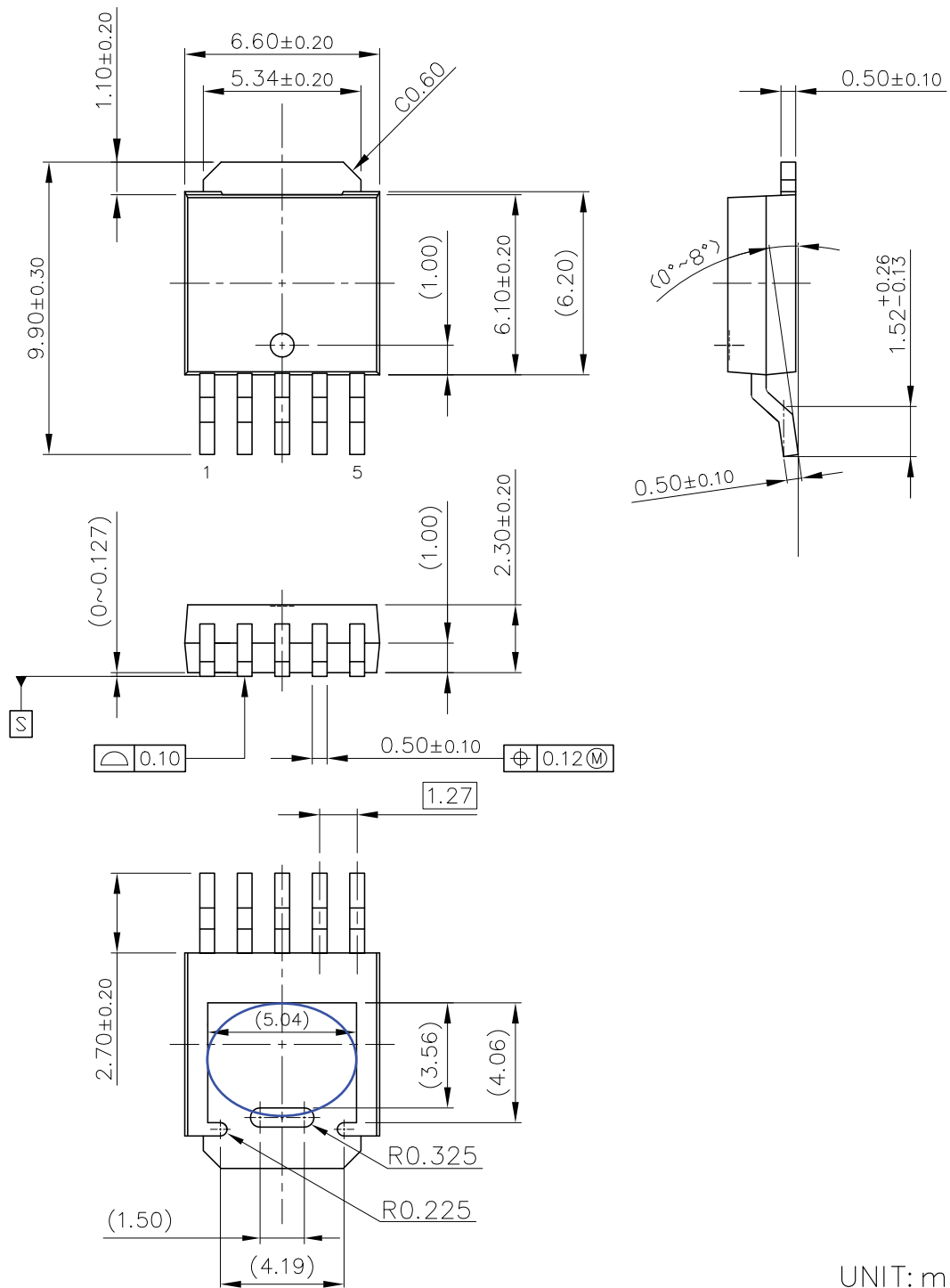
The above graph shows the power dissipation of the package at Tjmax = 125°C and Tjmax = 150°C. Operating the device in the hatched range might have a negative influence on its lifetime. The total hours of use and the total years of use must be limited as follows:

Total Hours of Use	Total Years of Use (4 hours/day)
13,000 hours	9 years

PACKAGE DIMENSIONS

TO-252-5-P2

Ver. A



UNIT: mm

TO-252-5-P2 Package Dimensions

* The tab on the bottom of the package shown by blue circle is a substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.



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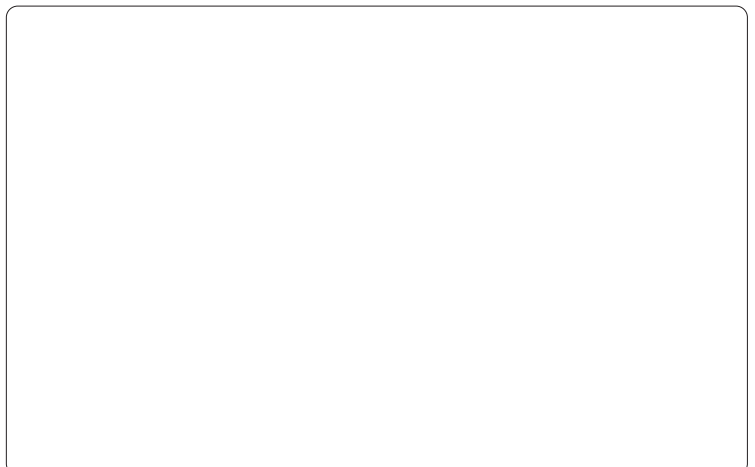
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[RP131H331B-T1-FE](#) [RP131H121D-T1-FE](#) [RP131S101D-E2-FE](#) [RP131S121B-E2-FE](#) [RP131H121B-T1-FE](#)
[RP131H301D-T1-FE](#) [RP131S121D-E2-FE](#) [RP131H151B-T1-FE](#) [RP131H501D-T1-FE](#) [RP131H331D-T1-FE](#)
[RP131S501B-E2-FE](#) [RP131S181B-E2-FE](#) [RP131S251B-E2-FE](#) [RP131S181D-E2-FE](#) [RP131K431B-TR](#)
[RP131K251D-TR](#) [RP131S341B-E2-FE](#) [RP131K441D-TR](#) [RP131S321B-E2-FE](#) [RP131K101B-TR](#) [RP131H221D-T1-FE](#)
[RP131H351B-T1-FE](#) [RP131K081B-TR](#) [RP131K101D-TR](#) [RP131K081D-TR](#) [RP131S521D-E2-FE](#) [RP131K121D-TR](#)
[RP131K331D-TR](#) [RP131H121D5-T1-FE](#) [RP131H201D-T1-FE](#) [RP131H421B-T1-FE](#) [RP131K151D-TR](#)
[RP131K181D-TR](#) [RP131K501B-TR](#) [RP131K501D-TR](#) [RP131K121B-TR](#) [RP131H361D-T1-FE](#) [RP131H131B-T1-FE](#)
[RP131S401B-E2-FE](#) [RP131K251B-TR](#) [RP131S121B5-E2-FE](#) [RP131K411B-TR](#) [RP131J331D-T1-FE](#) [RP131S341D-E2-FE](#)
[RP131K341D-TR](#) [RP131H111D-T1-FE](#) [RP131H131D-T1-FE](#) [RP131H141D-T1-FE](#) [RP131H181D5-T1-FE](#)
[RP131H211D-T1-FE](#) [RP131H281B-T1-FE](#) [RP131S291D-E2-FE](#) [RP131S301B-E2-FE](#) [RP131S351D-E2-FE](#)
[RP131S361D-E2-FE](#) [RP131S401D-E2-FE](#) [RP131S421D-E2-FE](#) [RP131S131B-E2-FE](#) [RP131S131D-E2-FE](#)
[RP131S181D5-E2-FE](#) [RP131S261B-E2-FE](#) [RP131S261D-E2-FE](#) [RP131S281B-E2-FE](#) [RP131S081D-E2-FE](#)
[RP131S091B-E2-FE](#) [RP131S091D-E2-FE](#) [RP131S111B-E2-FE](#) [RP131S111D-E2-FE](#) [RP131S121D5-E2-FE](#)
[RP131S081B-E2-FE](#) [RP131K461D-TR](#) [RP131K511B-TR](#) [RP131K511D-TR](#) [RP131K551B-TR](#) [RP131K401B-TR](#)
[RP131K401D-TR](#) [RP131K421B-TR](#) [RP131K421D-TR](#) [RP131K431D-TR](#) [RP131K451D-TR](#)