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FAIRCHILD SEMICONDUCTOR®

April 2013

FDP8440

N-Channel PowerTrench® MOSFET

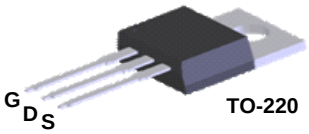
40 V, 277 A, 2.2 mΩ

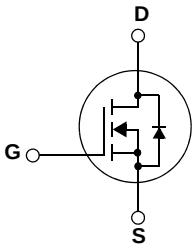
Features

- $R_{DS(on)}$ = 1.64 mΩ (Typ.)@ V_{GS} = 10 V, I_D = 80 A
- $Q_{g(tot)}$ = 345 nC (Typ.)@ V_{GS} = 10 V
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- RoHS Compliant

Applications

- Power Tools
- Motor Drives and Uninterruptible Power Supplies
- Synchronous Rectification
- Battery Protection Circuit





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		FDP8440	Unit
V_{DSS}	Drain to Source Voltage		40	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	- Continuous (T_C = 25°C, Silicon Limited) - Continuous (T_C = 100°C, Silicon Limited) - Continuous (T_C = 25°C, Package Limited)	277* 196* 100	A
I_{DM}	Drain Current	- Pulsed (Note 1)	500	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	1682	mJ
P_D	Power Dissipation	(T_C = 25°C)	306	W
		- Derate above 25°C	2.04	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 100A.

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.49	°C/W
$R_{\theta CS}$	Thermal Resistance, Case to Sink (Typ.)	0.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	°C/W

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Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP8440	FDP8440	TO-220	N/A	N/A	50units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA		40	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32V		--	--	1	μA
		V_{GS} = 0V	T_C = 150°C	--	--	250	μA
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20V		--	--	±100	nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA		1	--	3	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5V, I_D = 80A		--	1.88	2.4	mΩ
		V_{GS} = 10V, I_D = 80A		--	1.64	2.2	
		V_{GS} = 10V, I_D = 80A, T_C = 175°C		--	3.00	4.4	
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz		--	18600	24740	pF
C_{oss}	Output Capacitance			--	1840	2450	pF
C_{rss}	Reverse Transfer Capacitance			--	1400	2100	pF
R_G	Gate Resistance	V_{GS} = 0.5V, f = 1MHz		--	1.1	--	Ω
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V	V_{DD} = 20V, I_D = 80A, I_g = 1.0mA	--	345	450	nC
$Q_{g(2)}$	Threshold Gate Charge	V_{GS} = 0V to 2V		--	32.5	--	nC
Q_{gs}	Gate to Source Gate Charge			--	49	--	nC
Q_{gs2}	Gate Charge Threshold to Plateau			--	16.5	--	nC
Q_{gd}	Gate to Drain “Miller” Charge			--	74	--	nC
Switching Characteristics (V_{GS} = 10V)							
t_{ON}	Turn-On Time	V_{DD} = 20V, I_D = 80A, V_{GS} = 10V, R_{GEN} = 7Ω		--	175	360	ns
$t_{d(on)}$	Turn-On Delay Time			--	43	95	ns
t_r	Rise Time			--	130	275	ns
$t_{d(off)}$	Turn-Off Delay Time			--	435	875	ns
t_f	Fall Time			--	290	590	ns
t_{OFF}	Turn-Off Time			--	730	1470	ns
Drain-Source Diode Characteristics and Maximum Ratings							
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 80A		--	--	1.25	V
		I_{SD} = 40A		--	--	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 75A, dI_{SD}/dt = 100A/μs		--	59	--	ns
Q_{RR}	Reverse Recovery Charge	I_{SD} = 75A, dI_{SD}/dt = 100A/μs		--	77	--	nC

NOTES:

1: Pulse width limited by maximum junction temperature.

2: Starting T_J = 25°C, L = 1mH, I_{AS} = 58A, V_{DD} = 36V, V_{GS} = 10V.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

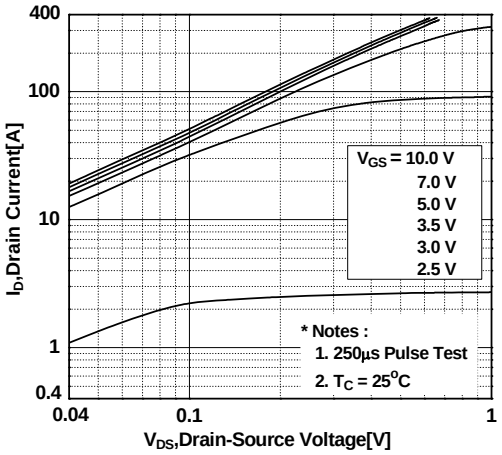


Figure 2. Transfer Characteristics

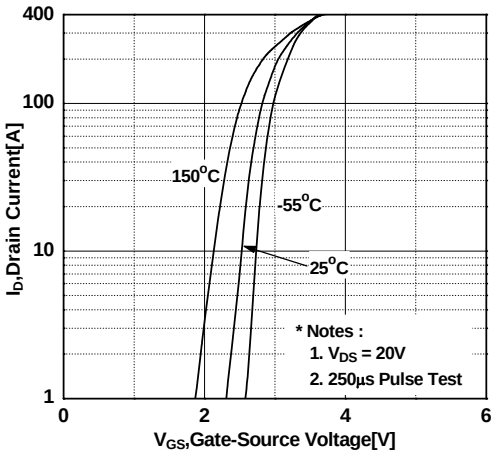


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

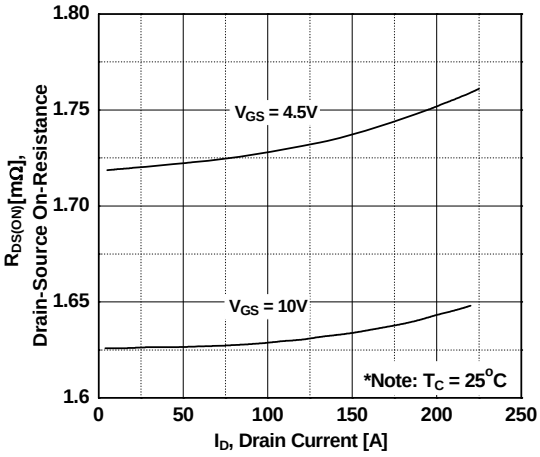


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

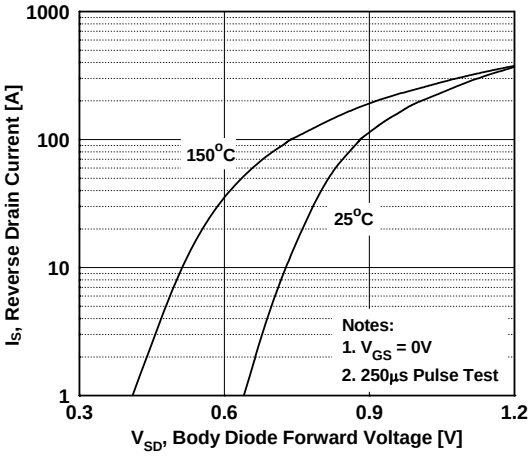


Figure 5. Capacitance Characteristics

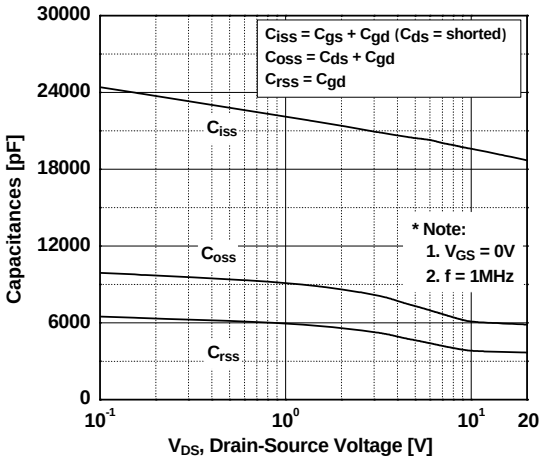
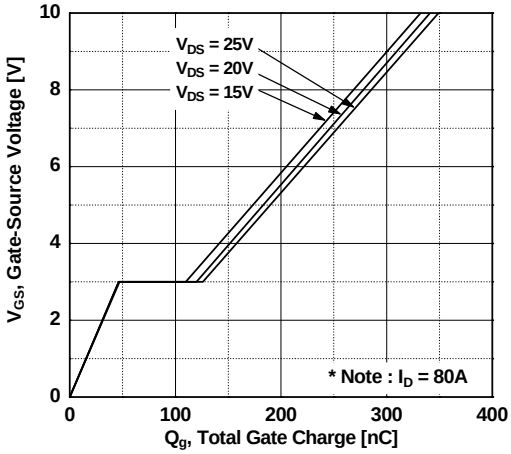


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

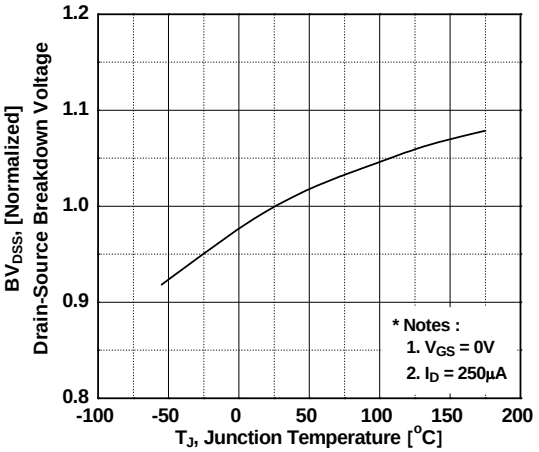


Figure 8. On-Resistance Variation vs. Temperature

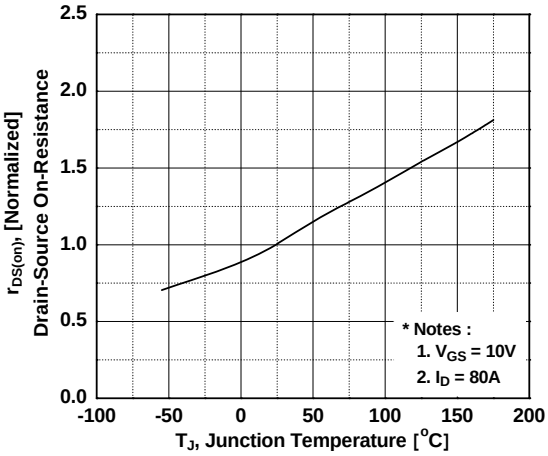


Figure 9. Unclamped Inductive Switching Capability

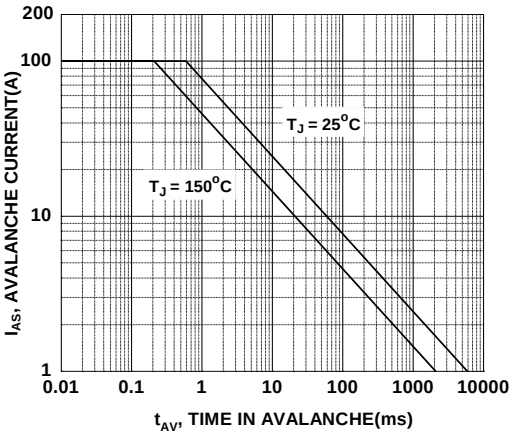


Figure 10. Safe Operating Area

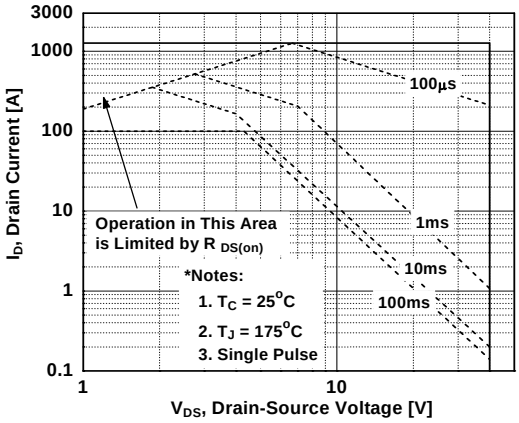
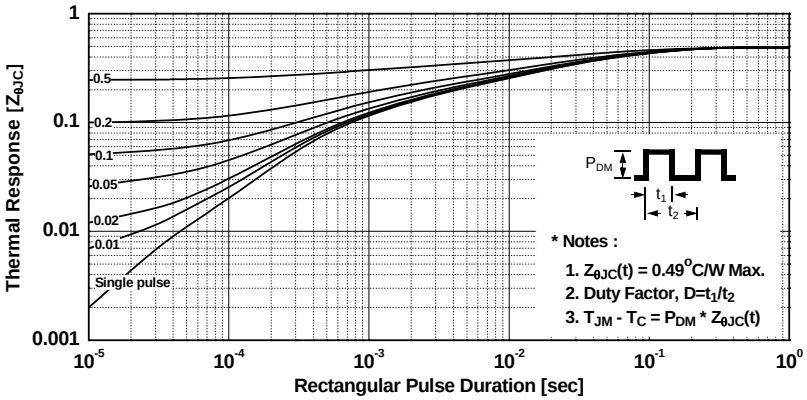
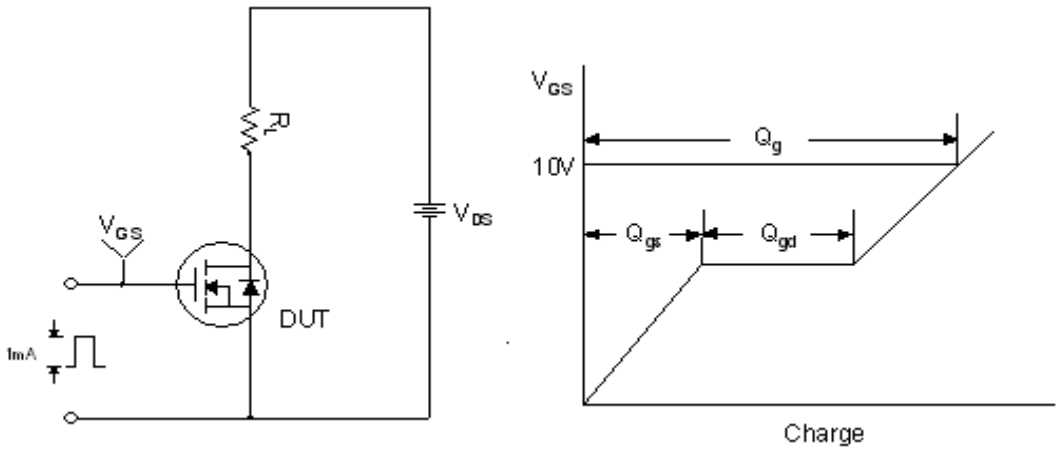


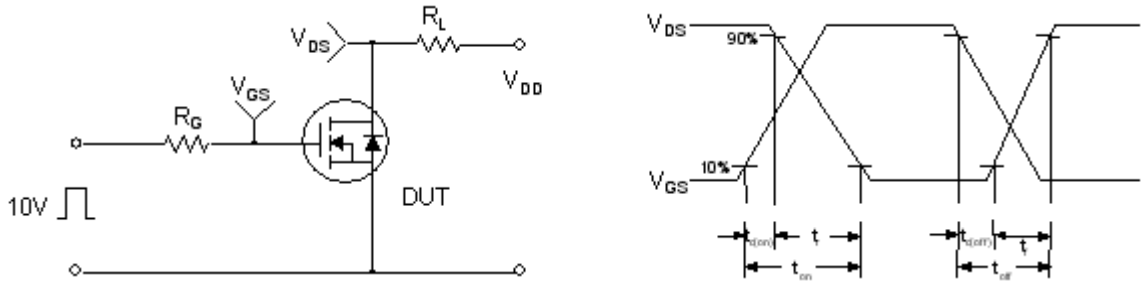
Figure 11. Transient Thermal Response Curve



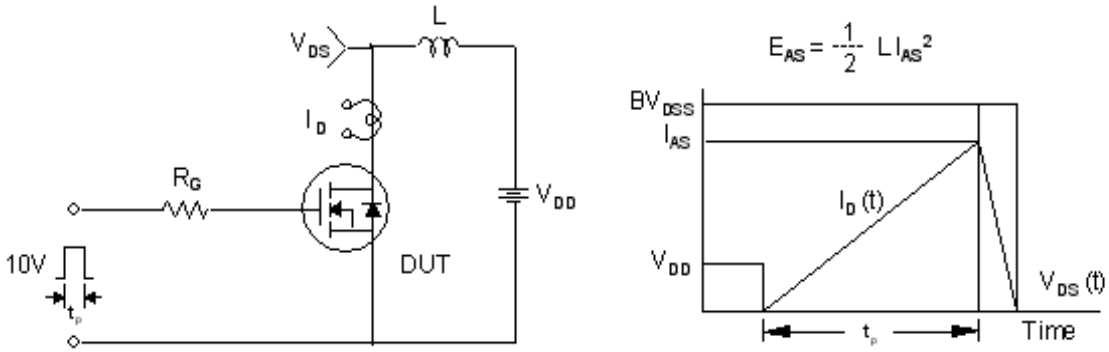
Gate Charge Test Circuit & Waveform



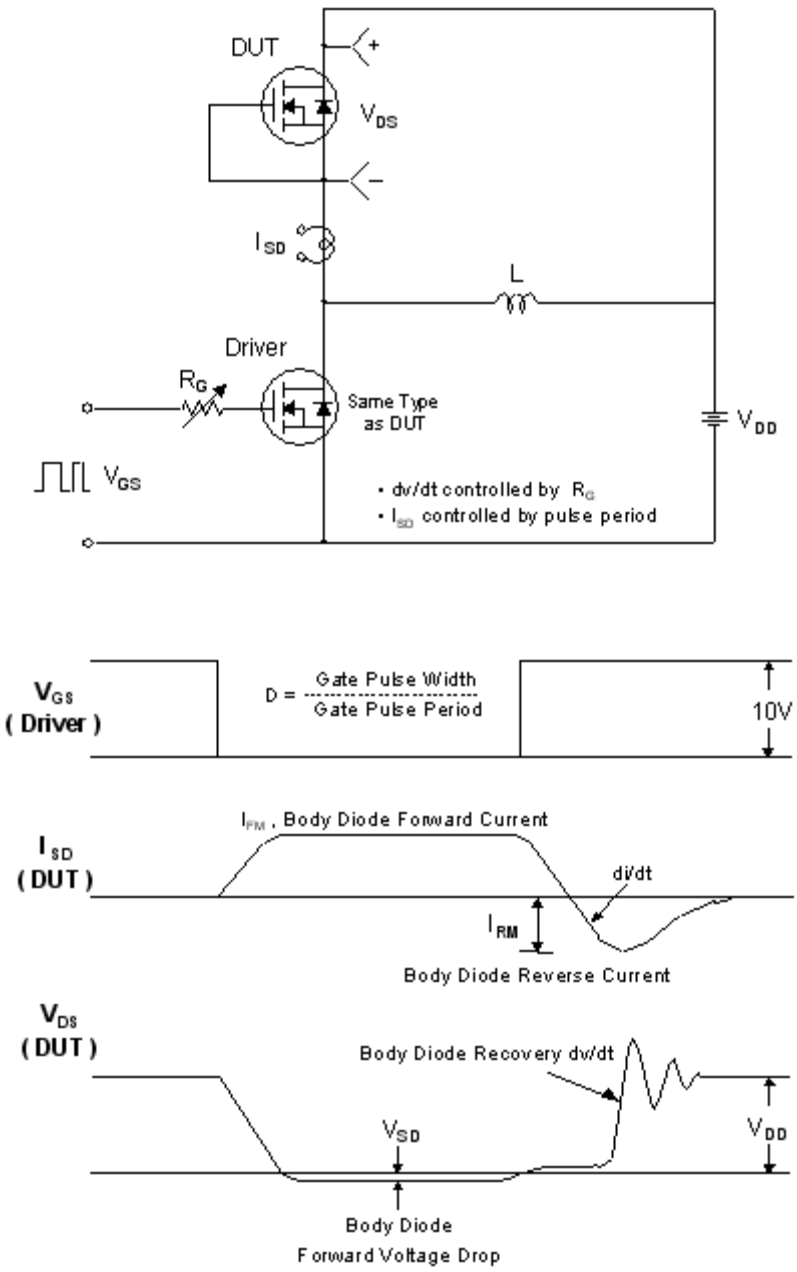
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

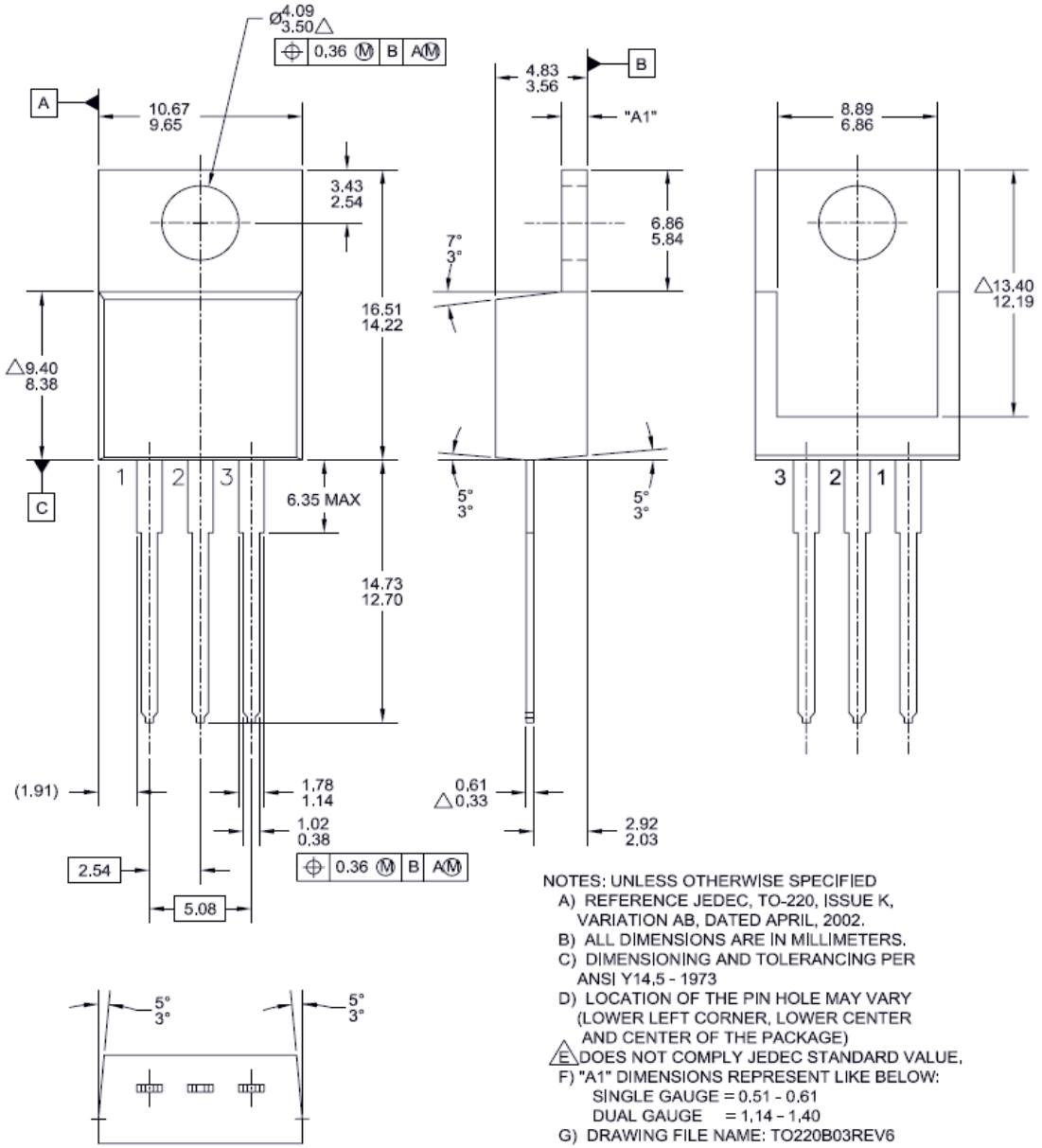


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-220B03



NOTES: UNLESS OTHERWISE SPECIFIED
A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1973
D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.14 – 1.40
G) DRAWING FILE NAME: TO220B03REV6

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