

# MC10EL58, MC100EL58

## 5.0 V ECL 2:1 Multiplexer

### Description

The MC10EL/100EL58 is a 2:1 multiplexer. The device is functionally equivalent to the E158 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E158, the EL58 is ideally suited for those applications which require the ultimate in AC performance.

The 100 Series contains temperature compensation.

### Features

- 230 ps Propagation Delay
- PECL Mode Operating Range:
  - ♦  $V_{CC} = 4.2\text{ V to }5.7\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:
  - ♦  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -4.2\text{ V to }-5.7\text{ V}$
- Internal Input Pulldown Resistors on  $D_a$ ,  $D_b$ , and SEL
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

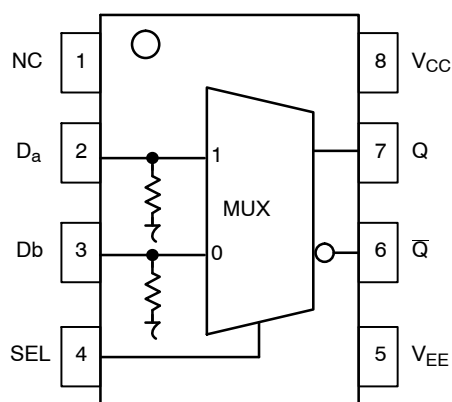


Figure 1. Logic Diagram and Pin Assignment



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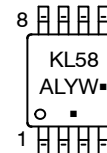
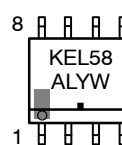
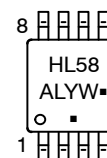
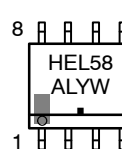


SOIC-8 NB  
D SUFFIX  
CASE 751-07



TSSOP-8  
DT SUFFIX  
CASE 948R-02

### MARKING DIAGRAMS\*



|                       |                     |
|-----------------------|---------------------|
| H = MC10              | L = Wafer Lot       |
| K = MC100             | Y = Year            |
| 4Z = MC10             | W = Work Week       |
| 2O = MC100            | M̄ = Date Code      |
| A = Assembly Location | ▪ = Pb-Free Package |

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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**Table 1. PIN DESCRIPTION**

| PIN                             | FUNCTION         |
|---------------------------------|------------------|
| D <sub>a</sub> , D <sub>b</sub> | ECL Data Inputs  |
| Q, Q̄                           | ECL Data Outputs |
| SEL                             | ECL Select Input |
| V <sub>CC</sub>                 | Positive Supply  |
| V <sub>EE</sub>                 | Negative Supply  |
| NC                              | No Connect       |

**Table 2. FUNCTION TABLE**

| SEL* | Data |
|------|------|
| H    | a    |
| L    | b    |

\* Pin will default low when left open.

**Table 3. ATTRIBUTES**

| Characteristics  | Value                |
|--|----------------------|
| Internal Input Pulldown Resistor   | 75 kΩ                |
| Internal Input Pullup Resistor   | N/A                  |
| ESD Protection<br>Human Body Model<br>Machine Model                                | > 1 kV<br>> 100 V    |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)<br>SOIC-8<br>TSSOP-8 | Level 1<br>Level 3   |
| Flammability Rating<br>Oxygen Index: 28 to 34                                      | UL 94 V-0 @ 0.125 in |
| Transistor Count   | 45                   |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test                             |                      |

1. Refer to Application Note [AND8003/D](#) for additional information.

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**Table 4. MAXIMUM RATINGS**

| Symbol           | Parameter  | Condition 1                                    | Condition 2  | Rating      | Unit |
|------------------|--|--|--|-------------|------|
| V <sub>CC</sub>  | PECL Mode Power Supply                             | V <sub>EE</sub> = 0 V                          |  | 8           | V    |
| V <sub>EE</sub>  | NECL Mode Power Supply                             | V <sub>CC</sub> = 0 V                          |  | -8          | V    |
| V <sub>I</sub>   | PECL Mode Input Voltage<br>NECL Mode Input Voltage | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> ≤ V <sub>CC</sub><br>V <sub>I</sub> ≥ V <sub>EE</sub> | 6<br>-6     | V    |
| I <sub>out</sub> | Output Current                                     | Continuous<br>Surge                            |  | 50<br>100   | mA   |
| T <sub>A</sub>   | Operating Temperature Range                        |  |  | -40 to +85  | °C   |
| T <sub>stg</sub> | Storage Temperature Range                          |  |  | -65 to +150 | °C   |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | SOIC-8 NB  | 190<br>130  | °C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)              |  | SOIC-8 NB  | 41 to 44    | °C/W |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | TSSOP-8  | 185<br>140  | °C/W |
| T <sub>sol</sub> | Wave Solder (Pb-Free)                              | <2 to 3 sec @ 260°C                            |  | 265         | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

**Table 5. 10EL SERIES PECL DC CHARACTERISTICS** (V<sub>CC</sub> = 5.0 V; V<sub>EE</sub> = 0.0 V (Note 1))

| Symbol          | Characteristic               | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit |
|-----------------|------------------------------|-------|------|------|------|------|------|------|------|------|------|
|                 |                              | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |      |
| I <sub>EE</sub> | Power Supply Current         |       | 14   | 17   |      | 14   | 17   |      | 14   | 17   | mA   |
| V <sub>OH</sub> | Output HIGH Voltage (Note 2) | 3920  | 4010 | 4110 | 4020 | 4105 | 4190 | 4090 | 4185 | 4280 | mV   |
| V <sub>OL</sub> | Output LOW Voltage (Note 2)  | 3050  | 3200 | 3350 | 3050 | 3210 | 3370 | 3050 | 3227 | 3405 | mV   |
| V <sub>IH</sub> | Input HIGH Voltage           | 3770  |      | 4110 | 3870 |      | 4190 | 3940 |      | 4280 | mV   |
| V <sub>IL</sub> | Input LOW Voltage            | 3050  |      | 3500 | 3050 |      | 3520 | 3050 |      | 3555 | mV   |
| I <sub>IH</sub> | Input HIGH Current           |       |      | 150  |      |      | 150  |      |      | 150  | μA   |
| I <sub>IL</sub> | Input LOW Current            | 0.5   |      |      | 0.5  |      |      | 0.3  |      |      | μA   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.06 V / -0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V<sub>CC</sub>-2 volts.

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**Table 6. 10EL SERIES NECL DC CHARACTERISTICS** ( $V_{CC}= 0.0\text{ V}$ ;  $V_{EE}= -5.0\text{ V}$  (Note 1))

| Symbol   | Characteristic               | -40°C |       |       | 25°C  |       |       | 85°C  |       |       | Unit |
|----------|------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|------|
|          |                              | Min   | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |      |
| $I_{EE}$ | Power Supply Current         |       | 14    | 17    |       | 14    | 17    |       | 14    | 17    | mA   |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | -1080 | -990  | -890  | -980  | -895  | -810  | -910  | -815  | -720  | mV   |
| $V_{OL}$ | Output LOW Voltage (Note 2)  | -1950 | -1800 | -1650 | -1950 | -1790 | -1630 | -1950 | -1773 | -1595 | mV   |
| $V_{IH}$ | Input HIGH Voltage           | -1230 |       | -890  | -1130 |       | -810  | -1060 |       | -720  | mV   |
| $V_{IL}$ | Input LOW Voltage            | -1950 |       | -1500 | -1950 |       | -1480 | -1950 |       | -1445 | mV   |
| $I_{IH}$ | Input HIGH Current           |       |       | 150   |       |       | 150   |       |       | 150   | μA   |
| $I_{IL}$ | Input LOW Current            | 0.5   |       |       | 0.5   |       |       | 0.3   |       |       | μA   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.06 V / -0.5 V.
2. Outputs are terminated through a 50 ohm resistor to  $V_{CC}-2$  volts.

**Table 7. 100EL SERIES PECL DC CHARACTERISTICS** ( $V_{CC}= 5.0\text{ V}$ ;  $V_{EE}= 0.0\text{ V}$  (Note 1))

| Symbol   | Characteristic               | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit |
|----------|------------------------------|-------|------|------|------|------|------|------|------|------|------|
|          |                              | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |      |
| $I_{EE}$ | Power Supply Current         |       | 14   | 17   |      | 14   | 17   |      | 16   | 19   | mA   |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 3915  | 3995 | 4120 | 3975 | 4045 | 4120 | 3975 | 4050 | 4120 | mV   |
| $V_{OL}$ | Output LOW Voltage (Note 2)  | 3170  | 3305 | 3445 | 3190 | 3295 | 3380 | 3190 | 3295 | 3380 | mV   |
| $V_{IH}$ | Input HIGH Voltage           | 3835  |      | 4120 | 3835 |      | 4120 | 3835 |      | 4120 | mV   |
| $V_{IL}$ | Input LOW Voltage            | 3190  |      | 3525 | 3190 |      | 3525 | 3190 |      | 3525 | mV   |
| $I_{IH}$ | Input HIGH Current           |       |      | 150  |      |      | 150  |      |      | 150  | μA   |
| $I_{IL}$ | Input LOW Current            | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | μA   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50 ohm resistor to  $V_{CC}-2$  volts.

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**Table 8. 100EL SERIES NECL DC CHARACTERISTICS** ( $V_{CC}= 0.0\text{ V}$ ;  $V_{EE}= -5.0\text{ V}$  (Note 1))

| Symbol   | Characteristic               | -40°C |       |       | 25°C  |       |       | 85°C  |       |       | Unit          |
|----------|------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
|          |                              | Min   | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |               |
| $I_{EE}$ | Power Supply Current         |       | 14    | 17    |       | 14    | 17    |       | 16    | 19    | mA            |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | -1085 | -1005 | -880  | -1025 | -955  | -880  | -1025 | -955  | -880  | mV            |
| $V_{OL}$ | Output LOW Voltage (Note 2)  | -1830 | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV            |
| $V_{IH}$ | Input HIGH Voltage           | -1165 |       | -880  | -1165 |       | -880  | -1165 |       | -880  | mV            |
| $V_{IL}$ | Input LOW Voltage            | -1810 |       | -1475 | -1810 |       | -1475 | -1810 |       | -1475 | mV            |
| $I_{IH}$ | Input HIGH Current           |       |       | 150   |       |       | 150   |       |       | 150   | $\mu\text{A}$ |
| $I_{IL}$ | Input LOW Current            | 0.5   |       |       | 0.5   |       |       | 0.5   |       |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

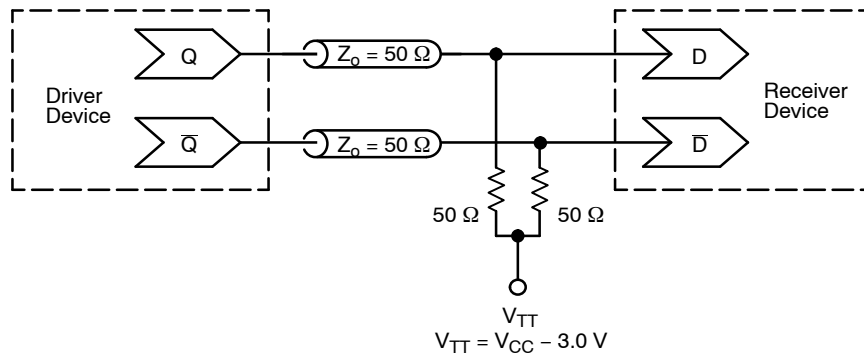
1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50 ohm resistor to  $V_{CC}-2$  volts.

**Table 9. AC CHARACTERISTICS** ( $V_{CC}= 5.0\text{ V}$ ;  $V_{EE}= 0.0\text{ V}$  or  $V_{CC}= 0.0\text{ V}$ ;  $V_{EE}= -5.0\text{ V}$  (Note 1))

| Symbol                 | Characteristic                                    | -40°C    |            |            | 25°C       |            |            | 85°C       |            |            | Unit |
|------------------------|---|----------|------------|------------|------------|------------|------------|------------|------------|------------|------|
|                        |   | Min      | Typ        | Max        | Min        | Typ        | Max        | Min        | Typ        | Max        |      |
| $f_{max}$              | Maximum Toggle Frequency                          |          |            |            |            | 1.5        |            |            |            |            | GHz  |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay to Output<br>D to Q<br>SEL to Q | 60<br>90 | 220<br>250 | 380<br>410 | 120<br>150 | 230<br>260 | 340<br>370 | 140<br>170 | 250<br>280 | 360<br>390 | ps   |
| $t_{JITTER}$           | Random Clock Jitter (RMS)                         |          |            |            |            | 0.9        |            |            |            |            | ps   |
| $t_r$<br>$t_f$         | Output Rise/Fall Times Q<br>(20% - 80%)           | 100      | 225        | 350        | 100        | 225        | 350        | 100        | 225        | 350        | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. 10 Series:  $V_{EE}$  can vary +0.06 V / -0.5 V.  
100 Series:  $V_{EE}$  can vary +0.8 V / -0.5 V.



**Figure 2. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

## MC10EL58, MC100EL58

### ORDERING INFORMATION

| Device        | Package              | Shipping <sup>†</sup> |
|---------------|----------------------|-----------------------|
| MC10EL58DG    | SOIC-8<br>(Pb-Free)  | 98 Units / Rail       |
| MC10EL58DR2G  | SOIC-8<br>(Pb-Free)  | 2500 / Tape & Reel    |
| MC10EL58DTG   | TSSOP-8<br>(Pb-Free) | 100 Units / Rail      |
| MC100EL58DG   | SOIC-8<br>(Pb-Free)  | 98 Units / Rail       |
| MC100EL58DR2G | SOIC-8<br>(Pb-Free)  | 2500 / Tape & Reel    |
| MC100EL58DTG  | TSSOP-8<br>(Pb-Free) | 100 Units / Rail      |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

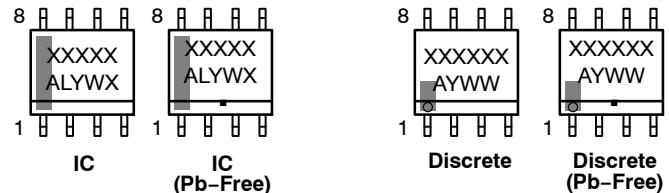
| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

|                  |             |  |
|------------------|-------------|--|
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| DESCRIPTION:     | SOIC-8 NB   | PAGE 1 OF 2  |

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |  |   |   |   |
|--|---|---|---|
| <p><b>STYLE 1:</b><br/> PIN 1. EMITTER<br/> 2. COLLECTOR<br/> 3. COLLECTOR<br/> 4. EMITTER<br/> 5. EMITTER<br/> 6. BASE<br/> 7. BASE<br/> 8. EMITTER</p>   | <p><b>STYLE 2:</b><br/> PIN 1. COLLECTOR, DIE, #1<br/> 2. COLLECTOR, #1<br/> 3. COLLECTOR, #2<br/> 4. COLLECTOR, #2<br/> 5. BASE, #2<br/> 6. EMITTER, #2<br/> 7. BASE, #1<br/> 8. EMITTER, #1</p>               | <p><b>STYLE 3:</b><br/> PIN 1. DRAIN, DIE #1<br/> 2. DRAIN, #1<br/> 3. DRAIN, #2<br/> 4. DRAIN, #2<br/> 5. GATE, #2<br/> 6. SOURCE, #2<br/> 7. GATE, #1<br/> 8. SOURCE, #1</p>                            | <p><b>STYLE 4:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. ANODE<br/> 4. ANODE<br/> 5. ANODE<br/> 6. ANODE<br/> 7. ANODE<br/> 8. COMMON CATHODE</p>   |
| <p><b>STYLE 5:</b><br/> PIN 1. DRAIN<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. DRAIN<br/> 5. GATE<br/> 6. GATE<br/> 7. SOURCE<br/> 8. SOURCE</p>   | <p><b>STYLE 6:</b><br/> PIN 1. SOURCE<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. SOURCE<br/> 5. SOURCE<br/> 6. GATE<br/> 7. GATE<br/> 8. SOURCE</p>  | <p><b>STYLE 7:</b><br/> PIN 1. INPUT<br/> 2. EXTERNAL BYPASS<br/> 3. THIRD STAGE SOURCE<br/> 4. GROUND<br/> 5. DRAIN<br/> 6. GATE 3<br/> 7. SECOND STAGE Vd<br/> 8. FIRST STAGE Vd</p>                    | <p><b>STYLE 8:</b><br/> PIN 1. COLLECTOR, DIE #1<br/> 2. BASE, #1<br/> 3. BASE, #2<br/> 4. COLLECTOR, #2<br/> 5. COLLECTOR, #2<br/> 6. EMITTER, #2<br/> 7. EMITTER, #1<br/> 8. COLLECTOR, #1</p>                              |
| <p><b>STYLE 9:</b><br/> PIN 1. EMITTER, COMMON<br/> 2. COLLECTOR, DIE #1<br/> 3. COLLECTOR, DIE #2<br/> 4. EMITTER, COMMON<br/> 5. EMITTER, COMMON<br/> 6. BASE, DIE #2<br/> 7. BASE, DIE #1<br/> 8. EMITTER, COMMON</p> | <p><b>STYLE 10:</b><br/> PIN 1. GROUND<br/> 2. BIAS 1<br/> 3. OUTPUT<br/> 4. GROUND<br/> 5. GROUND<br/> 6. BIAS 2<br/> 7. INPUT<br/> 8. GROUND</p>  | <p><b>STYLE 11:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. DRAIN 2<br/> 7. DRAIN 1<br/> 8. DRAIN 1</p>   | <p><b>STYLE 12:</b><br/> PIN 1. SOURCE<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 13:</b><br/> PIN 1. N.C.<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>  | <p><b>STYLE 14:</b><br/> PIN 1. N-SOURCE<br/> 2. N-GATE<br/> 3. P-SOURCE<br/> 4. P-GATE<br/> 5. P-DRAIN<br/> 6. P-DRAIN<br/> 7. N-DRAIN<br/> 8. N-DRAIN</p>   | <p><b>STYLE 15:</b><br/> PIN 1. ANODE 1<br/> 2. ANODE 1<br/> 3. ANODE 1<br/> 4. ANODE 1<br/> 5. CATHODE, COMMON<br/> 6. CATHODE, COMMON<br/> 7. CATHODE, COMMON<br/> 8. CATHODE, COMMON</p>               | <p><b>STYLE 16:</b><br/> PIN 1. EMITTER, DIE #1<br/> 2. BASE, DIE #1<br/> 3. EMITTER, DIE #2<br/> 4. BASE, DIE #2<br/> 5. COLLECTOR, DIE #2<br/> 6. COLLECTOR, DIE #2<br/> 7. COLLECTOR, DIE #1<br/> 8. COLLECTOR, DIE #1</p> |
| <p><b>STYLE 17:</b><br/> PIN 1. VCC<br/> 2. V2OUT<br/> 3. V1OUT<br/> 4. TXE<br/> 5. RXE<br/> 6. VEE<br/> 7. GND<br/> 8. ACC</p>  | <p><b>STYLE 18:</b><br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. CATHODE<br/> 8. CATHODE</p>   | <p><b>STYLE 19:</b><br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. MIRROR 2<br/> 7. DRAIN 1<br/> 8. MIRROR 1</p>   | <p><b>STYLE 20:</b><br/> PIN 1. SOURCE (N)<br/> 2. GATE (N)<br/> 3. SOURCE (P)<br/> 4. GATE (P)<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p><b>STYLE 21:</b><br/> PIN 1. CATHODE 1<br/> 2. CATHODE 2<br/> 3. CATHODE 3<br/> 4. CATHODE 4<br/> 5. CATHODE 5<br/> 6. COMMON ANODE<br/> 7. COMMON ANODE<br/> 8. CATHODE 6</p>  | <p><b>STYLE 22:</b><br/> PIN 1. I/O LINE 1<br/> 2. COMMON CATHODE/VCC<br/> 3. COMMON CATHODE/VCC<br/> 4. I/O LINE 3<br/> 5. COMMON ANODE/GND<br/> 6. I/O LINE 4<br/> 7. I/O LINE 5<br/> 8. COMMON ANODE/GND</p> | <p><b>STYLE 23:</b><br/> PIN 1. LINE 1 IN<br/> 2. COMMON ANODE/GND<br/> 3. COMMON ANODE/GND<br/> 4. LINE 2 IN<br/> 5. LINE 2 OUT<br/> 6. COMMON ANODE/GND<br/> 7. COMMON ANODE/GND<br/> 8. LINE 1 OUT</p> | <p><b>STYLE 24:</b><br/> PIN 1. BASE<br/> 2. EMITTER<br/> 3. COLLECTOR/ANODE<br/> 4. COLLECTOR/ANODE<br/> 5. CATHODE<br/> 6. CATHODE<br/> 7. COLLECTOR/ANODE<br/> 8. COLLECTOR/ANODE</p>                                      |
| <p><b>STYLE 25:</b><br/> PIN 1. VIN<br/> 2. N/C<br/> 3. REXT<br/> 4. GND<br/> 5. IOUT<br/> 6. IOUT<br/> 7. IOUT<br/> 8. IOUT</p>   | <p><b>STYLE 26:</b><br/> PIN 1. GND<br/> 2. dv/dt<br/> 3. ENABLE<br/> 4. ILIMIT<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. VCC</p>  | <p><b>STYLE 27:</b><br/> PIN 1. ILIMIT<br/> 2. OVLO<br/> 3. UVLO<br/> 4. INPUT+<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. DRAIN</p>  | <p><b>STYLE 28:</b><br/> PIN 1. SW_TO_GND<br/> 2. DASIC OFF<br/> 3. DASIC_SW_DET<br/> 4. GND<br/> 5. V_MON<br/> 6. VBULK<br/> 7. VBULK<br/> 8. VIN</p>  |
| <p><b>STYLE 29:</b><br/> PIN 1. BASE, DIE #1<br/> 2. EMITTER, #1<br/> 3. BASE, #2<br/> 4. EMITTER, #2<br/> 5. COLLECTOR, #2<br/> 6. COLLECTOR, #2<br/> 7. COLLECTOR, #1<br/> 8. COLLECTOR, #1</p>                        | <p><b>STYLE 30:</b><br/> PIN 1. DRAIN 1<br/> 2. DRAIN 1<br/> 3. GATE 2<br/> 4. SOURCE 2<br/> 5. SOURCE 1/DRAIN 2<br/> 6. SOURCE 1/DRAIN 2<br/> 7. SOURCE 1/DRAIN 2<br/> 8. GATE 1</p>                           |   |   |

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

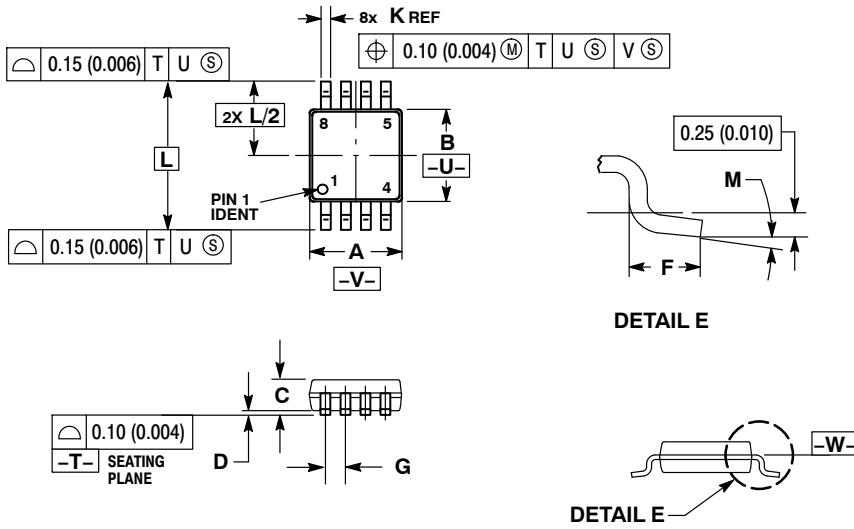
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SCALE 2:1

### TSSOP 8 CASE 948R-02 ISSUE A

DATE 04/07/2000



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 2.90        | 3.10 | 0.114     | 0.122 |
| B   | 2.90        | 3.10 | 0.114     | 0.122 |
| C   | 0.80        | 1.10 | 0.031     | 0.043 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.40        | 0.70 | 0.016     | 0.028 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| K   | 0.25        | 0.40 | 0.010     | 0.016 |
| L   | 4.90 BSC    |      | 0.193 BSC |       |
| M   | 0°          | 6°   | 0°        | 6°    |

|                         |                    |  |
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