MCP48FXBX4/8

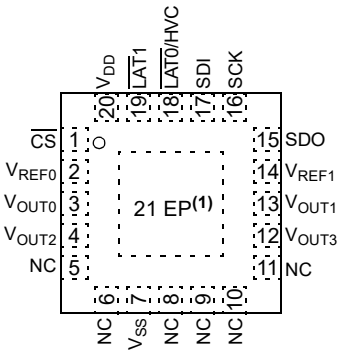
8/10/12-Bit Quad/Octal Voltage Output, 6 LSb INL Digital-to-Analog Converters with SPI Interface

Features

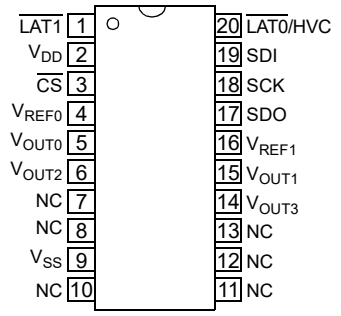
- Operating Voltage Range:
  - 2.7V to 5.5V – Full specifications
  - 1.8V to 2.7V – Reduced device specifications
- Output Voltage Resolutions:
  - 8-bit: **MCP48FXB0X** (256 steps)
  - 10-bit: **MCP48FXB1X** (1024 steps)
  - 12-bit: **MCP48FXB2X** (4096 steps)
- Rail-to-Rail Output
- Fast Settling Time of 7.8 µs (Typical)
- DAC Voltage Reference Source Options:
  - Device V_{DD}
  - External V_{REF} pin (buffered or unbuffered)
  - Internal band gap (1.22V typical)
- Output Gain Options:
  - 1x (unity)
  - 2x (available when not using internal V_{DD} as voltage source)
- Nonvolatile Memory (EEPROM) Option:
  - User-programmable Power-on Reset (POR)/Brown-out Reset (BOR) output setting and device Configuration bits recall
  - Auto-recall of saved DAC register setting
  - Auto-recall of saved device configuration (voltage reference, gain, power-down)
- Power-on/Brown-out Reset Protection
- Power-Down Modes:
  - Disconnects output buffer (high-impedance)
  - Selection of V_{OUT} pull-down resistors (125 kΩ or 1 kΩ)
- Low-Power Consumption:
  - Normal operation: <2.6 mA (quad), 3.2 mA (octal)
  - Power-down operation: 680 nA typical
  - EEPROM write cycle: 2.2 mA (quad), 2.7 mA (octal) maximum
- SPI Interface:
  - Supports Mode 0,0 and Mode 1,1
  - Up to 20 MHz writes and 10 MHz reads
  - Input buffers support interfacing to low-voltage digital devices
- Package Types: 20-Lead TSSOP, 20-Lead 5 mm x 5 mm VQFN
- Extended Temperature Range: -40°C to +125°C

Package Types

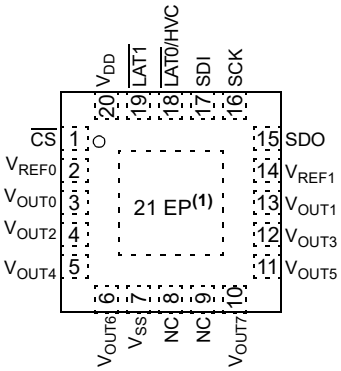
MCP48FXBX4
20-Lead VQFN
5x5 mm Quad



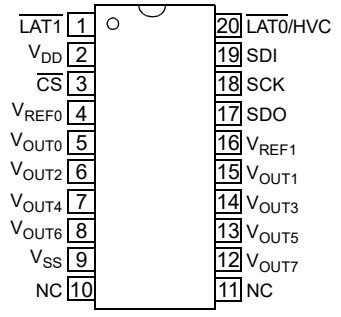
MCP48FXBX4
20-Lead TSSOP
Quad



MCP48FXBX8
20-Lead VQFN
5x5 mm Octal



MCP48FXBX8
20-Lead TSSOP
Octal



Note 1: Includes Exposed Thermal Pad (EP); see Table 3-1 and Table 3-2.

General Description

The MCP48FXBX4/8 devices are a family of buffered voltage output Digital-to-Analog Converters (DAC), with the following options:

- Quad or octal output channel configurations
- 8/10/12-bit resolution
- Volatile or nonvolatile user memory

The quad and octal options differ only by the number of output channels. The volatile and nonvolatile versions have an identical analog circuit structure.

There are three voltage reference sources: the external V_{REF} pin, the device's V_{DD} or an internal band gap voltage source.

When the V_{DD} mode is selected, it is internally connected to the DAC's reference circuit. When the external V_{REF} pin is used, the user has the option to select between a gain of 1 and 2 if the Buffered mode is used, or the internal buffer can be bypassed entirely in the External V_{REF} Unbuffered mode.

In the Internal Band Gap Voltage Reference mode, the gain can be selected between 2 and 4.

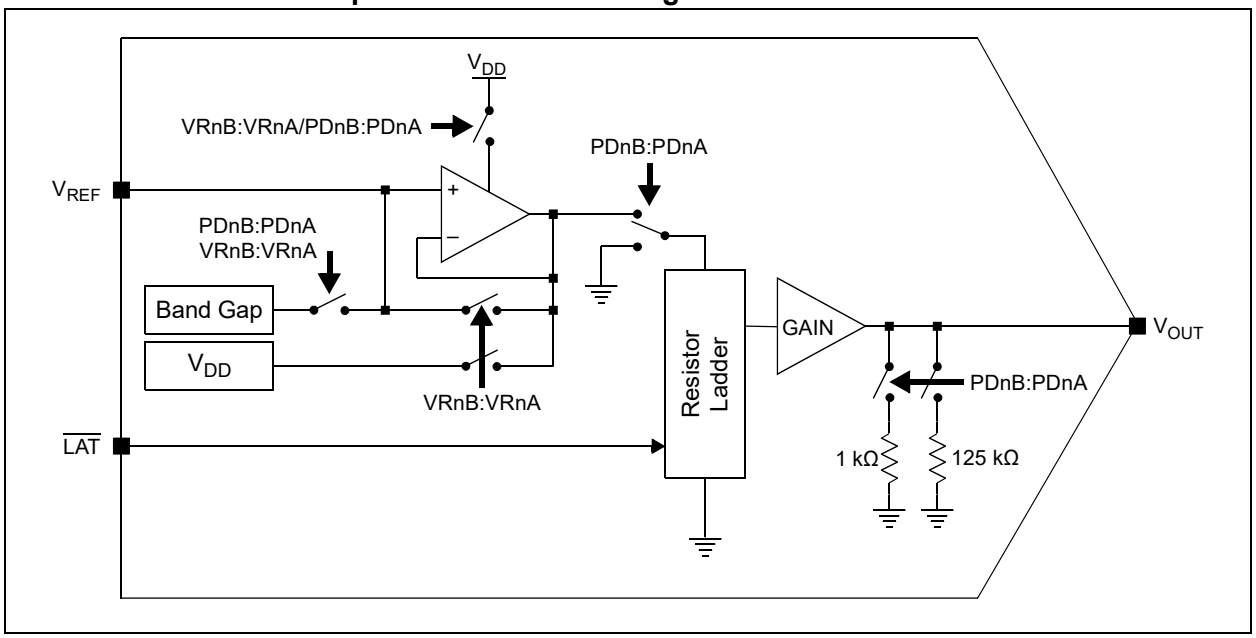
This family of devices features WiperLock™ functionality, which prevents inadvertent changes of the output value. It uses a high voltage on a specific pin, together with dedicated commands, to lock the values that are stored in memory.

These devices have an SPI compatible serial interface. `WRITE` commands are supported up to 20 MHz, while `READ` commands are supported up to 10 MHz.

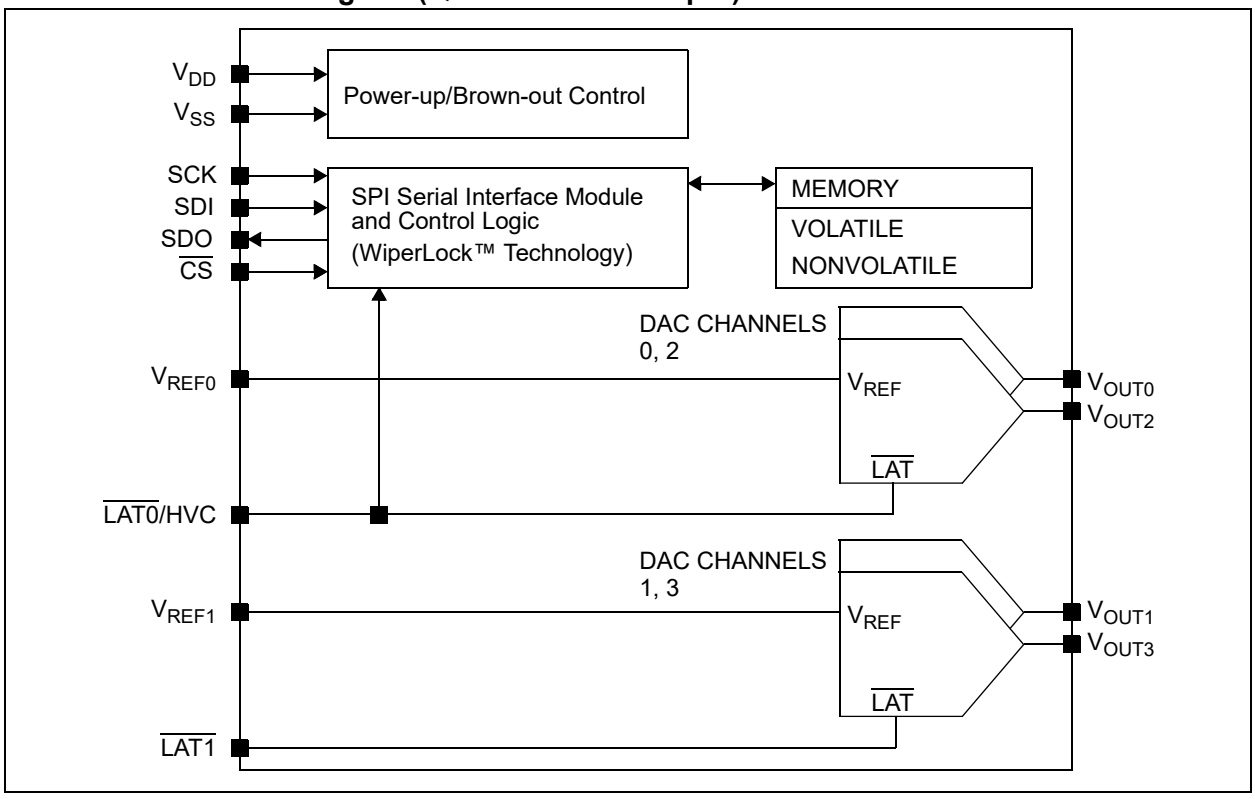
Applications

- Set Point or Offset Trimming
- Sensor Calibration
- Low-Power Portable Instrumentation
- PC Peripherals
- Data Acquisition Systems
- Motor Control

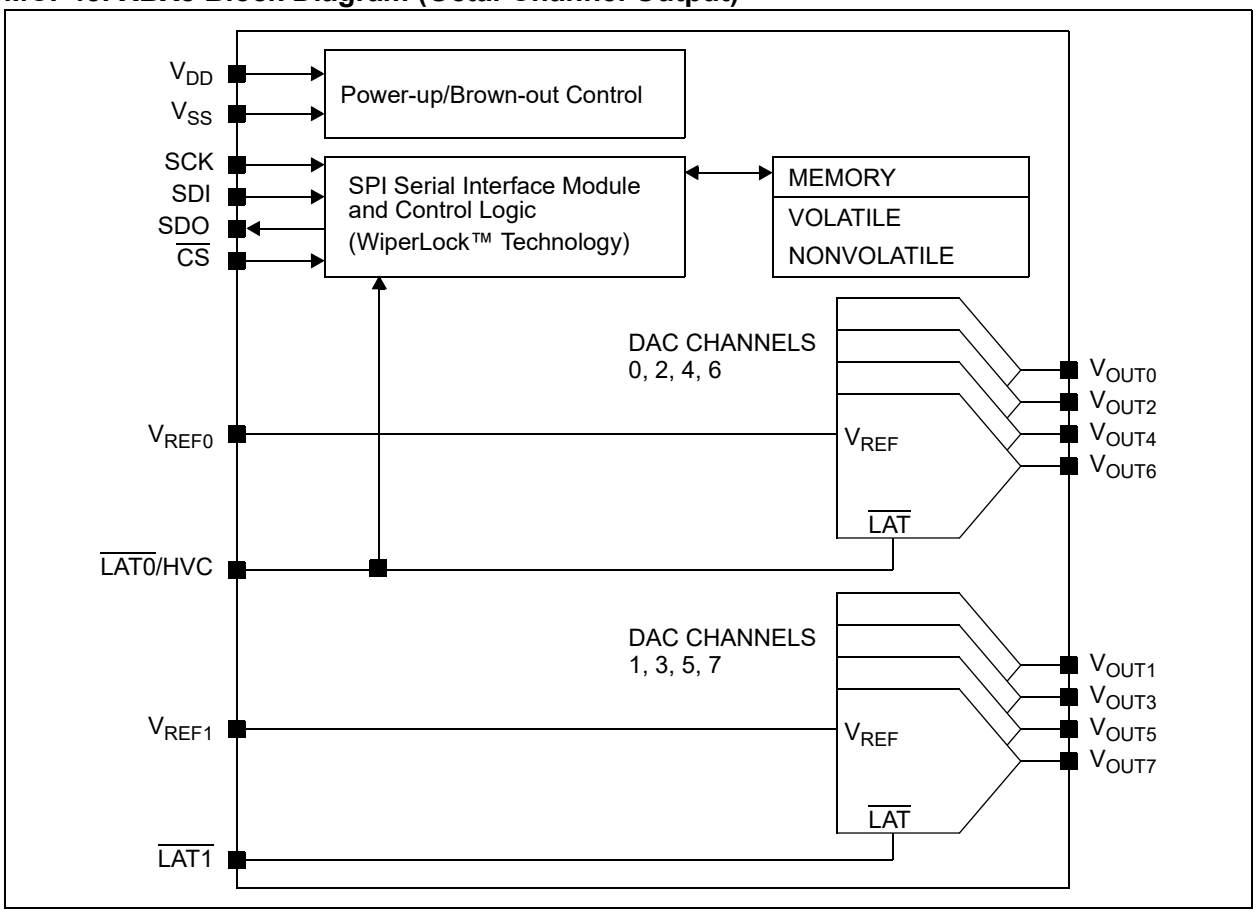
MCP48FXBX4/8 DAC Output Channel Block Diagram



MCP48FXBX4 Block Diagram (Quad-Channel Output)



MCP48FXBX8 Block Diagram (Octal-Channel Output)



Device Features

Device	Package Type	# of Channels	Resolution (bits)	DAC Output POR/BOR Setting(1)	# of V_{REF} Inputs	# of $\overline{LAT}$ Inputs	Internal Band Gap	Memory
MCP48FVB04	VQFN-20 5 x 5, TSSOP-20	4	8	7Fh	2	2	Yes	RAM
MCP48FVB14	VQFN-20 5 x 5, TSSOP-20	4	10	1FFh	2	2	Yes	RAM
MCP48FVB24	VQFN-20 5 x 5, TSSOP-20	4	12	7FFh	2	2	Yes	RAM
MCP48FVB08	VQFN-20 5 x 5, TSSOP-20	8	8	7Fh	2	2	Yes	RAM
MCP48FVB18	VQFN-20 5 x 5, TSSOP-20	8	10	1FFh	2	2	Yes	RAM
MCP48FVB28	VQFN-20 5 x 5, TSSOP-20	8	12	7FFh	2	2	Yes	RAM
MCP48FEB04	VQFN-20 5 x 5, TSSOP-20	4	8	7Fh	2	2	Yes	EEPROM
MCP48FEB14	VQFN-20 5 x 5, TSSOP-20	4	10	1FFh	2	2	Yes	EEPROM
MCP48FEB24	VQFN-20 5 x 5, TSSOP-20	4	12	7FFh	2	2	Yes	EEPROM
MCP48FEB08	VQFN-20 5 x 5, TSSOP-20	8	8	7Fh	2	2	Yes	EEPROM
MCP48FEB18	VQFN-20 5 x 5, TSSOP-20	8	10	1FFh	2	2	Yes	EEPROM
MCP48FEB28	VQFN-20 5 x 5, TSSOP-20	8	12	7FFh	2	2	Yes	EEPROM

Note 1: The factory default value. The DAC output POR/BOR value can be modified via the nonvolatile DAC Output register (available only on nonvolatile devices – MCP48FEBXX).

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Voltage on V_{DD} with Respect to V_{SS} ..... -0.6V to +6.5V
Voltage on All Pins with Respect to V_{SS} ..... -0.6V to V_{DD}+0.3V
Input Clamp Current, I_{IK} ($V_I < 0$, $V_I > V_{DD}$, $V_I > V_{PP}$ on HV Pins) ..... ±20 mA
Output Clamp Current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) ..... ±20 mA
Maximum Current out of the V_{SS} Pin (Quad) ..... 150 mA
(Octal) ..... 150 mA
Maximum Current into the V_{DD} Pin (Quad) ..... 150 mA
(Octal) ..... 150 mA
Maximum Current Sourced by the V_{OUT} Pin ..... 20 mA
Maximum Current Sunk by the V_{OUT} Pin ..... 20 mA
Maximum Current Sunk by the V_{REF} Pin ..... 125 µA
Maximum Input Current Source/Sunk by the SDI, SCK and $\overline{CS}$ Pins ..... 2 mA
Maximum Output Current Sunk by the SDO Output Pin ..... 25 mA
Total Power Dissipation(1) ..... 400 mW
Package Power Dissipation (T_A = +50°C, T_J = +150°C)
20-Lead TSSOP ..... 1300 mW
20-Lead VQFN (5 x 5 mm, ML) ..... 2800 mW
ESD Protection on all Pins ..... ≥ ±6 kV (HBM)
..... ≥ ±400V (MM)
..... ≥ ±2 kV (CDM)
Latch-up (per JEDEC® JESD78A) at +125°C ..... ±100 mA
Storage Temperature ..... -65°C to +150°C
Ambient Temperature with Power Applied ..... -55°C to +125°C
Soldering Temperature of Leads (10 seconds) ..... +300°C
Maximum Junction Temperature (T_J) ..... +150°C

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Power dissipation is calculated as follows:
$P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD} - V_{OH}) \times I_{OH}\} + \Sigma(V_{OL} \times I_{OL})$

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended).
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{DD}	2.7	—	5.5	V	
		1.8	—	2.7	V	Serial interface operational, DAC operation with reduced analog specifications
V_{DD} Voltage (Rising) to Ensure Device Power-on Reset	$V_{POR/BOR}$	—	—	1.7	V	RAM retention voltage: (V_{RAM}) < V_{POR}, V_{DD} voltages greater than the $V_{POR/BOR}$ limit ensure that the device is out of Reset
V_{DD} Rise Rate to Ensure Power-on Reset	V_{DDRR}	Note 3			V/ms	
High-Voltage Commands Voltage Range (HVC Pin)	V_{HV}	V_{SS}	—	12.5	V	The HVC pin will be at one of the three input levels (V_{IL}, V_{IH} or V_{IHH})(1)
High-Voltage Input Entry Voltage	V_{IHHEN}	9.0	—	—	V	Threshold for entry into WiperLock™ technology
High-Voltage Input Exit Voltage	V_{IHHEX}	—	—	V_{DD} + 0.8V	V	Note 1

Note 1: This parameter is ensured by design.
3: POR/BOR voltage trip point is not slope dependent. Hysteresis implemented with time delay.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended).
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions		
Supply Current	I_{DD}	—	—	1.0	mA	Quad	1 MHz(1)	Serial interface active (not High-Voltage Command), VRnB:VRnA = All Modes(4), V_{OUT} is unloaded, V_{DD} = 5.5V, Volatile DAC Register = Midscale
		—	—	1.7	mA		10 MHz(1)	
		—	—	2.6	mA		20 MHz	
		—	—	1.6	mA	Octal	1 MHz(1)	
		—	—	2.3	mA		10 MHz(1)	
		—	—	3.2	mA		20 MHz	
		—	—	0.85	mA	Quad	Serial interface inactive(1) (not High-Voltage Command), VRnB:VRnA = All Modes, SCK = SDI = V_{SS}, V_{OUT} is unloaded, Volatile DAC Register = Midscale	
		—	—	1.6	mA	Octal		
		—	—	2.2	mA	Quad	EE write current, V_{REF} = V_{DD} = 5.5V (after write, serial interface is inactive), write 0x7FF to nonvolatile DAC0 (address 10h), V_{OUT} pins are unloaded	
		—	—	2.7	mA	Octal		
		—	560	700	µA	Quad	HVC = 12.5V (High-Voltage Command), serial interface inactive, V_{REF} = V_{DD} = 5.5V, $\overline{LAT}$/HVC = V_{IHH}, DAC Registers = Midscale, V_{OUT} pins are unloaded	
		—	1100	1300	µA	Octal		
Power-Down Current	I_{DDP}	—	0.68	3.8	µA	PDnB:PDnA = 01(5), V_{OUT} not connected		

Note 1: This parameter is ensured by characterization.
4: Supply current is independent of current through the resistor ladder in mode VRnB:VRnA = 10.
5: The PDnB:PDnA = 00, 10 and 11 configurations should have the same current.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended).
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Resistor Ladder Resistance	R_L	100	140	180	kΩ	VRnB:VRnA = 10, V_{REF} = V_{DD} (6)	
Resolution; # of Resistors and # of Taps (see **B.1 "Resolution"**)	N	256			Taps	8-bit	No missing codes
		1024			Taps	10-bit	No missing codes
		4096			Taps	12-bit	No missing codes
Nominal V_{OUT} Match (11)	$\lvert V_{OUT} - V_{OUTMEAN} \rvert / V_{OUTMEAN}$	—	0.5	1.0	%	2.7V ≤ V_{DD} ≤ 5.5V (2)	
		—	—	1.2	%	1.8V (2)	
V_{OUT} Temperature Coefficient (see **B.19 "V_{OUT} Temperature Coefficient"**)	$\Delta V_{OUT}/\Delta T$	—	15	—	ppm/°C	Code = Midscale (7Fh, 1FFh or 7FFh)	
V_{REF} Pin Input Voltage Range	V_{REF}	V_{SS}	—	V_{DD}	V	1.8V ≤ V_{DD} ≤ 5.5V (1)	

Note 1: This parameter is ensured by design.

2: This parameter is ensured by characterization.

6: Resistance is defined as the resistance between the V_{REF} pin (mode VRnB:VRnA = 10) to V_{SS} pin. For octal-channel devices (MCP48FXBX8), this is the effective resistance of each resistor ladder. The resistance measurement is one of the two resistor ladders measured in parallel.

11: Variation of one output voltage to mean output voltage.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended).
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Zero-Scale Error; Code = 000h (see **B.5 "Zero-Scale Error (EZS)"**)	E_{ZS}	—	—	0.75	LSb	8-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		—	—	3	LSb	10-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		—	—	12	LSb	12-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0 "Typical Performance Curves"**(1)			LSb		VRnB:VRnA = 11, Gx = 0, Gx = 1, V_{REF} = 0.5 × V_{DD} = 2.7, no load
		See **Section 2.0 "Typical Performance Curves"**(1)			LSb		VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7-5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(1)			LSb		VRnB:VRnA = 10, Gx = 0, Gx= 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7-5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(1)			LSb		VRnB:VRnA = 00, Gx = 0, V_{REF} = V_{DD} = 2.7-5.5V, no load
Full-Scale Error (see **B.4 "Full-Scale Error (EFS)"**)	E_{FS}	—	—	4.5	LSb	8-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		—	—	18	LSb	10-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		—	—	70	LSb	12-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0 "Typical Performance Curves"**(1)			LSb		VRnB:VRnA = 11, Gx = 0, Gx = 1, V_{REF} = 0.5 × V_{DD} = 2.7, no load
		See **Section 2.0 "Typical Performance Curves"**(1)			LSb		VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7-5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(1)			LSb		VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7-5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(1)			LSb		VRnB:VRnA = 00, Gx = 0, V_{REF} = V_{DD} = 2.7-5.5V, no load
Offset Error (see **B.7 "Offset Error (EOS)"**)	E_{OS}	-15	±1.5	+15	mV	VRnB:VRnA = 00, Gx = 0, no load	
Offset Voltage Temperature Coefficient	V_{OSTC}	—	±10	—	µV/°C		

Note 1: This parameter is ensured by characterization.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended).
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Gain Error (see **B.9 "Gain Error (EG)"**)(8)	E_G	-1.0	±0.1	+1.0	% of FSR	8-bit	Code = 250, no load, VRnB:VRnA = 00, Gx = 0
		-1.0	±0.1	+1.0	% of FSR	10-bit	Code = 1000, no load, VRnB:VRnA = 00, Gx = 0
		-1.0	±0.1	+1.0	% of FSR	12-bit	Code = 4000, no load, VRnB:VRnA = 00, Gx = 0
Gain Error Drift (see **B.10 "Gain Error Drift (EGD)"**)	ΔG/°C	—	-3	—	ppm/°C		
Total Unadjusted Error (see **B.6 "Total Unadjusted Error (ET)"**)(2)	E_T	-2.5	—	+0.5	LSb	8-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		-10.0	—	+2.0	LSb	10-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		-40.0	—	+8.0	LSb	12-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0 "Typical Performance Curves"**(1)					VRnB:VRnA = 11, Gx = 0, Gx = 1, V_{REF} = 0.5 × V_{DD} = 2.7, no load
		See **Section 2.0 "Typical Performance Curves"**(1)					VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7-5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(1)					VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7-5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(1)					VRnB:VRnA = 00, Gx = 0, V_{REF} = V_{DD} = 2.7-5.5V, no load

Note 1: This parameter is ensured by characterization.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended).
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Integral Nonlinearity (see **B.11 "Integral Nonlinearity (INL)"**)(7,10)	INL	-0.5	±0.1	+0.5	LSb	8-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		-1.5	±0.4	+1.5	LSb	10-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		-6	±1.5	+6	LSb	12-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0 "Typical Performance Curves"**(1)			LSb		VRnB:VRnA = 11, Gx = 0, Gx = 1, V_{REF} = 0.5 × V_{DD} = 2.7, no load
		See **Section 2.0 "Typical Performance Curves"**(1)			LSb		VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7-5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(1)			LSb		VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7-5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**(1)			LSb		VRnB:VRnA = 00, Gx = 0, V_{REF} = V_{DD} = 2.7-5.5V, no load

Note 1: This parameter is ensured by characterization.
7: INL and DNL are measured at V_{OUT} with V_{RL} = V_{DD} (VRnB:VRnA = 00).
10: Code range is dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, 100 to 4000.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended).
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Differential Nonlinearity (see **B.12 "Differential Nonlinearity (DNL)"**)[7,10]	DNL	-0.25	±0.0125	+0.25	LSb	8-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		-0.5	±0.05	+0.5	LSb	10-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		-1.0	±0.2	+1.0	LSb	12-bit	VRnB:VRnA = 10, Gx = 0, V_{REF} = V_{DD}, no load
		See **Section 2.0 "Typical Performance Curves"**[1]			LSb		VRnB:VRnA = 11, Gx = 0, Gx = 1, V_{REF} = 0.5 × V_{DD} = 2.7, no load
		See **Section 2.0 "Typical Performance Curves"**[1]			LSb		VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7-5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**[1]			LSb		VRnB:VRnA = 10, Gx = 0, Gx = 1, V_{REF} = V_{DD}/2, V_{REF} = V_{DD}, V_{DD} = 2.7-5.5V, no load
		See **Section 2.0 "Typical Performance Curves"**[1]			LSb		VRnB:VRnA = 00, Gx = 0, V_{REF} = V_{DD} = 2.7-5.5V, no load

Note 1: This parameter is ensured by characterization.
7: INL and DNL are measured at V_{OUT} with V_{RL} = V_{DD} (VRnB:VRnA = 00).
10: Code range is dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, 100 to 4000.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended).
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
-3 dB Bandwidth (see **B.16 "-3 dB Bandwidth"**)	BW	—	86.5	—	kHz	V_{REF} = 2.048V ±0.1V, VRnB:VRnA = 10, Gx = 0
		—	67.7	—	kHz	V_{REF} = 2.048V ±0.1V, VRnB:VRnA = 10, Gx = 1
Output Amplifier						
Minimum Output Voltage	$V_{OUT(MIN)}$	—	0.01	—	V	1.8V ≤ V_{DD} < 5.5V, output amplifier's minimum drive
Maximum Output Voltage	$V_{OUT(MAX)}$	—	V_{DD} – 0.016	—	V	1.8V ≤ V_{DD} < 5.5V, output amplifier's maximum drive
Phase Margin	PM	—	58	—	°C	C_L = 400 pF, R_L = ∞
Slew Rate[9]	SR	—	0.44	—	V/µs	R_L = 5 kΩ
Short-Circuit Current	I_{SC}	3	9	22	mA	Short to V_{SS}, DAC Code = Full Scale
		3	9	22	mA	Short to V_{DD}, DAC Code = 000h
Internal Band Gap						
Band Gap Voltage	V_{BG}	1.18	1.22	1.26	V	
Band Gap Voltage Temperature Coefficient	V_{BGTC}	—	15	—	ppm/°C	
Operating Range	V_{DD}	2.0	—	5.5	V	V_{REF} pin voltage stable
		2.2	—	5.5	V	V_{OUT} output linear
External Reference (V_{REF})						
Input Range[1]	V_{REF}	V_{SS}	—	V_{DD} – 0.04	V	VRnB:VRnA = 11 (Buffered mode)
		V_{SS}	—	V_{DD}	V	VRnB:VRnA = 10 (Unbuffered mode)
Input Capacitance	C_{REF}	—	1	—	pF	VRnB:VRnA = 10 (Unbuffered mode)
Total Harmonic Distortion[1]	THD	—	-64	—	dB	V_{REF} = 2.048V ±0.1V, VRnB:VRnA = 10, Gx = 0, Frequency = 1 kHz
Dynamic Performance						
Major Code Transition Glitch (see **B.14 "Major Code Transition Glitch"**)	—	—	45	—	nV-s	1 LSb change around major carry (7FFh to 800h)
Digital Feedthrough (see **B.15 "Digital Feedthrough"**)	—	—	<10	—	nV-s	

Note 1: This parameter is ensured by design.
9: Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in a 12-bit device.)

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended).
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Digital Inputs/Outputs ($\overline{CS}$, SCK, SDI, SDO, $\overline{LAT0}$/HVC, $\overline{LAT1}$)						
Schmitt Trigger High Input Threshold	V_{IH}	0.45 V_{DD}	—	—	V	2.7V ≤ V_{DD} ≤ 5.5V
		0.5 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 2.7V
Schmitt Trigger Low Input Threshold	V_{IL}	—	—	0.2 V_{DD}	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.1 V_{DD}	—	V	
Output Low Voltage	V_{OL}	V_{SS}	—	0.3 V_{DD}	V	I_{OL} = 5 mA, V_{DD} = 5.5V
		V_{SS}	—	0.3 V_{DD}	V	I_{OL} = 1 mA, V_{DD} = 1.8V
Output High Voltage	V_{OH}	0.7 V_{DD}	—	V_{DD}	V	I_{OH} = -2.5 mA, V_{DD} = 5.5V
		0.7 V_{DD}	—	V_{DD}	V	I_{OH} = -1 mA, V_{DD} = 1.8V
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{IN} = V_{DD} and V_{IN} = V_{SS}
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	f_C = 20 MHz

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended).
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +2.048V to V_{DD}, V_{SS} = 0V, Gx = 0, R_L = 5 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
RAM Value							
Value Range	N	0h	—	FFh	Hex	8-bit	
		0h	—	3FFh	Hex	10-bit	
		0h	—	FFFh	Hex	12-bit	
DAC Register POR/BOR Value	N	See Table 4-2			Hex	8-bit	
		See Table 4-2			Hex	10-bit	
		See Table 4-2			Hex	12-bit	
PDCON Initial Factory Setting	N	See Table 4-2			Hex		
EEPROM							
Endurance	EN_{EE}	—	1M	—	Cycles	**Notes 1, 2**	
Data Retention	DR_{EE}	—	200	—	Years	At +25°C(1,2)	
EEPROM Range	N	0h	—	FFh	Hex	8-bit	DACn register(s)
		0h	—	3FFh	Hex	10-bit	DACn register(s)
		0h	—	FFFh	Hex	12-bit	DACn register(s)
Initial Factory Setting	N	See Table 4-2					
EEPROM Programming Write Cycle Time	t_{WC}	—	11	16	ms	V_{DD} = +1.8V to 5.5V	
Power Requirements							
Power Supply Sensitivity (**B.17 "Power Supply Sensitivity (PSS)"**)	PSS	—	0.002	0.005	%/%	8-bit	Code = 7Fh
		—	0.002	0.005	%/%	10-bit	Code = 1FFh
		—	0.002	0.005	%/%	12-bit	Code = 7FFh

Note 1: This parameter is ensured by design.
2: This parameter is ensured by characterization.

DC Notes:

1. This parameter is ensured by design.
2. This parameter is ensured by characterization.
3. POR/BOR voltage trip point is not slope-dependent. Hysteresis is implemented with time delay.
4. Supply current is independent of current through the resistor ladder in mode VRnB:VRnA = `10`.
5. The PDnB:PDnA bits = `01`, `10` and `11` configurations should have the same current.
6. Resistance is defined as the resistance between the V_{REF} pin (mode VRnB:VRnA = `10`) to V_{SS} pin. For octal-channel devices (MCP48FXBX8), this is the effective resistance of each resistor ladder. The resistance measurement is one of the two resistor ladders measured in parallel.
7. INL and DNL are measured at V_{OUT} with $V_{RL} = V_{DD}$ (VRnB:VRnA = `00`).
8. This gain error does not include an offset error.
9. Within 1/2 LSb of the final value when the code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in a 12-bit device.)
10. Code range is dependent on resolution: 8-bit, codes 6 to 250; 10-bit, codes 25 to 1000; 12-bit, codes 100 to 4000.
11. Variation of one output voltage to mean output voltage.

1.1 Timing Waveforms and Requirements

1.1.1 WIPER SETTLING TIME

FIGURE 1-1: *V_{OUT} Settling Time Waveforms.*

TABLE 1-1: WIPER SETTLING TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified)**: Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended). All parameters apply across the specified operating ranges unless noted. V_{DD} = +1.8V to 5.5V, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
V_{OUT} Settling Time; ±0.5 LSb Error Band, C_L = 100 pF (see **B.13 "Settling Time"**)	t_S	—	7.8	—	µs	12-bit	Code = 400h → C00h; C00h → 400h[(1)]

Note 1: Within 1/2 LSb of the final value when the code changes from 1/4 to 3/4 of FSR.

1.1.2 LATCH PIN ($\overline{LAT}$) TIMING

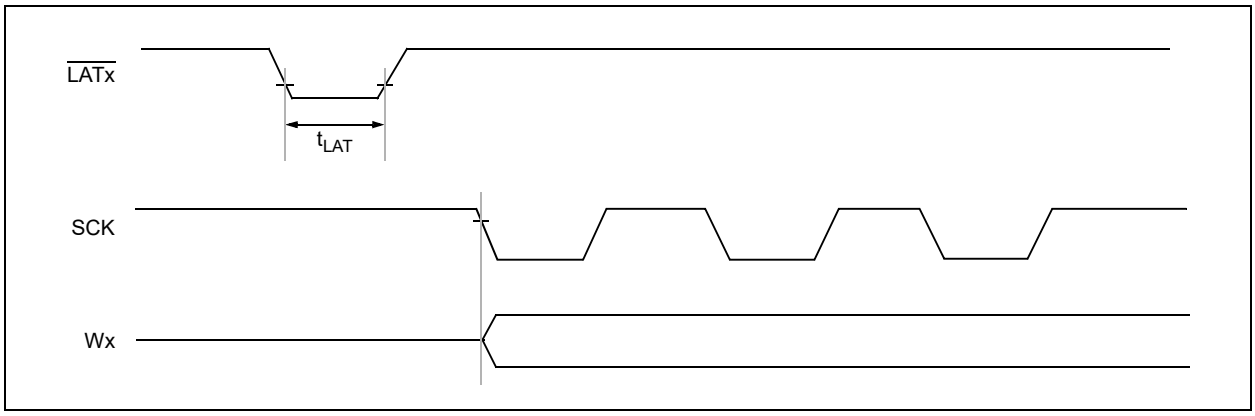


FIGURE 1-2: *$\overline{LAT}$ Pin Waveforms.*

TABLE 1-2: $\overline{LAT}$ PIN TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended). All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
$\overline{LATx}$ Pin Pulse Width	t_{LAT}	20	—	—	ns	

1.1.3 RESET AND POWER-DOWN TIMING

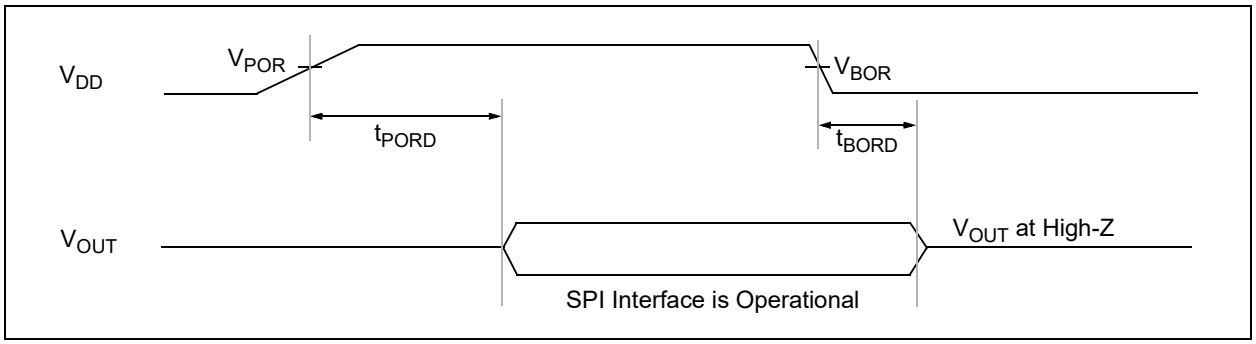


FIGURE 1-3: *Power-on and Brown-out Reset Waveforms.*

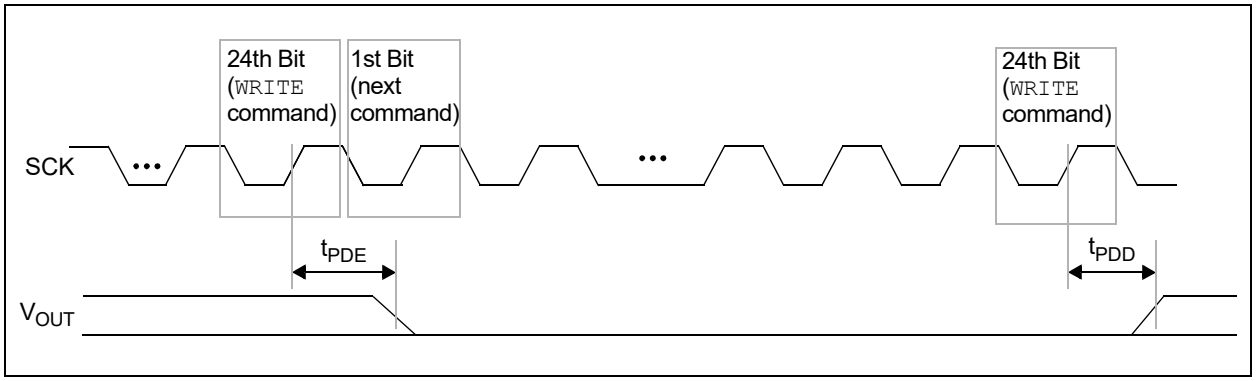


FIGURE 1-4: *SPI Power-Down Command Waveforms.*

TABLE 1-3: RESET AND POWER-DOWN TIMING

Timing Characteristics		**Standard Operating Conditions (unless otherwise specified):** Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended. Unless otherwise noted, all parameters apply across these specified operating ranges: V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, R_L = 5 kΩ from V_{OUT} to V_{SS}, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.				
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power-on Reset Delay	t_{PORD}	—	60	—	µs	V_{DD} rising, V_{DD} > V_{POR}
Brown-out Reset Delay	t_{BORD}	—	45	—	µs	V_{DD} transitions from $V_{DD(MIN)}$ → > V_{POR}, V_{OUT} driven to V_{OUT} disabled
Power-Down DAC Output Disable Time Delay	T_{PDE}	—	10.5	—	µs	PDnB:PDnA = 00 → 11, 10 or 01 started from the falling edge of the SCK at the end of the 24th clock cycle, V_{OUT} = V_{OUT} – 10 mV, V_{OUT} not connected
Power-Down DAC Output Enable Time Delay	T_{PDD}	—	1	—	µs	PDnB:PDnA = 11, 10 or 01 → 00 started from the falling edge of the SCK at the end of the 24th clock cycle, Volatile DAC Register = FFh, V_{OUT} = 10 mV, V_{OUT} not connected

1.2 SPI Mode Timing Waveforms and Requirements

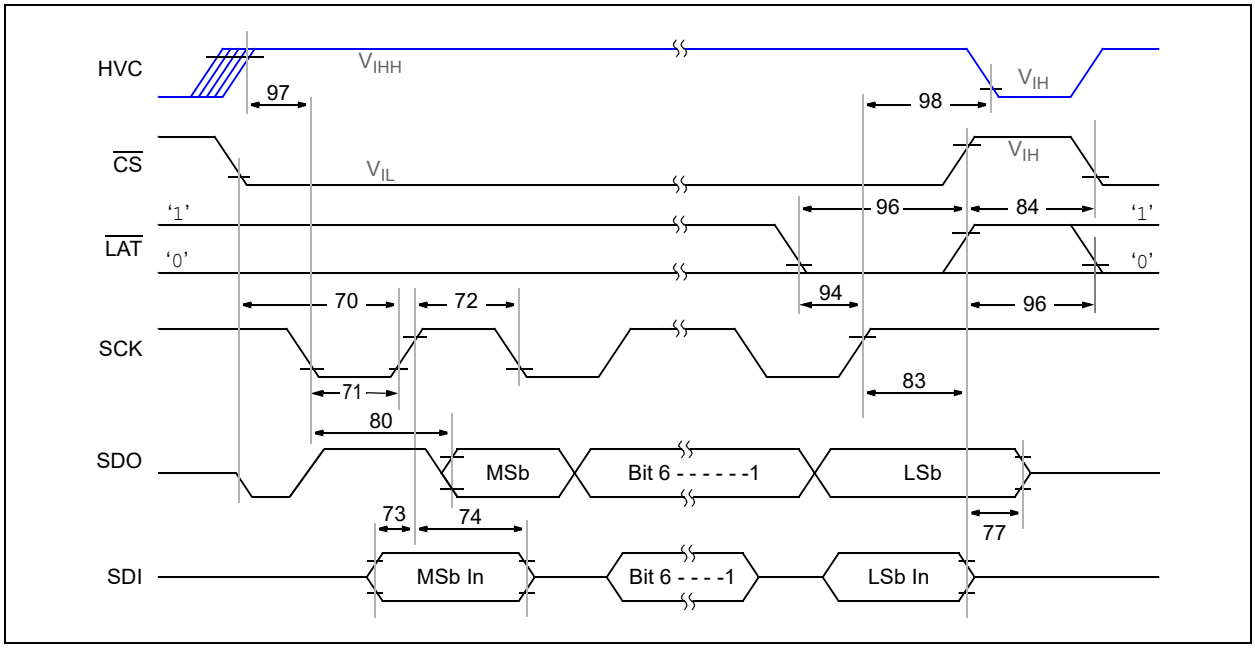


FIGURE 1-5: *SPI Timing Waveforms – Mode 1,1.*

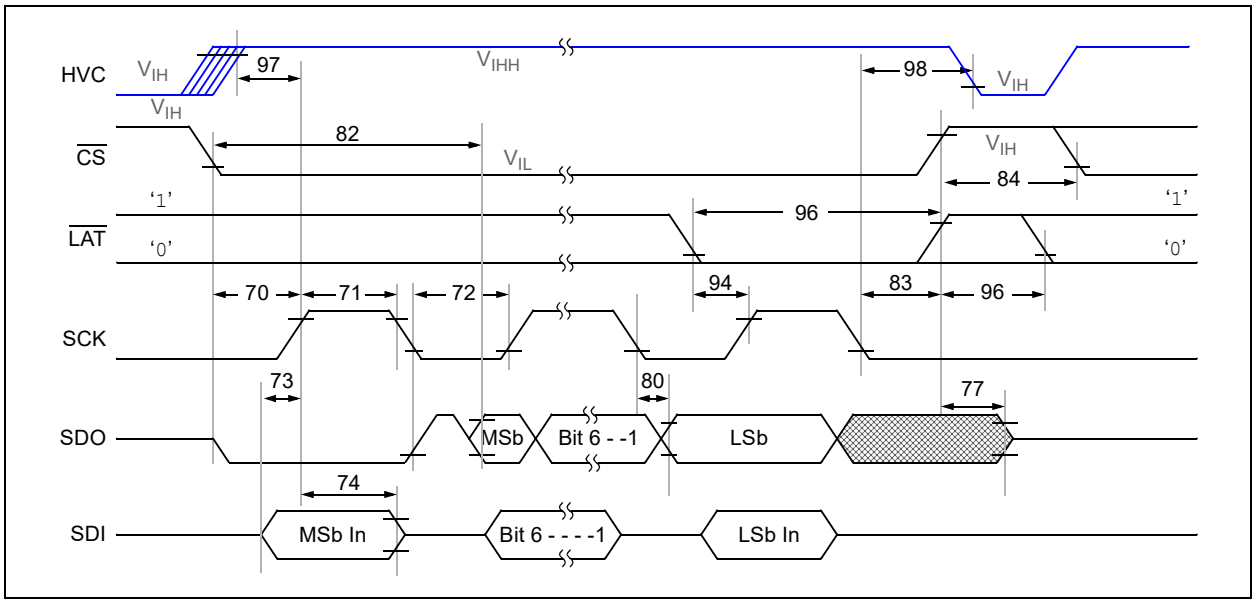


FIGURE 1-6: *SPI Timing (Mode 0,0) Waveforms.*

TABLE 1-4: SPI REQUIREMENTS (MODE 1,1)

#	Characteristic	Symbol	Min.	Max.	Units	Conditions
	SCK Input Frequency	F_{SCK}	—	10	MHz	V_{DD} = 2.7V to 5.5V (READ command)
			—	20	MHz	V_{DD} = 2.7V to 5.5V (all other commands)
70	$\overline{CS}$ Active (V_{IL}) to Command's 1st SCK ↑ Input	$T_{CSA2SCH}$	60	—	ns	
71	SCK Input High Time	T_{SCH}	20	—	ns	V_{DD} = 2.7V to 5.5V
			400	—	ns	V_{DD} = 1.8V to 2.7V
72	SCK Input Low Time	T_{SCL}	20	—	ns	V_{DD} = 2.7V to 5.5V
			400	—	ns	V_{DD} = 1.8V to 2.7V
73	Setup Time of SDI Input to SCK ↑ Edge	$T_{DIV2SCH}$	10	—	ns	
74	Hold Time of SDI Input from SCK ↑ Edge	$T_{SCH2DIL}$	20	—	ns	
77	$\overline{CS}$ Inactive (V_{IH}) to SDO Output High-Impedance	$T_{CSH2DOZ}$	—	50	ns	**Note 1**
80	SDO Data Output Valid after SCK ↓ Edge	$T_{SCL2DOV}$	—	45	ns	V_{DD} = 2.7V to 5.5V
			—	170	ns	V_{DD} = 1.8V to 2.7V
83	$\overline{CS}$ Inactive (V_{IH}) after SCK ↑ Edge	$T_{SCH2CSL}$	100	—	ns	V_{DD} = 2.7V to 5.5V
			1		µs	V_{DD} = 1.8V to 2.7V
84	$\overline{CS}$ High Time (V_{IH})	T_{CSH}	50	—	ns	
94	$\overline{LAT}$ ↓ to SCK ↑ (write data 24th bit) Setup Time	T_{LATSU}	20	—	ns	Write data transferred(3)
96	$\overline{LAT}$ High or Low Time	T_{LAT}	20	—	ns	
97	HVC ↑ to SCK ↓ (1st data bit) (HVC setup time)	T_{HVCSU}	0	—	ns	High-Voltage Commands(1)
98	SCK ↑ (last bit of command, 8th or 24th bit) to HVC ↓ (HVC hold time)	T_{HVCHD}	25	—	ns	High-Voltage Commands(1)

Note 1: This parameter is ensured by design.

3: Within 1/2 LSb of the final value when the code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device.) The transition of the $\overline{LAT}$ signal must occur 10 ns before the rising edge of the 24th SCK signal (Spec 94) or the current register data value may not be transferred to the output latch (V_{OUT}) before the register is overwritten with the new value.

TABLE 1-5: SPI REQUIREMENTS (MODE 0,0)

#	Characteristic	Sym.	Min.	Max.	Units	Conditions
	SCK Input Frequency	F_{SCK}	—	10	MHz	V_{DD} = 2.7V to 5.5V (READ command)
			—	20	MHz	V_{DD} = 2.7V to 5.5V (all other commands)
70	$\overline{CS}$ Active (V_{IL}) to SCK ↑ Input	$T_{CSA2SCH}$	60	—	ns	
71	SCK Input High Time	T_{SCH}	20	—	ns	V_{DD} = 2.7V to 5.5V
			400	—	ns	V_{DD} = 1.8V to 2.7V
72	SCK Input Low Time	T_{SCL}	20	—	ns	V_{DD} = 2.7V to 5.5V
			400	—	ns	V_{DD} = 1.8V to 2.7V
73	Setup Time of SDI Input to SCK ↑ Edge	$T_{DIV2SCH}$	10	—	ns	
74	Hold Time of SDI Input from SCK ↑ Edge	$T_{SCH2DIL}$	20	—	ns	
77	$\overline{CS}$ Inactive (V_{IH}) to SDO Output High-Impedance	$T_{CSH2DOZ}$	—	50	ns	**Note 1**
80	SDO Data Output Valid after SCK ↓ Edge	$T_{SCL2DOV}$	—	45	ns	V_{DD} = 2.7V to 5.5V
			—	170	ns	V_{DD} = 1.8V to 2.7V
82	SDO Data Output Valid after $\overline{CS}$ Active (V_{IL})	$T_{SSL2DOV}$	—	70	ns	
83	$\overline{CS}$ Inactive (V_{IH}) after SCK ↓ Edge	$T_{SCH2CSL}$	100	—	ns	V_{DD} = 2.7V to 5.5V
			1		µs	V_{DD} = 1.8V to 2.7V
84	$\overline{CS}$ High Time (V_{IH})	T_{CSH}	50	—	ns	
94	$\overline{LAT}$ ↓ to SCK ↑ (write data 24th bit) Setup Time	T_{LATSU}	10	—	ns	Write data transferred(3)
96	$\overline{LAT}$ High or Low Time	T_{LAT}	50	—	ns	
97	HVC ↑ to SCK ↑ (1st data bit) (HVC setup time)	T_{HVCSU}	0	—	ns	High-Voltage Commands(1)
98	SCK ↓ (last bit of command, 8th or 24th bit) to HVC ↓ (HVC hold time)	T_{HVCHD}	25	—	ns	High-Voltage Commands(1)

Note 1: This parameter is ensured by design.

3: Within 1/2 LSb of the final value when the code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device.) The transition of the $\overline{LAT}$ signal must occur 10 ns before the rising edge of the 24th SCK signal (Spec 94) or the current register data value may not be transferred to the output latch (V_{OUT}) before the register is overwritten with the new value.

Timing Table Notes:

1. This parameter is ensured by design.
2. This parameter is ensured by characterization.
3. Within 1/2 LSb of the final value when the code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in 12-bit device).The transition of the $\overline{LAT}$ signal must occur 10 ns before the rising edge of the 24th SCK signal (Spec 94) or the current register data value may not be transferred to the output latch (V_{OUT}) before the register is overwritten with the new value.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 20-Lead TSSOP	θ_{JA}	—	90	—	°C/W	
Thermal Resistance, 20-Lead VQFN (5x5 mm, P8X)	θ_{JA}	—	36.1	—	°C/W	

Note 1: Operation in this range must not cause T_J to exceed the Maximum Junction Temperature of +150°C.

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

2.1 Electrical Data

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

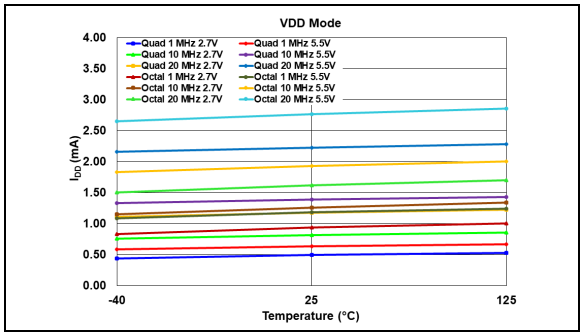


FIGURE 2-1: *Average Device Supply Current vs. F_{SCK} Frequency, Voltage and Temperature – Active Interface, VRnB:VRnA = 00, (V_{DD} Mode).*

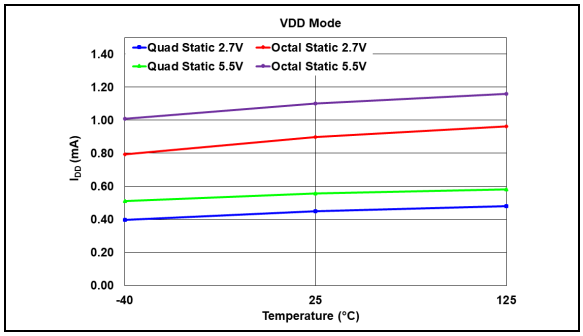


FIGURE 2-4: *Average Device Supply Current – Inactive Interface (SCK = V_{IH} or V_{IL}) vs. Voltage and Temperature, VRnB:VRnA = 00 (V_{DD} Mode).*

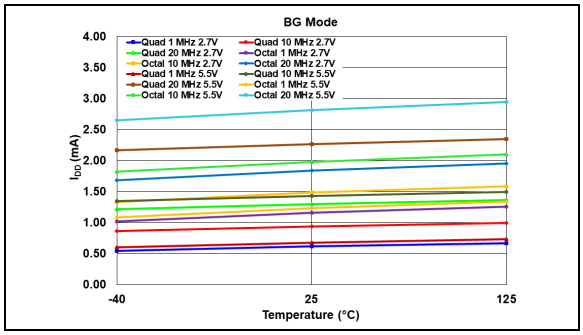


FIGURE 2-2: *Average Device Supply Current vs. F_{SCK} Frequency, Voltage and Temperature – Active Interface, VRnB:VRnA = 01 (Band Gap Mode).*

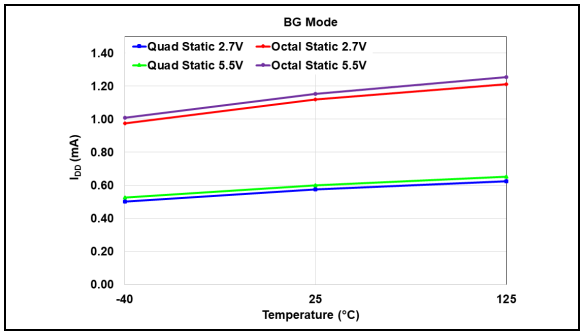


FIGURE 2-5: *Average Device Supply Current – Inactive Interface (SCK = V_{IH} or V_{IL}) vs. Voltage and Temperature, VRnB:VRnA = 01 (Band Gap Mode).*

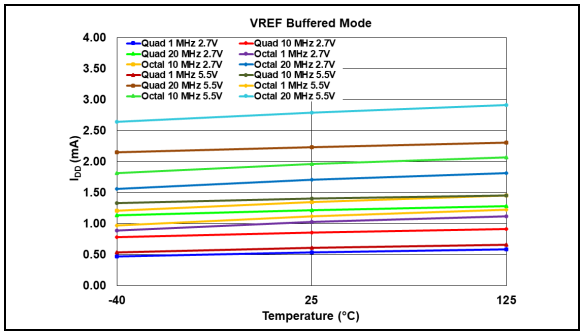


FIGURE 2-3: *Average Device Supply Current vs. F_{SCK} Frequency, Voltage and Temperature – Active Interface, VRnB:VRnA = 11 (V_{REF} Buffered Mode).*

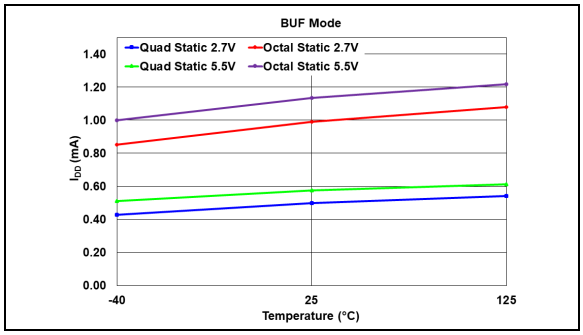


FIGURE 2-6: *Average Device Supply Current – Inactive Interface (SCK = V_{IH} or V_{IL}) vs. Voltage and Temperature, VRnB:VRnA = 11 (V_{REF} Buffered Mode).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

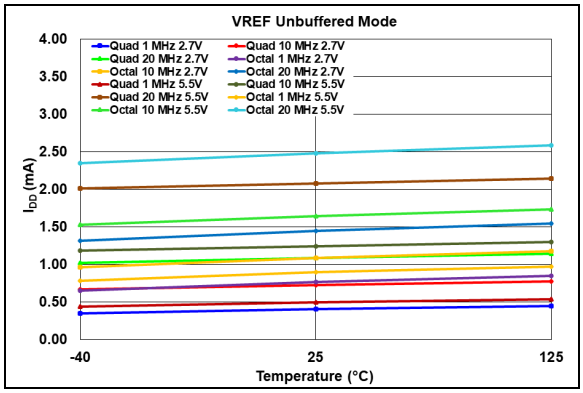


FIGURE 2-7: *Average Device Supply Current vs. F_{SCK} Frequency, Voltage and Temperature – Active Interface, VRnB:VRnA = 10 (V_{REF} Unbuffered Mode).*

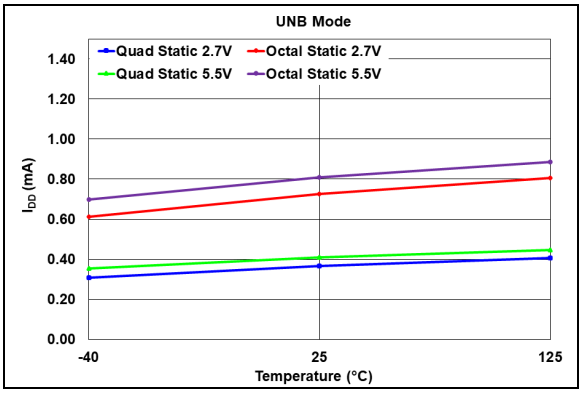


FIGURE 2-9: *Average Device Supply Current – Inactive Interface (SCK = V_{IH} or V_{IL}) vs. Voltage and Temperature, VRnB:VRnA = 10 (V_{REF} Unbuffered Mode).*

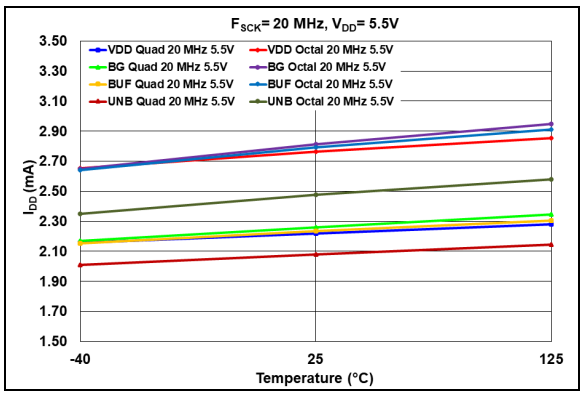


FIGURE 2-8: *Average Device Supply Active Current (I_{DDA}) (at 5.5V and F_{SCK} = 20 MHz) vs. Temperature and DAC Reference Voltage Mode.*

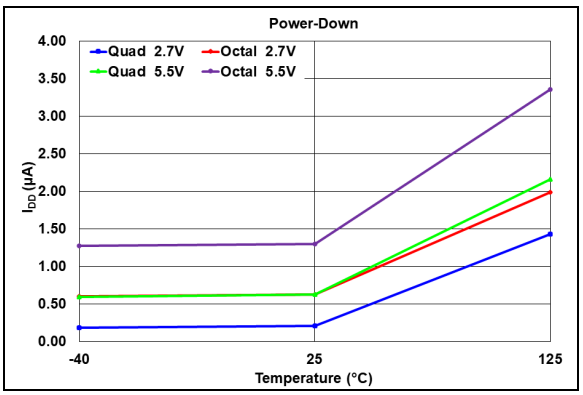


FIGURE 2-10: *Power-Down Currents.*

2.2 Linearity Data

2.2.1 TOTAL UNADJUSTED ERROR (TUE) – MCP48FXB28 (12-BIT), $V_{REF} = V_{DD}$ (VRnB:VRnA = 00), GAIN = 1x, CODE 100-4000

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V

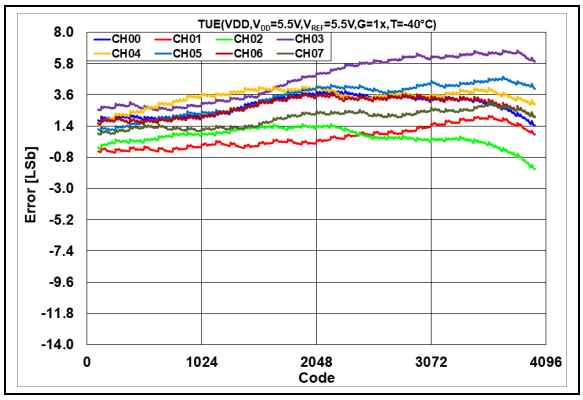


FIGURE 2-11: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

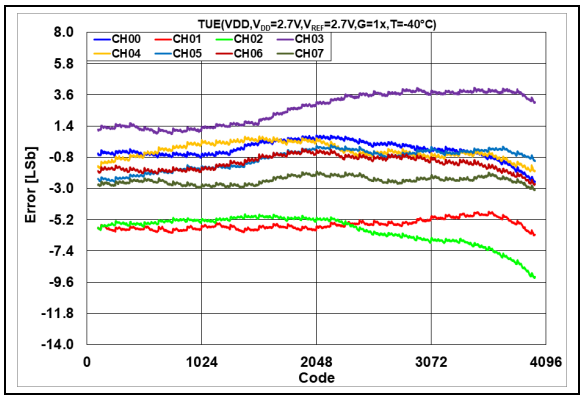


FIGURE 2-14: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

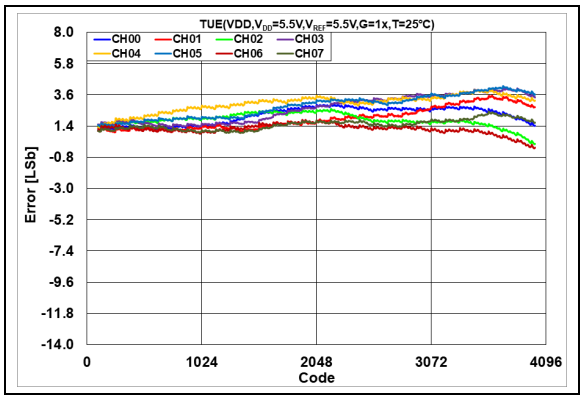


FIGURE 2-12: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

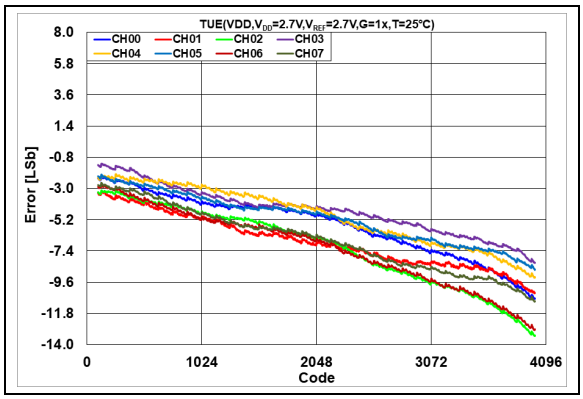


FIGURE 2-15: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

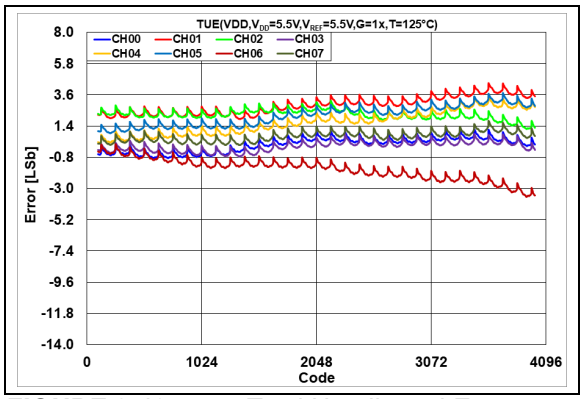


FIGURE 2-13: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

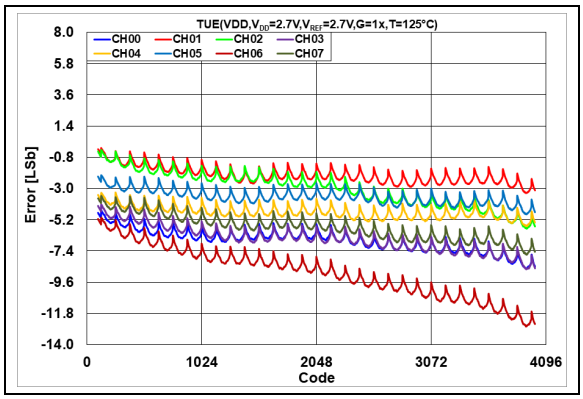


FIGURE 2-16: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.2 INTEGRAL NONLINEARITY (INL) – MCP48FXB28 (12-BIT), $V_{REF} = V_{DD}$ (VRnB:VRnA = 00), GAIN = 1x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

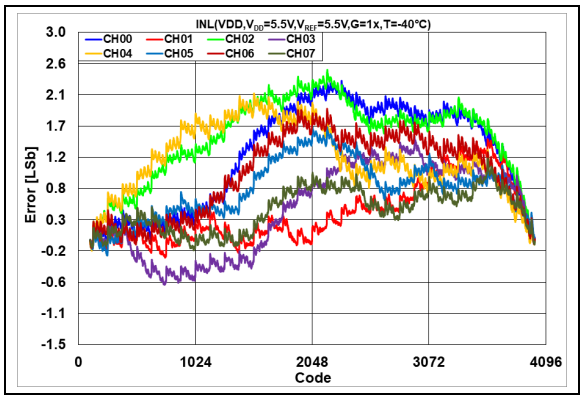


FIGURE 2-17: *INL Error vs. DAC Code, T = 40°C, V_{DD} = 5.5V.*

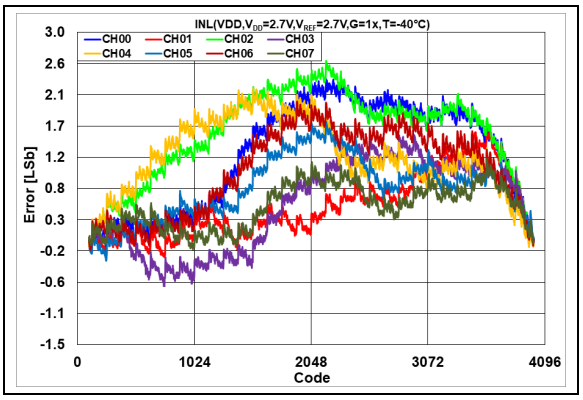


FIGURE 2-20: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

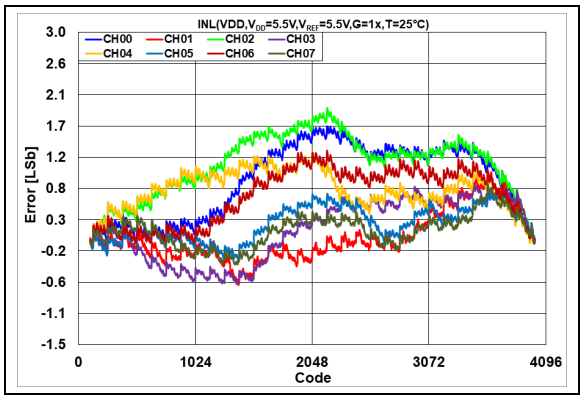


FIGURE 2-18: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

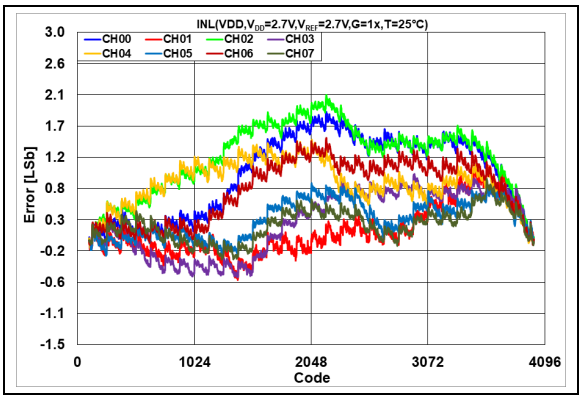


FIGURE 2-21: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

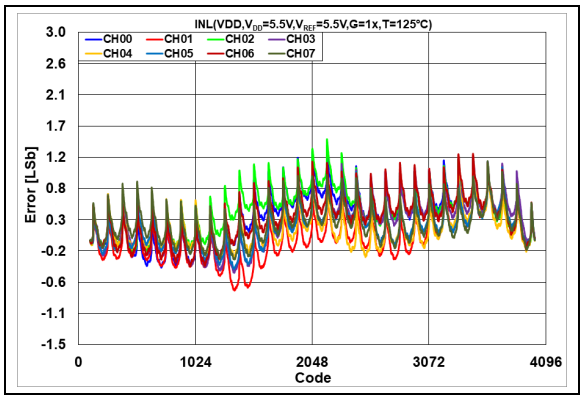


FIGURE 2-19: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

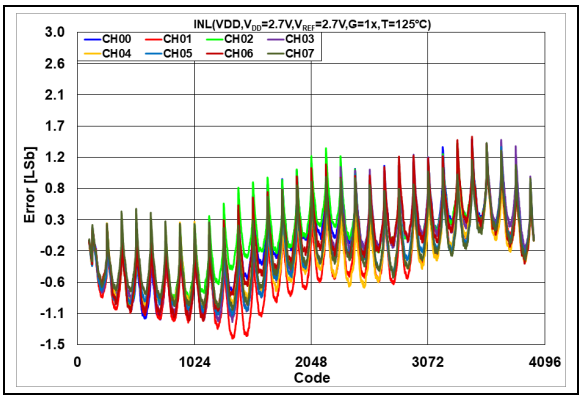


FIGURE 2-22: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.3 DIFFERENTIAL NONLINEARITY (DNL) – MCP48FXB28 (12-BIT), $V_{REF} = V_{DD}$ (VRnB:VRnA = 00), GAIN = 1x, CODE 64-4032

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

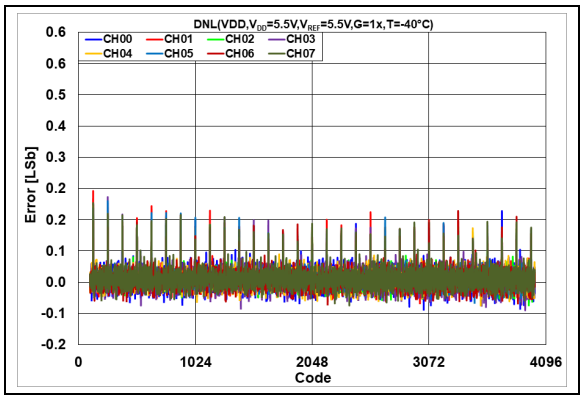


FIGURE 2-23: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

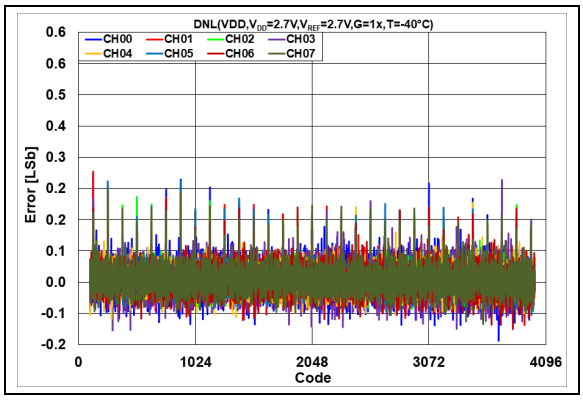


FIGURE 2-26: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

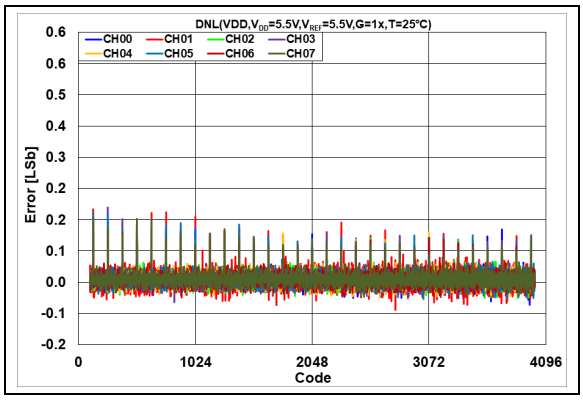


FIGURE 2-24: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

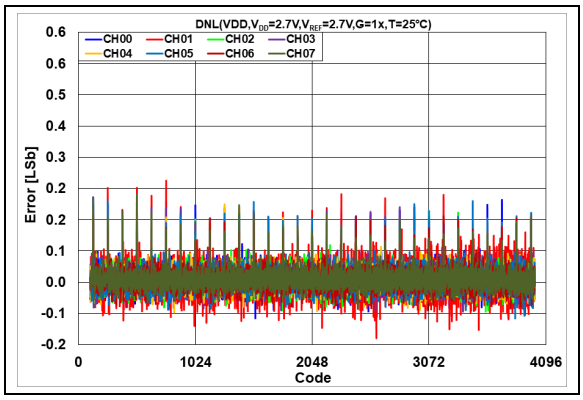


FIGURE 2-27: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

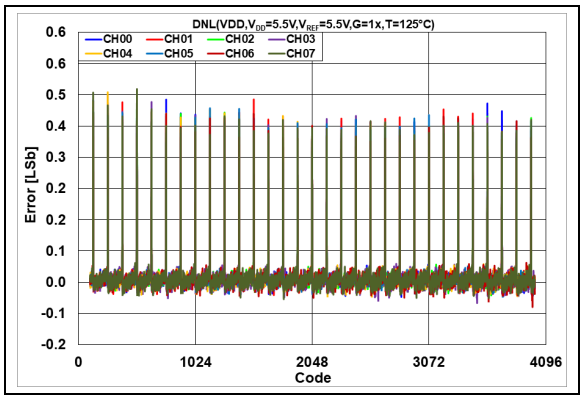


FIGURE 2-25: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

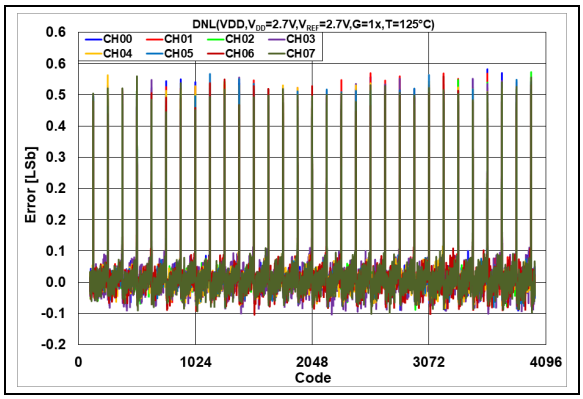


FIGURE 2-28: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.4 TOTAL UNADJUSTED ERROR (TUE) – MCP48FXB28 (12-BIT), BAND GAP MODE (VRnB:VRnA = 01), GAIN = 2x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

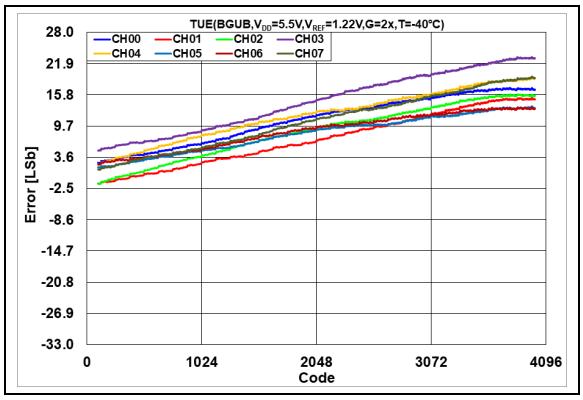


FIGURE 2-29: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

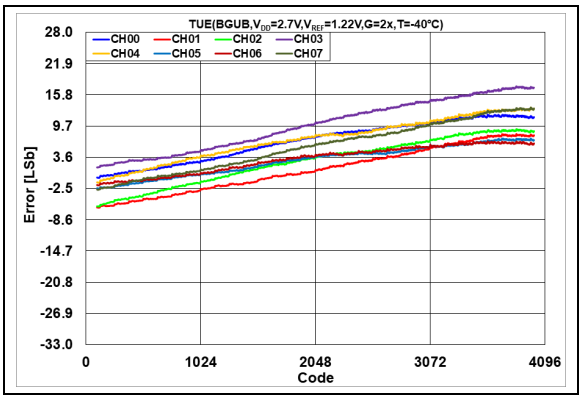


FIGURE 2-32: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

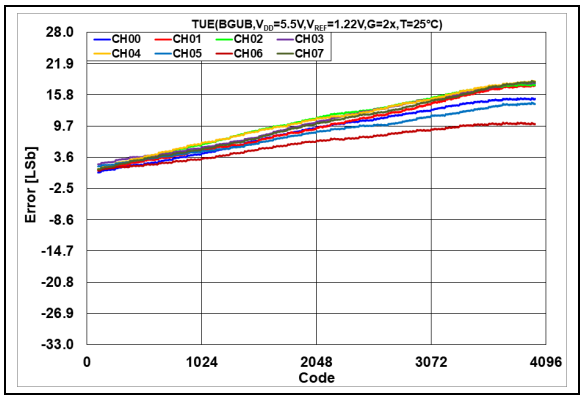


FIGURE 2-30: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

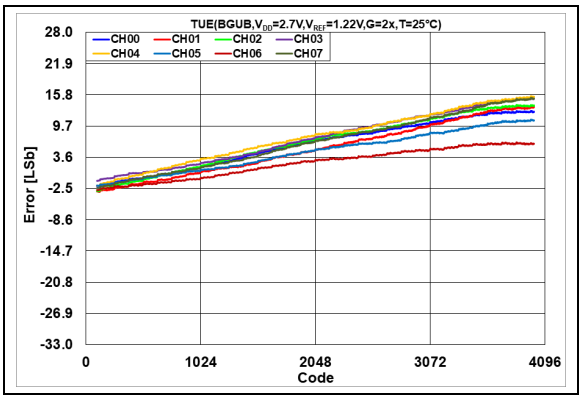


FIGURE 2-33: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

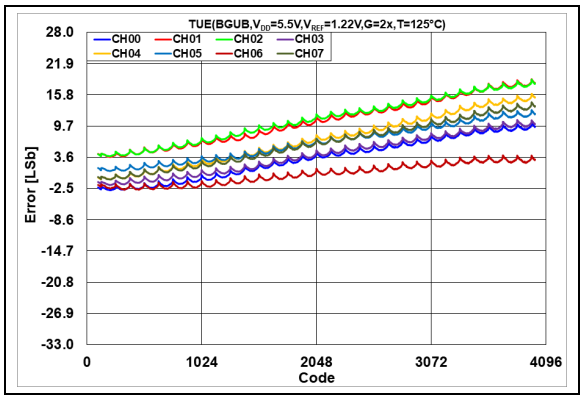


FIGURE 2-31: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

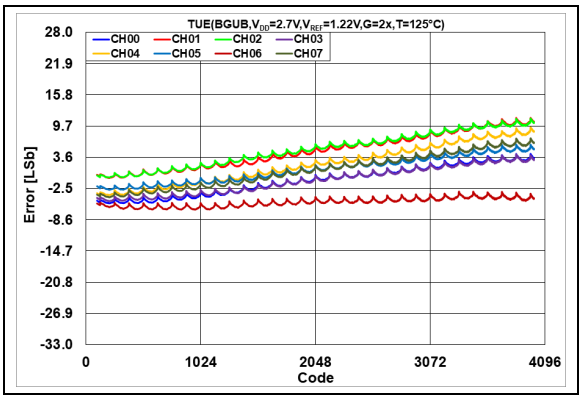


FIGURE 2-34: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.5 TOTAL UNADJUSTED ERROR (TUE) – MCP48FXB28 (12-BIT), BAND GAP MODE (VRnB:VRnA = 01), GAIN = 4x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

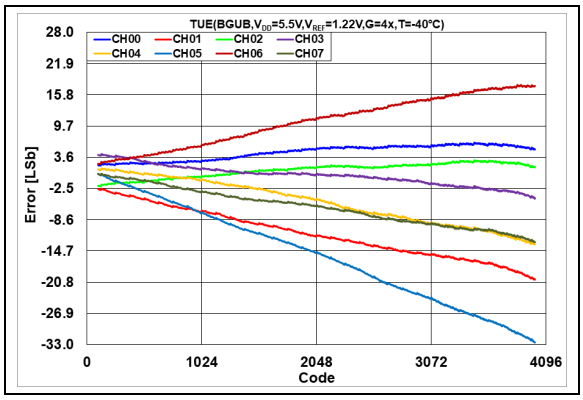


FIGURE 2-35: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

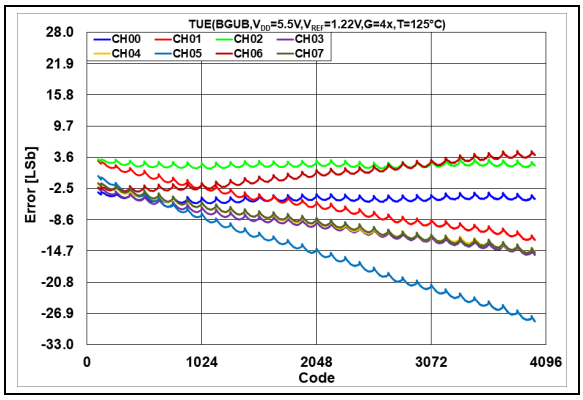


FIGURE 2-37: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

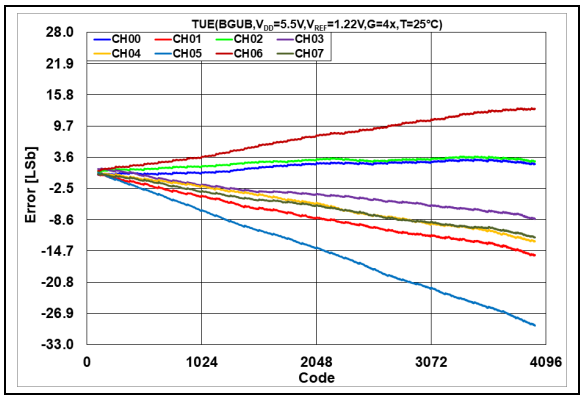


FIGURE 2-36: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

2.2.6 INTEGRAL NONLINEARITY (INL) – MCP48FXB28 (12-BIT), BAND GAP MODE (VRnB:VRnA = 01), GAIN = 2x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

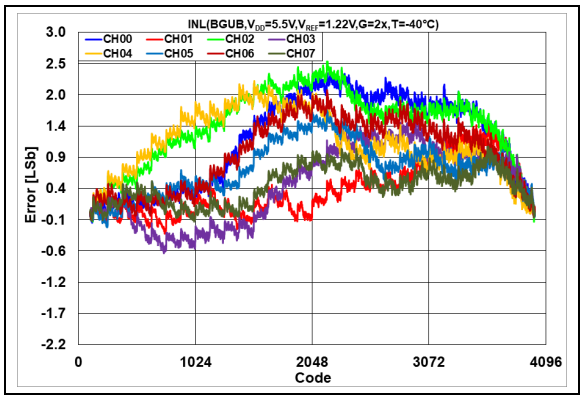


FIGURE 2-38: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

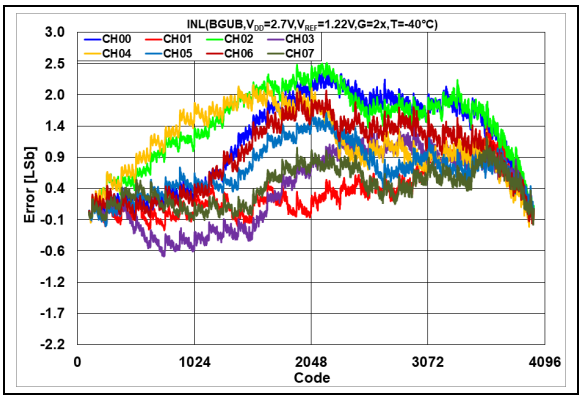


FIGURE 2-41: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

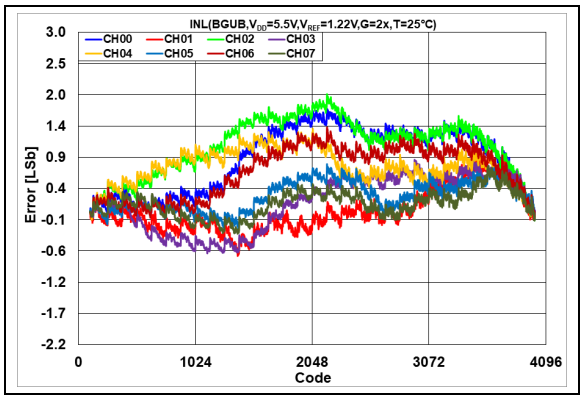


FIGURE 2-39: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

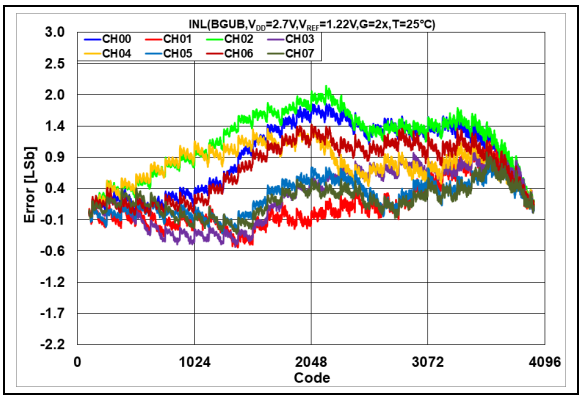


FIGURE 2-42: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

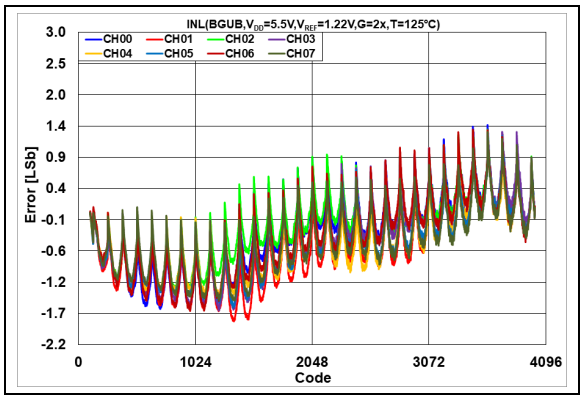


FIGURE 2-40: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

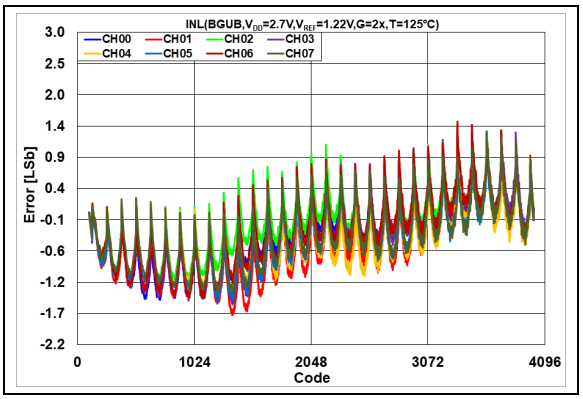


FIGURE 2-43: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.7 INTEGRAL NONLINEARITY (INL) – MCP48FXB28 (12-BIT), BAND GAP MODE (VRnB:VRnA = 01), GAIN = 4x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

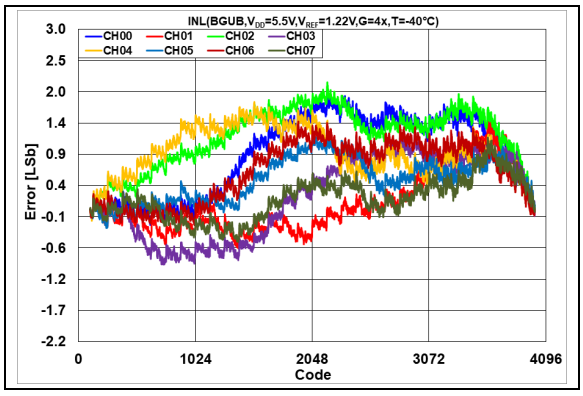


FIGURE 2-44: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

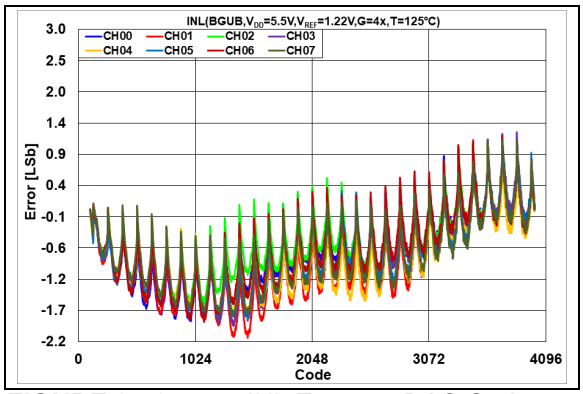


FIGURE 2-46: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

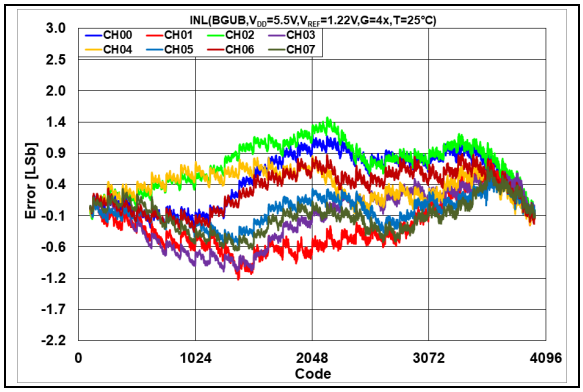


FIGURE 2-45: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

2.2.8 DIFFERENTIAL NONLINEARITY ERROR (DNL) – MCP48FXB28 (12-BIT), BAND GAP MODE (VRnB:VRnA = 01), GAIN = 2x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

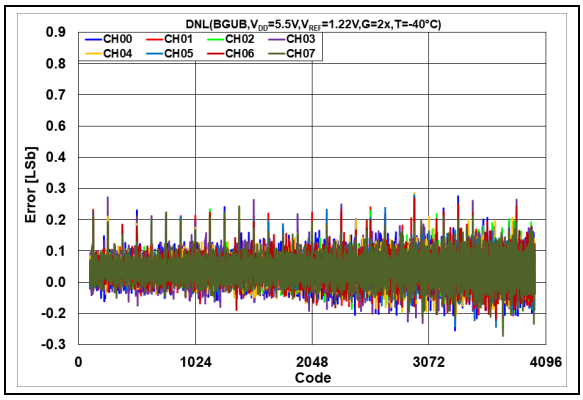


FIGURE 2-47: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

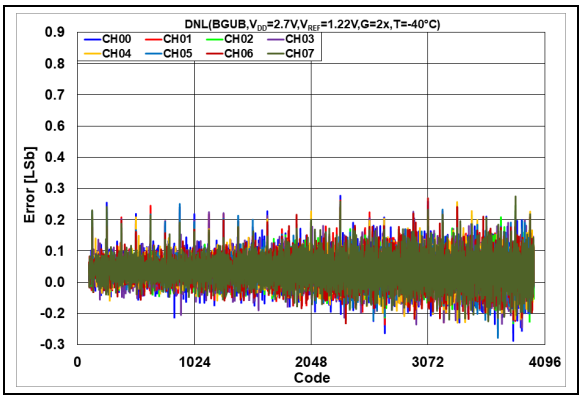


FIGURE 2-50: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

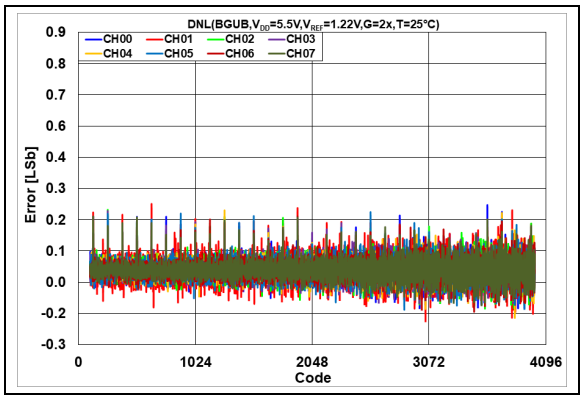


FIGURE 2-48: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

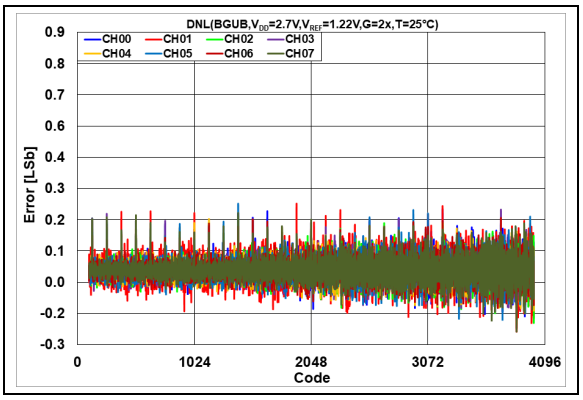


FIGURE 2-51: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

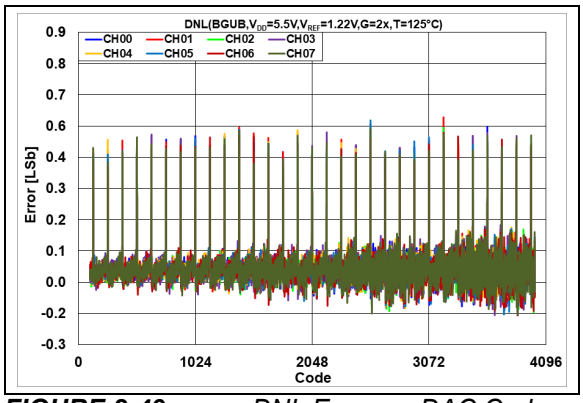


FIGURE 2-49: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

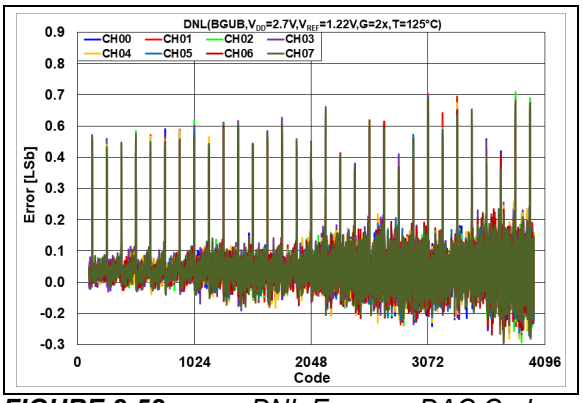


FIGURE 2-52: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.9 DIFFERENTIAL NONLINEARITY ERROR (DNL) – MCP48FXB28 (12-BIT), BAND GAP MODE (VRnB:VRnA = 01), GAIN = 4x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

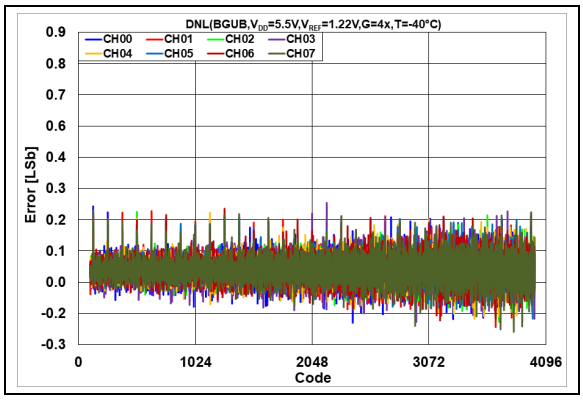


FIGURE 2-53: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

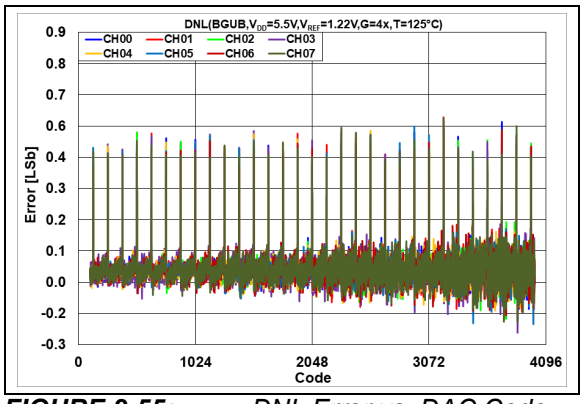


FIGURE 2-55: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

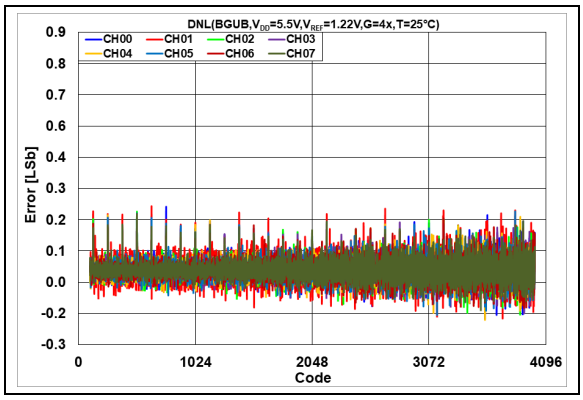


FIGURE 2-54: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

2.2.10 TOTAL UNADJUSTED ERROR (TUE) – MCP48FXB28 (12-BIT), EXTERNAL V_{REF} UNBUFFERED MODE (VRnB:VRnA = 10), V_{REF} = V_{DD}, GAIN = 1x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

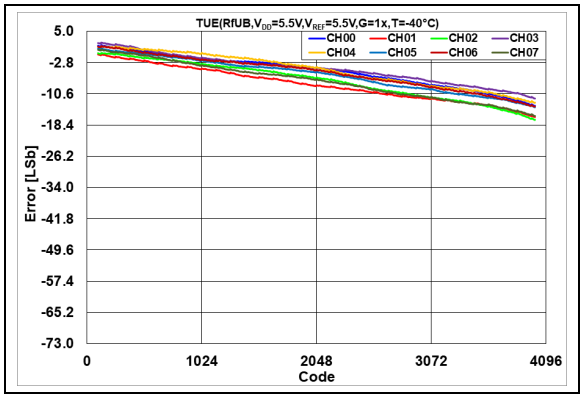


FIGURE 2-56: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

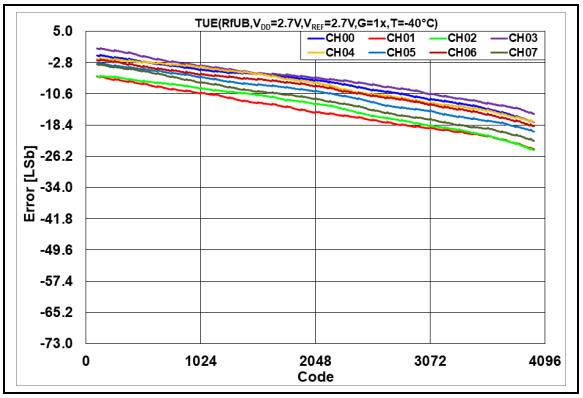


FIGURE 2-59: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

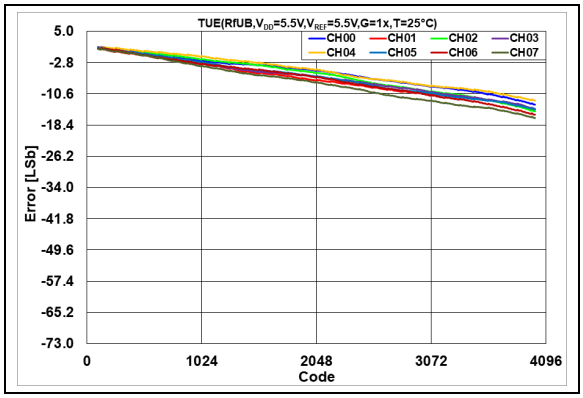


FIGURE 2-57: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C,V_{DD} = 5.5V.*

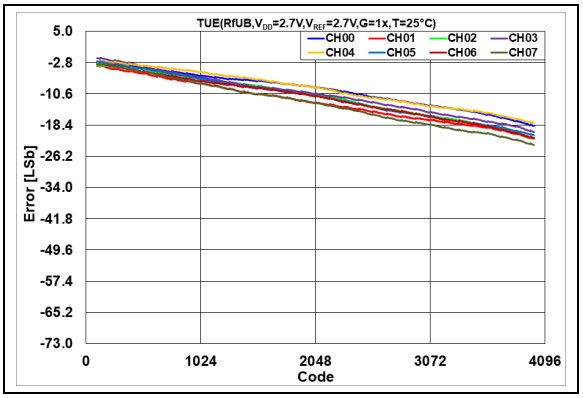


FIGURE 2-60: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

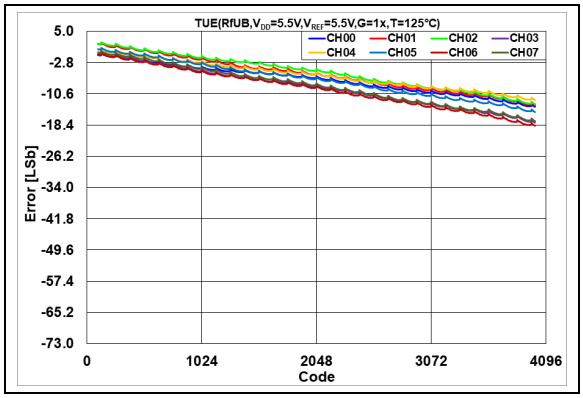


FIGURE 2-58: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

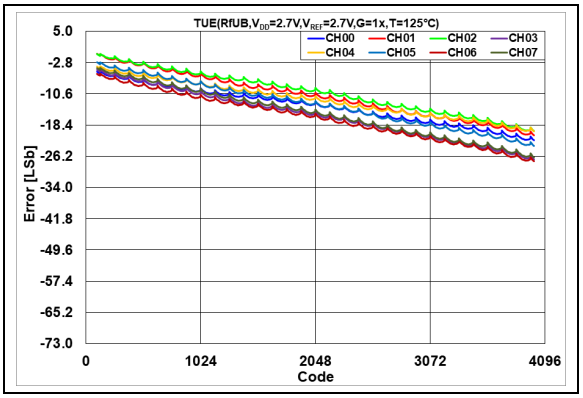


FIGURE 2-61: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.11 TOTAL UNADJUSTED ERROR (TUE) – MCP48FXB28 (12-BIT), EXTERNAL V_{REF} UNBUFFERED MODE (VRnB:VRnA = 10), $V_{REF} = V_{DD}/2$, GAIN = 2x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

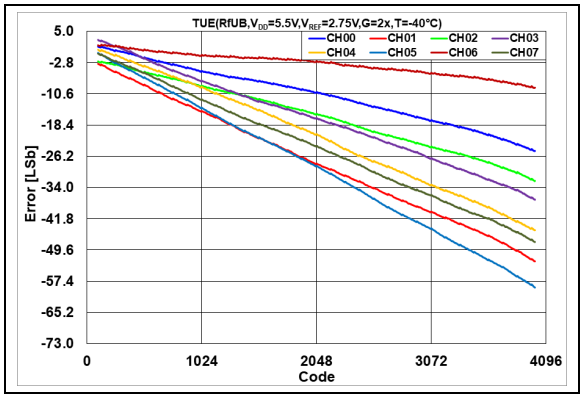


FIGURE 2-62: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

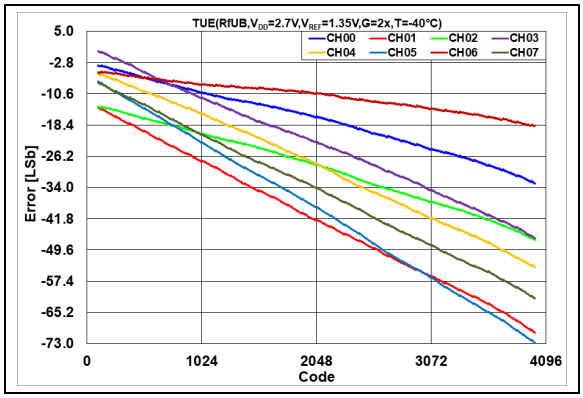


FIGURE 2-65: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

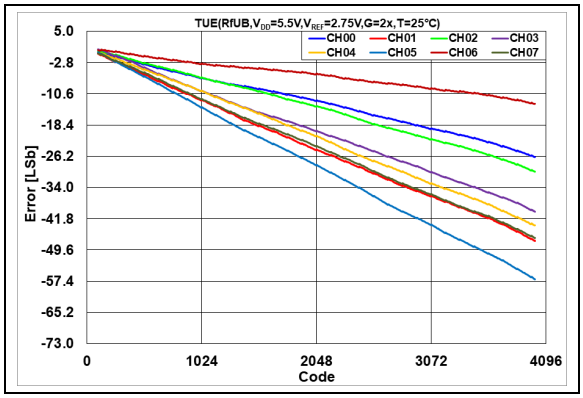


FIGURE 2-63: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C,V_{DD} = 5.5V.*

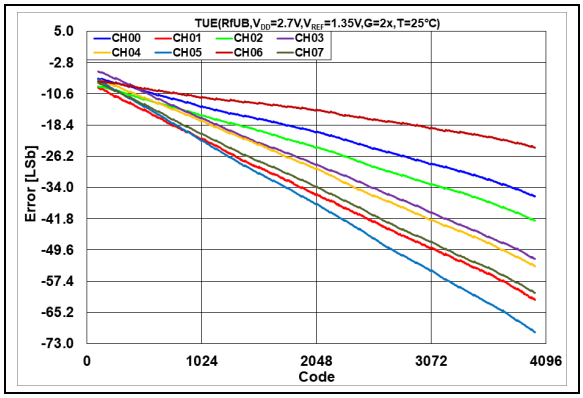


FIGURE 2-66: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

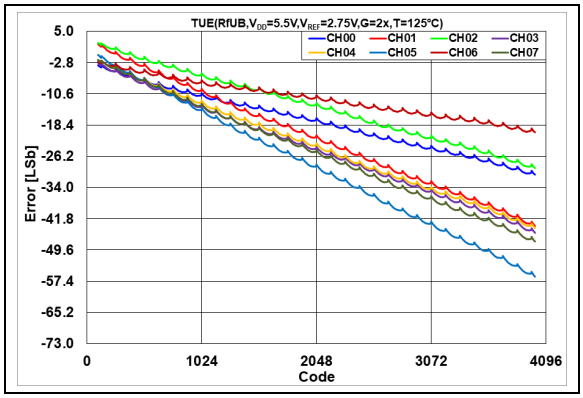


FIGURE 2-64: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

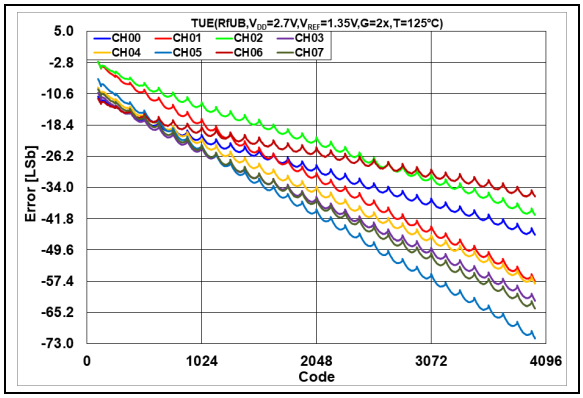


FIGURE 2-67: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.12 INTEGRAL NONLINEARITY ERROR (INL) – MCP48FXB28 (12-BIT), EXTERNAL V_{REF} MODE, UNBUFFERED (VRnB:VRnA = 10), $V_{REF} = V_{DD}$, GAIN = 1x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

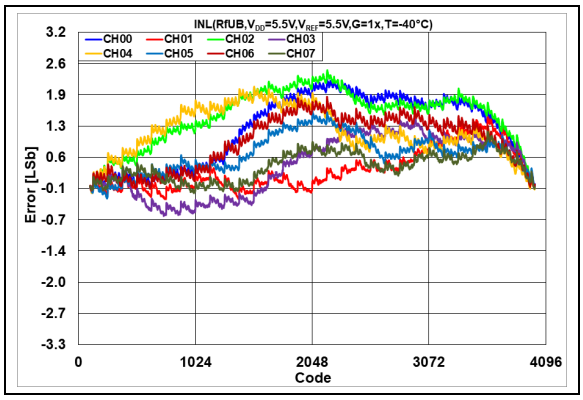


FIGURE 2-68: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

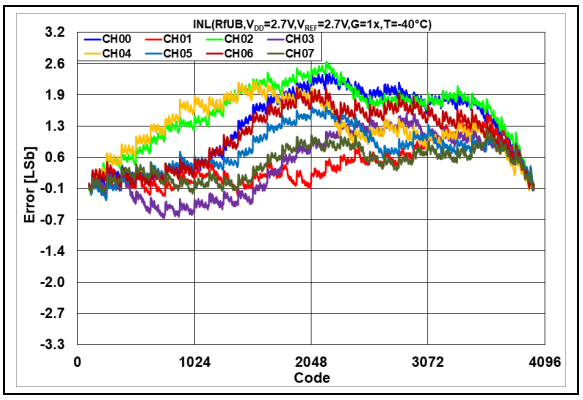


FIGURE 2-71: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

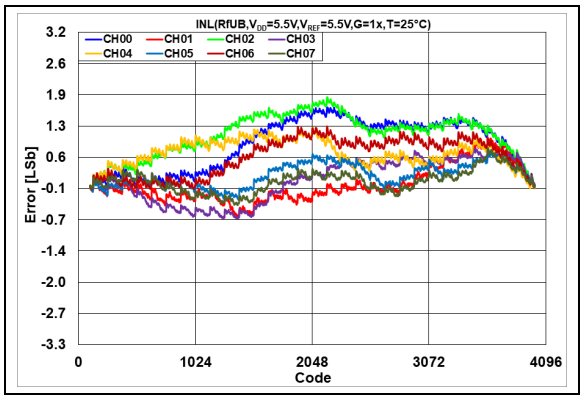


FIGURE 2-69: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

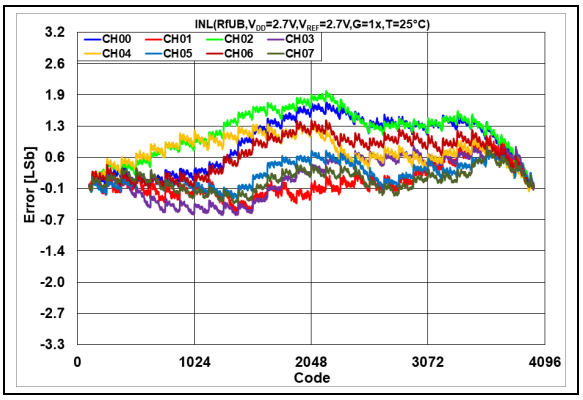


FIGURE 2-72: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

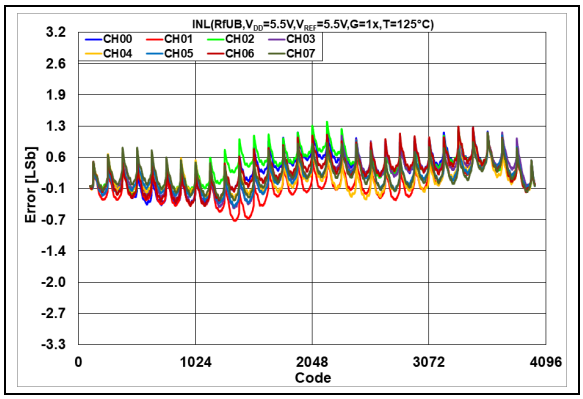


FIGURE 2-70: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

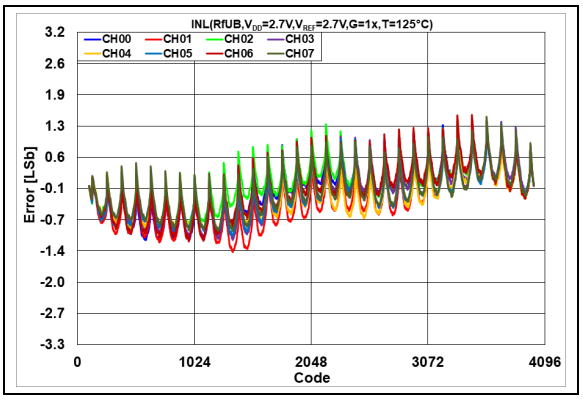


FIGURE 2-73: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.13 INTEGRAL NONLINEARITY ERROR (INL) – MCP48FXB28 (12-BIT), EXTERNAL V_{REF} MODE, UNBUFFERED (VRnB:VRnA = 10), V_{REF} = V_{DD}/2, GAIN = 2x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

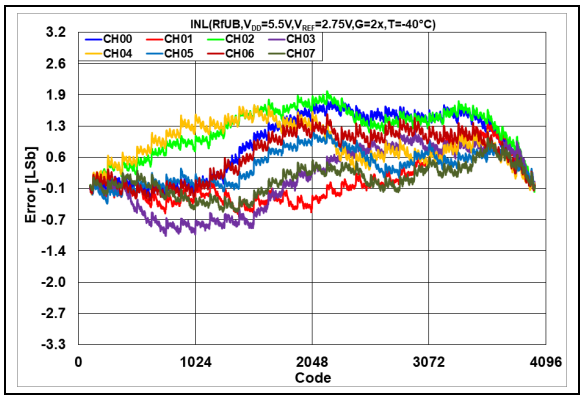


FIGURE 2-74: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

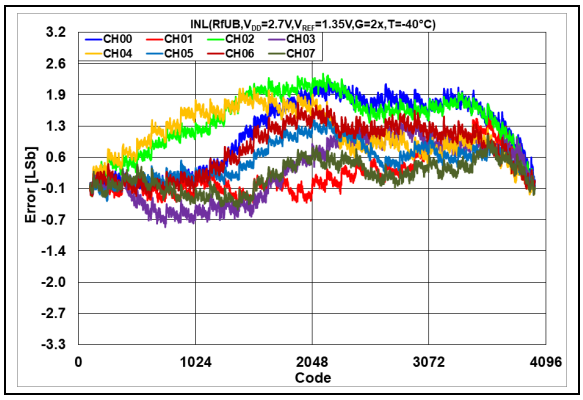


FIGURE 2-77: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

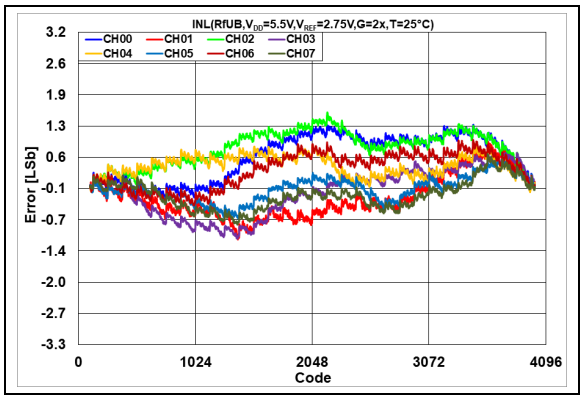


FIGURE 2-75: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

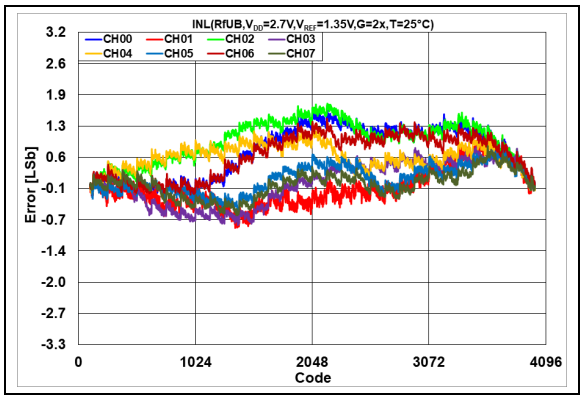


FIGURE 2-78: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

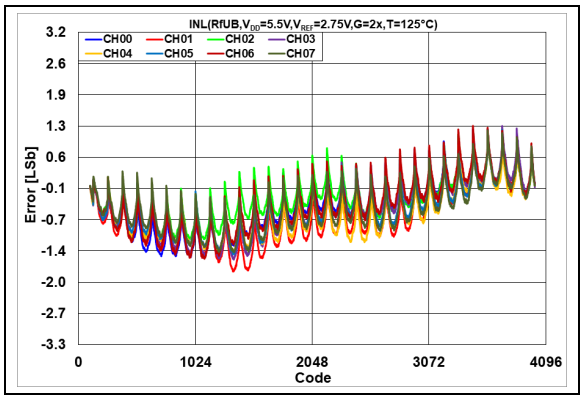


FIGURE 2-76: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

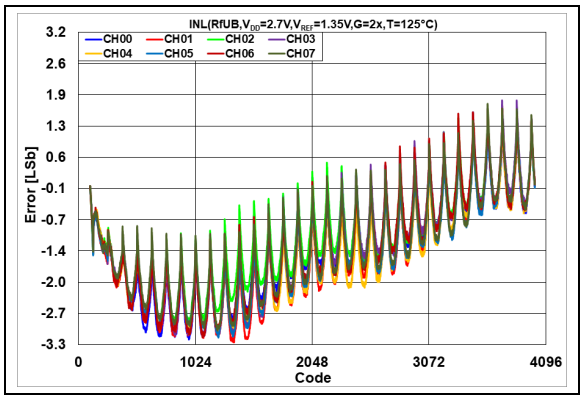


FIGURE 2-79: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.14 DIFFERENTIAL NONLINEARITY ERROR (DNL) – MCP48FXB28 (12-BIT), EXTERNAL V_{REF} MODE, UNBUFFERED (VRnB:VRnA = 10), V_{REF} = V_{DD}, GAIN = 1x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

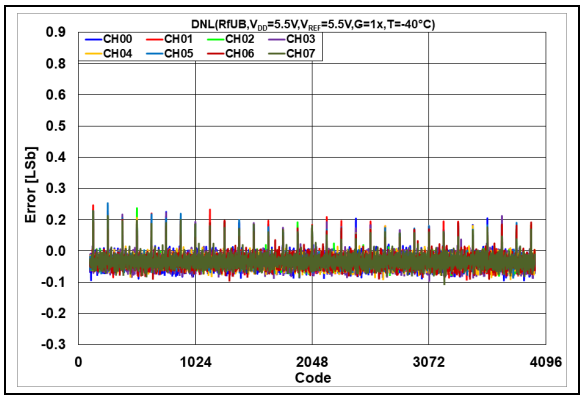


FIGURE 2-80: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

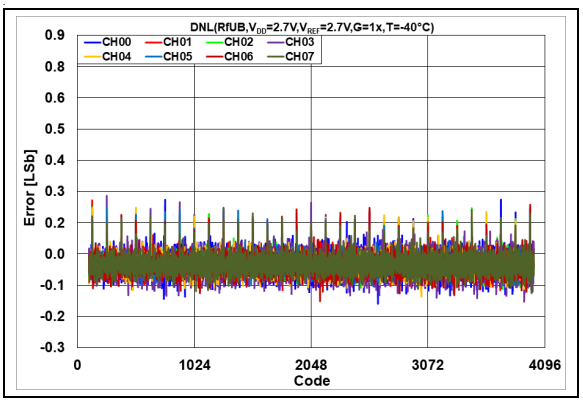


FIGURE 2-83: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

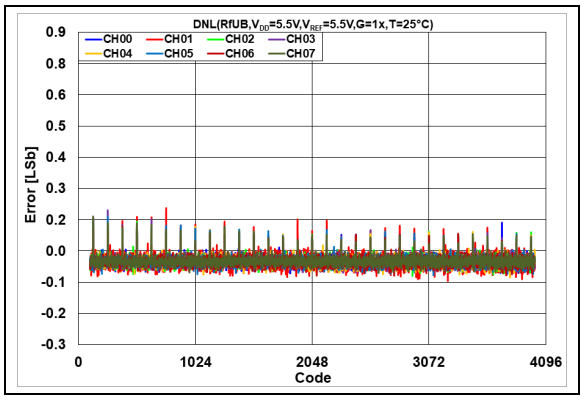


FIGURE 2-81: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

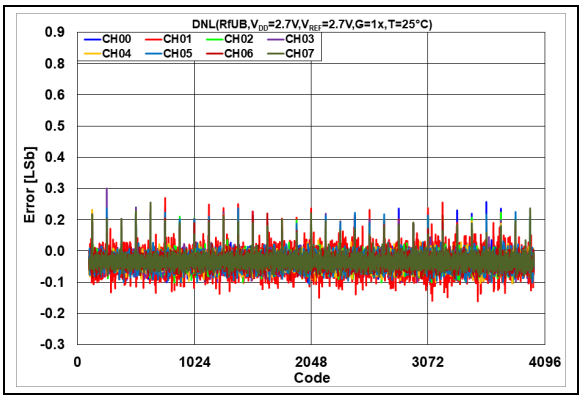


FIGURE 2-84: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

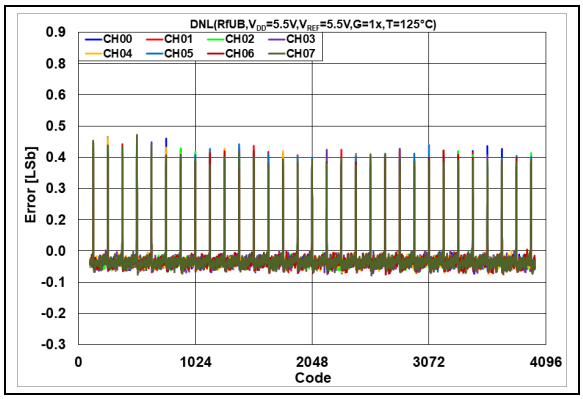


FIGURE 2-82: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

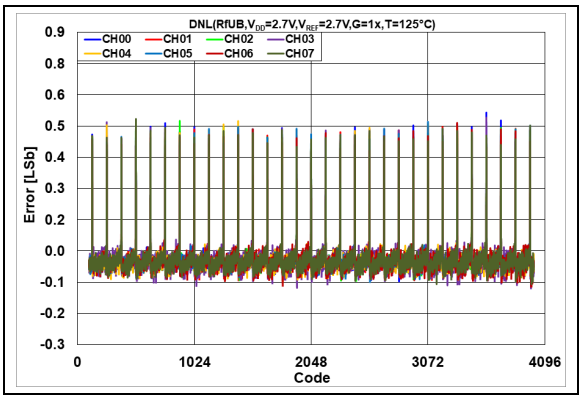


FIGURE 2-85: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.15 DIFFERENTIAL NONLINEARITY ERROR (DNL) – MCP48FXB28 (12-BIT), EXTERNAL V_{REF} MODE, UNBUFFERED (VRnB:VRnA = 10), $V_{REF} = V_{DD}/2$, GAIN = 2x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

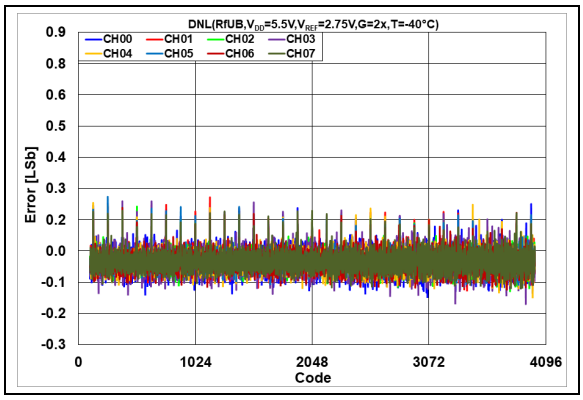


FIGURE 2-86: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

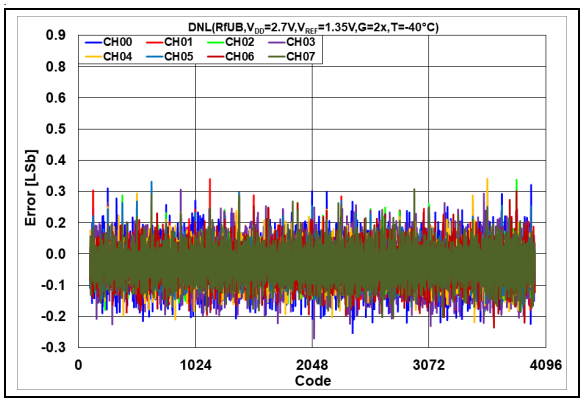


FIGURE 2-89: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

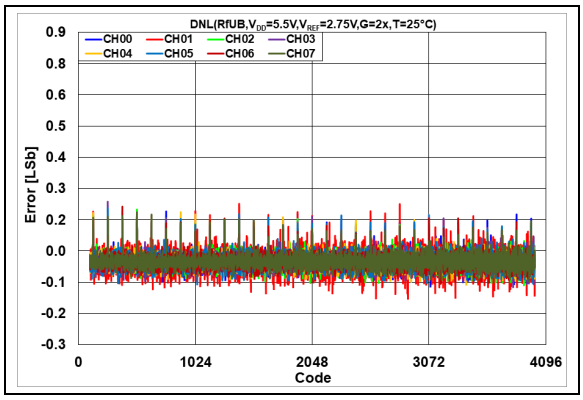


FIGURE 2-87: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

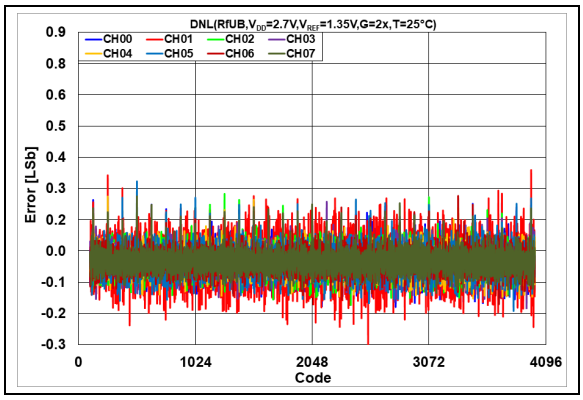


FIGURE 2-90: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

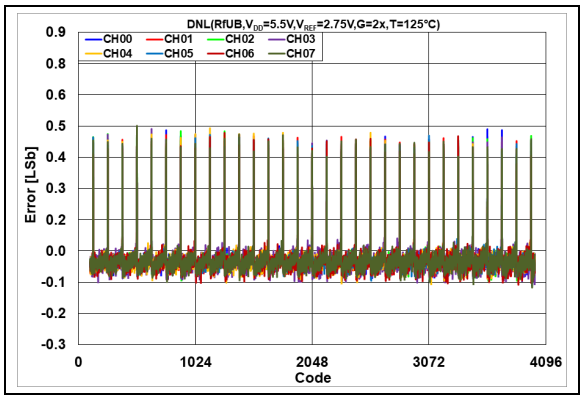


FIGURE 2-88: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

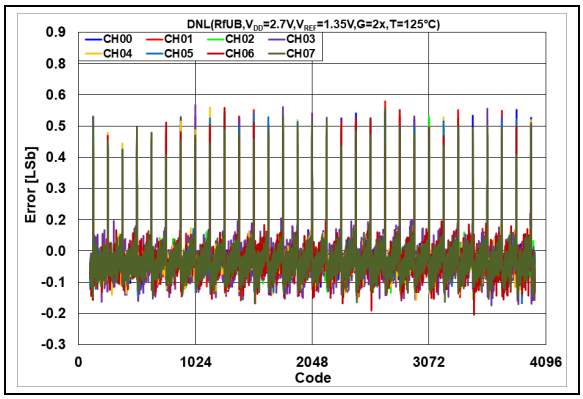


FIGURE 2-91: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.16 TOTAL UNADJUSTED ERROR (TUE) – MCP48FXB28 (12-BIT), EXTERNAL V_{REF} BUFFERED MODE (VRnB:VRnA = 10), V_{REF} = V_{DD}, GAIN = 1x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

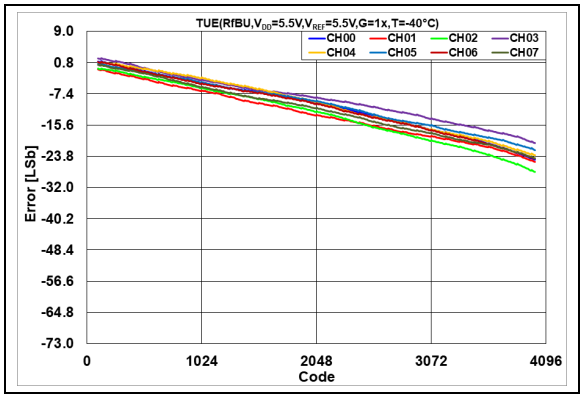


FIGURE 2-92: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

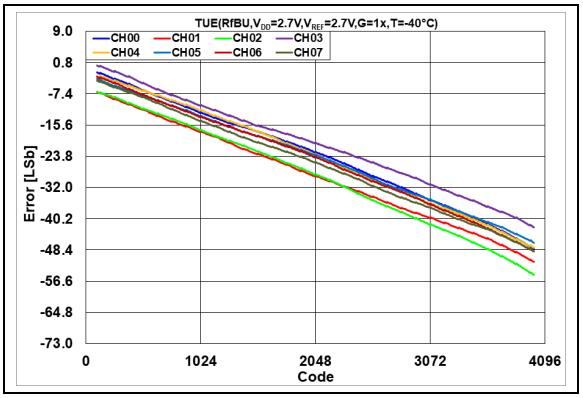


FIGURE 2-95: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

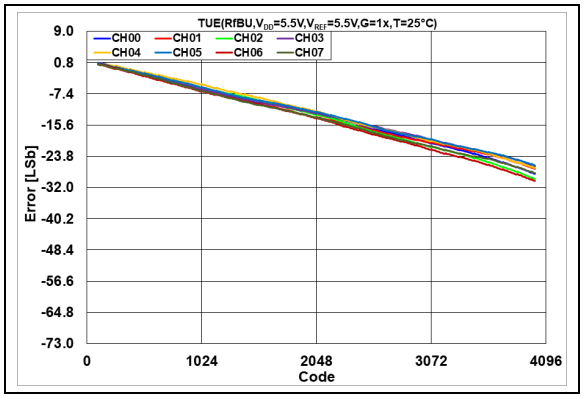


FIGURE 2-93: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C,V_{DD} = 5.5V.*

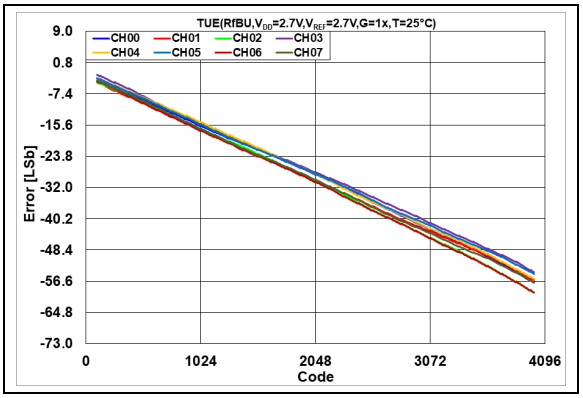


FIGURE 2-96: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

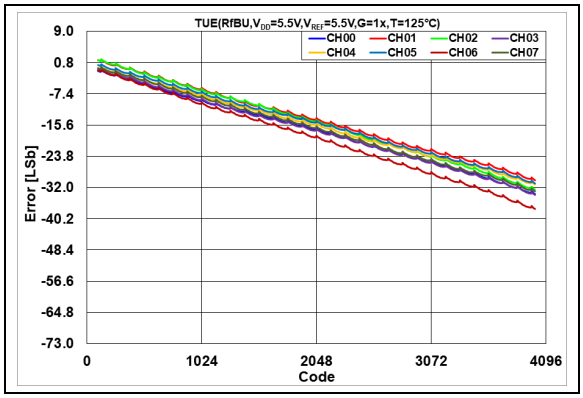


FIGURE 2-94: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

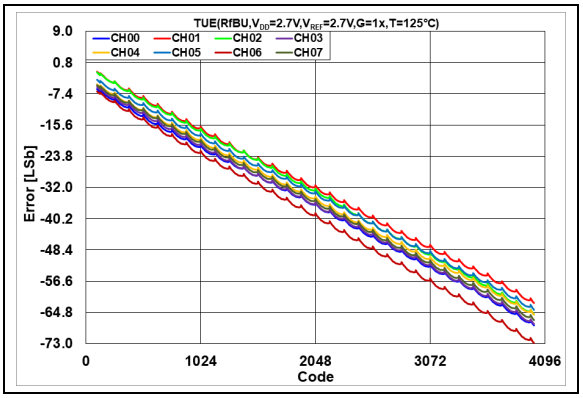


FIGURE 2-97: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.17 TOTAL UNADJUSTED ERROR (TUE) – MCP48FXB28 (12-BIT), EXTERNAL V_{REF} BUFFERED MODE (VRnB:VRnA = 10), $V_{REF} = V_{DD}/2$, GAIN = 2x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

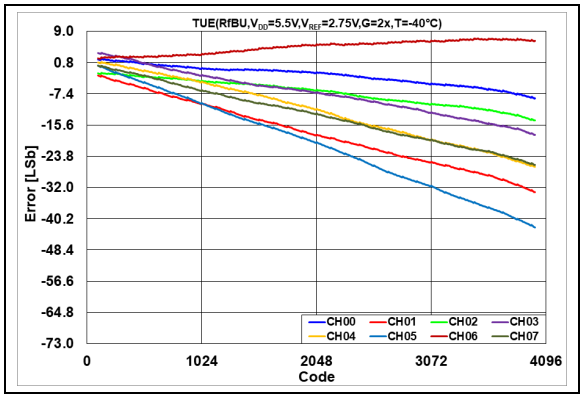


FIGURE 2-98: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

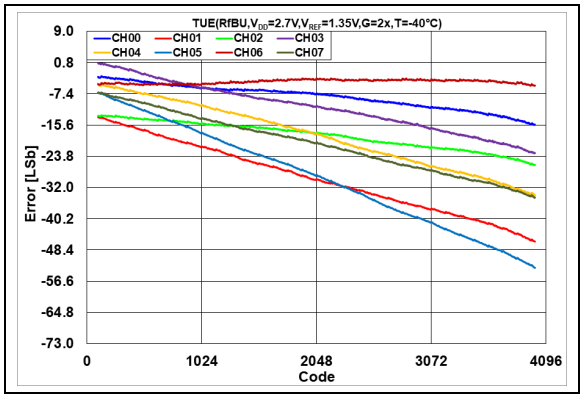


FIGURE 2-101: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

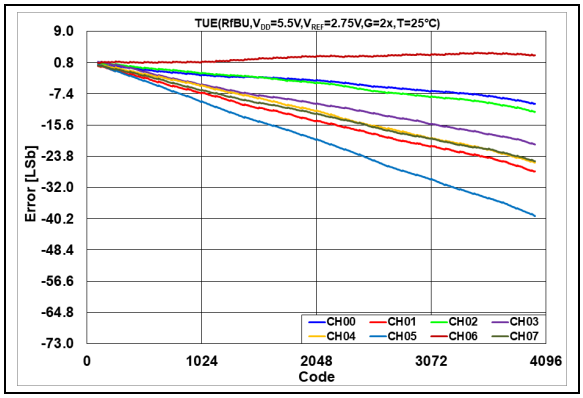


FIGURE 2-99: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C,V_{DD} = 5.5V.*

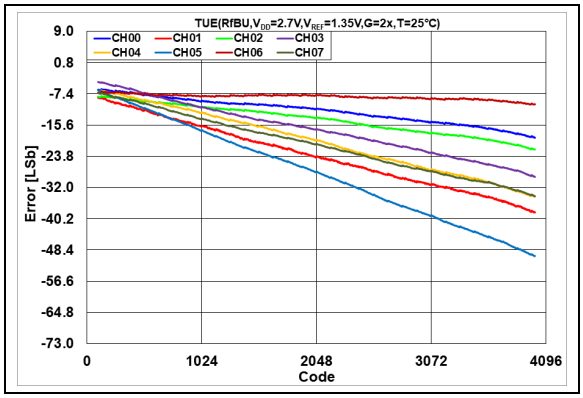


FIGURE 2-102: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

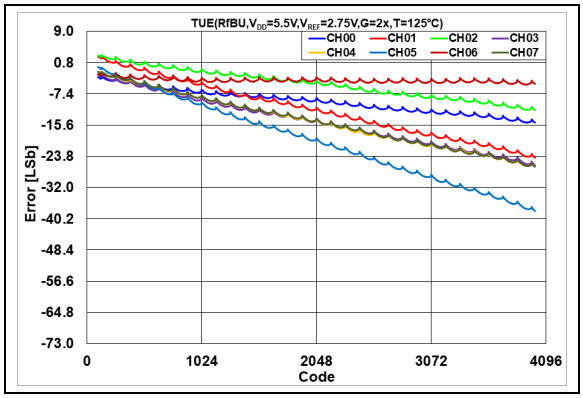


FIGURE 2-100: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

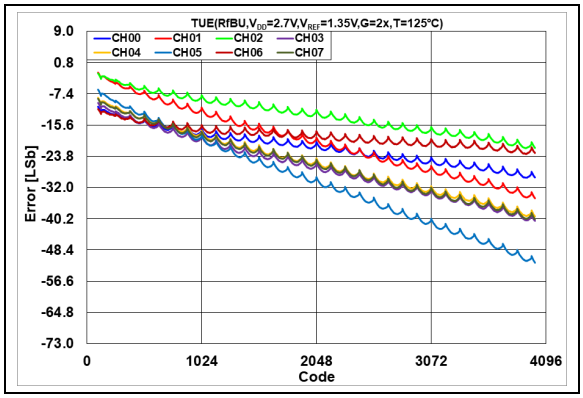


FIGURE 2-103: *Total Unadjusted Error (V_{OUT}) vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.18 INTEGRAL NONLINEARITY ERROR (INL) – MCP48FXB28 (12-BIT), EXTERNAL V_{REF} MODE, BUFFERED (VRnB:VRnA = 11), $V_{REF} = V_{DD}$, GAIN = 1x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

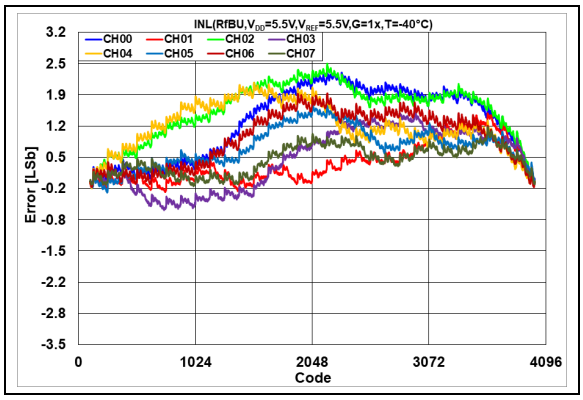


FIGURE 2-104: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

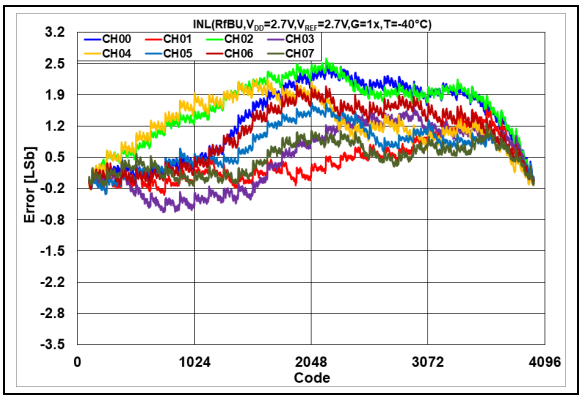


FIGURE 2-107: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

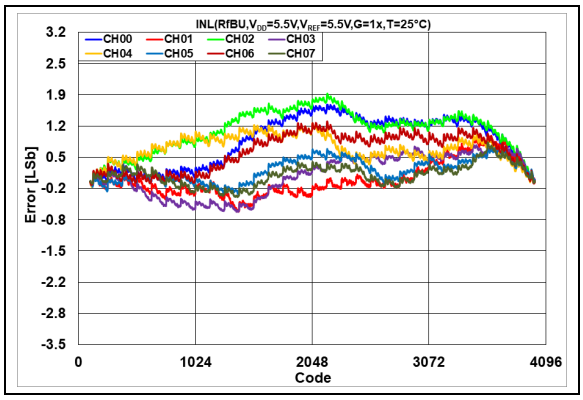


FIGURE 2-105: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

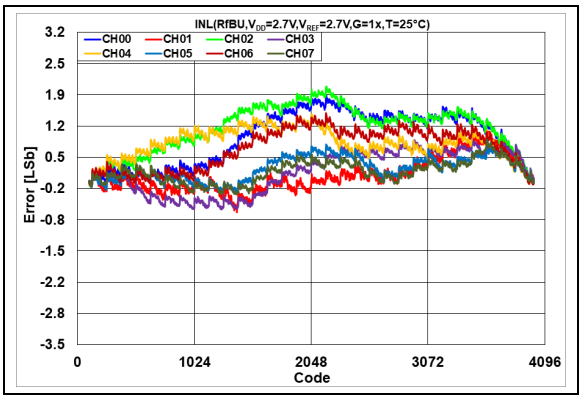


FIGURE 2-108: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

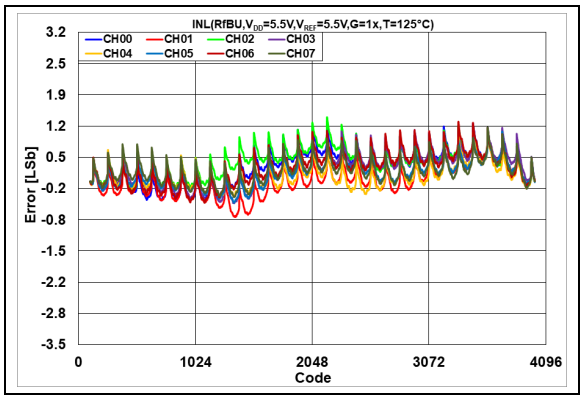


FIGURE 2-106: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

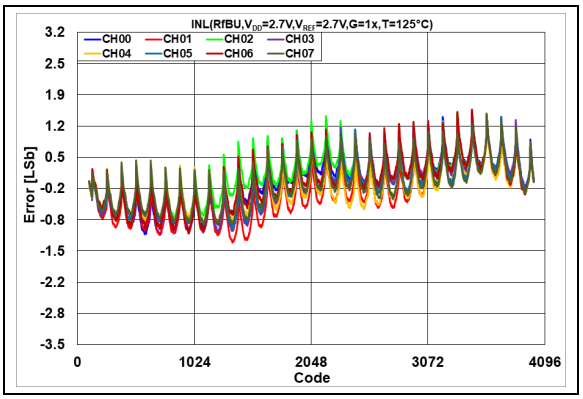


FIGURE 2-109: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.19 INTEGRAL NONLINEARITY ERROR (INL) – MCP48FXB28 (12-BIT), EXTERNAL V_{REF} MODE, BUFFERED (VRnB:VRnA = 11), $V_{REF} = V_{DD}/2$, GAIN = 2x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

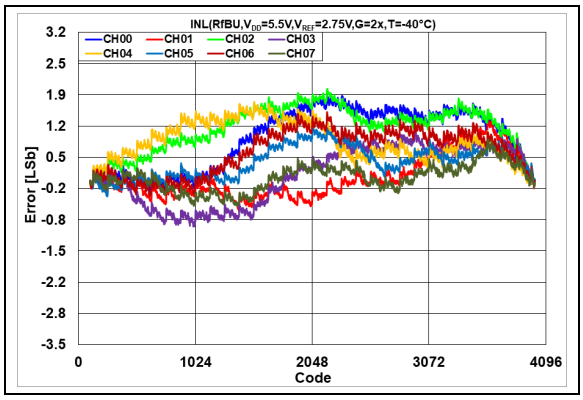


FIGURE 2-110: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

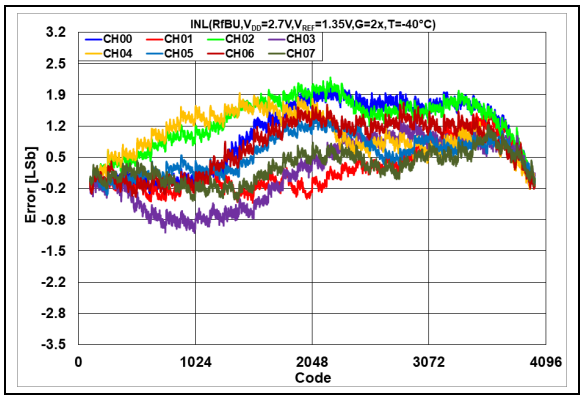


FIGURE 2-113: *INL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

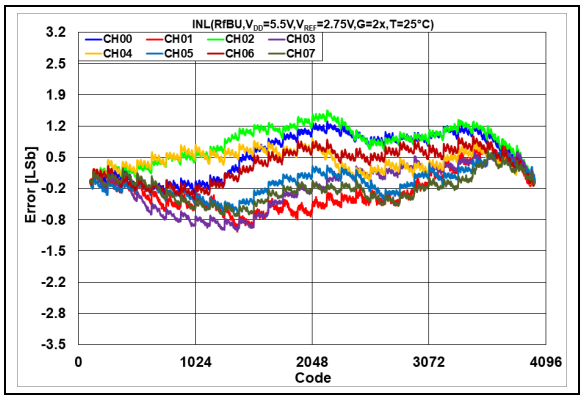


FIGURE 2-111: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

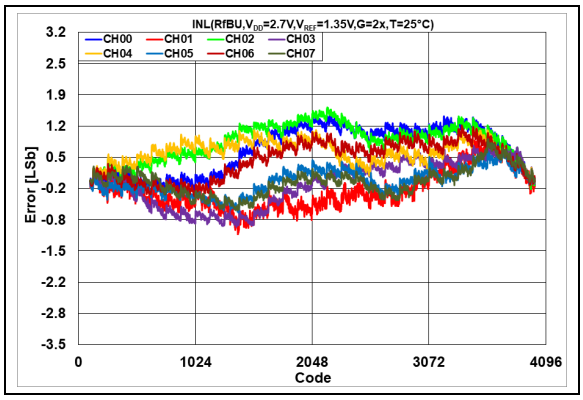


FIGURE 2-114: *INL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

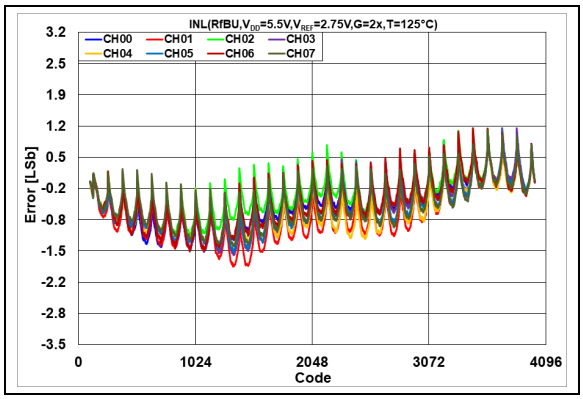


FIGURE 2-112: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

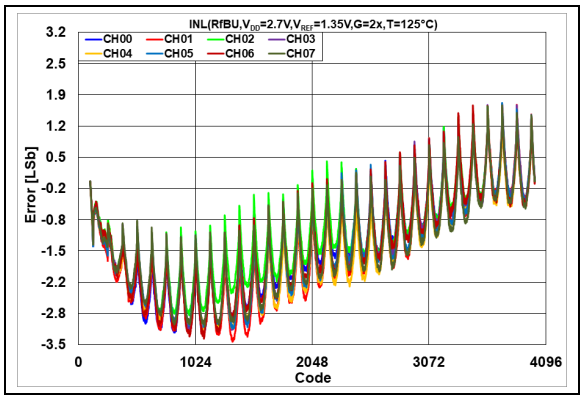


FIGURE 2-115: *INL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.20 DIFFERENTIAL NONLINEARITY ERROR (DNL) – MCP48FXB28 (12-BIT), EXTERNAL V_{REF} MODE, BUFFERED (VRnB:VRnA = 11), $V_{REF} = V_{DD}$, GAIN = 1x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

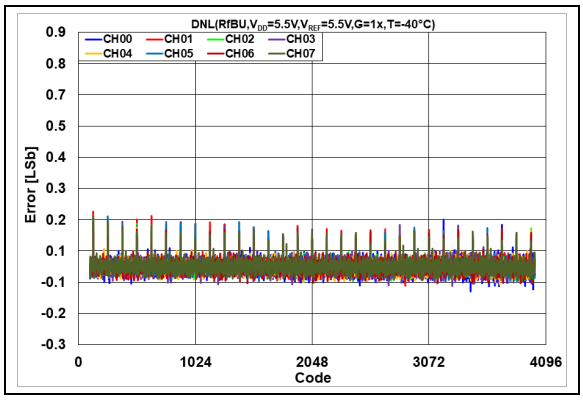


FIGURE 2-116: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

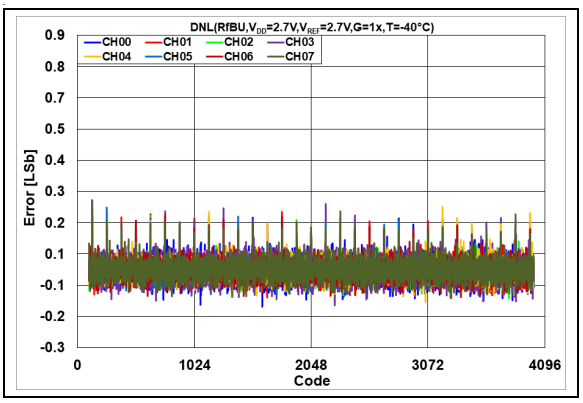


FIGURE 2-119: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

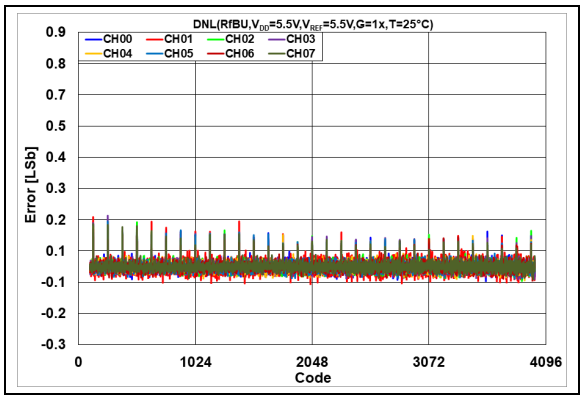


FIGURE 2-117: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

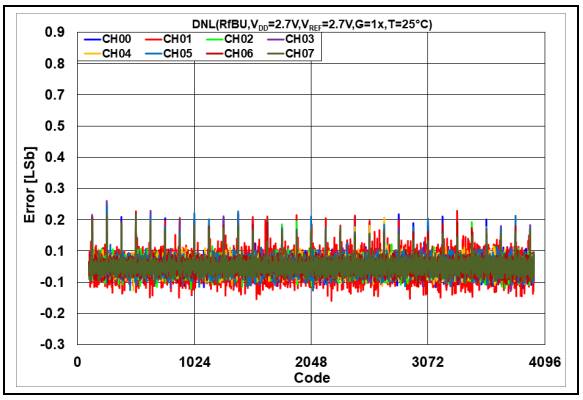


FIGURE 2-120: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

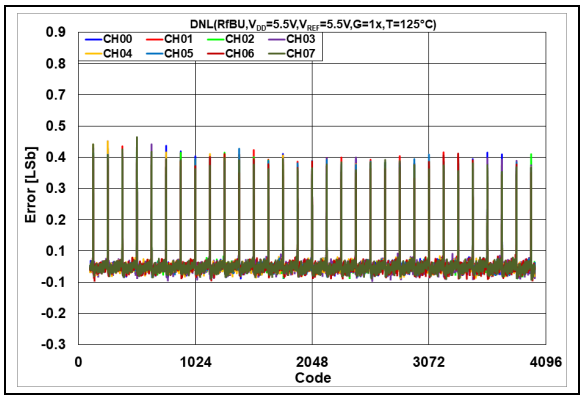


FIGURE 2-118: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

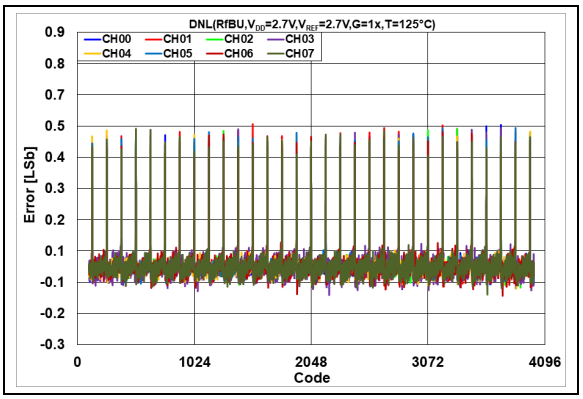


FIGURE 2-121: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

2.2.21 DIFFERENTIAL NONLINEARITY ERROR (DNL) – MCP48FXB28 (12-BIT), EXTERNAL V_{REF} MODE, BUFFERED (VRnB:VRnA = 11), $V_{REF} = V_{DD}/2$, GAIN = 2x, CODE 100-4000

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

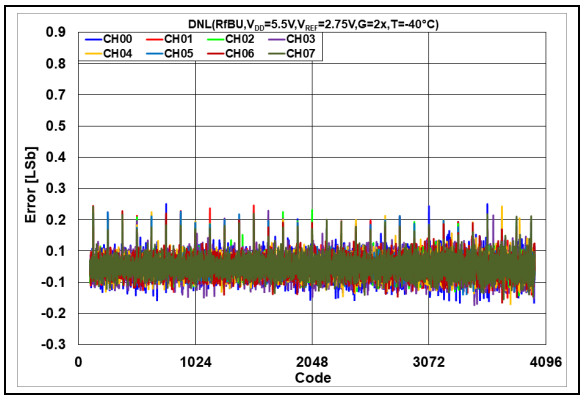


FIGURE 2-122: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 5.5V.*

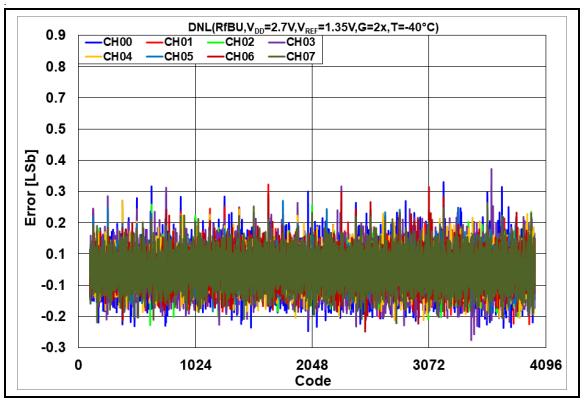


FIGURE 2-125: *DNL Error vs. DAC Code, T = -40°C, V_{DD} = 2.7V.*

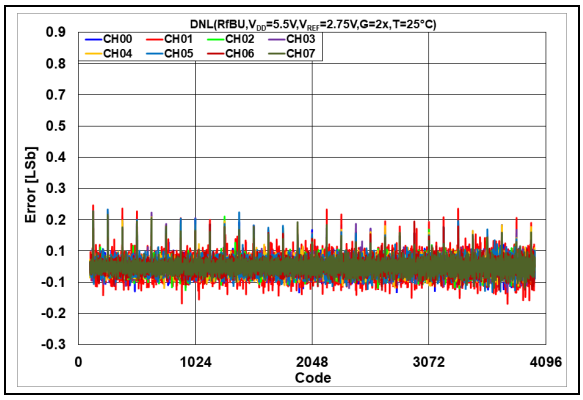


FIGURE 2-123: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 5.5V.*

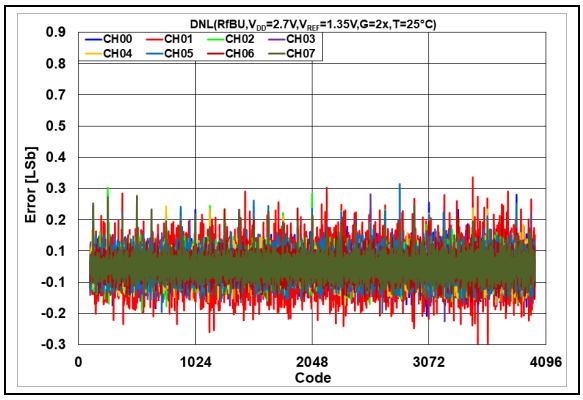


FIGURE 2-126: *DNL Error vs. DAC Code, T = +25°C, V_{DD} = 2.7V.*

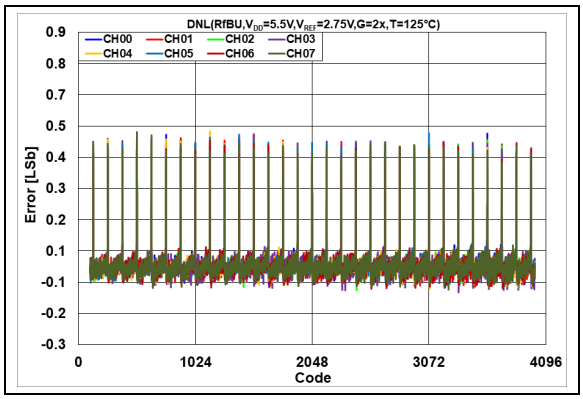


FIGURE 2-124: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 5.5V.*

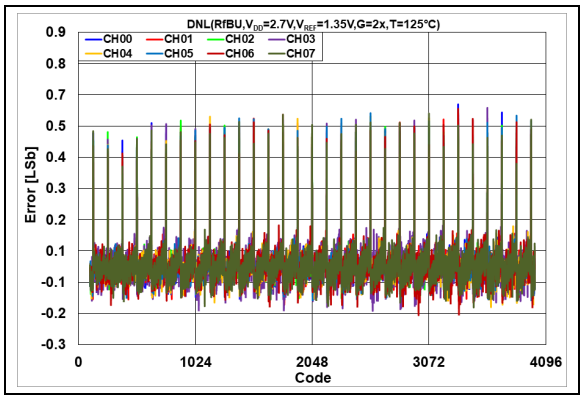


FIGURE 2-127: *DNL Error vs. DAC Code, T = +125°C, V_{DD} = 2.7V.*

NOTES:

3.0 PIN DESCRIPTIONS

Overviews of the pin functions are provided in **Section 3.1 "Positive Power Supply Input Pin (V_{DD})"** through **Section 3.10 "No Connect Pin (NC)"**. The descriptions of the pins for the quad DAC output devices are listed in Table 3-1 and descriptions for the octal DAC output devices are listed in Table 3-2.

TABLE 3-1: MCP48FXBX4 (QUAD DAC) PIN FUNCTION TABLE

Pin					Description
20-Lead TSSOP	20-Lead VQFN	Symbol	I/O	Buffer Type	
1	19	$\overline{LAT1}$	I	ST	DAC Register Latch Pin. The Latch 1 pin allows the value in the volatile DAC1/DAC3 registers (wiper and Configuration bits) to be transferred to the DAC1/DAC3 outputs (V_{OUT1}, V_{OUT3}).
2	20	V_{DD}	—	P	Supply Voltage Pin
3	1	$\overline{CS}$	I	ST	SPI Chip Select Pin
4	2	V_{REF0}	A	Analog	Voltage Reference Input 0 Pin
5	3	V_{OUT0}	A	Analog	Buffered Analog Voltage Output – Channel 0 Pin
6	4	V_{OUT2}	A	Analog	Buffered Analog Voltage Output – Channel 2 Pin
7, 8, 10, 11, 12, 13	5, 6, 8, 9, 10,11	NC	—	—	Not internally connected
9	7	V_{SS}	—	P	Ground Reference Pin for all circuitries on the device
14	12	V_{OUT3}	—	—	Buffered Analog Voltage Output – Channel 3 Pin
15	13	V_{OUT1}	—	—	Buffered Analog Voltage Output – Channel 1 Pin
16	14	V_{REF1}	A	Analog	Voltage Reference Input 1 Pin
17	15	SDO	I	—	SPI Serial Data Output Pin
18	16	SCK	I	ST	SPI Serial Clock Pin
19	17	SDI	I	ST	SPI Serial Data Input Pin
20	18	$\overline{LAT0}$/HVC	I	ST	DAC Register Latch/High-Voltage Command Pin. The Latch 0 pin allows the value in the volatile DAC0/DAC2 registers (wiper and Configuration bits) to be transferred to the DAC0/DAC2 outputs (V_{OUT0}, V_{OUT2}). The High-Voltage Command (HVC) allows user Configuration bits to be written.
—	21	EP	—	—	Exposed Thermal Pad Pin(1)

Note 1: A = Analog, ST = Schmitt Trigger, HV = High Voltage, I = Input, O = Output, I/O = Input/Output, P = Power.

TABLE 3-2: MCP48FXBX8 (OCTAL DAC) PIN FUNCTION TABLE

Pin					Description
20-Lead TSSOP	20-Lead VQFN	Symbol	I/O	Buffer Type	
1	19	$\overline{LAT1}$	I	ST	DAC Register Latch Pin. The Latch 1 pin allows the value in the volatile DAC1/DAC3/DAC5/DAC7 registers (wiper and Configuration bits) to be transferred to the DAC1/DAC3/DAC5/DAC7 outputs (V_{OUT1}, V_{OUT3}, V_{OUT5}, V_{OUT7}).
2	20	V_{DD}	—	P	Supply Voltage Pin
3	1	$\overline{CS}$	I	ST	SPI Chip Select Pin
4	2	V_{REF0}	A	Analog	Voltage Reference Input 0 Pin
5	3	V_{OUT0}	A	Analog	Buffered Analog Voltage Output – Channel 0 Pin
6	4	V_{OUT2}	A	Analog	Buffered Analog Voltage Output – Channel 2 Pin
7	5	V_{OUT4}	A	Analog	Buffered Analog Voltage Output – Channel 4 Pin
8	6	V_{OUT6}	A	Analog	Buffered Analog Voltage Output – Channel 6 Pin
9	7	V_{SS}	—	P	Ground Reference Pin for all circuitries on the device
10, 11	8, 9	NC	—	—	Not internally connected
12	10	V_{OUT7}	A	Analog	Buffered Analog Voltage Output – Channel 7 Pin
13	11	V_{OUT5}	A	Analog	Buffered Analog Voltage Output – Channel 5 Pin
14	12	V_{OUT3}	A	Analog	Buffered Analog Voltage Output – Channel 3 Pin
15	13	V_{OUT1}	A	Analog	Buffered Analog Voltage Output – Channel 1 Pin
16	14	V_{REF1}	A	Analog	Voltage Reference Input 1 Pin
17	15	SDO	I	—	SPI Serial Data Output Pin
18	16	SCK	I	ST	SPI Serial Clock Pin
19	17	SDI	I	ST	SPI Serial Data Input Pin
20	18	$\overline{LAT0}$/HVC	I	ST	DAC Register Latch/High-Voltage Command Pin. The Latch 0 pin allows the value in the volatile DAC0/DAC2/DAC4/DAC6 registers (wiper and Configuration bits) to be transferred to the DAC0/DAC2/DAC4/DAC6 outputs (V_{OUT0}, V_{OUT2}, V_{OUT4}, V_{OUT6}). The High-Voltage Command (HVC) allows user Configuration bits to be written.
—	21	EP	—	—	Exposed Thermal Pad Pin(1)

Note 1: A = Analog, ST = Schmitt Trigger, HV = High Voltage, I = Input, O = Output, I/O = Input/Output, P = Power.

3.1 Positive Power Supply Input Pin (V_{DD})

V_{DD} is the positive supply voltage input pin. The input supply voltage is relative to V_{SS}.

The power supply at the V_{DD} pin should be as clean as possible for a good DAC performance. It is recommended to use an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate noise present in application boards.

3.2 Ground Pin (V_{SS})

The V_{SS} pin is the device ground reference.

The user must connect the V_{SS} pin to a ground plane through a low-impedance connection. If an analog ground path is available in the application PCB (Printed Circuit Board), it is highly recommended that the V_{SS} pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.3 Voltage Reference Pins (V_{REF})

The V_{REF} pin is either an input or an output. When the DAC's voltage reference is configured as the V_{REF} pin, the pin is an input. When the DAC's voltage reference is configured as the internal band gap, the pin is an output.

When the DAC's voltage reference is configured as the V_{REF} pin, there are two options for this voltage input:

- V_{REF} pin voltage buffered
- V_{REF} pin voltage unbuffered

The buffered option is offered in cases where the external reference voltage does not have sufficient current capability to not drop its voltage when connected to the internal resistor ladder circuit.

When the DAC's voltage reference is configured as the device V_{DD}, the V_{REF} pin is disconnected from the internal circuit.

When the DAC's voltage reference is configured as the internal band gap, the V_{REF} pin's drive capability is minimal, so the output signal should be buffered.

There are two V_{REF} pins, each corresponding to a group of output channels. V_{REF0} is connected to even channels: 0-6, while V_{REF1} is connected to odd channels: 1-7. See **Section 5.2 "Voltage Reference Selection"** and Register 4-2 for more details on the configuration bits.

3.4 Analog Output Voltage Pins (V_{OUTn})

V_{OUT} is the DAC analog voltage output pin. The DAC output has an output amplifier. The DAC output range depends on the selection of the voltage reference source (and potential output gain selection). These are:

- Device V_{DD} – The full-scale range of the DAC output is from V_{SS} to approximately V_{DD}.
- V_{REF} Pin – The full-scale range of the DAC output is from V_{SS} to G × V_{RL}, where G is the gain selection option (1x or 2x).
- Internal Band Gap – The full-scale range of the DAC output is from V_{SS} to G × (2 × V_{BG}), where G is the gain selection option (1x or 2x).

In Normal mode, the DC impedance of the output pin is about 1Ω. In Power-Down mode, the output pin is internally connected to a known pull-down resistor of 1 kΩ, 125 kΩ or open. The power-down selection bits setting are shown in Register 4-3 and Table 5-4.

3.5 Latch Pin ($\overline{LAT}$)/High-Voltage Command Pin (HVC)

The DAC output value update event can be controlled and synchronized using the $\overline{LAT}$ pins, for one or both channels, on a single or different devices.

The $\overline{LAT}$ pins control the effect of the Volatile Wiper registers, and the VRnB:VRnA, PDnB:PDnA and Gx bits on the DAC output.

If the $\overline{LAT}$ pins are held at V_{IH}, the values sent to the Volatile Wiper registers and Configuration bits have no effect on the DAC outputs.

Once voltage on the pin transitions to V_{IL}, the values in the Volatile Wiper registers and Configuration bits are transferred to the DAC outputs.

The pin is level-sensitive, so writing to the Volatile Wiper registers and Configuration bits, while it is being held at V_{IL}, will trigger an immediate change in the outputs.

The HVC pin allows the device's nonvolatile user Configuration bits to be programmed when the voltage on the pin is greater than the V_{IHH} entry voltage.

3.6 SPI – Chip Select Pin ($\overline{CS}$)

The $\overline{CS}$ pin enables/disables the serial interface. The serial interface must be enabled for the SPI commands to be received by the device. See **Section 6.2 "SPI Serial Interface"** for more details on the SPI serial interface communication.

3.7 SPI – Serial Data Input Pin (SDI)

The SDI pin is the serial data input pin of the SPI interface. The SDI pin is used to read the DAC registers and Configuration bits.

See **Section 6.2 "SPI Serial Interface"** for more details on the SPI serial interface communication.

3.8 SPI – Serial Data Output Pin (SDO)

The SDO pin is the serial data output pin of the SPI interface. The SDO pin is used to write the DAC registers and Configuration bits.

See **Section 6.2 "SPI Serial Interface"** for more details on the SPI serial interface communication.

3.9 SPI – Serial Clock Pin (SCK)

The SCK pin is the serial clock pin of the SPI interface. The MCP48FXBX4/8 SPI interface only accepts external serial clocks.

See **Section 6.2, SPI Serial Interface** for more details on the SPI serial interface communication.

3.10 No Connect Pin (NC)

The NC pins are not connected to the device.

3.11 Exposed Pad Pin

This pad is conductively connected to the device's substrate. It should be tied to the same potential as the V_{SS} pin (or left unconnected). This pad could be used to assist in heat dissipation for the device when connected to a PCB heat sink. The pad is only present on the VQFN package.

4.0 GENERAL DESCRIPTION

The MCP48FXBX4 (MCP48FXB04, MCP48FXB14 and MCP48FXB24) devices are quad-channel voltage output devices. The MCP48FXBX8 (MCP48FXB08, MCP48FXB18 and MCP48FXB28) devices are octal-channel voltage output devices.

These devices are offered with 8-bit (MCP48FXB0X), 10-bit (MCP48FXB1X) and 12-bit (MCP48FXB2X) resolutions and include nonvolatile memory (EEPROM), an SPI serial interface and two write Latch pins ($\overline{LAT0}$, $\overline{LAT1}$) to control the update of the written DAC value to the DAC output pin.

The devices use a resistor ladder architecture. The resistor ladder DAC is driven from a software-selectable voltage reference source. The source can be either the device's internal V_{DD}, an external V_{REF} pin voltage (buffered or unbuffered) or an internal band gap voltage source.

The DAC output is buffered with a low-power and precision output amplifier (op amp). This output amplifier provides a rail-to-rail output with low offset voltage and low noise. The gain (1x or 2x) of the output buffer is software configurable.

This device family also has a user-programmable nonvolatile memory (EEPROM) option, which allows the user to save the desired POR/BOR value of the DAC register and device Configuration bits.

High-voltage lock bits can be used to ensure that the device's output settings are not accidentally modified.

The device operates from a single-supply voltage. This voltage is specified from 2.7V to 5.5V for full specified operation and from 1.8V to 5.5V for digital operation. The device can operate between 1.8V and 2.7V, but its analog performance is significantly reduced; therefore, most device parameters are not specified for this range.

The main functional blocks are:

- **Power-on Reset/Brown-out Reset (POR/BOR)**
- **Device Memory**
- **Resistor Ladder**
- **Output Buffer/V_{OUT} Operation**
- **Internal Band Gap**
- **SPI Serial Interface Module**

4.1 Power-on Reset/Brown-out Reset (POR/BOR)

The internal POR/BOR circuit monitors the power supply voltage (V_{DD}) during operation. This circuit ensures correct device start-up at system power-up and power-down events. The device's RAM Retention Voltage (V_{RAM}) is lower than the POR/BOR Voltage (V_{POR}/V_{BOR}) trip point. The maximum V_{POR}/V_{BOR} voltage is less than 1.8V.

POR occurs as the voltage rises (typically from 0V), while BOR occurs as the voltage falls (typically from $V_{DD(MIN)}$ or higher).

The POR and BOR trip points are at the same voltage and the condition is determined by whether the V_{DD} voltage is rising or falling (see Figure 4-1). What occurs is different depending on whether the reset is a POR or BOR.

When $V_{POR}/V_{BOR} < V_{DD} < 2.7V$, the electrical performance may not meet the data sheet specifications. In this region, the device is capable of reading and writing to its EEPROM and reading and writing to its volatile memory if the proper serial command is executed.

4.1.1 POWER-ON RESET

The Power-on Reset is the case where the V_{DD} has power applied to it, ramping up from the V_{SS} voltage level. As the device powers up, the V_{OUT} pin floats to an unknown value. When V_{DD} is above the transistor threshold voltage of the device, the output starts to be pulled low. After the V_{DD} is above the POR/BOR trip point (V_{BOR}/V_{POR}), the resistor network's wiper is loaded with the POR value (midscale). The volatile memory determines the analog output (V_{OUT}) pin voltage. After the device is powered up, the user can update the device's memory.

When the rising V_{DD} voltage crosses the V_{POR} trip point, the following occurs:

- The nonvolatile DAC register value is latched into the volatile DAC register.
- The nonvolatile Configuration bit values are latched into the volatile Configuration bits.
- The POR status bit is set ('1').
- The POR Reset Delay Timer (t_{PORD}) starts; when the POR Reset Delay Timer (t_{PORD}) times out, the serial interface is operational. During this delay time, the serial interface will not accept commands.
- The Device Memory Address Pointer is forced to 00h.

The Analog Output (V_{OUT}) state is determined by the state of the volatile Configuration bits and the DAC register. This is called a Power-on Reset (event).

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

4.1.2 BROWN-OUT RESET

The Brown-out Reset occurs when a device has power applied to it and that power (voltage) drops below the specified range.

When the falling V_{DD} voltage crosses the V_{POR} trip point (BOR event), the following occurs:

- The serial interface is disabled.
- EEPROM writes are disabled.
- The device is forced into a Power-Down state (PDnB:PDnA = 11). Analog circuitry is turned off.
- The volatile DAC register is forced to 000h.
- Volatile Configuration bits, VRnB:VRnA and Gx, are forced to '0'.

If the V_{DD} voltage decreases below the V_{RAM} voltage, all volatile memory may become corrupted.

As the voltage recovers above the V_{POR}/V_{BOR} voltage, see **Section 4.1.1 "Power-on Reset"**.

Serial commands not completed due to a brown-out condition may cause the memory location (volatile and nonvolatile) to become corrupted.

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

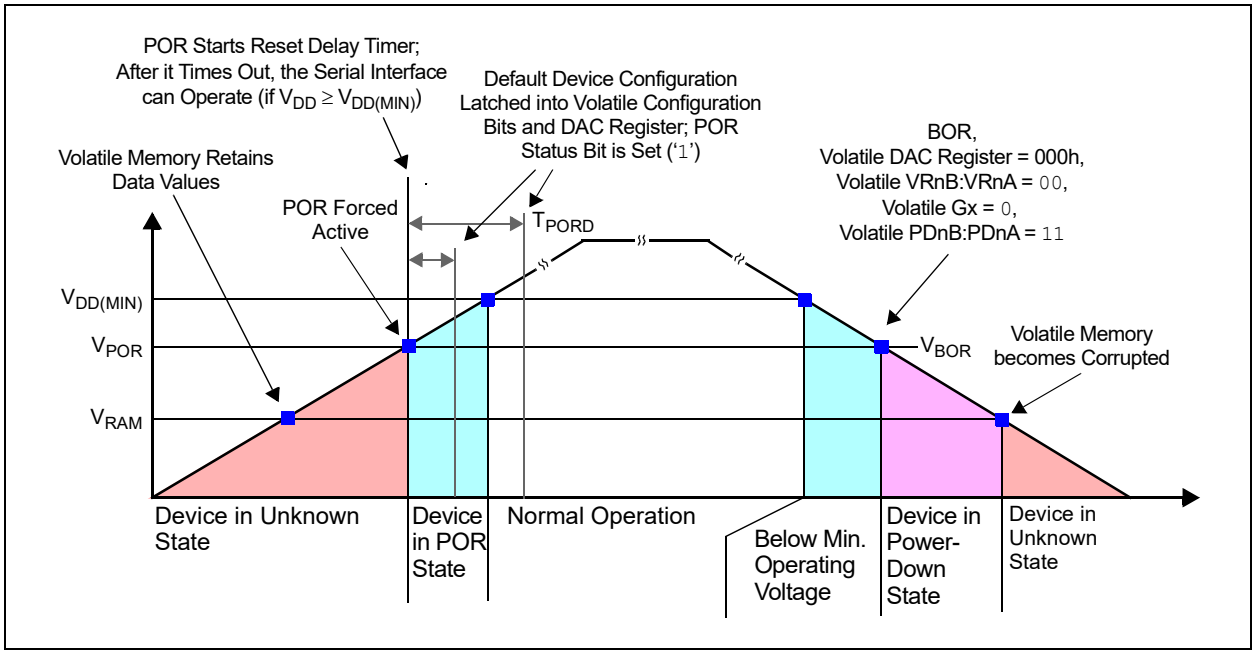


FIGURE 4-1: *POR/BOR Operation.*

4.2 Device Memory

User memory includes the following types:

- **Volatile Register Memory (RAM)**
- **Nonvolatile Register Memory**
- **Device Configuration Memory**

Each memory address is 16 bits wide. There are up to 17 nonvolatile user control bits that do not reside in memory-mapped register space (see **Section 4.2.3 "Device Configuration Memory"**).

4.2.1 VOLATILE REGISTER MEMORY (RAM)

There are up to twelve volatile memory locations:

- DAC0 through DAC7 Output Value registers
- V_{REF} Select register
- Power-Down Configuration register
- Gain and Status register
- WiperLock Technology Status register

The volatile memory starts functioning when the device V_{DD} is at (or above) the RAM Retention Voltage (V_{RAM}). The volatile memory will be loaded with the default device values when the V_{DD} rises across the V_{POR}/V_{BOR} voltage trip point.

4.2.2 NONVOLATILE REGISTER MEMORY

This device family uses the nonvolatile memory for the DAC output value and Configuration registers:

- Nonvolatile DAC0 through DAC7 Output Value registers
- Nonvolatile V_{REF} Select register
- Nonvolatile Power-Down Configuration register
- Nonvolatile Gain register

The nonvolatile memory starts functioning below the device's V_{POR}/V_{BOR} trip point, and is loaded into the corresponding volatile registers whenever the device rises above the POR/BOR voltage trip point.

The device starts writing the nonvolatile (EEPROM) memory location at the completion of the serial interface command, after the Acknowledge pulse of the `WRITE` single command. Continuous `WRITE` commands addressing the nonvolatile memory are not permitted.

Note:	When the nonvolatile memory is written, the corresponding volatile memory is **not** modified.

Nonvolatile DAC registers enable the stand-alone operation of the device (without microcontroller control) after being programmed to the desired value.

4.2.3 DEVICE CONFIGURATION MEMORY

There are up to sixteen nonvolatile user bits that are not directly mapped into the address space. These non-volatile device Configuration bits control the WiperLock technology for DAC registers and configuration (two bits per DAC).

The Status register shows the states of the device WiperLock technology Configuration bits. The Status register is described in Register 4-6.

The operation of WiperLock technology is discussed in **Section 4.2.6 "WiperLock Technology"**.

4.2.4 UNIMPLEMENTED REGISTER BITS

`READ` commands of a valid location will read unimplemented bits as '`0`'.

4.2.5 UNIMPLEMENTED (RESERVED) LOCATIONS

Normal (voltage) commands (`READ` or `WRITE`) to any unimplemented memory address (reserved) will result in a Command Error (CMDERR) condition. `READ` commands of a reserved location will read bits as '`1`'.

High-Voltage Commands (enable or disable) to any unimplemented Configuration bits will result in a Command Error (CMDERR) condition.

4.2.5.1 Default Factory POR Memory State of Nonvolatile Memory (EEPROM)

Table 4-2 shows the default factory POR initialization of the device memory map for the 8, 10 and 12-bit devices. In the case of volatile memory devices (MCP48FVBXX), the factory default values cannot be modified.

Note:	The volatile memory locations will be determined by the nonvolatile memory states (registers and device Configuration bits).

TABLE 4-1: MCP48FXBX4/8 MEMORY MAP

Address	Function	Config Bit(1)	Quad	Octal
00h	Volatile DAC0 Register	CL0	Y	Y
01h	Volatile DAC1 Register	CL1	Y	Y
02h	Volatile DAC2 Register	CL2	Y	Y
03h	Volatile DAC3 Register	CL3	Y	Y
04h	Volatile DAC4 Register	CL4	—	Y
05h	Volatile DAC5 Register	CL5	—	Y
06h	Volatile DAC6 Register	CL6	—	Y
07h	Volatile DAC7 Register	CL7	—	Y
08h	V_{REF} Register	—	Y	Y
09h	Power-Down Register	—	Y	Y
0Ah	Gain and Status Register	—	Y	Y
0Bh	WiperLock™ Technology Status Register	—	Y	Y
10h	Nonvolatile DAC0 Register	DL0	Y	Y
11h	Nonvolatile DAC1 Register	DL1	Y	Y
12h	Nonvolatile DAC2 Register	DL2	Y	Y
13h	Nonvolatile DAC3 Register	DL3	Y	Y
14h	Nonvolatile DAC4 Register	DL4	—	Y
15h	Nonvolatile DAC5 Register	DL5	—	Y
16h	Nonvolatile DAC6 Register	DL6	—	Y
17h	Nonvolatile DAC7 Register	DL7	—	Y
18h	Nonvolatile V_{REF} Register	—	Y	Y
19h	Nonvolatile Power-Down Register	—	Y	Y
1Ah	Nonvolatile Gain Register	—	Y	Y
1Bh	Reserved	—	—	—

Volatile Memory Address Range

Nonvolatile Memory Address Range

Note 1: Device Configuration memory bits require a high-voltage enable or disable command ($\overline{LATn}$ = V_{IHH} or $\overline{CS}$ = V_{IHH}) to modify the bit value.

TABLE 4-2: FACTORY DEFAULT POR/BOR VALUES

Address	Function	POR/BOR Value		
		8-Bit	10-Bit	12-Bit
00h	Volatile DAC0 Register	7Fh	1FFh	7FFh
01h	Volatile DAC1 Register	7Fh	1FFh	7FFh
02h	Volatile DAC2 Register	FFh	3FFh	FFFh
03h	Volatile DAC3 Register	FFh	3FFh	FFFh
04h	Volatile DAC4 Register	FFh	3FFh	FFFh
05h	Volatile DAC5 Register	FFh	3FFh	FFFh
06h	Volatile DAC6 Register	FFh	3FFh	FFFh
07h	Volatile DAC7 Register	FFh	3FFh	FFFh
08h	V_{REF} Register	0000h	0000h	0000h
09h	Power-Down Register	0000h	0000h	0000h
0Ah	Gain and Status Register	0080h	0080h	0080h
0Bh	WiperLock™ Technology Status Register	0000h	0000h	0000h
10h	Nonvolatile DAC0 Register	7Fh	1FFh	7FFh
11h	Nonvolatile DAC1 Register	7Fh	1FFh	7FFh
12h	Nonvolatile DAC2 Register	FFh	3FFh	FFFh
13h	Nonvolatile DAC3 Register	FFh	3FFh	FFFh
14h	Nonvolatile DAC4 Register	FFh	3FFh	FFFh
15h	Nonvolatile DAC5 Register	FFh	3FFh	FFFh
16h	Nonvolatile DAC6 Register	FFh	3FFh	FFFh
17h	Nonvolatile DAC7 Register	FFh	3FFh	FFFh
18h	Nonvolatile V_{REF} Register	0000h	0000h	0000h
19h	Nonvolatile Power-Down Register	0000h	0000h	0000h
1Ah	Nonvolatile Gain Register	0000h	0000h	0000h
1Bh	Reserved(1)	—	—	—

Volatile Memory address range

Nonvolatile Memory address range

Note 1: Reading a reserved memory location results in the SPI command error condition. The SDO pin will output all '0's. Forcing the $\overline{CS}$ pin to the V_{IH} state will reset the SPI interface.

4.2.6 WIPERLOCK TECHNOLOGY

The MCP48FXBX4/8 WiperLock technology allows application-specific device settings (DAC register and configuration) to be secured without requiring the use of an additional write-protect pin. There are two Configuration bits (DLn:CLn) for each DAC channel (DAC0 through DAC7).

Dependent on the state of the DLn:CLn Configuration bits, WiperLock technology prevents the serial commands from the following actions on the DACn registers and bits:

- Writing to the specified volatile DACn register memory location
- Writing to the specified nonvolatile DACn register memory location
- Writing to the specified volatile DACn Configuration bits
- Writing to the specified nonvolatile DACn Configuration bits

Each pair of these Configuration bits controls one of the four modes.

To modify the Configuration bits, the HVC pin must be forced to the V_{IHH} state and then an enable or disable command must be received for the desired pair of DAC register addresses.

Example: To modify the CL0 bit, the enable or disable command specifies address 00h; while to modify the DL0 bit, the enable or disable command specifies address 10h.

Note: During device communication, if the device address/command combination is invalid or an unimplemented address is specified, the MCP48FXBX4/8 will command error that command byte. To reset the serial interface state machine, the $\overline{CS}$ pin must be driven to the Inactive state (V_{IH}) before returning to the Active state (V_{IL} or V_{IHH}).

4.2.6.1 POR/BOR Operation with WiperLock Technology Enabled

The WiperLock Technology state is not affected by a POR/BOR event. A POR/BOR event will load the volatile DACn register values with the nonvolatile or default factory values (in case of volatile memory only devices).

TABLE 4-3: WIPERLOCK™ TECHNOLOGY CONFIGURATION BITS – FUNCTIONAL DESCRIPTION

DLn:CLn[1]	Register/Bits				Comments
	DACn Wiper		DACn Configuration[1]		
	Volatile	Nonvolatile	Volatile	Nonvolatile	
11	Locked	Locked	Locked	Locked	All DACn registers are locked.
10	Locked	Locked	Unlocked	Locked	All DACn registers are locked, except for volatile DACn Configuration registers. This allows operation of Power-Down modes.
01	Unlocked	Locked	Unlocked	Locked	Volatile DACn registers are unlocked, nonvolatile DACn registers are locked.
00	Unlocked	Unlocked	Unlocked	Unlocked	All DACn registers are unlocked.

Note 1: The state of these Configuration bits (DLn:CLn) is reflected in the WLnB:WLnA bits, as shown in Register 4-6. DAC Configuration bits include Voltage Reference Control bits (VRnB:VRnA), Power-Down Control bits (PDnB:PDnA) and Output Gain bits (Gx).

4.2.7 DEVICE REGISTERS

Register 4-1 shows the format of the DAC Output Value registers for both volatile and nonvolatile memory locations. These registers will be either 8 bits, 10 bits or 12 bits wide. The values are right justified.

REGISTER 4-1: DAC0 TO DAC7: DAC OUTPUT VALUE REGISTERS (ADDRESSES 00h THROUGH 07h/10h THROUGH 17h; VOLATILE/NONVOLATILE)

	U-0	U-0	U-0	U-0	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
12-bit	—	—	—	—	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
10-bit	—	—	—	—	—(1)	—(1)	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
8-bit	—	—	—	—	—(1)	—(1)	—(1)	—(1)	D07	D06	D05	D04	D03	D02	D01	D00
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= 12-bit device	= 10-bit device	= 8-bit device	

12-Bit	**10-Bit**	**8-Bit**	
bit 15-12	bit 15-10	bit 15-8	**Unimplemented:** Read as '0'
bit 11-0	—	—	**D11-D00:** DAC Output Value – 12-bit devices FFFh = Full-scale output value 7FFh = Midscale output value 000h = Zero scale output value
—	bit 9-0	—	**D09-D00:** DAC Output Value – 10-bit devices 3FFh = Full-scale output value 1FFh = Midscale output value 000h = Zero scale output value
—	—	bit 7-0	**D07-D00:** DAC Output Value – 8-bit devices FFh = Full-scale output value 7Fh = Midscale output value 000h = Zero scale output value

Note 1: Unimplemented bit, read as '0'.

Register 4-2 shows the format of the Voltage Reference Control register. Each DAC has two bits to control the source of the DAC's voltage reference. This register is for both volatile and nonvolatile memory locations.

REGISTER 4-2: VREF: VOLTAGE REFERENCE CONTROL REGISTER (ADDRESSES 08h AND 18h; VOLATILE/NONVOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
Octal	VR7B	VR7A	VR6B	VR6A	VR5B	VR5A	VR4B	VR4A	VR3B	VR3A	VR2B	VR2A	VR1B	VR1A	VR0B	VR0A
Quad	__(1)	__(1)	__(1)	__(1)	__(1)	__(1)	__(1)	__(1)	VR3B	VR3A	VR2B	VR2A	VR1B	VR1A	VR0B	VR0A
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad-channel device	= Octal-channel device		

Octal	**Quad**	
—	bit 15-8	**Unimplemented:** Read as '0'
bit 15-0	bit 7-0	**VRnB:VRnA:** DAC Voltage Reference Control 11 = V_{REF} pin (buffered); V_{REF} buffer enabled 10 = V_{REF} pin (unbuffered); V_{REF} buffer disabled 01 = Internal band gap (1.22V typical); V_{REF} buffer enabled, V_{REF} voltage driven when powered down 00 = V_{DD} (unbuffered); V_{REF} buffer disabled Use this state with Power-Down bits for lowest current.

Note 1: Unimplemented bit, read as '0'.

Register 4-3 shows the format of the Power-Down Control register. Each DAC has two bits to control the Power-Down state of the DAC. This register is for both volatile and nonvolatile memory locations.

REGISTER 4-3: POWER-DOWN CONTROL REGISTER (ADDRESSES 09h, 19h; VOLATILE/NONVOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
Octal	PD7B	PD7A	PD6B	PD6A	PD5B	PD5A	PD4B	PD4A	PD3B	PD3A	PD2B	PD2A	PD1B	PD1A	PD0B	PD0A
Quad	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	—(1)	PD0B	PD0A	PD0B	PD0A	PD0B	PD0A	PD0B	PD0A
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad-channel device	= Octal-channel device		

Octal	Quad	
—	bit 15-8	**Unimplemented:** Read as '1'
bit 15-0	bit 7-0	**PDnB:PDnA:** DAC Power-Down Control(2) 11 = Powered down – V_{OUT} is open circuit 10 = Powered down – V_{OUT} is loaded with a 125 kΩ resistor to ground 01 = Powered down – V_{OUT} is loaded with a 1 kΩ resistor to ground 00 = Normal operation (not powered down)

Note 1: Unimplemented bit, read as '0'.

2: See Table 5-4 for more details.

Register 4-4 shows the format of the volatile Gain Control and System Status register. Each DAC has one bit to control the gain of the DAC and three status bits.

REGISTER 4-4: GAIN CONTROL AND SYSTEM STATUS REGISTER (ADDRESS 0Ah; VOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/C-1	R-0	U-0	U-0	U-0	U-0	U-0	U-0
Octal	G7	G6	G5	G4	G3	G2	G1	G0	POR	EEWA	—	—	—	—	—	—
Quad	—(1)	—(1)	—(1)	—(1)	G3	G2	G1	G0	POR	EEWA	—	—	—	—	—	—
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad-channel device	= Octal-channel device		

Octal	Quad	
—	bit 15-12	**Unimplemented:** Read as '0'
bit 15-8	bit 11-8	**Gn:** DAC Channel n Output Driver Gain Control 1 = 2x gain 0 = 1x gain
bit 7	bit 7	**POR:** Power-on Reset (Brown-out Reset) Status bit This bit indicates if a POR or BOR event has occurred since the last READ command of this register. Reading this register clears the state of the POR status bit. 1 = A POR (BOR) event has occurred since the last read of this register; reading this register clears this bit 0 = A POR (BOR) event has not occurred since the last read of this register
bit 6	bit 6	**EEWA:** EEPROM Write Active Status This bit indicates if the EEPROM write cycle is occurring. 1 = An EEPROM write cycle is currently occurring; only serial commands to the volatile memory are allowed 0 = An EEPROM write cycle is NOT currently occurring
bit 5-0	bit 5-0	**Unimplemented:** Read as '0'

Note 1: Unimplemented bit, read as '0'.

Register 4-5 shows the format of the nonvolatile Gain Control register. Each DAC has one bit to control the gain of the DAC.

REGISTER 4-5: GAIN CONTROL REGISTER (ADDRESS 1Ah; NONVOLATILE)

	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
Octal	G7	G6	G5	G4	G3	G2	G1	G0	—	—	—	—	—	—	—	—
Quad	—(1)	—(1)	—(1)	—(1)	G3	G2	G1	G0	—	—	—	—	—	—	—	—
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad-channel device	= Octal-channel device		

Octal	**Quad**	
—	bit 15-12	**Unimplemented:** Read as '0'
bit 15-8	bit 11-8	**Gn:** DACn Output Driver Gain Control bits 1 = 2x gain 0 = 1x gain
bit 7-0	bit 7-0	Unimplemented bits.

Note 1: Unimplemented bit, read as '0'.

Register 4-6 shows the format of the DAC WiperLock Technology Status register.

REGISTER 4-6: DAC WiperLock™ TECHNOLOGY STATUS REGISTER (ADDRESS 0Bh; VOLATILE)

	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)	R-0(1)
Octal	WL7B	WL7A	WL6B	WL6A	WL5B	WL5A	WL4B	WL4A	WL3B	WL3A	WL2B	WL2A	WL1B	WL1A	WL0B	WL0A
Quad	—(2)	—(2)	—(2)	—(2)	—(2)	—(2)	—(2)	—(2)	WL3B	WL3A	WL2B	WL2A	WL1B	WL1A	WL0B	WL0A
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
= Quad-channel device	= Octal-channel device		

Octal	Quad	
—	bit 15-8	**Unimplemented:** Read as '0'
bit 15-0	bit 7-0	**WLnB:WLnA:** WiperLock™ Technology Status These bits reflect the state of the DLn:CLn nonvolatile Configuration bits. 11 = DAC Wiper and DAC Configuration (volatile and nonvolatile registers) are locked (DLn = CLn = Enabled) 10 = DAC Wiper (volatile and nonvolatile) and DAC Configuration (nonvolatile registers) are locked (DLn = Enabled; CLn = Disabled) 01 = DAC Wiper (nonvolatile) and DAC Configuration (nonvolatile registers) are locked (DLn = Disabled; CLn = Enabled) 00 = DAC Wiper and DAC Configuration are unlocked (DLn = CLn = Disabled)

Note 1: POR value depends on the programmed values of the DLn:CLn Configuration bits. The devices are shipped with a default DLn:CLn Configuration bit state of '0'.

2: Unimplemented bit, read as '0'.

NOTES:

5.0 DAC CIRCUITRY

The Digital-to-Analog Converter circuitry converts a digital value into its analog representation. The description shows the functional operation of the device.

The DAC circuit uses a resistor ladder implementation. Devices have up to eight DACs.

Figure 5-1 shows the functional block diagram for the MCP48FXBX4/8 DAC circuitry.

The functional blocks of the DAC include:

- **Resistor Ladder**
- **Voltage Reference Selection**
- **Output Buffer/V_{OUT} Operation**
- **Internal Band Gap**
- **Latch Pins (LATn)**
- **Power-Down Operation**

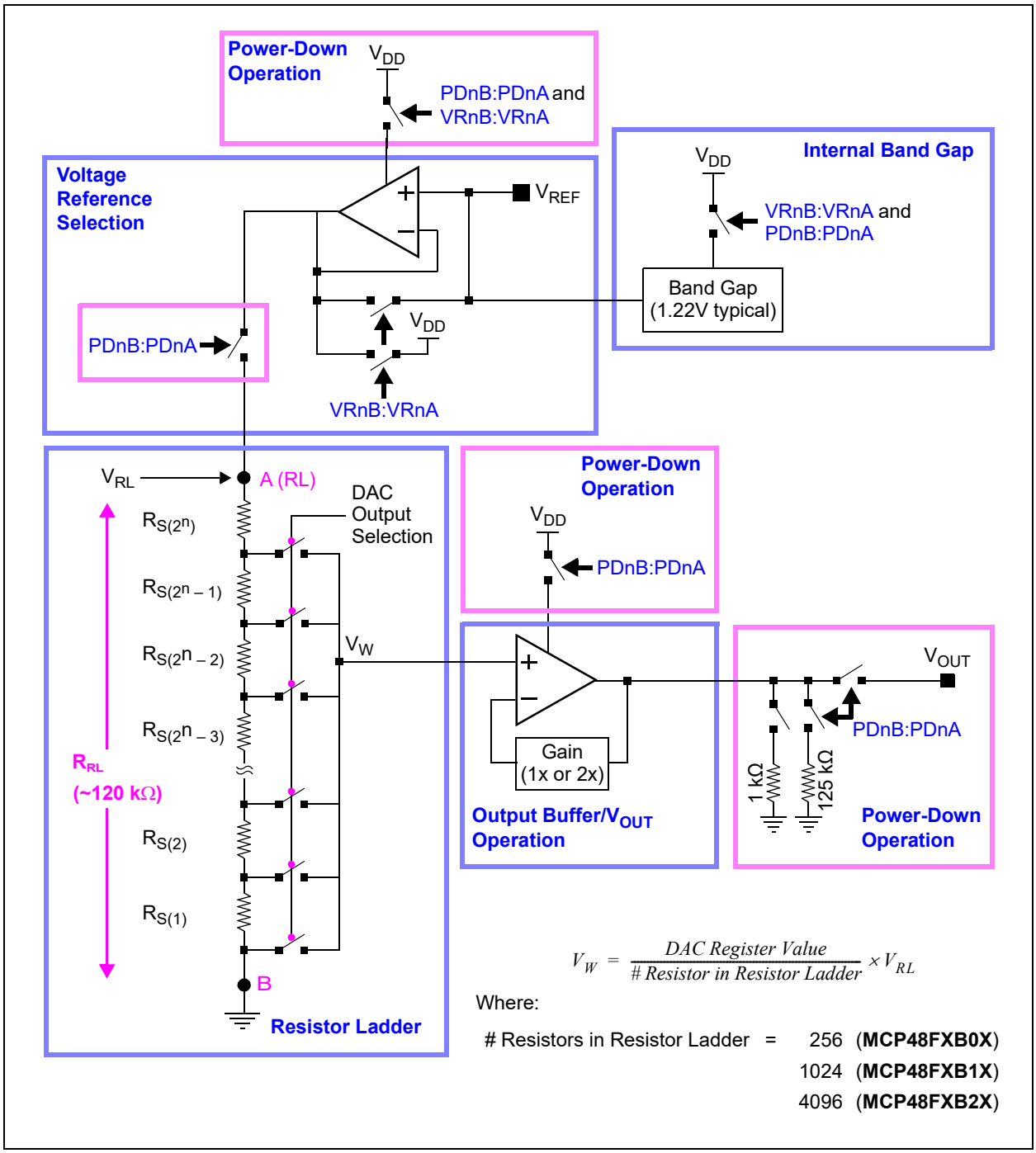
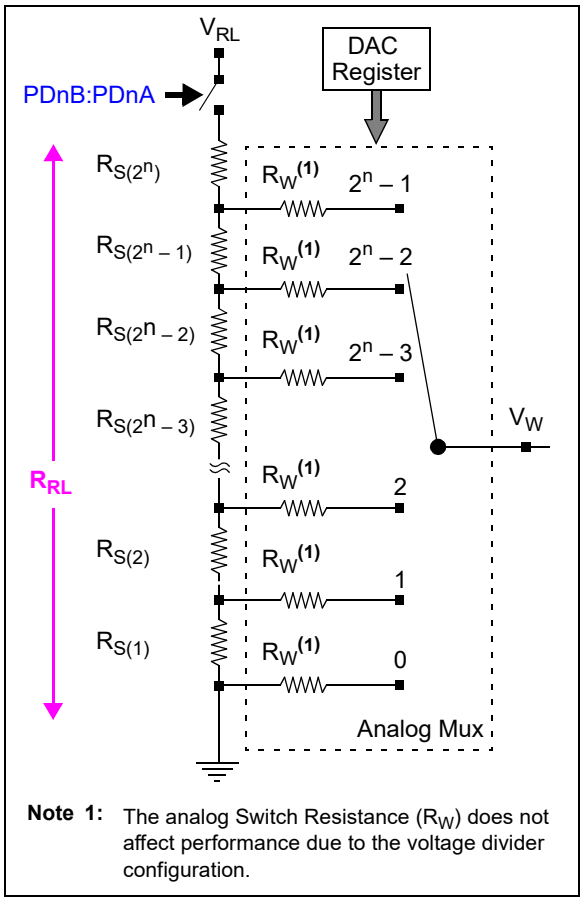


FIGURE 5-1: *MCP48FXBX4/8 DAC Module Block Diagram.*

5.1 Resistor Ladder

The resistor ladder is a digital potentiometer with the B Terminal internally grounded and the A Terminal connected to the selected reference voltage (see Figure 5-2). The volatile DAC register controls the wiper position. The Wiper Voltage (V_W) is proportional to the DAC register value divided by the number of Resistor Elements (R_S) in the ladder (256, 1024 or 4096) related to the V_{RL} voltage.

The output of the resistor network will drive the input of an output buffer.



Note 1: The analog Switch Resistance (R_W) does not affect performance due to the voltage divider configuration.

FIGURE 5-2: *Resistor Ladder Model.*

The resistor network is made of these three parts:

- Resistor ladder (string of R_S elements)
- Wiper switches
- DAC register decode

The Resistor Ladder (R_{RL}) has a typical impedance of approximately 120 kΩ. This resistance may vary from device to device by up to ±20%. Since this is a voltage divider configuration, the actual R_{RL} resistance does not affect the output given a fixed voltage at V_{RL}.

Equation 5-1 shows the calculation for the step resistance:

EQUATION 5-1: R_S CALCULATION

$$R_S = \frac{R_{RL}}{(256)} \quad \text{8-Bit Device}$$

$$R_S = \frac{R_{RL}}{(1024)} \quad \text{10-Bit Device}$$

$$R_S = \frac{R_{RL}}{(4096)} \quad \text{12-Bit Device}$$

Note: The maximum wiper position is $2^n - 1$, while the number of resistors in the resistor ladder is 2^n. This means that when the DAC register is at full scale, there is one Resistor Element (R_S) between the wiper and the V_{RL} voltage.

If the unbuffered V_{REF} pin is used as the V_{RL} voltage source, this voltage source should have a low output impedance.

When the DAC is powered down, the resistor ladder is disconnected from the selected reference voltage.

5.2 Voltage Reference Selection

The resistor ladder has up to four sources for the reference voltage. Two user control bits (VRnB:VRnA) are used to control the selection with the selection connected to the V_{RL} node (see Figure 5-3 and Figure 5-4).

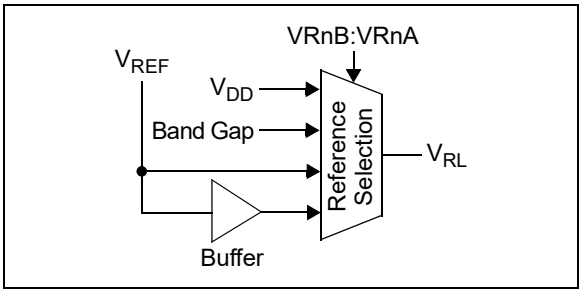


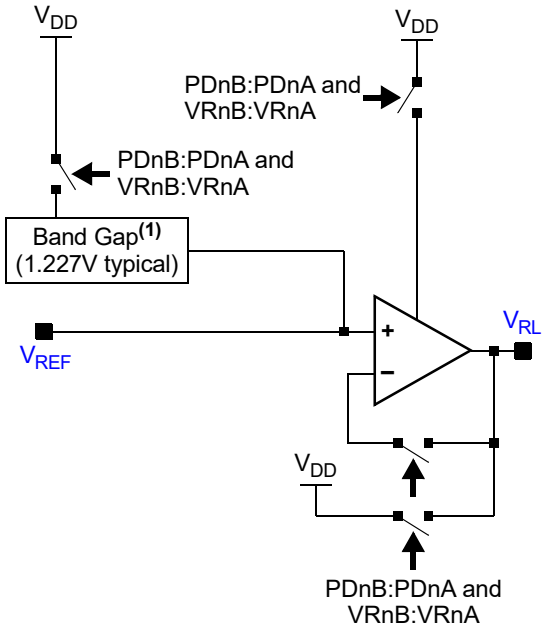
FIGURE 5-3: *Resistor Ladder Reference Voltage Selection Block Diagram.*

The four voltage source options for the resistor ladder are:

1. V_{DD} pin voltage.
2. Internal Voltage Reference (V_{BG}).
3. V_{REF} pin voltage unbuffered.
4. V_{REF} pin voltage internally buffered.

The selection of the voltage is specified with the volatile VRnB:VRnA Configuration bits (see Register 4-2). There are nonvolatile and volatile VRnB:VRnA Configuration bits. On a POR/BOR event, the state of the nonvolatile VRnB:VRnA Configuration bits is latched into the volatile VRnB:VRnA Configuration bits.

When the user selects the V_{DD} as reference, the V_{REF} pin voltage is not connected to the resistor ladder.



Note 1: The Band Gap Voltage (V_{BG}) is 1.22V typical. The band gap output goes through the buffer with a 2x gain to create the V_{RL} voltage. See Table 5-1 for additional information on the band gap circuit.

FIGURE 5-4: *Reference Voltage Selection Implementation Block Diagram.*

If the V_{REF} pin is selected, then a selection has to be made between the Buffered and Unbuffered mode.

5.2.1 BUFFERED MODE

The V_{REF} pin voltage may be from 0.01V to V_{DD} – 0.04V. The input buffer (amplifier) provides low offset voltage, low noise and a very high input impedance, with only minor limitations on the input range and frequency response.

Note 1: Any variation or noises on the reference source can directly affect the DAC output. The reference voltage needs to be as clean as possible for accurate DAC performance.

2: If the V_{REF} pin is tied to the V_{DD} voltage, the V_{DD} mode (VRnB:VRnA = 00) is recommended.

5.2.2 UNBUFFERED MODE

The V_{REF} pin voltage may be from V_{SS} to V_{DD}.

Note 1: The voltage source should have a low output impedance. If the voltage source has a high output impedance, then the voltage on the V_{REF} pin is lower than expected. The resistor ladder has a typical impedance of 140 kΩ and a typical capacitance of 29 pF.

2: If the V_{REF} pin is tied to the V_{DD} voltage, the V_{DD} mode (VRnB:VRnA = 00) is recommended.

5.2.3 BAND GAP MODE

If the internal band gap is selected, then the external V_{REF} pin should not be driven and should only use high-impedance loads.

The band gap output is buffered, but the internal switches limit the current that the output should source to the V_{REF} pin. The resistor ladder buffer is used to drive the band gap voltage for the cases of multiple DAC outputs. This ensures that the resistor ladders are always properly sourced when the band gap is selected.

5.3 Internal Band Gap

The internal band gap is designed to drive the resistor ladder buffer.

The resistance of a Resistor Ladder (R_{RL}) is targeted to be 140 kΩ (±40 kΩ), which means a minimum resistance of 100 kΩ.

The band gap selection can be used across the V_{DD} voltages while maximizing the V_{OUT} voltage ranges. For V_{DD} voltages below the 2 × Gain × V_{BG} voltage, the output for the upper codes will be clipped to the V_{DD} voltage. Table 5-1 shows the maximum DAC register code given device V_{DD} and Gain bit setting.

TABLE 5-1: V_{OUT} USING BAND GAP

V_{DD}(3)	DAC Gain	Max DAC Code(1)			Comment
		12-Bit	10-Bit	8-Bit	
5.5	1	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 2.44V(2)
	2	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 4.88V(2)
2.7	1	FFFh	3FFh	FFh	$V_{OUT(max)}$ = 2.44V(2)
	2	8CDh	233h	8Ch	~ 0 to 56% range

Note 1: Without the V_{OUT} pin voltage being clipped.

2: When V_{BG} = 1.22V typical.

3: Band gap performance achieves full performance starting from a V_{DD} of 2.0V.

5.4 Output Buffer/V_{OUT} Operation

The output driver buffers the Wiper Voltage (V_W) of the resistor ladder.

The DAC output is buffered with a low-power and precision output amplifier (op amp). This amplifier provides a rail-to-rail output with low offset voltage and low noise. The amplifier's output can drive the resistive and high capacitive loads without oscillation. The amplifier provides a maximum load current, which is enough for most programmable voltage reference applications. See **Section 1.0 "Electrical Characteristics"** for the specifications of the output amplifier.

Note:	The load resistance must be kept higher than 5 kΩ for the stable and expected analog output (to meet electrical specifications).

Figure 5-5 shows the block diagram of the output driver circuit.

The user can select the output gain of the output amplifier. The gain options are:

a) Gain of 1, when either the V_{DD}, External V_{REF} or Band Gap mode are used. In case of the Band Gap mode, the effective gain is 2; see **Section 5.3 "Internal Band Gap"**.

b) Gain of 2, when the External V_{REF} or Internal Band Gap modes are used. In case of the Band Gap mode, the effective gain is 4; see **Section 5.3 "Internal Band Gap"**.

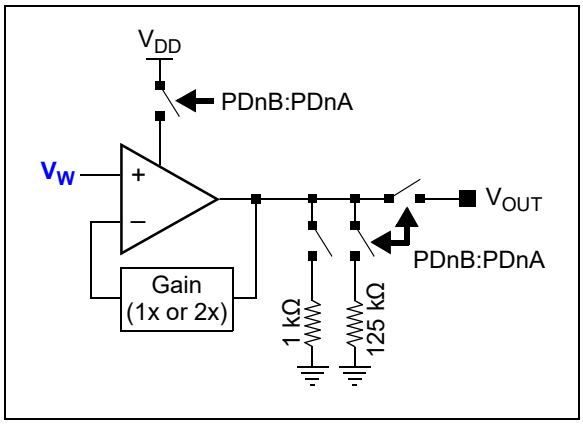


FIGURE 5-5: *Output Driver Block Diagram.*

5.4.1 PROGRAMMABLE GAIN

The amplifier's gain is controlled by the Gain (G) Configuration bit (see Register 4-5) and the V_{RL} reference selection.

The volatile Gain bit value can be modified by:

- POR events
- BOR events
- SPI `WRITE` commands

5.4.2 OUTPUT VOLTAGE

The volatile DAC register values, along with the device's Configuration bits, control the analog V_{OUT} voltage. The volatile DAC register's value is unsigned binary. The formula for the output voltage is given in Equation 5-2. Table 5-5 shows examples of volatile DAC register values and the corresponding theoretical V_{OUT} voltage for the MCP48FXBX4/8 devices.

EQUATION 5-2: CALCULATING OUTPUT VOLTAGE (V_{OUT})

$$V_{OUT} = \frac{V_{RL} \times DAC\ Register\ Value}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

Resistors in R-Ladder = 4096 **(MCP48FXB2X)**
1024 **(MCP48FXB1X)**
256 **(MCP48FXB0X)**

Note:	When Gain = 2 (V_{RL}= V_{REF}) and if V_{REF} > V_{DD}/2, the V_{OUT} voltage will be limited to V_{DD}. So if V_{REF} = V_{DD}, then the V_{OUT} voltage will not change for volatile DAC register values midscale and greater, since the op amp is at full-scale output.

The following events update the DAC register value, and therefore, the analog Voltage Output (V_{OUT}):

- POR
- BOR
- `WRITE` command

The V_{OUT} voltage starts driving to the new value after the event has occurred.

5.4.3 STEP VOLTAGE (V_S)

The step voltage depends on the device resolution and the calculated output voltage range. One LSb is defined as the ideal voltage difference between two successive codes. The step voltage can be easily calculated by using Equation 5-3 (DAC register value is equal to 1). Theoretical step voltages are shown in Table 5-2 for several V_{REF} voltages.

EQUATION 5-3: V_S CALCULATION

$$V_S = \frac{V_{RL}}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

Resistors in R-Ladder = 4096 **(12-bit)**
1024 **(10-bit)**
256 **(8-bit)**

TABLE 5-2: THEORETICAL STEP VOLTAGE (V_S)(1)

	V_{REF}					
	5.0	**2.7**	**1.8**	**1.5**	**1.0**	
V_S	1.22 mV	659 µV	439 µV	366 µV	244 µV	12-bit
	4.88 mV	2.64 mV	1.76 mV	1.46 mV	977 µV	10-bit
	19.5 mV	10.5 mV	7.03 mV	5.86 mV	3.91 mV	8-bit

Note 1: When Gain = 1x, $V_{FS} = V_{RL}$ and $V_{ZS} = 0V$.

5.4.4 OUTPUT SLEW RATE

Figure 5-6 shows an example of the slew rate for the V_{OUT} pin. The slew rate can be affected by the characteristics of the circuit connected to the V_{OUT} pin.

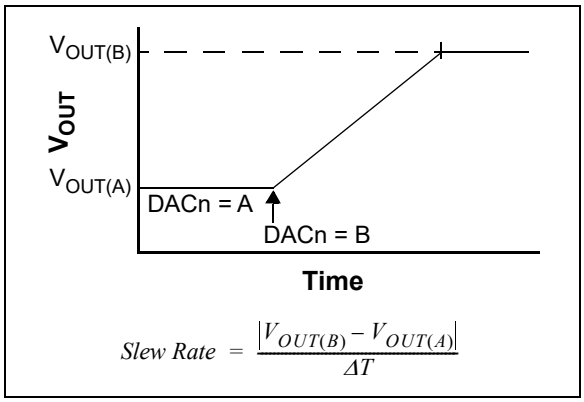


FIGURE 5-6: *V_{OUT} Pin Slew Rate.*

5.4.4.1 Small Capacitive Load

With a small Capacitive Load (C_L), the output buffer's current is not affected, but the V_{OUT} pin's voltage is not a step transition from one output value (DAC register value) to the next output value. The change of the V_{OUT} voltage is limited by the output buffer's characteristics, so the V_{OUT} pin voltage will have a slope from the old voltage to the new one. This slope is fixed for the output buffer and is referred to as the Buffer Slew Rate (SR_{BUF}).

5.4.4.2 Large Capacitive Load

With a larger capacitive load, the slew rate is determined by two factors:

- The output buffer's Short-Circuit Current (I_{SC})
- The V_{OUT} pin's external load

I_{OUT} cannot exceed the output buffer's Short-Circuit Current (I_{SC}), which fixes the output Buffer Slew Rate (SR_{BUF}). The voltage on the Capacitive Load, V_{CL}, changes at a rate proportional to I_{OUT}, which fixes a Capacitive Load Slew Rate (SR_{CL}).

The V_{CL} voltage slew rate is limited to the slower of the output buffer's internally set Slew Rate (SRBUF) and the Capacitive Load Slew Rate (SR_{CL}).

5.4.5 DRIVING RESISTIVE AND CAPACITIVE LOADS

The V_{OUT} pin can drive up to 100 pF of capacitive load in parallel with a 5 kΩ resistive load (to meet electrical specifications).

V_{OUT} drops slowly as the load resistance decreases after about 3.5 kΩ. It is recommended to use a load with R_L greater than 5 kΩ.

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response with overshoot and ringing in the step response. That is, since the V_{OUT} pin's voltage does not quickly follow the buffer's input voltage (due to the large capacitive load), the output buffer will overshoot the desired target voltage. Once the driver detects this overshoot, it compensates by forcing it to a voltage below the target. This causes voltage ringing on the V_{OUT} pin.

When driving large capacitive loads with the output buffer, a small Series Resistor (R_{ISO}) at the output (see Figure 5-7) improves the output buffer's stability (feedback loop's phase margin) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

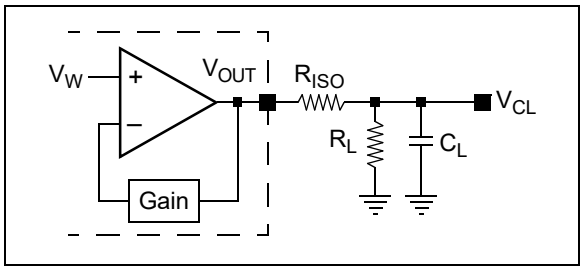


FIGURE 5-7: *Circuit to Stabilize the Output Buffer for Large Capacitive Loads (C_L).*

The R_{ISO} resistor value for your circuit needs to be selected. The resulting frequency response peaking and step response overshoot for this R_{ISO} resistor value should be verified on the bench. Modify the R_{ISO}'s resistance value until the output characteristics meet your requirements.

A method to evaluate the system's performance is to inject a step voltage on the V_{REF} pin and observe the V_{OUT} pin's characteristics.

Note: Additional insight into circuit design for driving capacitive loads can be found in AN884, *"Driving Capacitive Loads with Op Amps"* (DS00884).

5.5 Power-Down Operation

To allow the application to conserve power when the DAC operation is not required, three Power-Down modes are available. The Power-Down configuration bits (PDnB:PDnA) control the power-down operation (Figure 5-8 and Table 5-3). On devices with multiple DACs, each DACs Power-Down mode is individually controllable. All Power-Down modes do the following:

- Turn off most DAC module's internal circuits (output op amp, resistor ladder, etc.)
- Op amp output becomes high-impedance to the V_{OUT} pin
- Disconnect the resistor ladder from the Reference Voltage (V_{RL})
- Retain the value of the volatile DAC register and Configuration bits and the nonvolatile (EEPROM) DAC register and Configuration bits

Depending on the selected Power-Down mode, the following will occur:

- V_{OUT} pin is switched to one of the two resistive pull-downs (see Table 5-4):
  - 125 kΩ (typical)
  - 1 kΩ (typical)
- Op amp is powered down and the V_{OUT} pin becomes high-impedance

There is a delay (T_{PDE}) between the PDnB:PDnA bits, changing from '00' to either '01', '10' or '11', with the op amp no longer driving the V_{OUT} output and the pull-down resistors sinking current.

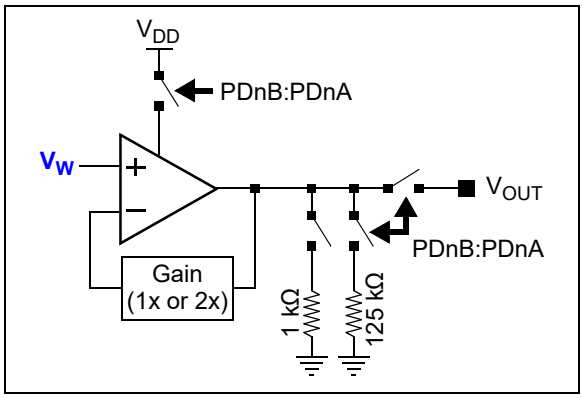


FIGURE 5-8: *V_{OUT} Power-Down Block Diagram.*

In any of the Power-Down modes where the V_{OUT} pin is not externally connected (sinking or sourcing current), the power-down current will typically be 680 nA for a quad DAC device. As the number of DACs increases, the device's power-down current will also increase.

The Power-Down bits are modified by using a WRITE command to the volatile Power-Down register or a POR event which transfers the nonvolatile Power-Down register to the volatile Power-Down register.

TABLE 5-3: POWER-DOWN BITS AND OUTPUT RESISTIVE LOAD

PDnB	PDnA	Function
0	0	Normal operation
0	1	1 kΩ resistor to ground
1	0	125 kΩ resistor to ground
1	1	Open circuit

Table 5-4 shows the current sources for the DAC based on the selected source of the DAC's reference voltage and if the device is in a normal operating mode or in one of the Power-Down modes.

TABLE 5-4: DAC CURRENT SOURCES

Device V_{DD} Current Source	PDnB:A = 00, VRnB:A =				PDnB:A ≠ 00, VRnB:A =			
	00	01	10	11	00	01	10	11
Output Op Amp	Y	Y	Y	Y	N	N	N	N
Resistor Ladder	Y	Y	N(1)	Y	N	N	N(1)	N
RL Op Amp	N	Y	N	Y	N	N	N	N
Band Gap	N	Y	N	N	N	Y	N	N

Note 1: Current is sourced from the V_{REF} pin, not the device V_{DD}.

Section 7.0 "SPI Device Commands" describes the SPI commands for writing the power-down bits. The command that can update the volatile PDnB:PDnA bits is a WRITE command (normal and high voltage).

Note: The SPI serial interface circuit is not affected by the Power-Down mode. This circuit remains active in order to receive any command that might come from the master device.

5.5.1 EXITING POWER-DOWN

When the device exits Power-Down mode, the following occurs:

- Disabled circuits (op amp, resistor ladder, etc.) are turned on
- The resistor ladder is connected to the selected Reference Voltage (V_{RL})
- The selected pull-down resistor is disconnected
- The V_{OUT} output will be driven to the voltage represented by the volatile DAC register's value and Configuration bits

The V_{OUT} output signal requires time as these circuits are powered up and the output voltage is driven to the specified value as determined by the volatile DAC register and Configuration bits.

Note:	Since the op amp and resistor ladder are powered off (0V), the op amp's Input Voltage (V_W) can be considered 0V. There is a delay (T_{PDD}) between the PDnB:PDnA bits updating to '00' and the op amp driving the V_{OUT} output. The op amp's settling time (from 0V) needs to be taken into account to ensure the V_{OUT} voltage reflects the selected value.

Any WRITE command where the PDnB:PDnA bits are '00' will cause the device to exit the Power-Down mode.

5.6 DAC Registers, Configuration Bits and Status Bits

The MCP48FXBX4/8 device family has both volatile and nonvolatile (EEPROM) memory options. Table 4-2 shows the volatile and nonvolatile memory, and their interaction due to a POR event.

There are five Configuration bits, DAC registers, and two volatile status bits in both the volatile and nonvolatile memory. The DAC registers (volatile and nonvolatile) will be either twelve bits (MCP48FXB2X), ten bits (MCP48FEB1X) or eight bits (MCP48FXB0X) wide.

When the device is first powered up, it automatically uploads the EEPROM memory values or factory default values (in case of MCP48FVBXX devices) to the volatile memory. The volatile memory determines the analog Output Voltage (V_{OUT}) pin. After the device is powered up, the user can update the memory.

This memory is read and written through the SPI interface. See **Section 6.0 "SPI Serial Interface Module"** and **Section 7.0 "SPI Device Commands"** for more details on reading and writing the device's memory.

When the nonvolatile memory is written, the device starts writing the EEPROM cell at the Acknowledge pulse of the WRITE single memory location command.

Register 4-4 shows the operation of the device status bits and Table 4-2 shows the factory default value of a POR/BOR event for the device Configuration bits.

There are two status bits. These are only in volatile memory and indicate the status of the device. The POR bit indicates if the device V_{DD} is above or below the POR trip point. During normal operation, this bit should be '1'. The EEWA bit indicates if an EEPROM write cycle is in progress. While the EEWA bit is '1' (during the EEPROM writing), all commands are ignored, except for the READ command.

5.7 Latch Pins ($\overline{\text{LATn}}$)

The Latch pins control when the volatile DAC register value is transferred to the DAC wiper. This is useful for applications that need to synchronize the wiper(s) updates to an external event, such as zero-crossing or updates to the other wipers on the device. The $\overline{\text{LAT}}$ pin functionality is asynchronous to the serial interface operation.

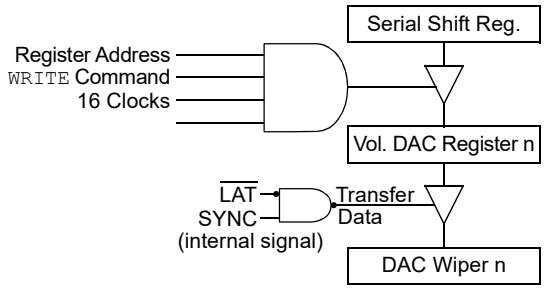
When the $\overline{\text{LAT}}$ pin is high, transfers from the volatile DAC register to the DAC wiper are inhibited. The volatile DAC register value(s) can continue to update.

When the $\overline{\text{LAT}}$ pin is low, the volatile DAC register value is transferred to the DAC wiper.

Note: This allows the volatile DAC0 through DAC7 registers to be updated while the $\overline{\text{LATn}}$ pins are high, and to have outputs synchronously updated as the $\overline{\text{LATn}}$ pins are driven low.

Figure 5-9 shows the interaction of the $\overline{\text{LAT}}$ pin and the loading of the DAC Wiper n (from the volatile DAC register n). The transfers are level-driven. If the $\overline{\text{LAT}}$ pin is held low, the corresponding DAC wiper is updated as soon as the volatile DAC register value is updated.

The $\overline{\text{LAT}}$ pin allows the DAC wiper to be updated to an external event and have multiple DAC channels/devices updating at a common event.



$\overline{\text{LAT}}$	SYNC	Transfer Data	Comment
1	1	0	No Transfer
1	0	0	No Transfer
0	1	1	Vol. DAC Register n → DAC Wiper n
0	0	0	No Transfer

FIGURE 5-9: *$\overline{\text{LAT}}$ and DAC Interaction.*

Since the DAC wiper n is updated from the volatile DAC register n, all DACs that are associated with a given $\overline{\text{LAT}}$ pin can be updated synchronously.

If the application does not require synchronization, then this signal should be tied low.

Figure 5-10 shows two examples of using the $\overline{\text{LAT}}$ pin to control when the Wiper register is updated relative to the value of a sine wave signal.

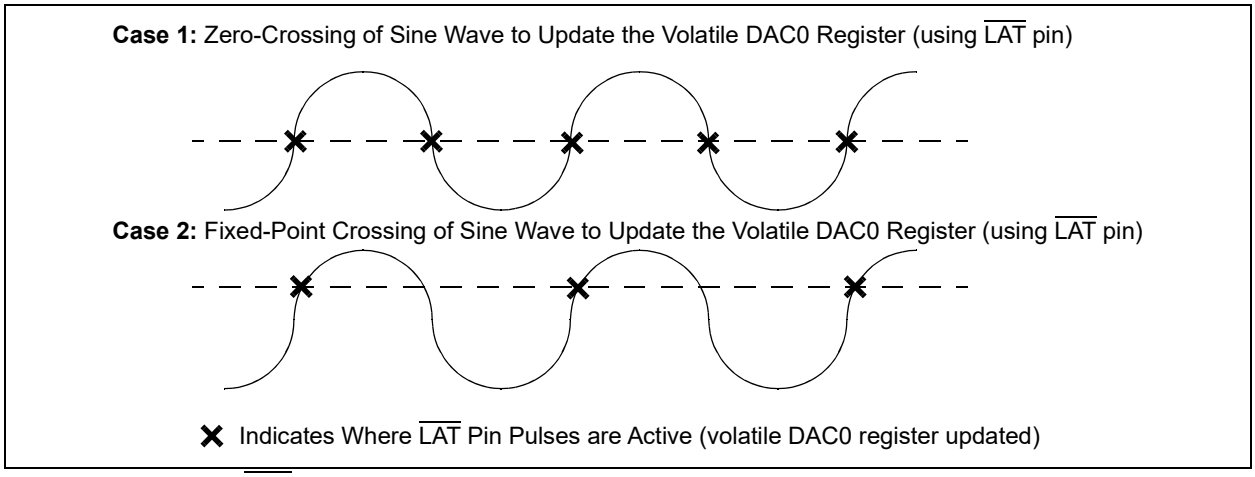


FIGURE 5-10: *$\overline{\text{LAT}}$ Pin Operation Example.*

TABLE 5-5: DAC INPUT CODE VS. CALCULATED ANALOG OUTPUT (V_{OUT}) (V_{DD} = 5.0V)

Device	Volatile DAC Register Value	V_{RL}[1]	LSb		Gain Selection[2]	V_{OUT}[3]	
			Equation	µV		Equation	V
MCP48FXB2X (12-bit)	1111 1111 1111	5.0V	5.0V/4096	1,220.7	1x	$V_{RL} * (4095/4096) * 1$	4.998779
		2.5V	2.5V/4096	610.4	1x	$V_{RL} * (4095/4096) * 1$	2.499390
					2x[2]	$V_{RL} * (4095/4096) * 2$)	4.998779
	0111 1111 1111	5.0V	5.0V/4096	1,220.7	1x	$V_{RL} * (2047/4096) * 1$)	2.498779
		2.5V	2.5V/4096	610.4	1x	$V_{RL} * (2047/4096) * 1$)	1.249390
					2x[2]	$V_{RL} * (2047/4096) * 2$)	2.498779
	0011 1111 1111	5.0V	5.0V/4096	1,220.7	1x	$V_{RL} * (1023/4096) * 1$)	1.248779
		2.5V	2.5V/4096	610.4	1x	$V_{RL} * (1023/4096) * 1$)	0.624390
					2x[2]	$V_{RL} * (1023/4096) * 2$)	1.248779
	0000 0000 0000	5.0V	5.0V/4096	1,220.7	1x	$V_{RL} * (0/4096) * 1$)	0
		2.5V	2.5V/4096	610.4	1x	$V_{RL} * (0/4096) * 1$)	0
					2x[2]	$V_{RL} * (0/4096) * 2$)	0
MCP48FEB1X (10-bit)	11 1111 1111	5.0V	5.0V/1024	4,882.8	1x	$V_{RL} * (1023/1024) * 1$	4.995117
		2.5V	2.5V/1024	2,441.4	1x	$V_{RL} * (1023/1024) * 1$	2.497559
					2x[2]	$V_{RL} * (1023/1024) * 2$	4.995117
	01 1111 1111	5.0V	5.0V/1024	4,882.8	1x	$V_{RL} * (511/1024) * 1$	2.495117
		2.5V	2.5V/1024	2,441.4	1x	$V_{RL} * (511/1024) * 1$	1.247559
					2x[2]	$V_{RL} * (511/1024) * 2$	2.495117
	00 1111 1111	5.0V	5.0V/1024	4,882.8	1x	$V_{RL} * (255/1024) * 1$	1.245117
		2.5V	2.5V/1024	2,441.4	1x	$V_{RL} * (255/1024) * 1$	0.622559
					2x[2]	$V_{RL} * (255/1024) * 2$	1.245117
	00 0000 0000	5.0V	5.0V/1024	4,882.8	1x	$V_{RL} * (0/1024) * 1$	0
		2.5V	2.5V/1024	2,441.4	1x	$V_{RL} * (0/1024) * 1$	0
					2x[2]	$V_{RL} * (0/1024) * 1$	0
MCP48FXB0X (8-bit)	1111 1111	5.0V	5.0V/256	19,531.3	1x	$V_{RL} * (255/256) * 1$	4.980469
		2.5V	2.5V/256	9,765.6	1x	$V_{RL} * (255/256) * 1$	2.490234
					2x[2]	$V_{RL} * (255/256) * 2$	4.980469
	0111 1111	5.0V	5.0V/256	19,531.3	1x	$V_{RL} * (127/256) * 1$	2.480469
		2.5V	2.5V/256	9,765.6	1x	$V_{RL} * (127/256) * 1$	1.240234
					2x[2]	$V_{RL} * (127/256) * 2$	2.480469
	0011 1111	5.0V	5.0V/256	19,531.3	1x	$V_{RL} * (63/256) * 1$	1.230469
		2.5V	2.5V/256	9,765.6	1x	$V_{RL} * (63/256) * 1$	0.615234
					2x[2]	$V_{RL} * (63/256) * 2$	1.230469
	0000 0000	5.0V	5.0V/256	19,531.3	1x	$V_{RL} * (0/256) * 1$	0
		2.5V	2.5V/256	9,765.6	1x	$V_{RL} * (0/256) * 1$	0
					2x[2]	$V_{RL} * (0/256) * 2$	0

Note 1: V_{RL} is the resistor ladder's reference voltage. It is independent of the VRnB:VRnA selection.

2: Gain selection of 2x (Gx = 1) requires the voltage reference source to come from the V_{REF} pin (VRnB:VRnA = 10 or 11) and requires a V_{REF} pin voltage (or V_{RL}) ≤ $V_{DD}/2$, or from the internal band gap (VRnB:VRnA = 01).

3: These theoretical calculations do not take into account the offset, gain and nonlinearity errors.

NOTES:

6.0 SPI SERIAL INTERFACE MODULE

The MCP48FXBX4/8 devices' SPI serial interface module supports the SPI serial protocol specification.

The command format and waveforms for the MCP48FXBX4/8 are defined in **Section 7.0 "SPI Device Commands"**.

6.1 Overview

This section discusses some of the specific characteristics of the MCP48FXBX4/8's serial interface module.

The following sections discuss some of these device-specific characteristics:

- **SPI Serial Interface**
- **Interface Pins (CS, SCK, SDI, SDO and LAT/HVC)**
- **Communication Data Rates**
- **POR/BOR**

6.2 SPI Serial Interface

The MCP48FXBX4/8 devices support the SPI serial protocol. This SPI operates in Slave mode (does not generate the serial clock).

The SPI interface uses up to four pins. These are:

- $\overline{CS}$ – Chip Select
- SCK – Serial Clock
- SDI – Serial Data In (MOSI)
- SDO – Serial Data Out (MISO)

Typical SPI interfaces are shown in Figure 6-1. In the SPI interface, the master's output pin is connected to the slave's input pin, and the master's input pin is connected to the slave's output pin.

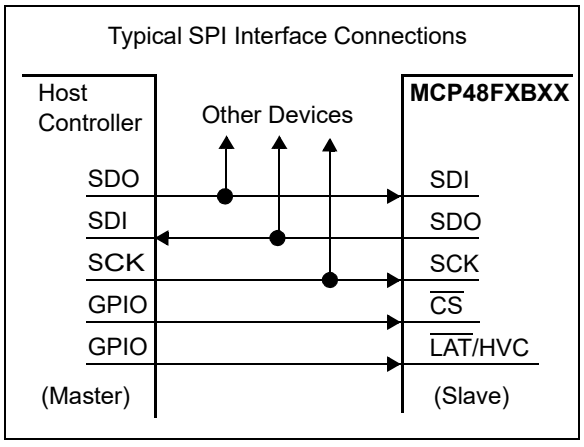


FIGURE 6-1: *Typical SPI Interface Block Diagram.*

The MCP48FXBX4/8 SPI's module supports two (of the four) standard SPI modes. These are Mode 0,0 and 1,1. The SPI mode is determined by the state of the SCK pin (V_{IH} or V_{IL}) when the $\overline{CS}$ pin transitions from inactive (V_{IH}) to active (V_{IL}).

An additional HVC pin is available for High-Voltage Command support. High-Voltage Commands allow the device to enable and disable nonvolatile Configuration bits. Without a high voltage present, those bits are inhibited from being modified.

The HVC pin is high-voltage tolerant. To enter a High-Voltage Command, the HVC pin must be greater than the V_{IHH} voltage.

6.2.1 SPI MODES

The SPI module supports two (of the four) standard SPI modes. These are Mode 0,0 and 1,1. The mode is determined by the state of the SDI pin on the rising edge of the first clock bit (of the 8-bit byte).

6.2.1.1 Mode 0,0

In Mode 0,0:

- SCK Idle state = low (V_{IL})
- Data are clocked in on the SDI pin on the rising edge of SCK
- Data are clocked out on the SDO pin on the falling edge of SCK

6.2.1.2 Mode 1,1

In Mode 1,1:

- SCK Idle state = high (V_{IH})
- Data are clocked in on the SDI pin on the rising edge of SCK
- Data are clocked out on the SDO pin on the falling edge of SCK

6.3 Interface Pins ($\overline{CS}$, SCK, SDI, SDO and LAT/HVC)

The operation of the five interface pins and the High-Voltage Command (HVC) pin is discussed in this section. The pins are:

- SDI (Serial Data In)
- SDO (Serial Data Out)
- SCK (Serial Clock)
- $\overline{CS}$ (Chip Select)
- $\overline{LAT}$/HVC (High-Voltage Command)

The serial interface works on either 8-bit or 24-bit boundaries depending on the selected command. The Chip Select ($\overline{CS}$) pin frames the SPI commands.

6.3.1 SERIAL DATA IN (SDI)

The Serial Data In (SDI) signal is the data signal into the device. The value on this pin is latched on the rising edge of the SCK signal.

6.3.2 SERIAL DATA OUT (SDO)

The Serial Data Out (SDO) signal is the data signal out of the device. The value on this pin is driven on the falling edge of the SCK signal.

Once the $\overline{CS}$ pin is forced to the active level (V_{IL} or V_{IHH}), the SDO pin will be driven. The state of the SDO pin is determined by the serial bit's position in the command, the command selected and if there is a Command Error (CMDERR) state.

6.3.3 SERIAL CLOCK (SCK) (SPI FREQUENCY OF OPERATION)

The SPI interface is specified to operate up to 20 MHz. The actual clock rate depends on the configuration of the system and the serial command used. Table 6-1 shows the SCK frequency for different configurations.

TABLE 6-1: SCK FREQUENCY

Memory Type Access		Command	
		Read	**Write, Enable, Disable**
Nonvolatile Memory	SDI, SDO	10 MHz	20 MHz(1,2)
Volatile Memory	SDI, SDO	10 MHz	20 MHz(2)

Note 1: After a `WRITE` command, the internal write cycle must be completed before the next SPI command is received.

2: This is a design goal. The SDO pin performance is believed to be the limiting factor.

6.3.4 $\overline{CS}$ SIGNAL

The Chip Select ($\overline{CS}$) signal is used to select the device and frame a command sequence. To start a command, or sequence of commands, the $\overline{CS}$ signal must transition from the Inactive state (V_{IH}) to an Active state (V_{IL} or V_{IHH}).

After the $\overline{CS}$ signal has gone active, the SDO pin is driven and the clock bit counter is reset.

Note: There is a required delay after the $\overline{CS}$ pin goes active to the first edge of the SCK pin.

If an error condition occurs for an SPI command, then the command byte's Command Error (CMDERR) bit (on the SDO pin) will be driven low (V_{IL}). To exit the error condition, the user must take the $\overline{CS}$ pin to the V_{IH} level.

When the $\overline{CS}$ pin returns to the Inactive state (V_{IH}), the SPI module resets (including the Address Pointer). While the $\overline{CS}$ pin is in the Inactive state (V_{IH}), the serial interface is ignored. This allows the host controller to interface to other SPI devices using the same SDI, SDO and SCK signals.

6.3.5 HVC SIGNAL

The high-voltage capability of the HVC pin allows High-Voltage Commands. High-Voltage Commands allow the device's WiperLock technology and write-protect features to be enabled and disabled.

6.4 Communication Data Rates

The MCP48FXBX4/8 devices support clock rates (bit rate) of up to 20 MHz for `WRITE` commands and 10 MHz for `READ` commands.

For most applications, the write time will be considered more important, since that is how the device operation is controlled.

6.5 POR/BOR

On a POR/BOR event, the SPI serial interface module state machine is reset, which means that the device's Memory Address Pointer is forced to 00h.

7.0 SPI DEVICE COMMANDS

The MCP48FXBX4/8 devices' SPI command format supports 32 memory address locations and four commands:

- WRITE command (C1:C0 = 00)
- READ command (C1:C0 = 11)
- Enable Configuration bit (high voltage, HVC = V_{IHH}):
  - Enable Configuration bit (C1:C0 = 10)
  - Disable Configuration bit (C1:C0 = 01)

The supported commands are shown in Table 7-1. These commands allow for both single data or continuous data operation. Table 7-2 also shows the required number of bit clocks for each command's different mode of operation.

Commands may have two modes. These are:

- Normal Serial Commands
- High-Voltage Serial Commands

Normal serial commands are those where the HVC pin is driven to either V_{IH} or V_{IL}. With high-voltage serial commands, the HVC pin is driven to V_{IHH}.

TABLE 7-1: COMMAND BITS OVERVIEW

C1:C0 Bit States	Command	# of Bits	Normal or HV
11	Read Data	24 Bits	Normal
00	Write Data	24 Bits	Normal
01	Enable(1)	8 Bits	HV Only
10	Disable(1)	8 Bits	HV Only

Note 1: High-voltage enable and disable commands on selected nonvolatile memory locations.

The 8-bit commands (see Figure 7-1) are used to modify the device Configuration bits (**Section 7.9 "Enable Configuration Bit (High Voltage)"** and **Section 7.10 "Disable Configuration Bit (High Voltage)"**) while the 24-bit commands (see Figure 7-2) are used to read and write to the device registers (**Section 7.8 "READ Command (Normal and High Voltage)"** and **Section 7.7 "WRITE Command (Normal and High Voltage)"**). These commands contain a command byte and two data bytes.

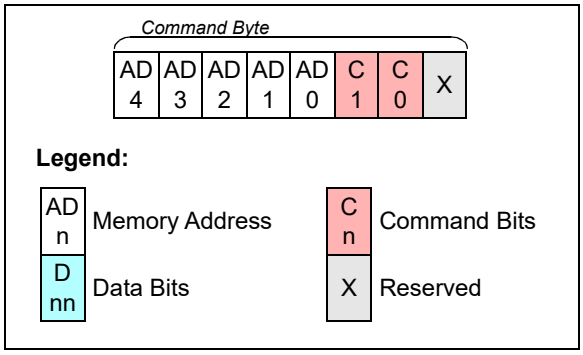


FIGURE 7-1: *8-Bit SPI Command Format.*

7.1 Command Byte

The command byte has three fields: the address, the command and one reserved bit (see Figure 7-1).

The device memory is accessed when the master sends a proper command byte to select the desired operation. The memory location getting accessed is contained in the command byte's AD4:AD0 bits. The action desired is contained in the command byte's C1:C0 bits; see Table 7-2. C1:C0 determines if the desired memory location will be read, written, enabled or disabled.

As the command byte is being loaded into the device (on the SDI pin), the device's SDO pin is driving. The SDO pin will output high bits for the first seven bits of that command. On the 8th bit, the SDO pin will output the CMDERR bit state (see **Section 7.6 "Error Condition"**).

7.2 Data Bytes

Data bytes are only present in the READ and WRITE commands. These commands concatenate the two data bytes, after the command byte, for a 24-bit long command (see Figure 7-2).

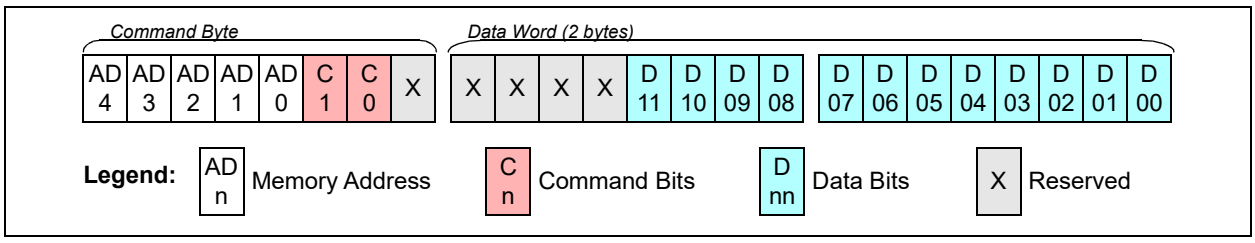


FIGURE 7-2: *24-Bit SPI Command Format.*

TABLE 7-2: SPI COMMANDS – OVERVIEW AND COMMAND RATE

Command					# of Bit Clocks[2]	Estimated Peak Command Rate (Commands/ms)[5]			Comments
Operation	Code		HV	Mode[1]		1 MHz	10 MHz	20 MHz	
	C1	C0							
WRITE Command	0	0	No[3]	Single	24	41	416	833	
	0	0	No[3]	Continuous	24 * n				
READ Command[4]	1	1	No[3]	Single	24				Read frequency can be up to 10 MHz
	1	1	No[3]	Continuous	24 * n				
Enable Configuration Bit (High Voltage)	1	0	Yes	Single	8	125	1250	2500	
	1	0	Yes	Continuous	8 * n				
Disable Configuration Bit (High Voltage)	0	1	Yes	Single	8				
	0	1	Yes	Continuous	8 * n				

Note 1: Nonvolatile registers can only use the Single mode.

2: "n" indicates the number of times the command operation is to be repeated.

3: If the state of the HVC pin is V_{IHH}, then the command is ignored, but a Command Error condition (CMDERR) will NOT be generated.

4: This command is used to determine when an EEPROM programming cycle is complete.

5: The actual voltage output update rate depends on several factors, such as output settling time, code, reference voltage or load impedance.

7.3 Continuous Commands

The devices support the ability to execute commands continuously. While the $\overline{CS}$ pin is in the Active state (V_{IL}), any sequence of valid commands may be received.

The following example is a valid sequence of events:

1. $\overline{CS}$ pin is driven active (V_{IL}).
2. READ command.
3. WRITE command (volatile memory).
4. WRITE command (nonvolatile memory).
5. $\overline{CS}$ pin is driven inactive (V_{IH}).

Note 1: It is recommended that while the $\overline{CS}$ pin is active, only one type of command should be issued. When changing commands, it is advisable to take the $\overline{CS}$ pin inactive, then force it back to the Active state.

2: Long command strings should be broken down into shorter command strings. This reduces the probability of noise on the SCK pin, corrupting the desired SPI command string.

7.4 Commands to Modify the Device Configuration Bits

The MCP48FXBX4/8 devices support two commands, which are used to program the device's Configuration bits. These commands require a High Voltage (V_{IHH}) on the HVC pin. The commands are:

- **Enable Configuration Bit (High Voltage)**
- **Disable Configuration Bit (High Voltage)**

The Configuration bits are used to inhibit the DAC values from inadvertent modification. High voltage is required to change the state of these bits if/when the DAC values need to be modified.

7.5 High-Voltage Command (HVC) Signal

The High-Voltage Command (HVC) signal is used to indicate that the command or sequence of commands are in the High-Voltage mode. Signals higher than V_{IHH} (~9.0V) on the $\overline{LAT}$/HVC pin puts the device into High-Voltage mode. High-voltage commands allow the device's WiperLock technology and write-protect features to be enabled and disabled.

Note 1: There is a required delay after the HVC pin is driven to the V_{IHH} level on the first edge of the SCK pin.

7.6 Error Condition

The Command Error (CMDERR) bit indicates if the five Address bits received (AD4:AD0) and the two Command bits received (C1:C0) are a valid combination (see Figures 7-1 and 7-2). The CMDERR bit is high if the combination is valid and low if the combination is invalid.

The Command Error bit will also be low if a write to a nonvolatile address has been specified and another SPI command occurs before the $\overline{CS}$ pin is driven inactive (V_{IH}).

SPI commands that do not have a multiple of eight clocks are ignored.

Once an error condition has occurred, any following commands are ignored. All following SDO bits will be low until the CMDERR condition is cleared by forcing the $\overline{CS}$ pin to the Inactive state (V_{IH}).

7.6.1 ABORTING A TRANSMISSION

All SPI transmissions must have the correct number of SCK pulses to be executed. The command is not executed until the complete number of clocks is received. Some commands also require the $\overline{CS}$ pin to be forced inactive (V_{IH}). If the $\overline{CS}$ pin is forced to the Inactive state (V_{IH}), the serial interface is reset. Partial commands are not executed.

SPI is more susceptible to noise than other bus protocols. The most likely case is that noise corrupts the value of the data being clocked into the MCP48FXBX4/8 or the SCK pin is injected with extra clock pulses. This may cause data to be corrupted in the device, or a Command Error to occur, since the address and command bits were not a valid combination. The extra SCK pulse will also cause the SPI data (SDI) and clock (SCK) to be out of sync. Forcing the $\overline{CS}$ pin to the Inactive state (V_{IH}) resets the serial interface. The SPI interface will ignore activity on the SDI and SCK pins until the $\overline{CS}$ pin transition to the Active state is detected (V_{IH} to V_{IL} or V_{IH} to V_{IHH}).

Note 1: When the MCP48FXBX4/8 devices do not receive data, it is recommended that the $\overline{CS}$ pin be forced to the Inactive Level (V_{IL}).

2: It is also recommended that long continuous command strings be broken down into single commands or shorter continuous command strings. This reduces the probability of noise on the SCK pin corrupting the desired SPI commands.

7.7 WRITE Command (Normal and High Voltage)

WRITE commands are used to transfer data to the desired memory location (from the host controller). The WRITE command can be issued to both the volatile and nonvolatile memory locations.

WRITE commands can be structured as either single or continuous.

The format of the command is shown in Figure 7-3 (single) and Figure 7-6 (continuous).

A WRITE command to a volatile memory location changes that location after a properly formatted WRITE command has been received.

A WRITE command to a nonvolatile memory location starts an EEPROM write cycle only after a properly formatted WRITE command has been received and the $\overline{CS}$ pin transitions to the Inactive state (V_{IH}).

Note 1: Writes to certain memory locations depend on the state of the WiperLock™ technology status bits.

2: During device communication, if an unimplemented address is specified, then the MCP48FXBX4/8 will generate a Command Error state. To reset the SPI state machine, the $\overline{CS}$ pin must transition to the Inactive state (V_{IH}).

7.7.1 SINGLE WRITE TO VOLATILE MEMORY

The write operation requires that the $\overline{CS}$ pin be in the Active state (V_{IL}). Typically, the $\overline{CS}$ pin will be in the Inactive state (V_{IH}) and it is driven to the Active state (V_{IL}). The 24-bit WRITE command (command byte and data bytes) is then clocked in on the SCK and SDI pins. Once all 24 bits have been received, the specified volatile address is updated. A write will not occur if the WRITE command is not exactly 24 clock pulses. This protects against system issues corrupting the nonvolatile memory locations.

Figures 7-4 and 7-5 show the waveforms for a single write (depending on the SPI mode).

7.7.2 SINGLE WRITE TO NONVOLATILE MEMORY

The sequence to write to a single nonvolatile memory location is the same as a single write to volatile memory, with the exception that after the $\overline{CS}$ pin is driven inactive (V_{IH}), the EEPROM Write Cycle (t_{WC}) is started. A write cycle will not start if the WRITE command is not exactly 24 clock pulses. This protects against system issues corrupting the nonvolatile memory locations.

Once a WRITE command to a nonvolatile memory location has been received, no other SPI commands should be received before the $\overline{CS}$ pin transitions to the Inactive state (V_{IH}) or the current SPI command will have a Command Error (CMDERR) occur.

After the $\overline{CS}$ pin is driven inactive (V_{IH}), the serial interface may immediately be re-enabled by driving the $\overline{CS}$ pin to the Active state (V_{IL}).

During an EEPROM write cycle, access to the volatile memory is allowed when using the appropriate command sequence. Commands that address nonvolatile memory are ignored until the EEPROM Write Cycle (t_{WC}) completes. This allows the host controller to operate on the volatile DAC registers.

Note:	The EEWA status bit indicates if an EEPROM write cycle is active (see Register 4-4).

7.7.3 CONTINUOUS WRITES TO VOLATILE MEMORY

A Continuous Write mode of operation is possible when writing to the device's volatile memory registers (see Table 7-3). Figure 7-6 shows the sequence for three continuous writes. The writes do not need to be to the same volatile memory address.

TABLE 7-3: VOLATILE MEMORY ADDRESSES

Address	Quad-Channel	Octal-Channel
00h-03h	Yes	Yes
04h-07h	**No**	Yes
08h	Yes	Yes
09h	Yes	Yes
0Ah	Yes	Yes

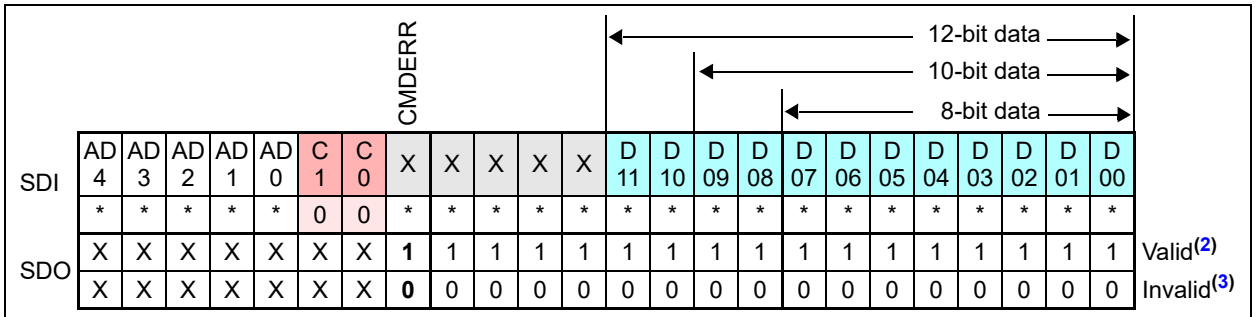
7.7.4 CONTINUOUS WRITES TO NONVOLATILE MEMORY

Continuous writes to nonvolatile memory are not allowed and attempts to do so will result in a Command Error (CMDERR) condition.

7.7.5 HIGH-VOLTAGE COMMAND (HVC) SIGNAL

The High-Voltage Command (HVC) signal is used to indicate that the command or sequence of commands are in the high-voltage operational state. HVC commands allow the device's WiperLock technology and write-protect features to be enabled and disabled.

Note:	Writes to a volatile DAC register will not transfer to the output register until the $\overline{LAT}$ (HVC) pin is transitioned from the V_{IHHEN} voltage to a V_{IL} voltage.

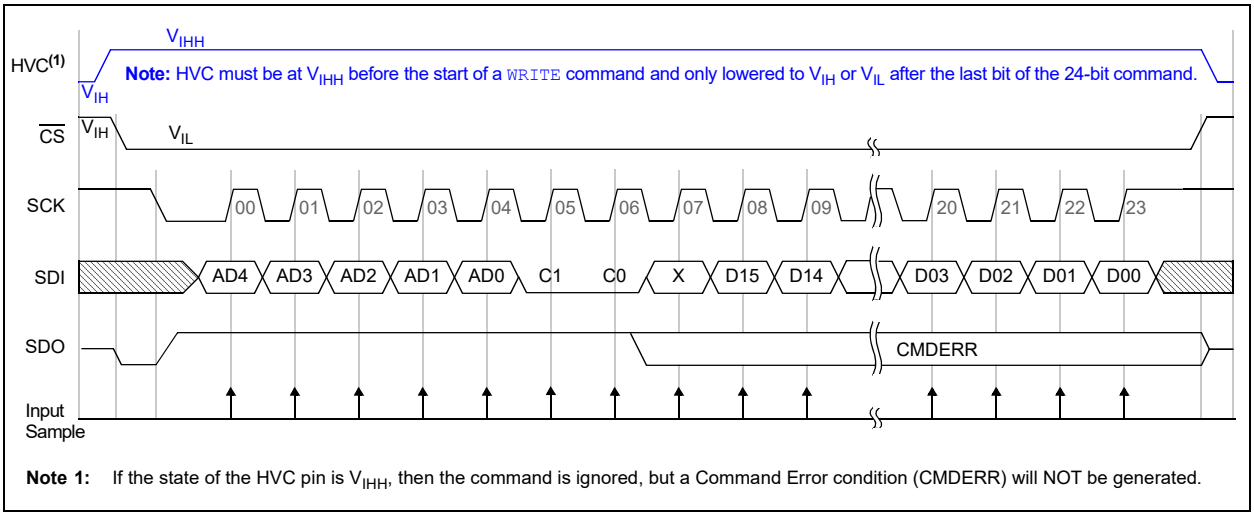


Note 1: For WRITE commands addressing the DAC Wiper registers, the data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00 and 8-bit = D07:D00. Data are right justified for easy host controller operation (no data manipulation before transmitting the desired value). The unimplemented bits are ignored.

2: After a valid memory address and WRITE command byte are received (CMDERR = 1), all the following SDO bits will be output as '1'.

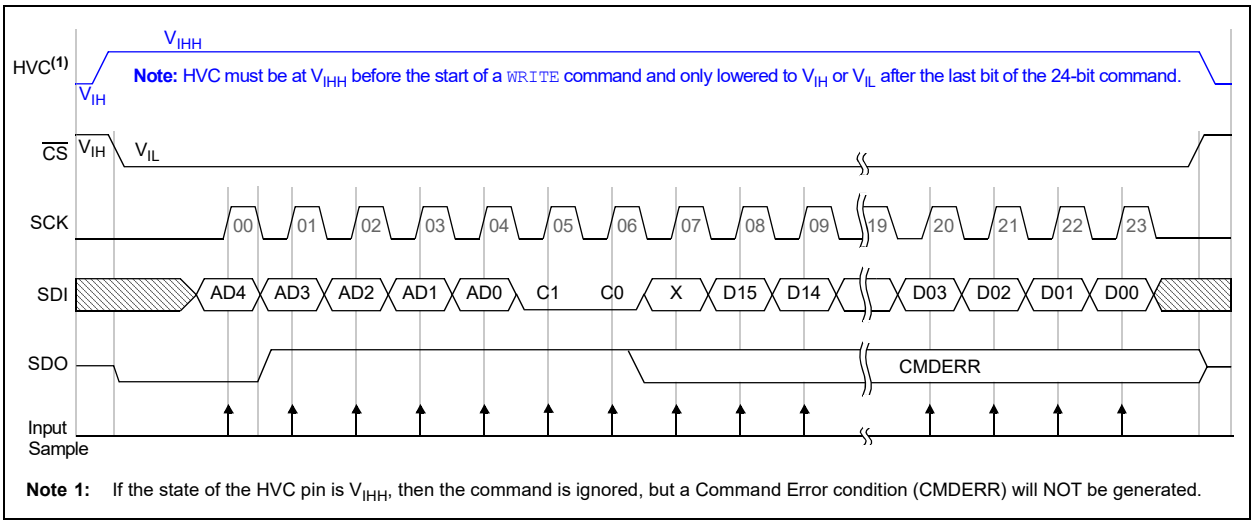
3: If an error condition occurs (CMDERR = 0), all the following SDO bits will be output as '0' until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the Inactive state).

FIGURE 7-3: *Write Single Memory Location Command – SDI and SDO States.*[1]



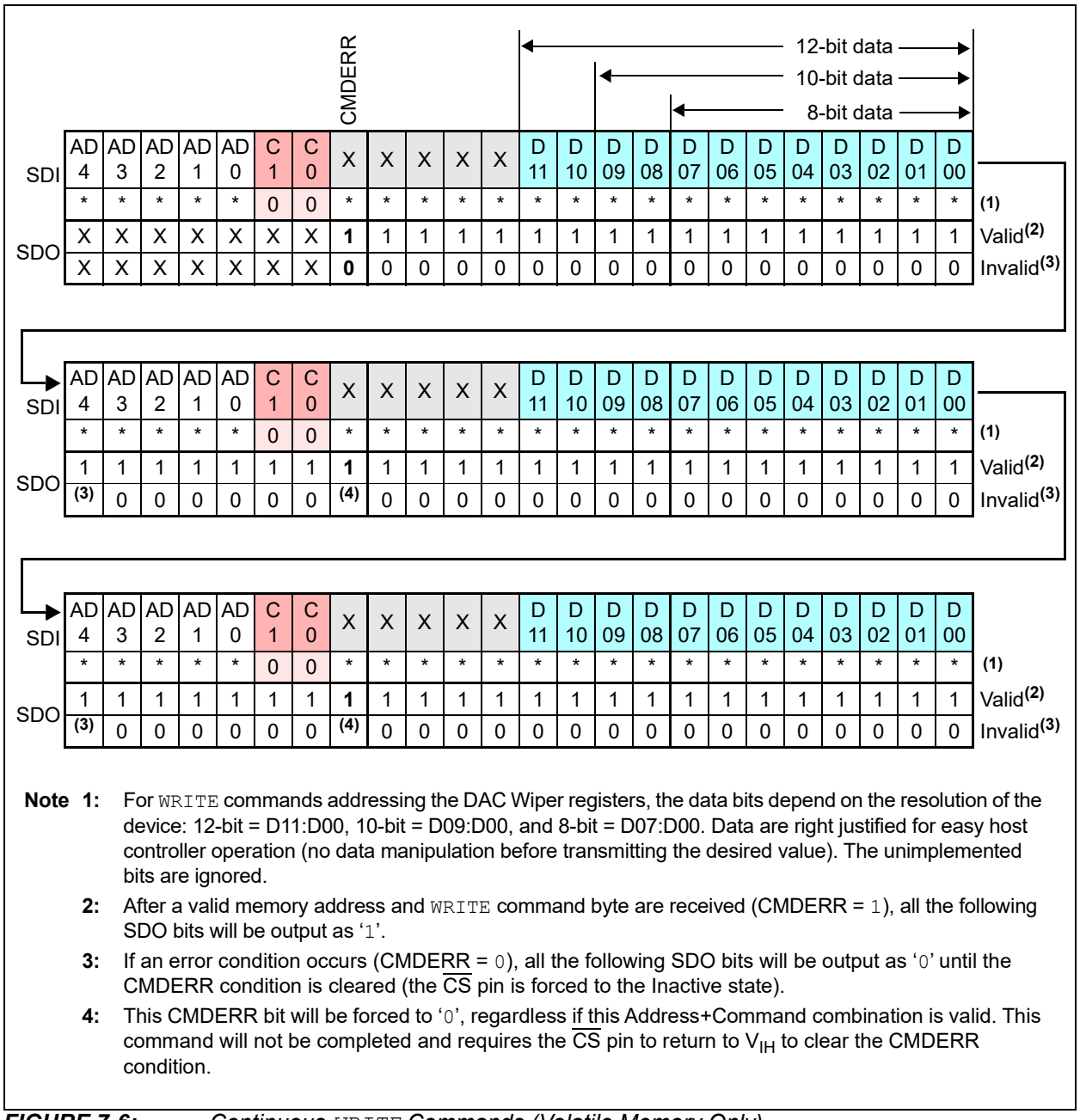
Note 1: If the state of the HVC pin is V_{IHH}, then the command is ignored, but a Command Error condition (CMDERR) will NOT be generated.

FIGURE 7-4: *24-Bit WRITE Command (C1:C0 = 00) – SPI Waveform (Mode 1,1).*



Note 1: If the state of the HVC pin is V_{IHH}, then the command is ignored, but a Command Error condition (CMDERR) will NOT be generated.

FIGURE 7-5: *24-Bit WRITE Command (C1:C0 = 00) – SPI Waveform (Mode 0,0).*



Note 1: For `WRITE` commands addressing the DAC Wiper registers, the data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00, and 8-bit = D07:D00. Data are right justified for easy host controller operation (no data manipulation before transmitting the desired value). The unimplemented bits are ignored.

2: After a valid memory address and `WRITE` command byte are received (CMDERR = `1`), all the following SDO bits will be output as '`1`'.

3: If an error condition occurs (CMDERR = `0`), all the following SDO bits will be output as '`0`' until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the Inactive state).

4: This CMDERR bit will be forced to '`0`', regardless if this Address+Command combination is valid. This command will not be completed and requires the $\overline{CS}$ pin to return to V_{IH} to clear the CMDERR condition.

FIGURE 7-6: *Continuous `WRITE` Commands (Volatile Memory Only).*

7.8 READ Command (Normal and High Voltage)

The READ command is a 24-bit command and is used to transfer data from the specified memory location to the host controller. The READ command can be issued to both the volatile and nonvolatile memory locations. The format of the command, as well as an example of SDI and SDO data, are shown in Figure 7-7.

The first seven bits of the READ command determine the address and the command. The 8th clock will output the CMDERR bit on the SDO pin. By means of the remaining 16 clocks, the device will transmit the data bits of the specified address (AD4:AD0).

During an EEPROM write cycle (write to nonvolatile memory location or enable/disable Configuration bit command), the READ command can only read the volatile memory locations. By reading the Status register (0Ah), the host controller can determine when the write cycle has been completed (via the state of the EEWA bit).

Note 1: During device communication, if an unimplemented address is specified, then the MCP48FXBX4/8 will command error that byte. To reset the SPI state machine, the $\overline{CS}$ pin must be driven to the V_{IH} state.

2: If the $\overline{LAT}$ pin is high (V_{IH}), reads of the volatile DAC register read the output value, not the internal register.

3: The READ commands operate the same regardless of the state of the High-Voltage Command (HVC) signal.

The READ command formats include:

- **Single Read**
- **Continuous Reads**

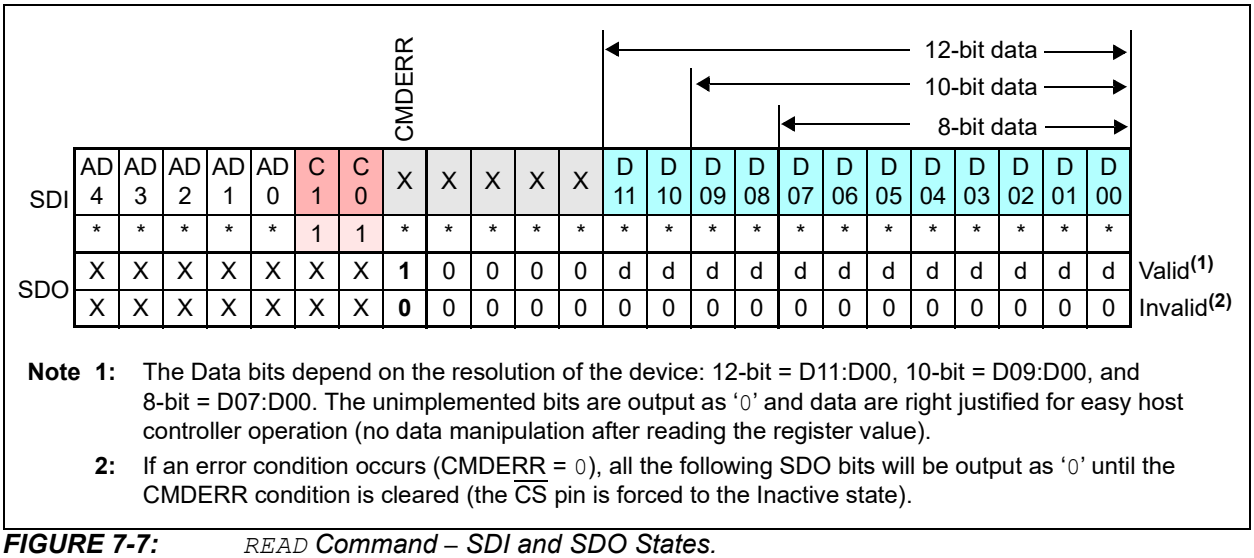
7.8.1 $\overline{LAT}$ PIN INTERACTION

During a READ command of the DACn registers, if the $\overline{LAT}$ pin transitions from V_{IH} to V_{IL}, then the read data may be corrupted. This is due to the fact that the data being read are the output value and not the DAC register value. The $\overline{LAT}$ pin transition causes an update of the output value. Based on the DAC output value, the DACn register value and the Command bit where the $\overline{LAT}$ pin transitions, the value being read could be corrupted.

If $\overline{LAT}$ pin transitions occur during a read of the DACn register, it is recommended that sequential reads be performed until the two most recent read values match. Then the most recent read data are good.

7.8.2 SINGLE READ

The READ command operation requires that the $\overline{CS}$ pin be in the Active state (V_{IL}). Typically, the $\overline{CS}$ pin will be in the Inactive state (V_{IH}) and is driven to the Active state (V_{IL}). The 24-bit READ command (command byte and data byte) is then clocked in on the SCK and SDI pins. The SDO pin starts driving data on the 8th bit (CMDERR bit) and the addressed data come out on the 9th through 24th clocks.



Note 1: The Data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00, and 8-bit = D07:D00. The unimplemented bits are output as '0' and data are right justified for easy host controller operation (no data manipulation after reading the register value).

2: If an error condition occurs (CMDERR = 0), all the following SDO bits will be output as '0' until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the Inactive state).

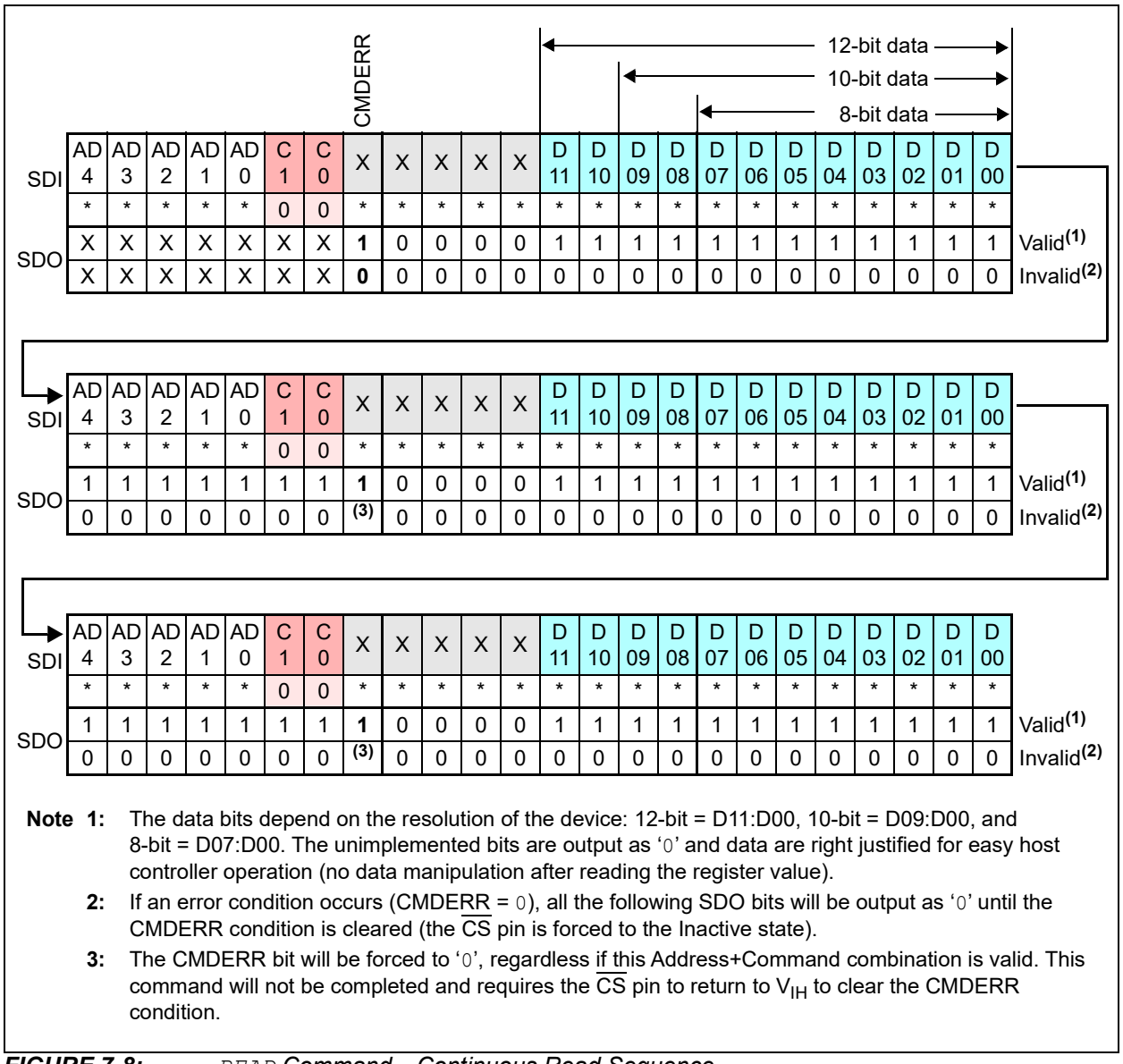
FIGURE 7-7: *READ Command – SDI and SDO States.*

7.8.3 CONTINUOUS READS

Continuous reads format allows the device's memory to be read quickly. Continuous reads are possible to all memory locations. If a nonvolatile memory write cycle is occurring, then READ commands may only access the volatile memory locations.

Figure 7-8 shows the sequence for three continuous reads. The reads do not need to be to the same memory address.

This is useful in reading the System Status register (0Ah) to determine if an EEPROM write cycle is complete (EEWA bit).

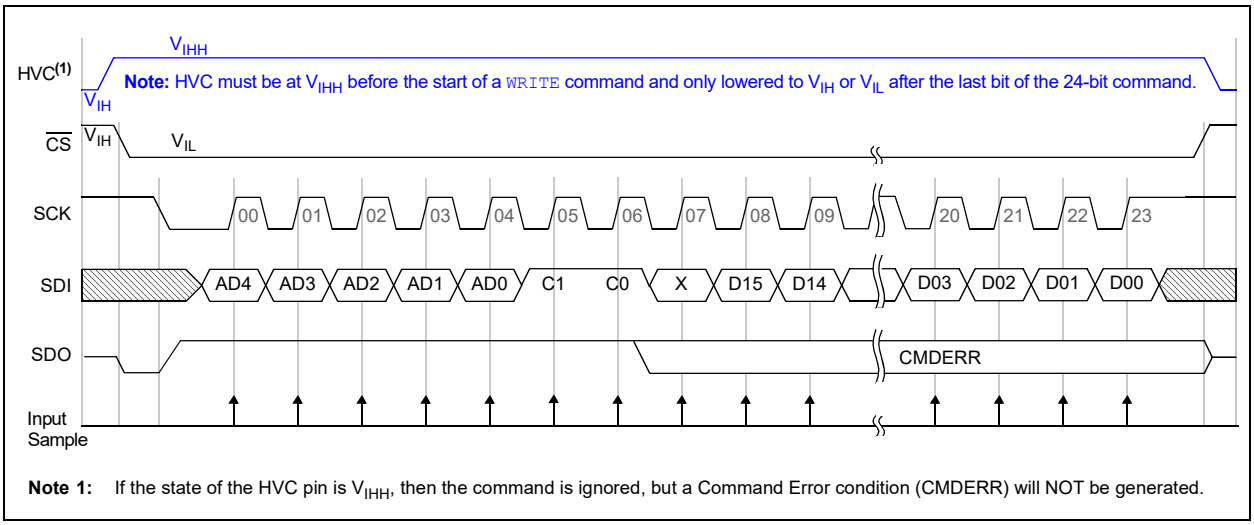


Note 1: The data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00, and 8-bit = D07:D00. The unimplemented bits are output as '0' and data are right justified for easy host controller operation (no data manipulation after reading the register value).

2: If an error condition occurs (CMDERR = 0), all the following SDO bits will be output as '0' until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the Inactive state).

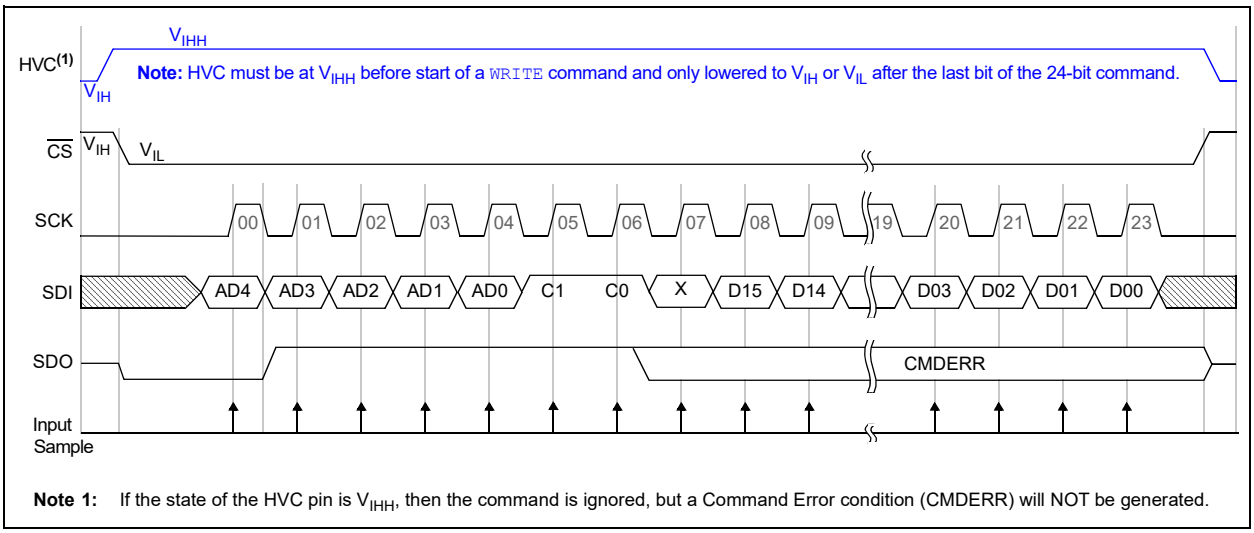
3: The CMDERR bit will be forced to '0', regardless if this Address+Command combination is valid. This command will not be completed and requires the $\overline{CS}$ pin to return to V_{IH} to clear the CMDERR condition.

FIGURE 7-8: *READ Command – Continuous Read Sequence.*



Note 1: If the state of the HVC pin is V_{IHH}, then the command is ignored, but a Command Error condition (CMDERR) will NOT be generated.

FIGURE 7-9: *24-Bit READ Command (C1:C0 = 11) – SPI Waveforms (Mode 1,1).*



Note 1: If the state of the HVC pin is V_{IHH}, then the command is ignored, but a Command Error condition (CMDERR) will NOT be generated.

FIGURE 7-10: *24-Bit READ Command (C1:C0 = 11) – SPI Waveforms (Mode 0,0).*

7.9 Enable Configuration Bit (High Voltage)

Figure 7-11 shows the formats for a single enable Configuration bit command. The command will only start the EEPROM Write Cycle (t_{WC}) after a properly formatted command has been received.

During an EEPROM write cycle, only serial commands to volatile memory are accepted. All other serial commands are ignored until the EEPROM Write Cycle (t_{WC}) completes. This allows the host controller to operate on the volatile DAC, the volatile V_{REF}, Power-Down, Gain and Status, and WiperLock Technology Status registers. The EEWA bit in the Status register indicates the status of the EEPROM write cycle.

								CMDERR																
	AD4	AD3	AD2	AD1	AD0	C1	C0	X	AD4	AD3	AD2	AD1	AD0	C1	C0	X	AD4	AD3	AD2	AD1	AD0	C1	C0	X
SDI	*	*	*	*	*	1	0	*	*	*	*	*	*	1	0	*	*	*	*	*	*	1	0	*
SDO	X	X	X	X	X	X	X	**1**	1	1	1	1	1	1	1	**1**	1	1	1	1	1	1	1	**1**
	X	X	X	X	X	X	X	**0**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Valid(1)

Invalid(2)

Note 1: If an error condition occurs (CMDERR = 0), all the following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the Inactive state).

2: The CMDERR bit will be forced to '0', regardless if this Address+Command combination is valid. This command will not be completed and requires the $\overline{CS}$ pin to return to V_{IH} to clear the CMDERR condition.

FIGURE 7-11: *Enable Command Sequence.*

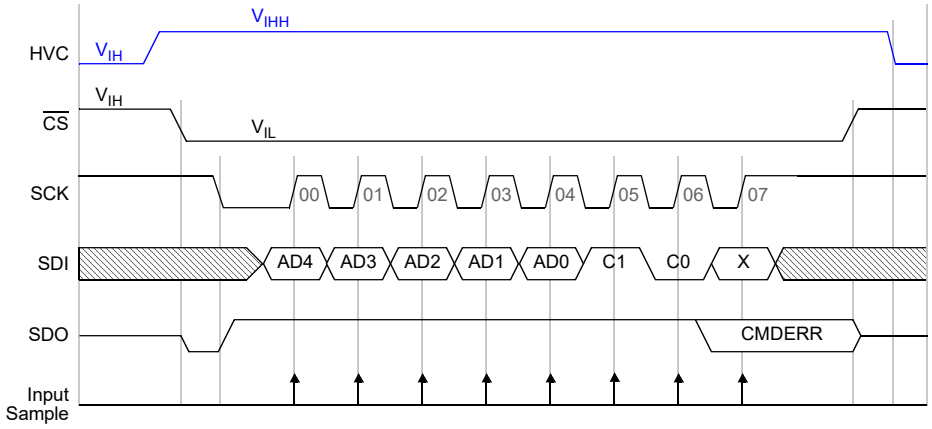


FIGURE 7-12: *8-Bit Enable Command (C1:C0 = 10) – SPI Waveforms (Mode 1,1).*

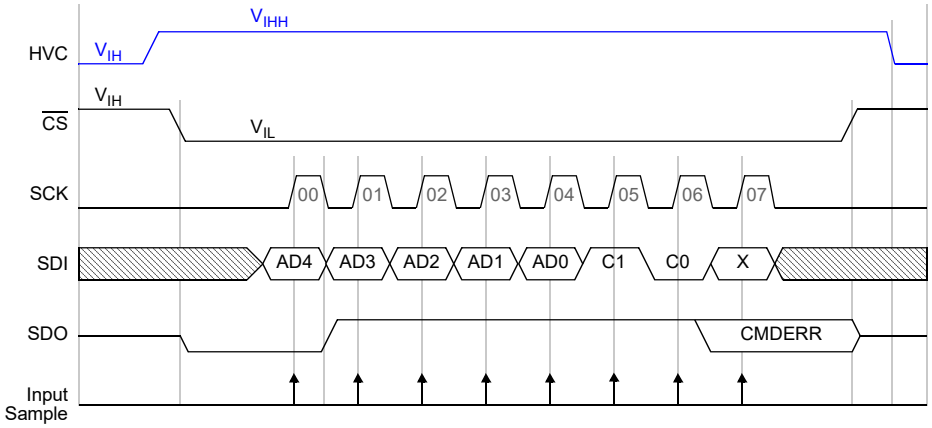


FIGURE 7-13: *8-Bit Enable Command (C1:C0 = 10) – SPI Waveforms (Mode 0,0).*

7.10 Disable Configuration Bit (High Voltage)

Figure 7-14 shows the formats for a single disable Configuration bit command. The command will only start an EEPROM Write Cycle (t_{WC}) after a properly formatted command has been received.

During an EEPROM write cycle, only serial commands to volatile memory are accepted. All other serial commands are ignored until the EEPROM Write Cycle (t_{WC}) completes. This allows the host controller to operate on the volatile DAC, the volatile V_{REF}, Power-Down, Gain and Status, and WiperLock Technology Status registers. The EEWA bit in the Status register indicates the status of an EEPROM write cycle.

								CMDERR																	
	AD4	AD3	AD2	AD1	AD0	C1	C0	X	AD4	AD3	AD2	AD1	AD0	C1	C0	X	AD4	AD3	AD2	AD1	AD0	C1	C0	X	
SDI	*	*	*	*	*	0	1	*	*	*	*	*	*	0	1	*	*	*	*	*	*	0	1	*	
SDO	X	X	X	X	X	X	X	**1**	1	1	1	1	1	1	1	**1**	1	1	1	1	1	1	1	**1**	Valid(1)
	X	X	X	X	X	X	X	**0**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Invalid(2)

Note 1: If an error condition occurs (CMDERR = 0), all the following SDO bits will be low until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the Inactive state).

2: The CMDERR bit will be forced to '0', regardless if this Address+Command combination is valid. This command will not be completed and requires the $\overline{CS}$ pin to return to V_{IH} to clear the CMDERR condition.

FIGURE 7-14: *Disable Command Sequence.*

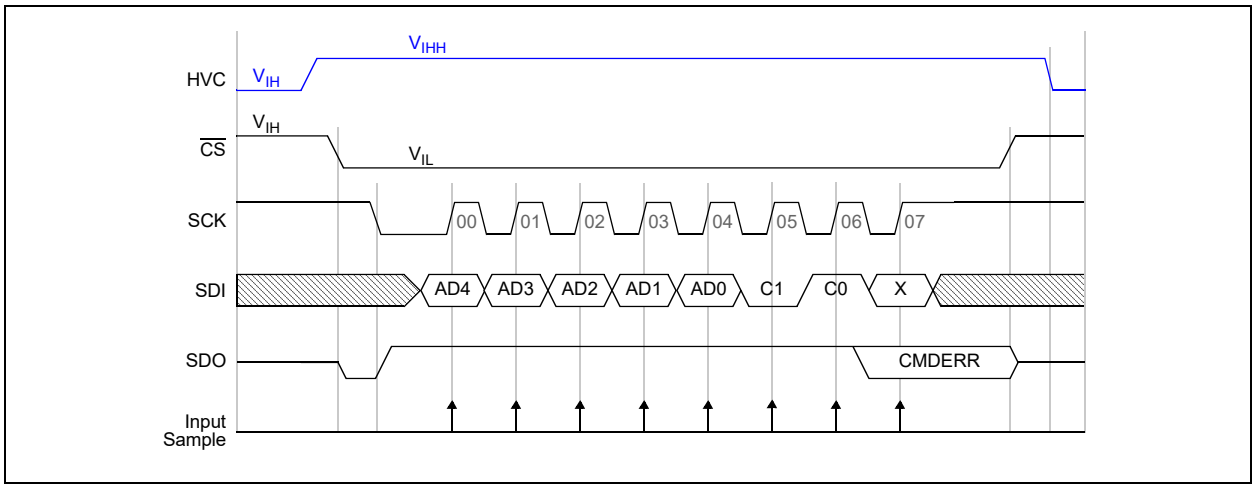


FIGURE 7-15: *8-Bit Disable Command (C1:C0 = 01) – SPI Waveforms (Mode 1,1).*

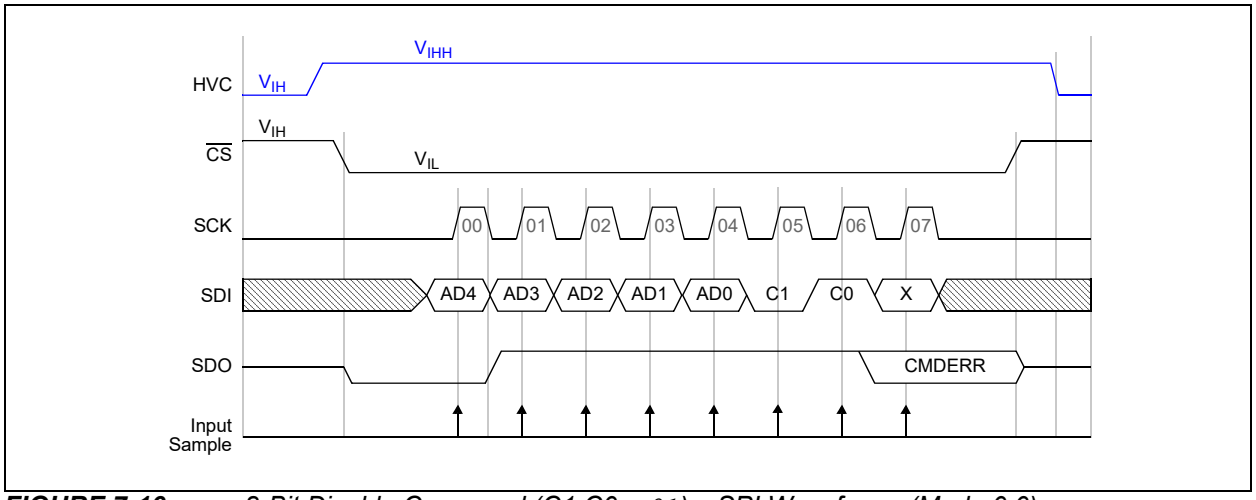


FIGURE 7-16: *8-Bit Disable Command (C1:C0 = 01) – SPI Waveforms (Mode 0,0).*

8.0 APPLICATIONS INFORMATION

The MCP48FXBX4/8 devices are general purpose, quad/octal-channel voltage output DACs for various applications, where a precision operation with low-power and nonvolatile EEPROM memory is needed.

Since the devices include a nonvolatile EEPROM memory, the user can utilize these devices for applications that require the output to return to the previous setup value on subsequent power-ups.

8.1 Power Supply Considerations

The power source should be as clean as possible. The power supply to the device is also used for the DAC voltage reference internally if the internal V_{DD} is selected as the resistor ladder's reference voltage (VRnB:VRnA = 00).

Any noise induced on the V_{DD} line can affect the DAC performance. Typical applications will require a bypass capacitor in order to filter out high-frequency noise on the V_{DD} line. The noise can be induced onto the power supply's traces or as a result of changes on the DAC output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-1 shows an example of using two bypass capacitors (a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor) in parallel on the V_{DD} line. These capacitors should be placed as close to the V_{DD} pin as possible (within 4 mm). If the application circuit has separate digital and analog power supplies, the V_{DD} and V_{SS} pins of the device should reside on the analog plane.

When setting the part voltage reference to Band Gap mode, the use of the V_{REF} pin decoupling capacitors is not recommended.

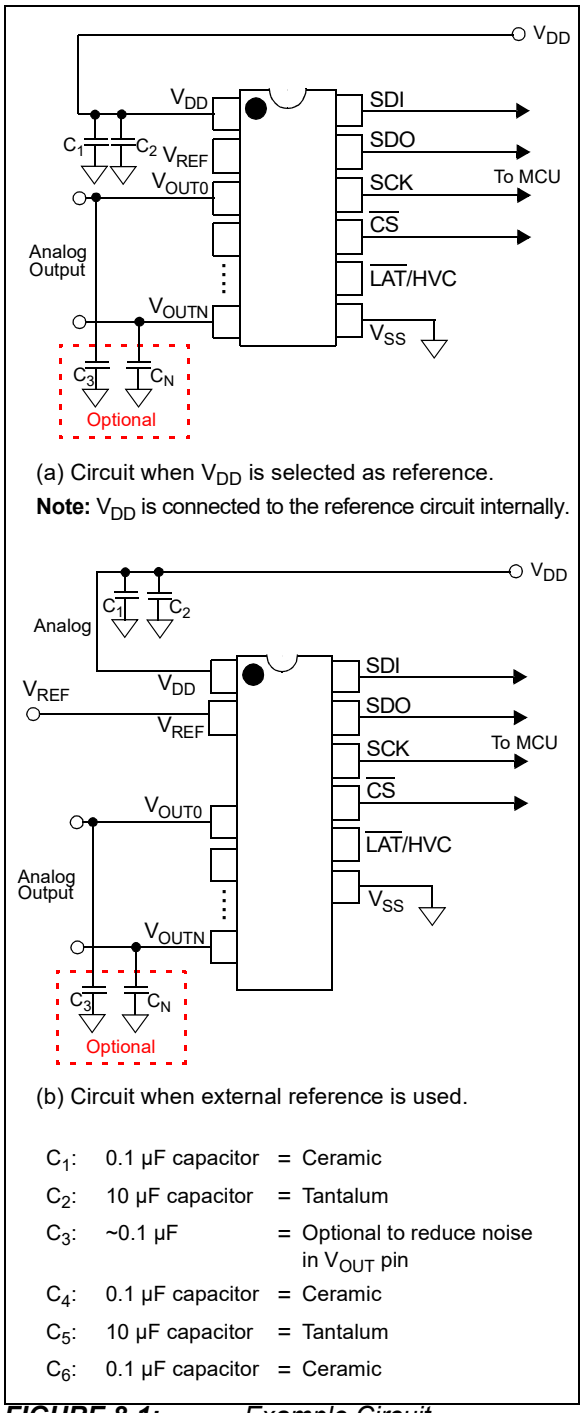


FIGURE 8-1: *Example Circuit.*

8.2 Layout Considerations

Several layout considerations may be applicable to your application. These may include:

- **Noise**
- **PCB Area Requirements**

8.2.0.1 Noise

Particularly harsh environments may require shielding of critical signals. Inductively coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP48FXBX4/8 devices' performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR).

Multilayer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing.

Separate digital and analog ground planes are recommended. In this case, the V_{SS} pin and the ground pins of the V_{DD} capacitors should be terminated to the analog ground plane.

Note:	Breadboards and wire-wrapped boards are not recommended.

8.2.0.2 PCB Area Requirements

In some applications, PCB area is a criteria for device selection. Table 8-1 shows the typical package dimensions and area for the different package options.

TABLE 8-1: PACKAGE FOOTPRINT(1)

Package			Package Footprint		
Pins	Type	Code	Dimensions (mm)		Area (mm^2)
			Length	Width	
20	TSSOP	ST	3.00	4.90	14.70
20	VQFN	MQ	5	5	25

Note 1: Does not include recommended land pattern dimensions. Dimensions are typical values.

9.0 DEVELOPMENT SUPPORT

Development support can be classified into two groups. These are:

- **Development Tools**
- **Technical Documentation**

9.1 Development Tools

Several development tools are available to assist in your design and evaluation of the MCP48FXBX4/8 devices. The currently available tools are shown in Table 9-1.

Figure 9-1 shows how the TSSOP20EV bond-out PCB can be populated to easily evaluate the MCP48FXBX4/8 devices. The PICkit™ Serial Analyzer can be used to control the DAC Output registers and state of the Configuration, Control and Status register.

The TSSOP20EV boards may be purchased directly from the Microchip website at www.microchip.com.

9.2 Technical Documentation

Several additional technical documents are available to assist you in your design and development. These technical documents include Application Notes, Technical Briefs and Design Guides. Table 9-2 lists some of these documents.

TABLE 9-1: DEVELOPMENT TOOLS(1)

Board Name	Part #	Comment
20-Pin TSSOP and SSOP Evaluation Board	TSSOP20EV	Most Flexible Option – Recommended Bond-out PCB

Note 1: Supports the PICkit™ Serial Analyzer. See the User's Guide for additional information and requirements.

TABLE 9-2: TECHNICAL DOCUMENTATION

Application Note Number	Title	Literature #
AN1326	Using the MCP4828 12-Bit DAC for LDMOS Amplifier Bias Control Applications	DS01326
—	Signal Chain Design Guide	DS21825
—	Analog Solutions for Automotive Applications Design Guide	DS01005

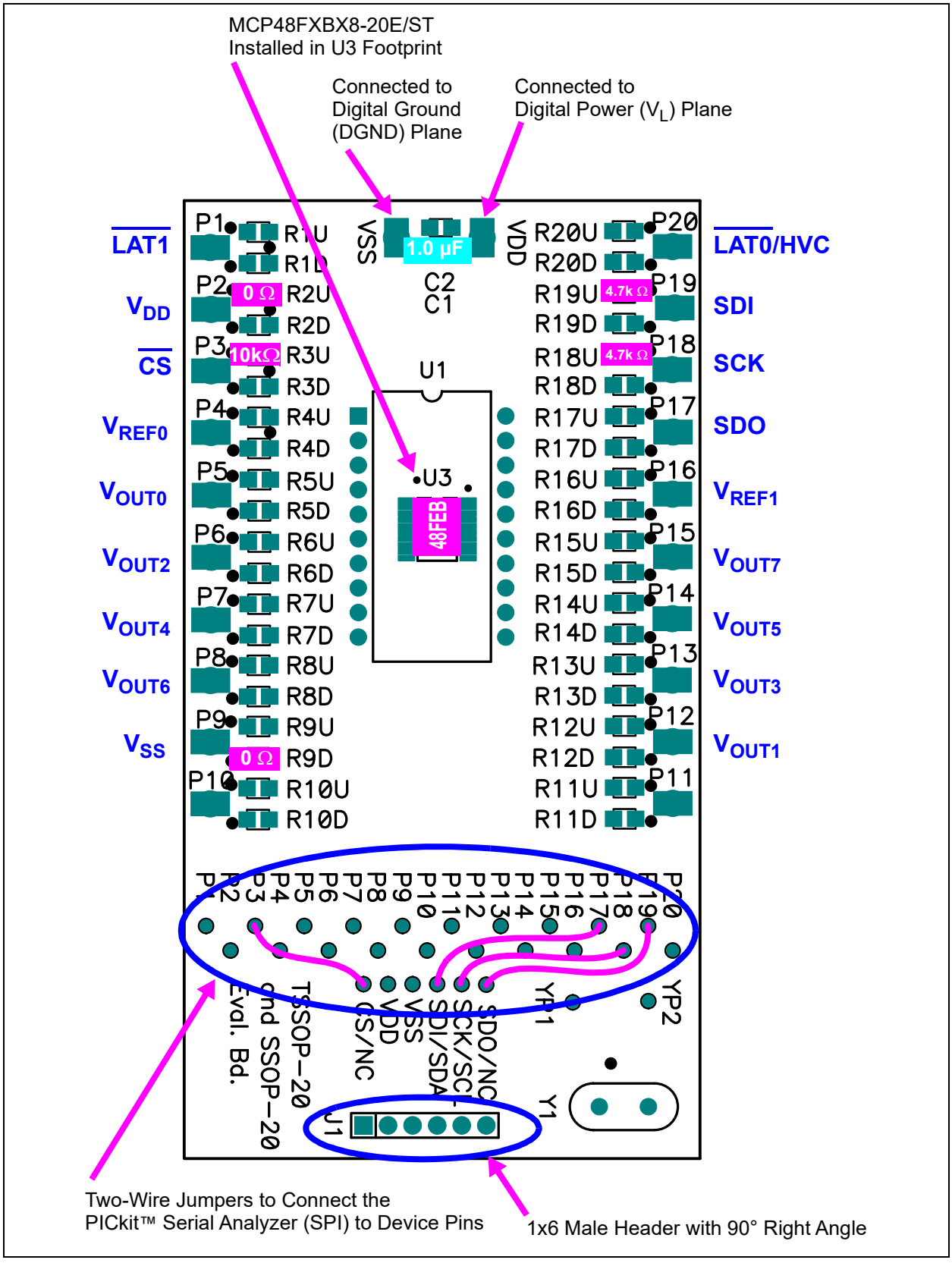
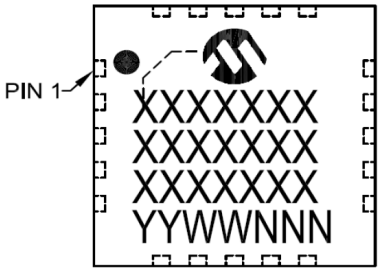


FIGURE 9-1: *MCP48FXBX4/8 Evaluation Board Circuit Using TSSOP20EV.*

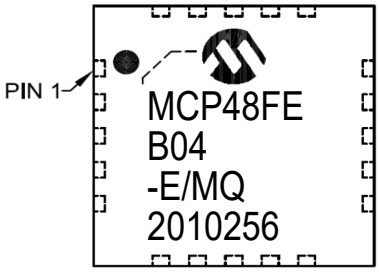
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

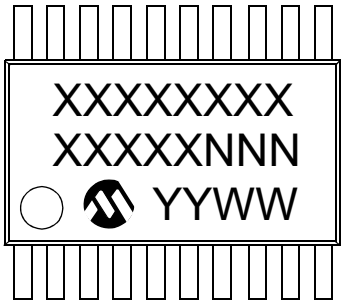
20-Lead 5 x 5 mm VQFN



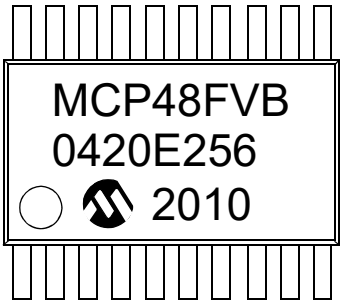
Example



20-Lead TSSOP



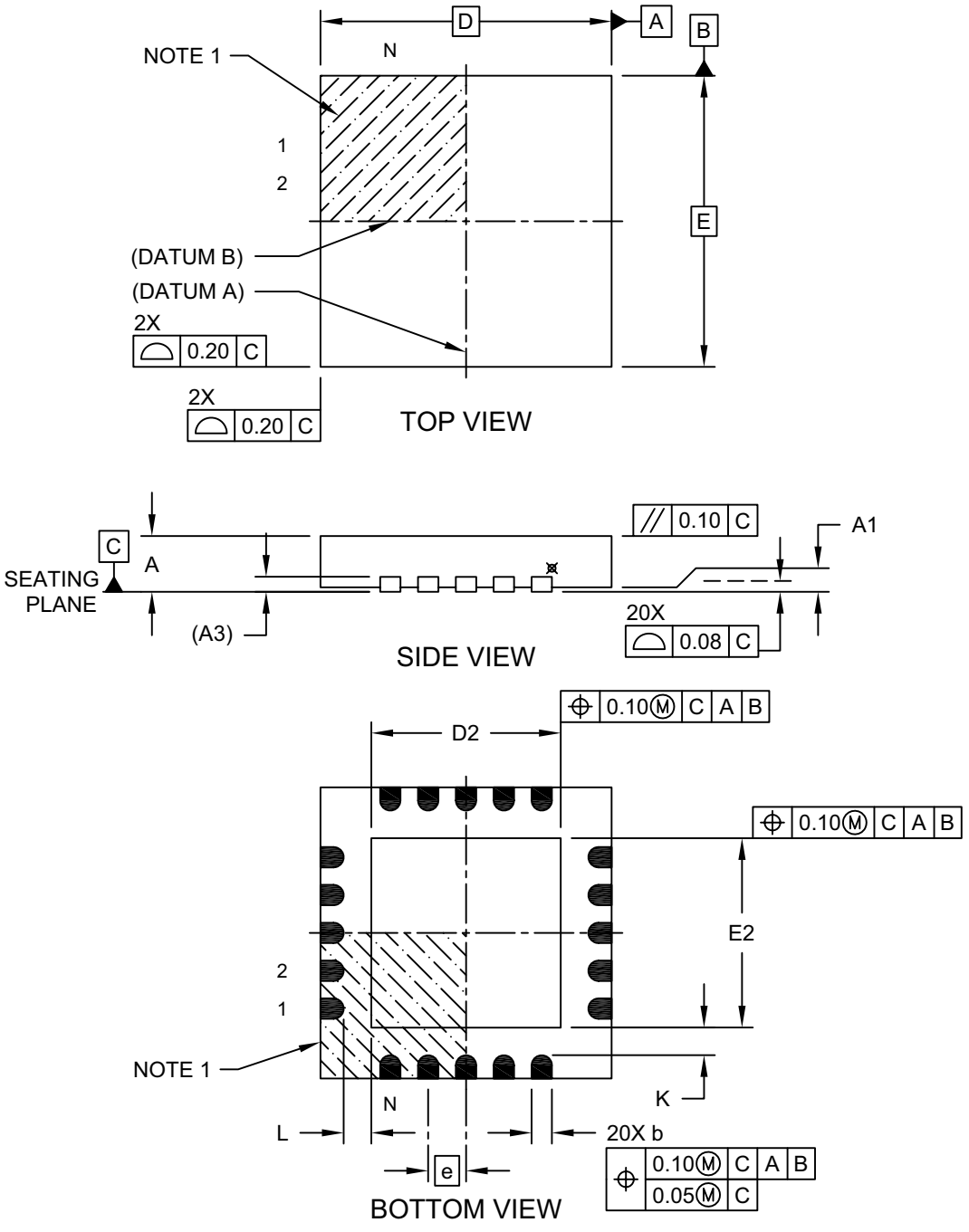
Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

20-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x1.0 mm Body [VQFN] With 0.40 mm Contact Length

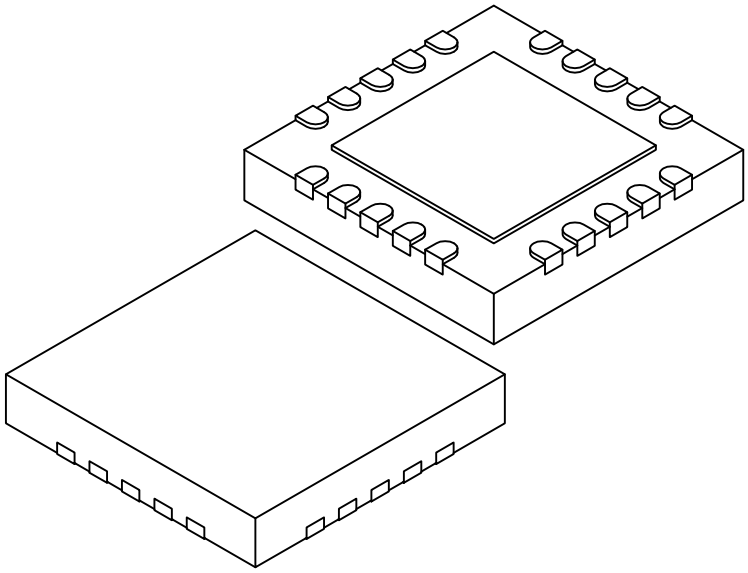
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-139C (MQ) Sheet 1 of 2

20-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x1.0 mm Body [VQFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	(A3)		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.15	3.25	3.35
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.15	3.25	3.35
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.35	0.40	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

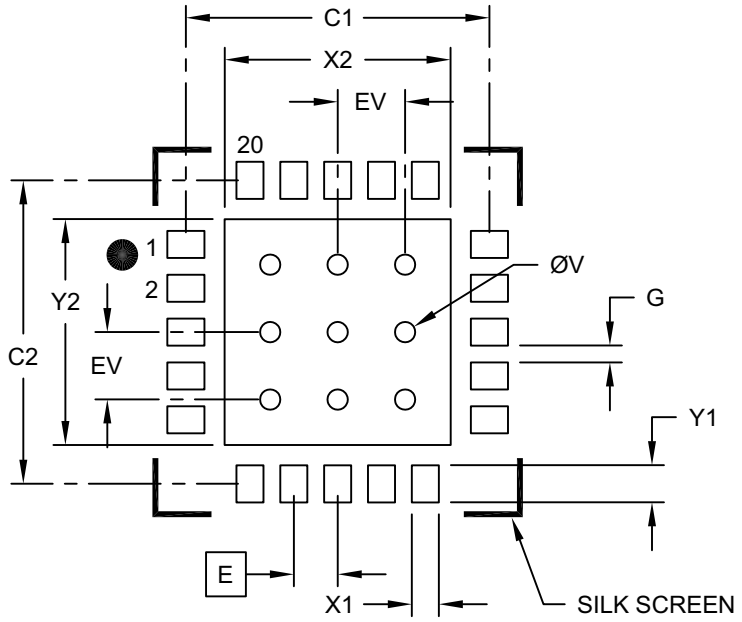
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-139C (MQ) Sheet 2 of 2

20-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x1.0 mm Body [VQFN] With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			3.35
Optional Center Pad Length	T2			3.35
Contact Pad Spacing	C1		4.50	
Contact Pad Spacing	C2		4.50	
Contact Pad Width (X20)	X1			0.40
Contact Pad Length (X20)	Y1			0.55
Distance Between Pads	G	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

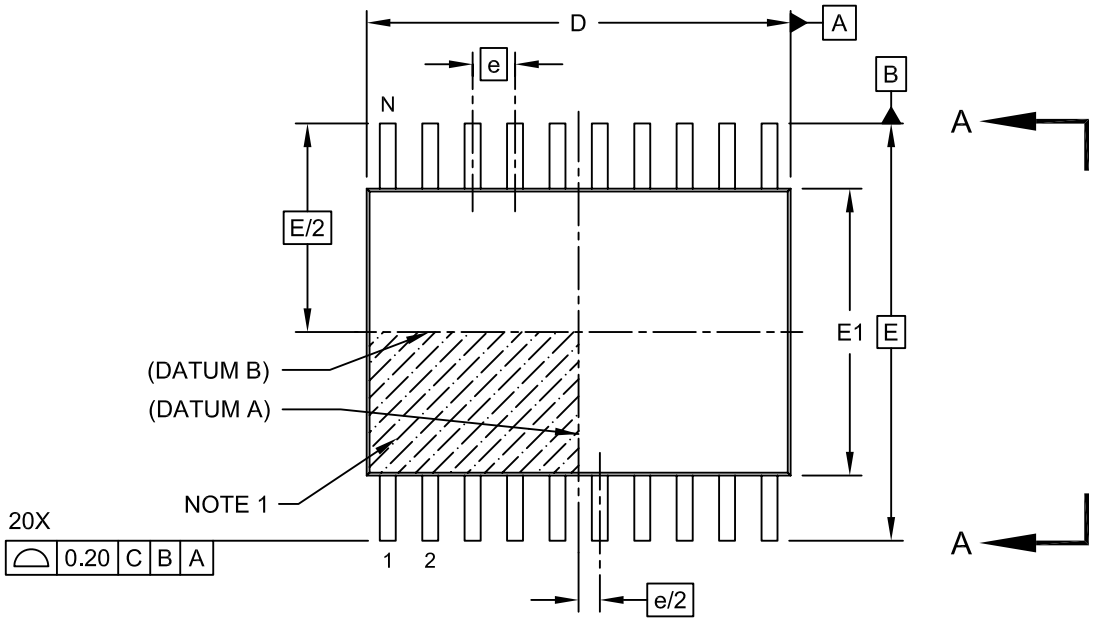
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

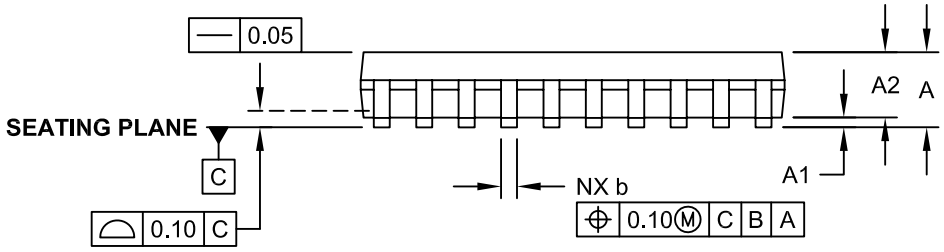
Microchip Technology Drawing C04-2139B (MQ)

20-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

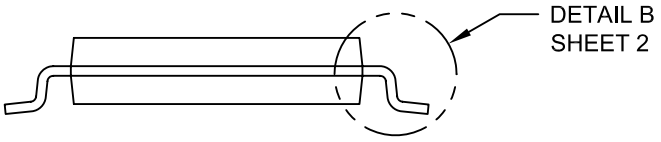
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

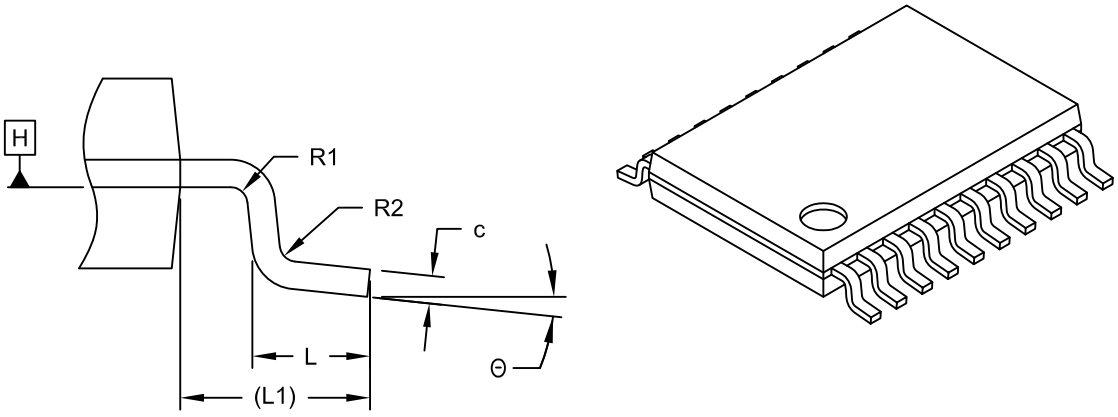


VIEW A—A

Microchip Technology Drawing C04-088C Sheet 1 of 2

20-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	6.40	6.50	6.60
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	Θ	0°	-	8°
Lead Width	b	0.19	-	0.30
Lead Thickness	c	0.09	-	0.20
Bend Radius	R1	0.09	-	-
Bend Radius	R2	0.09	-	-

Notes:

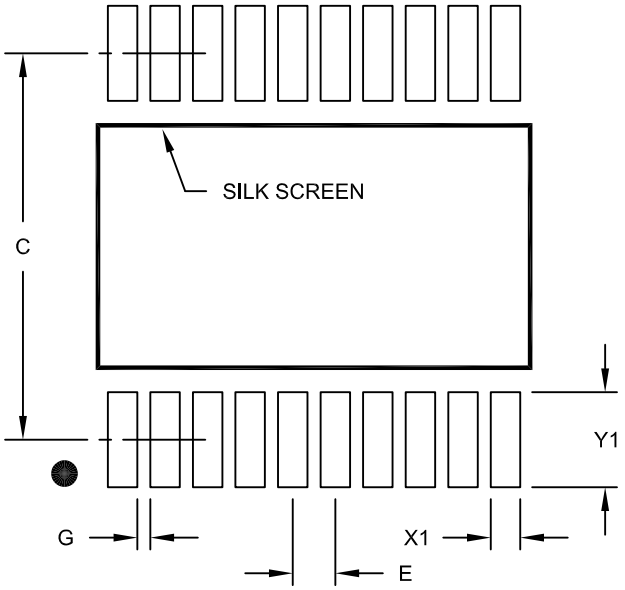
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-088C Sheet 2 of 2

20-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.90	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2088A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (May 2020)

- Original release of this document.

NOTES:

APPENDIX B: TERMINOLOGY

B.1 Resolution

The resolution is the number of DAC output states that divide the full-scale range. For the 12-bit DAC, the resolution is 2^{12}, meaning the DAC code ranges from 0 to 4095.

Note:	When there are 2^N resistors in the resistor ladder and 2^N tap points, the full-scale DAC register code is the resistor element (1 LSb) from the source reference voltage (V_{DD} or V_{REF}).

B.2 Least Significant Bit (LSb)

This is the voltage difference between two successive codes. For a given output voltage range, it is divided by the resolution of the device (Equation B-1). The range may be V_{DD} (or V_{REF}) to V_{SS} (ideal); the DAC register codes across the linear range of the output driver (Measured 1), or full scale to zero scale (Measured 2).

EQUATION B-1: LSb VOLTAGE CALCULATION

Ideal

$$V_{LSb(IDEAL)} = \frac{V_{DD}}{2^N} \quad \text{or} \quad \frac{V_{REF}}{2^N}$$

Measured 1

$$V_{LSb(Measured)} = \frac{V_{OUT(@4000)} - V_{OUT(@100)}}{(4000 - 100)}$$

Measured 2

$$V_{LSb} = \frac{V_{OUT(@FS)} - V_{OUT(@ZS)}}{2^N - 1}$$

2^N = 4096 (MCP48FXB2X)
= 1024 (MCP48FXB1X)
= 256 (MCP48FXB0X)

B.3 Monotonic Operation

Monotonic operation means that the device's output voltage (V_{OUT}) increases with every 1 code step (LSb) increment (from V_{SS} to the DAC's reference voltage (V_{DD} or V_{REF})).

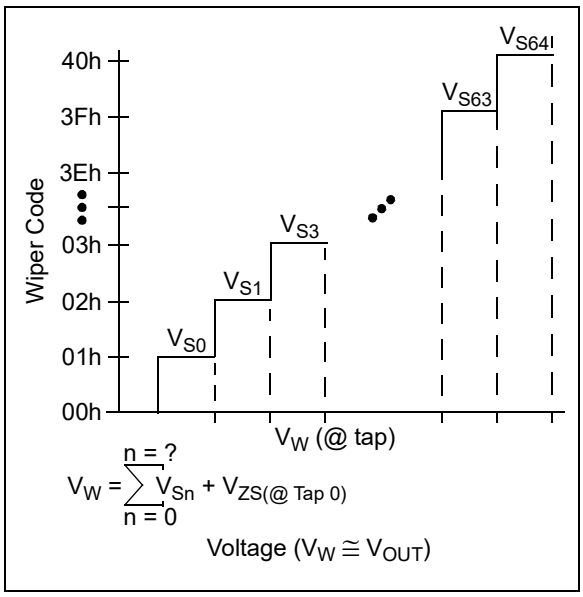


FIGURE B-1: V_W (V_{OUT}).

B.4 Full-Scale Error (E_{FS})

The Full-Scale Error (see Figure B-3) is the error on the V_{OUT} pin relative to the expected V_{OUT} voltage (theoretical) for the maximum device DAC register code (code FFFh for 12-bit, code 3FFh for 10-bit and code FFh for 8-bit); see Equation B-2. The error depends on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{SS}) greater than specified, the Full-Scale Error will be greater.

The error in bits is determined by the theoretical voltage step-size to give an error in LSb.

EQUATION B-2: FULL-SCALE ERROR

$$E_{FS} = \frac{V_{OUT(@FS)} - V_{IDEAL(@FS)}}{V_{LSb(IDEAL)}}$$

Where:

E_{FS} is expressed in LSb.

$V_{OUT(@FS)}$ = The V_{OUT} voltage when the DAC register code is at full scale.

$V_{IDEAL(@FS)}$ = The ideal output voltage when the DAC register code is at full scale.

$V_{LSb(IDEAL)}$ = The theoretical voltage step size.

B.5 Zero-Scale Error (E_{ZS})

The Zero-Scale Error (see Figure B-2) is the difference between the ideal and the measured V_{OUT} voltage with the DAC register code equal to 000h (Equation B-3). The error depends on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{DD}) greater than specified, the Zero-Scale Error will be greater.

The error in bits is determined by the theoretical voltage step-size to give an error in LSb.

EQUATION B-3: ZERO-SCALE ERROR

$$E_{ZS} = \frac{V_{OUT(@ZS)}}{V_{LSb(IDEAL)}}$$

Where:

E_{ZS} is expressed in LSb.

$V_{OUT(@ZS)}$ = The V_{OUT} voltage when the DAC register code is at zero scale.

$V_{LSb(IDEAL)}$ = The theoretical voltage step-size.

B.6 Total Unadjusted Error (E_T)

The Total Unadjusted Error (E_T) is the difference between the ideal and the measured V_{OUT} voltage. Typically, calibration of the output voltage is implemented to improve system performance.

The error in bits is determined by the theoretical voltage step-size to give an error in LSb.

Equation B-4 shows the Total Unadjusted Error calculation.

EQUATION B-4: TOTAL UNADJUSTED ERROR CALCULATION

$$E_T = \frac{(V_{OUT\_Actual(@Code)} - V_{OUT\_Ideal(@Code)})}{V_{LSb(Ideal)}}$$

Where:

E_T is expressed in LSb.

$V_{OUT\_Actual(@Code)}$ = The measured DAC output voltage at the specified code.

$V_{OUT\_Ideal(@Code)}$ = The calculated DAC output voltage at the specified code. (code × $V_{LSb(Ideal)}$).

$V_{LSb(Ideal)}$ = V_{REF}/# Steps
12-bit = V_{REF}/4096
10-bit = V_{REF}/1024
8-bit = V_{REF}/256

B.7 Offset Error (E_{OS})

The Offset Error is the delta voltage of the V_{OUT} voltage from the ideal output voltage at the specified code. This code is specified where the output amplifier is in the linear operating range; for the MCP48FXBX4/8, we specify code 100 (decimal). Offset error does not include Gain Error, see Figure B-2.

This error is expressed in mV. Offset Error can be negative or positive. The Offset Error can be calibrated by software in application circuits.

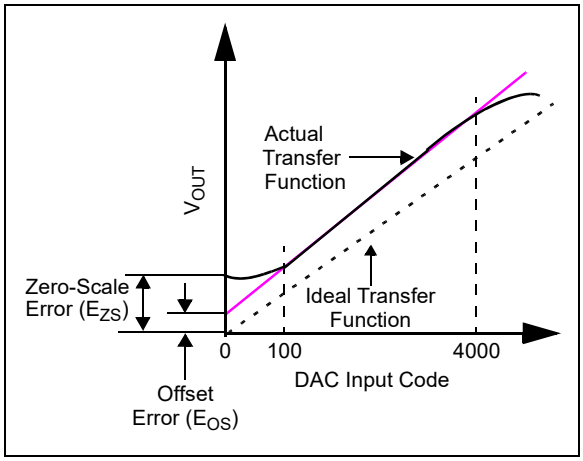


FIGURE B-2: *Offset Error and Zero-Scale Error.*

B.8 Offset Error Drift (E_{OSD})

The Offset Error Drift is the variation in Offset Error due to a change in ambient temperature. The Offset Error Drift is typically expressed in ppm/°C or µV/°C.

B.9 Gain Error (E_G)

Gain Error is a calculation based on the ideal slope using the voltage boundaries for the linear range of the output driver (ex.: code 100 and code 4000); see Figure B-3. The Gain Error calculation nullifies the device's Offset Error.

Gain Error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. Gain Error is usually expressed as a percent of full-scale range (% of FSR) or in LSb. FSR is the ideal full-scale voltage of the DAC (see Equation B-5).

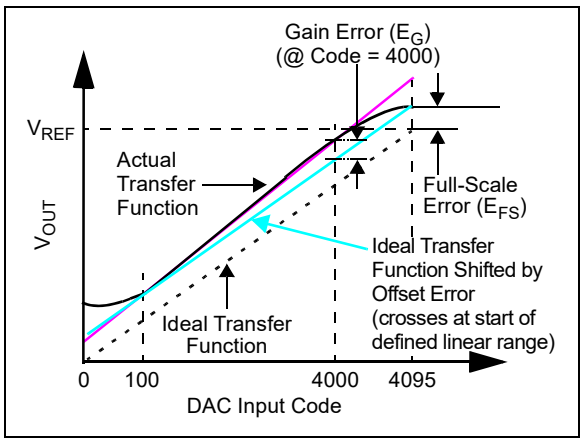


FIGURE B-3: *Gain Error and Full-Scale Error Example.*

EQUATION B-5: EXAMPLE GAIN ERROR

$$E_G = \frac{(V_{OUT(@4000)} - V_{OS} - V_{OUT\_Ideal(@4000)})}{V_{Full\text{-}Scale\ Range}} \cdot 100$$

Where:

E_G is expressed in % of FSR.

$V_{OUT(@4000)}$ = The measured DAC output voltage at the specified code.

$V_{OUT\_Ideal(@4000)}$ = The calculated DAC output voltage at the specified code (4000 * $V_{LSb(Ideal)}$).

V_{OS} = Measured offset voltage.

$V_{Full\text{-}Scale\ Range}$ = Expected full-scale output value (such as the V_{REF} voltage).

B.10 Gain Error Drift (E_{GD})

The Gain Error Drift is the variation in Gain Error due to a change in ambient temperature. Gain Error Drift is typically expressed in ppm/°C (of FSR).

B.11 Integral Nonlinearity (INL)

The Integral Nonlinearity (INL) error is the maximum deviation of an actual transfer function from an ideal transfer function (straight line) passing through the defined end points of the DAC transfer function (after offset and gain errors have been removed).

In the MCP48FXBX4/8, INL is calculated using the defined end points, DAC code 100 and code 4000. INL can be expressed as a percentage of FSR or in LSb. INL is also called 'Relative Accuracy'. Equation B-6 shows how to calculate the INL error in LSb and Figure B-4 shows an example of INL accuracy.

Positive INL means higher V_{OUT} voltage than the ideal one. Negative INL means lower V_{OUT} voltage than the ideal one.

EQUATION B-6: INL ERROR

$$E_{INL} = \frac{(V_{OUT} - V_{Calc\_Ideal})}{V_{LSb(Measured)}}$$

Where:

INL is expressed in LSb.

V_{Calc_Ideal} = Code × $V_{LSb(Measured)}$ + V_{OS}

$V_{OUT(Code = n)}$ = The measured DAC output voltage with a given DAC register code.

$V_{LSb(Measured)}$ = For Measured: $(V_{OUT(4000)} - V_{OUT(100)})/3900$.

V_{OS} = Measured offset voltage.

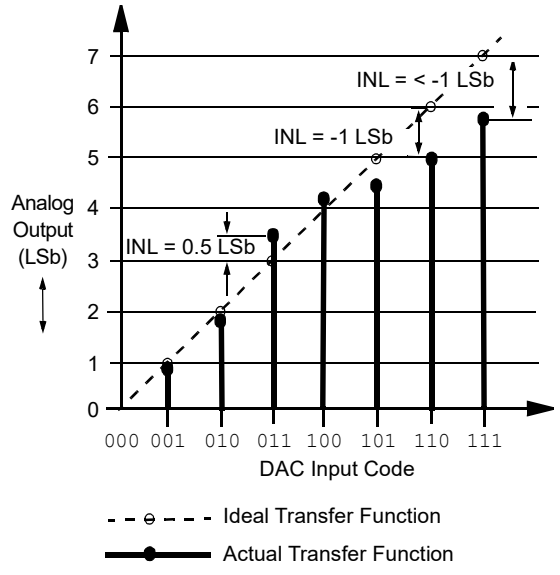


FIGURE B-4: *INL Accuracy.*

B.12 Differential Nonlinearity (DNL)

The Differential Nonlinearity (DNL) error (see Figure B-5) is the measure of step-size between codes in an actual transfer function. The ideal step-size between codes is 1 LSb. A DNL error of zero would imply that every code is exactly 1 LSb wide. If the DNL error is less than 1 LSb, the DAC ensures monotonic output and no missing codes. Equation B-7 shows how to calculate the DNL error between any two adjacent codes in LSb.

EQUATION B-7: DNL ERROR

$$E_{DNL} = \frac{(V_{OUT(code = n+1)} - V_{OUT(code = n)})}{V_{LSb(Measured)}} - 1$$

Where:

DNL is expressed in LSb.

$V_{OUT(code = n)}$ = The measured DAC output voltage with a given DAC register code.

$V_{LSb(Measured)}$ = For Measured: $(V_{OUT(4000)} - V_{OUT(100)})/3900$.

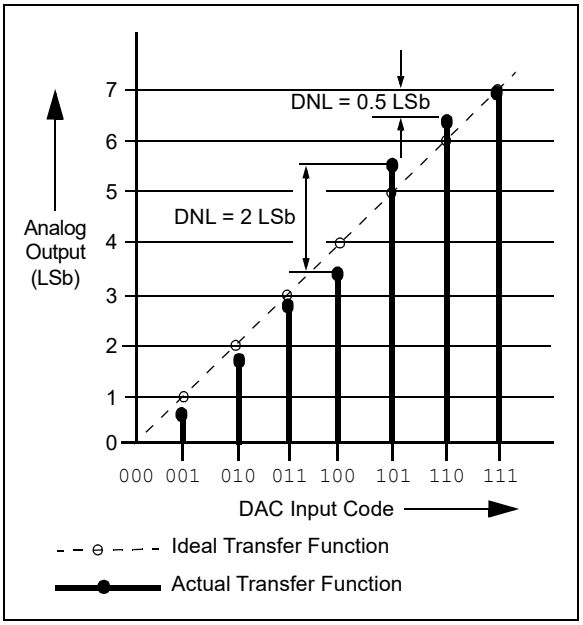


FIGURE B-5: *DNL Accuracy.*

B.13 Settling Time

The settling time is the time delay required for the V_{OUT} voltage to settle into its new output value. This time is measured from the start of code transition to when the V_{OUT} voltage is within the specified accuracy.

For the MCP48FXBX4/8, the settling time is a measurement of the time delay until the V_{OUT} voltage reaches within 0.5 LSb of its final value, when the volatile DAC register changes from 1/4 to 3/4 of the FSR (12-bit device: 400h to C00h).

B.14 Major Code Transition Glitch

Major code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes the state. It is normally specified as the area of the glitch in nV-Sec and is measured when the digital code is changed by 1 LSb at the major carry transition.

Example: `011...111` to `100...000`
or `100...000` to `011...111`

B.15 Digital Feedthrough

The digital feed-through is the glitch that appears at the analog output, caused by coupling from the digital input pins of the device. The area of the glitch is expressed in nV-Sec and is measured with a full-scale change on the digital input pins; example: all '`0`'s to all '`1`'s and vice versa. The digital feedthrough is measured when the DAC is not written to the output register.

B.16 -3 dB Bandwidth

This is the frequency of the signal at the V_{REF} pin that causes the voltage at the V_{OUT} pin to fall a -3 dB value from a static value on the V_{REF} pin. The output decreases due to the RC characteristics of the resistor ladder and the characteristics of the output buffer.

B.17 Power Supply Sensitivity (PSS)

PSS indicates how the output of the DAC is affected by changes in the supply voltage. PSS is the ratio of the change in V_{OUT} to a change in V_{DD} for midscale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied from 5.5V to 2.7V as a step (V_{REF} voltage held constant) and is expressed in %/%, which is the % change of the DAC output voltage with respect to the % change of the V_{DD} voltage.

EQUATION B-8: PSS CALCULATION

$$PSS = \frac{(V_{OUT(@5.5V)} - V_{OUT(@2.7V)}) / V_{OUT(@5.5V)}}{(5.5V - 2.7V) / (5.5V)}$$

Where:

PSS is expressed in %/%.

$V_{OUT(@5.5V)}$ = The measured DAC output voltage with V_{DD} = 5.5V.

$V_{OUT(@2.7V)}$ = The measured DAC output voltage with V_{DD} = 2.7V.

B.18 Power Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied ±10% (V_{REF} voltage held constant) and expressed in dB or µV/V.

B.19 V_{OUT} Temperature Coefficient

The V_{OUT} temperature coefficient quantifies the error in the resistor ladder's resistance ratio (DAC register code value) and output buffer due to temperature drift.

B.20 Absolute Temperature Coefficient

The absolute temperature coefficient quantifies the error in the end-to-end output voltage (nominal Output Voltage, V_{OUT}) due to temperature drift. For a DAC, this error is typically not an issue due to the ratiometric aspect of the output.

B.21 Noise Spectral Density

Noise spectral density is a measurement of the device's internally generated random noise and is characterized as a spectral density (voltage per √Hz). It is measured by loading the DAC to the midscale value and measuring the noise at the V_{OUT} pin. It is measured in nV/√Hz.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	— XX	X	/XX
Device	Tape and Reel	Pin Count	Temperature Range	Package

Device:	MCP48FXB0X:	Quad/Octal-Channel, 8-Bit DAC with SPI Interface
	MCP48FXB1X:	Quad/Octal-Channel, 10-Bit DAC with SPI Interface
	MCP48FXB2X:	Quad/Octal-Channel, 12-Bit DAC with SPI Interface
Tape and Reel:	T =	Tape and Reel
	Blank =	Tube
Pin Count:	20-Lead	
Temperature Range:	E =	-40°C to +125°C (Extended)
Package:	MQ =	Plastic Quad Flat, No Lead Package (VQFN), 5 x 5 mm, 20-Lead
	ST =	Plastic Thin Shrink Small Outline Package (TSSOP), 20-Lead

Examples:

a) MCP48FEB04-E/MQ: Quad-Channel, 8-Bit Nonvolatile DAC, Extended Temperature, 20-Lead VQFN.

b) MCP48FEB08T-E/MQ: Octal-Channel, 8-Bit Nonvolatile DAC, Tape and Reel, Extended Temperature, 20-Lead VQFN.

c) MCP48FEB18-20E/ST: Octal-Channel, 10-Bit Nonvolatile DAC, Extended Temperature, 20-Lead TSSOP.

d) MCP48FEB18T-20E/ST: Octal-Channel, 10-Bit Nonvolatile DAC, Tape and Reel, Extended Temperature, 20-Lead TSSOP.

e) MCP48FVB28-E/MQ: Octal-Channel, 12-Bit Volatile DAC, Extended Temperature, 20-Lead VQFN.

f) MCP48FVB28T-E/MQ: Octal-Channel, 12-Bit Volatile DAC, Tape and Reel, Extended Temperature, 20-Lead VQFN.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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