SA6880-S - Isolated 3.5 A / 1200 V IGBT Driver

1 Features

- Single-channel 1200 V isolated driver optimized for industrial and automotive applications
- 3.5 A peak output current
- 3.75 kV_{rms} input to output isolated voltage
- High common-mode transient immunity: higher than 50 kV/µs
- Less than 115 ns propagation delay
- Less than ±20 ns pulse width distortion
- Integrated IGBT protection functions:
  - IGBT soft turn-off
  - Desaturation detection (DESAT)
  - Active Miller-Current clamp
  - High Side undervoltage lockout (UVLO) protection with feedback
  - Fault sensing/reporting to system controller (DESAT & UVLO)
- TTL compatible inputs
- Automotive temperate range
- Bipolar or unipolar supply operation
- Wide 30 V output supply range
- UL1577 certified to V_{ISO} = 3750 V_{RMS} for 60 seconds.
- IEC60747-17 and VDE 0884-10 compliant

2 Applications

- AC/DC motor drives
- Air-conditioning inverters
- Welding/plasma equipment
- Uninterruptible power supplies
- Battery charging systems
- Automotive OBC and traction inverters
- Auxiliary inverters for HEV and EV
- PV solar inverters and optimizers

3 Description

The SA6880-S is a full-featured, galvanically isolated, 3.5 A / 1200 V-rated gate driver IC. This single-chip solution integrates features that improve performance and ensure long-life in harsh environments. It can be used for fast-switching drive and protection of power IGBT's, Si and SiC MOSFETs. The driver incorporates Solantro's on-chip coreless transformer technology to enable 3.75 kV_{rms} input to output isolated voltage and high transient immunity (>50 kV/µs) as required in industrial and automotive applications.

The driver is suitable for motor control, switch mode power supply (SMPS), PFC, UPS, EV-OBC, industrial pumps, and traction inverter applications. Its short propagation delay and small timing-skew help achieve optimum performance at higher switching speeds when compared with other driver solutions available in the market. All logic pins are TTL compatible for easy interface to standard controllers and MCUs.

The SA6880-S architecture includes several control features protecting the device in harsh industrial and automotive environments. These integrated features include over-current (desaturation) sensing with soft-shutdown protection, high-side undervoltage lockout, active Miller-Current clamping and fault reporting.

The driver supports bipolar and unipolar supply voltage configurations. In a bipolar configuration, the driver is typically supplied with voltages of +18 V and -5 V. For unipolar configuration, the driver is typically supplied with a positive 18 V (max 32 V).

To meet UL isolation, creepage and clearance requirements the SA6880-S is available in a standard SOIC-16W (wide-body) package.

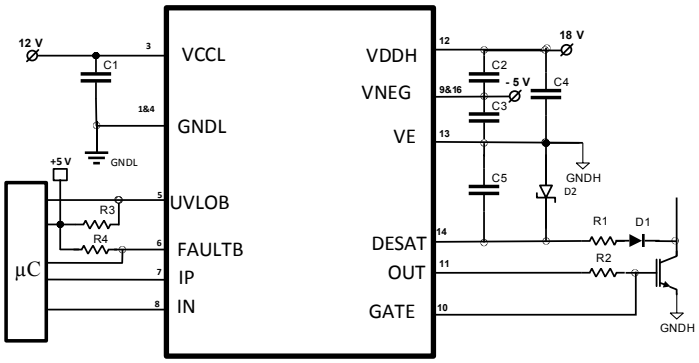


Figure 1- Typical application configuration

Content

4 Pin Configuration and Functional Diagram

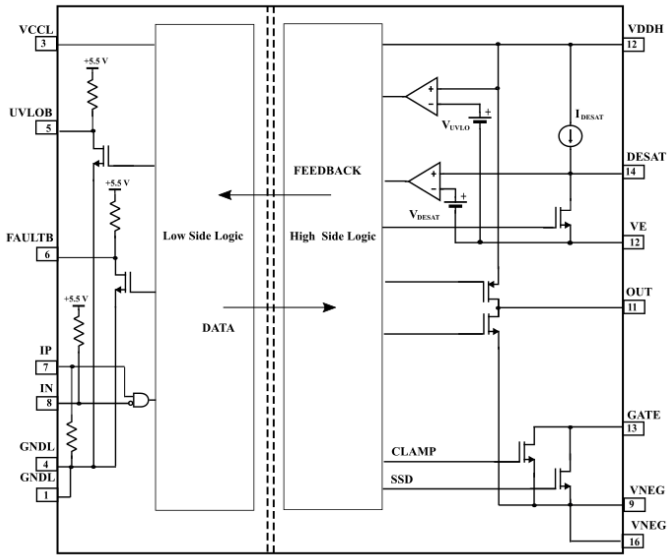


Figure 2- Functional block diagram

PIN	Name	Description
1	GNDL	Low side (LS) ground
2	NC	No connect – (note: *connecting to GND or other signals can result in damage to the IC*)
3	VCCL	Low side (LS) power supply
4	GNDL	Low side (LS) ground
5	UVLOB	Undervoltage lockout, open drain active LOW output
6	FAULTB	Desaturation (Over-current protection) Fault, open Drain active LOW output
7	IP	Non-inverting driver input.[1]
8	IN	Inverting driver input.[2]
9	VNEG	High side (HS) negative supply voltage (Ref. VNEG)
10	GATE	IGBT Gate connection for Miller current clamp and SSD (soft-shutdown) pull-down
11	OUT	Driver output
12	VDDH	High side (HS) positive supply
13	VE	Connected to IGBT emitter
14	DESAT	Desaturation (overcurrent) sensing input
15	NC	No connect, for factory test only
16	VNEG	High side negative supply voltage (Ref. VNEG)

Note:

1) IP input controls signal for the driver output while IN is set to low. The IGBT is turned on if IP is set to high and IN is set to low, otherwise is turned off. A minimum pulse width is required to suppress glitches while controlling the IGBT. An internal pull-down resistor ensures that the IGBT is kept in off-state if terminal IP is left unconnected.
2) IN input control signals for the driver output while IP is set to high. The IGBT is turned on if IN- is set to low, and is turned off if IN- is set to high, while IN is kept high.

5 Specifications

5.1 Absolute maximum rating

Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise specified, all voltages at input IC reference to GNDL, all voltages at output IC reference to VE.

Parameter	Symbol	Min	Max	Unit
Low side power supply	VCCL	-0.3	18	V
Positive power supply of high side	VDDH	-0.3	30	V
Negative power supply of high side	VNEG	-15	0.3	V
Maximum power supply voltage high side (VDDH-VNEG)	V_{MAX_OUT}		36	V
Gate driver output voltage	V_{OUT}	VNEG-0.3	VDDH+0.3	V
Peak source output current[1]	I_{OUT_SOURCE}	/	3.5	A
Peak sink output current[2]	I_{OUT_SINK}	3.5		A
Gate clamping sinking current[3]	I_{CLAMP_SINK}	/	1.2	A
Logic interface at input side (pins UVLOB, FAULTB, IN and IP)	V_{LOGIC}	-0.3	6.5	V
Pin DESAT voltage	V_{DESAT}	-0.3	VDDH+0.3	V
Pin GATE voltage	V_{CLAMP}	-0.3	VDDH+0.3	V
Driver junction temperature	T_J	-40	150	□
Storage temperature	T_S	-40	150	□
Operating temperature	T_A	-40	125	□
Max switching frequency[4]	f_{MAX}		400	kHz
Low side power dissipation	P_{D_IN}		150	mW
High side power dissipation	P_{D_OUT}		580	mW
ESD capability （Human Body Model）	V_{ESD_HBM}	/	2.5	kV
ESD capability （Machine model）	V_{ESD_HBM}	/	200	V
ESD capability (charged device model)	V_{ESD_CDM}	/	500	V
Isolation voltage RMS (1 s testing time)	V_{ISO_RMS}		4.5	kV

Note:
1) The peak output current is measured at maximum pulse width equal to 2.5 µs, maximum duty cycle 1%
2) The sink output current is measured at maximum OFF time equal to 2.5 µs, maximum duty cycle 99%
3) The gate clamp sink current is measured at Maximum OFF time equal to 2.5 µs, maximum duty cycle 99% and voltage between GATE and VNEG equal to 2 V.
4) The load is 1 nF and a 10 Ω resistor.
5) The LS pins are shorted and HS pins are shorted and V_{IO} = 500 V

5.2 Recommended operating conditions

Parameter	Symbol	Min	TYP	Max	Unit
Low side power supply	VCCL	8	12	18	V
High side positive power supply	VDDH-VE	12	-	24	V
High side negative power supply	VNEG-VE	-12	-	0	V
High side bipolar power supply	VDDH-VNEG	-	-	28	V
Inputs witching frequency[1]	f_{SW}			150	kHz
Operating temperature	T_A	-40		125	℃
Input voltage (ON)	V_{in_ON}		3.3	5.5	V
Input voltage (OFF)	V_{in_OFF}		0	0.5	V
Input minimum pulse width[1]	t_{ON}	250			ns

Note:

1) Tested with a load of 10 nF capacitor and a 10 Ω resistor.

5.3 Electrical characteristics

Unless otherwise specified, all Min/Max specification parameters are at recommended operating conditions, all voltages at input IC are referenced to GNDL, all voltages at output IC referenced to V_{NEG}. All typical values at TA = 25 °C, VCCL = 12 V, VDDH-V_{NEG} = 20 V, VE-V_{NEG} = 0 V

5.3.1 Power supply

Parameters	Symbol	MIN	TYP	MAX	Unit
Low side quiescent current driver set to OFF	$I_{Q\_LS\_OFF}$		8	9	mA
Low side quiescent current driver set to ON	$I_{Q\_LS\_ON}$		13.5	14.5	mA
High side quiescent current driver set to OFF	$I_{Q\_HS\_OFF}$		16	17	mA
High side quiescent current driver set to ON	$I_{Q\_HS\_ON}$		16.5	18	mA
UVLO threshold high (rising)	V_{UVLO_H}	11.8	11.9	12.2	V
UVLO threshold low (falling)	V_{UVLO_L}	11.1	11.4	11.7	V
UVLO hysteresis	V_{UVLO_HYS}		0.5		V
Minimum duration for UVLO report[1]	$t_{MIN\_UVLO\_REPORT}$			100	µs
VDDH UVLO to OUT go low delay[1]	t_{UVLO_ON}		5		µs
VDDH UVLO to OUT go high delay[1]	t_{UVLO_OFF}		5		µs
OUT to UVLOB high low communication delay[1]	$t_{HL\_UVLO\_COM\_DEL}$			5	µs
OUT to UVLOB low high communication delay[1]	$t_{LH\_UVLO\_COM\_DEL}$			5	µs

Note:

1) Guaranteed by design. (see Figure 6 thru Figure 8 for definition of the times.)

5.3.2 Logic inputs and outputs

VCCL-GNDL= 12 V; VDDH-VE= 20 V; VNEG-VE= 0 V; -40°<T_J<150°

Parameters	Symbol	MIN	TYP	MAX	Unit
IN inputs current when set to high[1]	I_{IN_H}		-5		µA
IP inputs current when set to high[1]	I_{IP_H}		45		µA
IN inputs current when set to low[2]	I_{IN_L}		-50		µA
IP inputs current when set to low[2]	I_{IP_L}		0		µA
IN input voltage when driver turns OFF	V_{IN_OFF}		2.4		V
IN input voltage when driver turns ON	V_{IN_ON}		2.2		V
IN inputs threshold voltage hysteresis	$V_{IN\_THR\_HYS}$		0.2		V
IP input voltage when driver turns OFF	V_{IP_OFF}		2.2		V
IP input voltage when driver turns ON	V_{IP_ON}		2.5		V
IP inputs threshold voltage hysteresis	$V_{IP\_THR\_HYS}$		0.3		V
FAULTB and UVLOB current when high[1]	I_{DIG_HIGH}		-5		µA
FAULTB and UVLOB current when low[2]	I_{DIG_LOW}		-50		µA
Voltage of UVLOB(FAULTB) pin when sinking 4 mA	V_{DIG_LOW}			300	mV

Note:
1) Pin set to 5 V.
2) Pin set to 1 V.

5.3.3 Gate Driver output characteristics

VCCL-GNDL= 12 V; VDDH-VE= 20 V; VNEG-VE= 0 V; C_L= 100 pF; -40°<T_J<150°

Parameters	Symbol	Conditions	MIN	TYP	MAX	Unit
High level output voltage[1]	V_{OUT_H}			VDDH-0.2		V
Low level output voltage[2]	V_{OUT_L}			VNEG+0.1		V
Peak source output current[3]	I_{OUT_SOURCE}			7.2		A
Peak sink output current[4]	I_{OUT_SINK}			7.6		A
Source output current at	$I_{OUT\_P\_3V}$	$V_{DS\_P\text{-}FET}$ = 3 V[5]		-2		A
	$I_{OUT\_P\_15V}$	$V_{DS\_P\text{-}FET}$ = 15 V[5]		-7		A
Sink output current at	$I_{OUT\_N\_2.5V}$	$V_{DS\_N\text{-}FET}$ = 2.5 V[6]		3.5		A
	$I_{OUT\_N\_6V}$	$V_{DS\_N\text{-}FET}$ = 6 V[6]		6.5		A
Output voltage rise time (10 % to 90%)	t_r	C_L= 10 nF		90		ns
Output voltage fall time (90% to10%)	t_f	C_L= 10 nF		70		ns
Turn ON propagation delay (50% to 50%)	t_{D_ON}			115	150	ns

Turn OFF propagation delay (50% to 50%)	t_{D_OFF}			90	125	ns
Pulsed width distortion[7]			-20		+20	ns
Dead time distortion[8]			-30		+30	ns
Common mode transient immunity Logic High[9]	CMTI_LH			50		kV/µs
Common mode transient immunity Logic Low[9]	CMTI_LL			50		kV/µs

Note:

1) Set voltage on pins IP to 5 V and IN to 0 V and I_{OUT} =-100 mA.
2) Set voltage on pins IP and IN to 0 V and I_{OUT} = 100 mA.
3) The peak output current is measured at maximum pulse width equal to 2.5 µs, maximum duty cycle 1%.
4) The sink output current is measured at maximum OFF time equal to 2.5 µs, maximum duty cycle 99% .
5) See Figure 3
6) see Figure 4
7) Pulse width distortion (PWD) is defined as (t_{D_ON} – t_{D_OFF}) of any given unit.
8) Dead time Distortion (DTD) is defined as (t_{D_OFF} – t_{D_ON}) between any two parts under the same test conditions.
9) V_{CM} = 1500 V

5.3.4 Active Miller clamp

VCCL-GNDL= 12 V; VDDH-VE= 20 V; VNEG-VE= 0 V; C_L= 100 pF; -40°<T_J<150°

Parameters	Symbol	MIN	TYP	MAX	Unit
Soft shutdown current during fault conditions	I_{OUT_FLT}		130		mA
Clamp threshold voltage	V_{CLP_TH}	1.6	1.8	2.4	V
Low level clamp sinking current[1]	I_{CLAMP}		1.7		A
Low level clamp voltage[2]	V_{CLP}		VNEG + 0.3		V

Note:

1) The gate clamp sink current is measured at V_{out} =VE+3 V
2) The voltage is measured at I =100 mA.

5.3.5 Desaturation protection

VCCL-GNDL= 12 V; VDDH-VE= 20 V; VNEG-VE= 0 V; C_L= 100 pF; -40°<T_J<150° (see Figure 10)

Parameters	Symbol	MIN	TYP	MAX	Unit
DESAT threshold voltage	V_{DESAT_TH}		6.5		V
DESAT charging current[1]	I_{DESAT_CH}		0.9		mA
DESAT soft turn-OFF current[2]	$I_{DESAT\_SOFT\_OFF}$		18		mA
Initial DESAT blanking time[3]	$t_{DESAT\_BLANKING}$		0.6		µs
DESAT output mute time	t_{DESAT_MUTE}		3.2		ms
DESAT to FAULTB low delay[3]	$t_{DESAT\_FAULTB\_LOW}$	-	5		µs
DESAT to 90% GATE delay[4]	$t_{DESAT\_90\%\_GATE}$		0.3		µs
DESAT to 10% GATE delay[4]	$t_{DESAT\_10\%\_GATE}$		0.1		µs
DESAT sense to start turn OFF	t_{DESAT_OUT}	-	-	150	ns
Input kept low before FAULTB go high time[3]	$t_{DESAT\_FAULTB\_RESET}$		3.2		ms

Notes:
1) V_{DESAT} = 0 V.
2) V_{DESAT} = 3 V.
3) Guaranteed by design.
4) C_{GATE} =1 nF.

5.3.6 Package characteristics

Parameters	Symbol	MIN	TYP	MAX	Unit
Input to output resistance[1]	R_{IN_OUT}		10^{12}		Ω
Input to output capacitance[1 and 2]	C_{IN_OUT}		1		pF
IC junction to case thermal resistance	Θ_{JC}		TBD		℃/W
IC junction to ambient thermal resistance	Θ_{JA}		75		℃/W

Note:
1) The driver is treated as a two-terminal device. Pin 1 through pin 8 are shorted together and pin 9 through pin 16 are shorted together.
2) f =1 MHz.

5.4 Insulation characteristics

5.4.1 Compliance with UL1577

Parameters	Symbol	Conditions	Value	Unit
External clearance	CLR	Shortest terminal-to-terminal distance through air	>8	mm
External creepage	CPG	Shortest terminal-to-terminal distance across the package surface	>8	mm
Distance through the insulation	DTI	Minimum internal gap (Internal clearance) of the double insulation	>17	μm
Insulation withstand voltage for 1min[1]	VI_{ISO_1MIN}		3750	V_{rms}
Insulation withstand voltage for 1sec[1]	V_{ISO_1SEC}			V_{rms}

Note:
1) The driver is treated as a two-terminal device. Pin 1 through pin 8 are shorted together and pin 9 through pin 16 are shorted together.

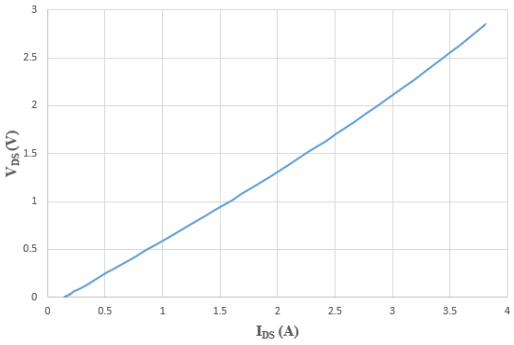


Figure 3 P-FET output characteristics

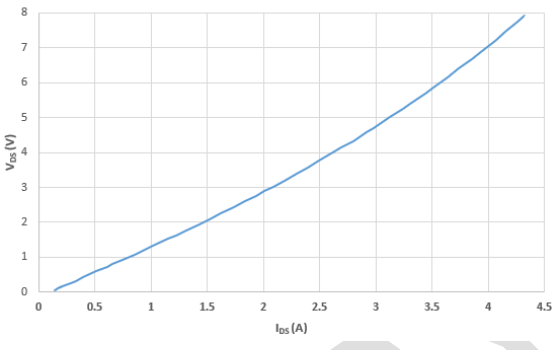


Figure 4 N-FET output characteristics

6 Detailed Description

The SA6880-S is a single channel, galvanically-isolated, 3.5 A / 1200 V gate driver in a SO-16 package. It can be used for fast-switching drive and control of current generation power IGBT's, Si and SiC MOSFETs. Reinforced galvanic isolation is provided by Solantro's on-chip coreless transformer technology. The SA6880-S architecture includes several control features that protect an IGBT in harsh industrial and automotive environments. These integrated features include IGBT desaturation (over-current) sensing with soft-shutdown protection, high-side undervoltage lockout, active Miller-Current clamping and fault reporting to the system controller.

6.1 Power Supplies

Separate power supplies are required for the low and high sides due to the input and output of the SA6880-S being galvanically isolated from each other. The low side power supply is connected to VCCL and GNDL. Its voltage can be between 8 and 18 V. The driver supports bipolar and unipolar supply voltage configurations. For unipolar configuration, VE and VNEG pins are shorted. The driver is typically supplied with a positive 18 V (max 32 V). In a bipolar configuration, the driver is typically supplied with voltages of +18 V on VDDH and VE pins and -5 V on VNEG and VE pins.

6.1.1 Input & Output

6.1.2 Non-Inverting and Inverting Inputs

There are two possible input modes to control an IGBT:

1) Non-inverting mode (IP controls the driver output while IN is set to low).
2) Inverting mode (IN controls the driver output while IP is set to high).
   A minimum input pulse width is defined to filter occasional glitches. Any glitch on IP or IN shorter than 40 ns would be ignored.

The truth table for input and output signals is shown below:

IP	IN	OUT
0	0	0
0	1	0
1	0	1
1	1	0

6.1.3 Rise and fall and propagation delay

The timing diagram for rise and fall time and propagation delay is shown below.

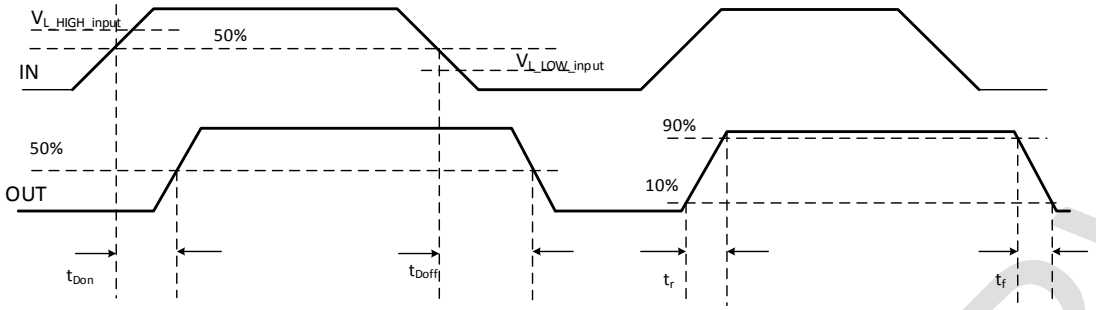


Figure 5 - Propagation delay and rise and fall time

6.1.4 FAULTB and UVLOB outputs

The device has default open-drain FAULTB and UVLOB outputs. The FAULTB input will transition to LOW when an IGBT over-current DESAT fault condition occurs. The UVLOB input will transition to LOW when an UVLO event occurs at the high side power supply. To ensure the low side outputs are HIGH when no faults are detected, pull-up resistors are used.

6.1.5 Driver output

The output driver section provides a rail-to-rail output, it clamps to LOW default. During normal operation, V_{OUT} drives the IGBT gate high or LOW according to the signals applied to IP and IN. The driver provides max 3.5 A sink & source currents.

6.2 Internal protection function

6.2.1 Undervoltage lockout (UVLO)

To ensure correct switching of the power devices, an undervoltage lockout (UVLO) function is integrated in the driver high side. If the high side power supply, VDDH, falls below $VDDH_{UVLO\_L}$, the IGBT is turned OFF and the input signals at IP and IN are ignored until VDDH rises above $VDDH_{UVLO\_H}$. The driver does not turn OFF and ON immediately. The time between UVLO detection until the driver output goes low is "VDDH UVLO to OUT go low delay", t_{UVLO_ON}. The time between VDDH rising above $VDDH_{UVLO\_H}$ to the driver output going high is "VDDH UVLO to OUT go high delay", t_{UVLO_OFF}.

When an UVLO event happens, a report is sent to low side pin UVLOB. The time between the driver output going low to the time pin UVLOB goes low is "OUT to UVLOB high low communication delay", $t_{HL\_UVLO\_COM\_DEL}$. The time between the driver output going high to the time pin UVLOB goes high is "OUT to UVLOB low high communication delay[3]", $t_{LH\_UVLO\_COM\_DEL}$. Figure 6 shows the SA6880-S during UVLO condition for time higher than $t_{MIN\_UVLO\_REPORT}$.

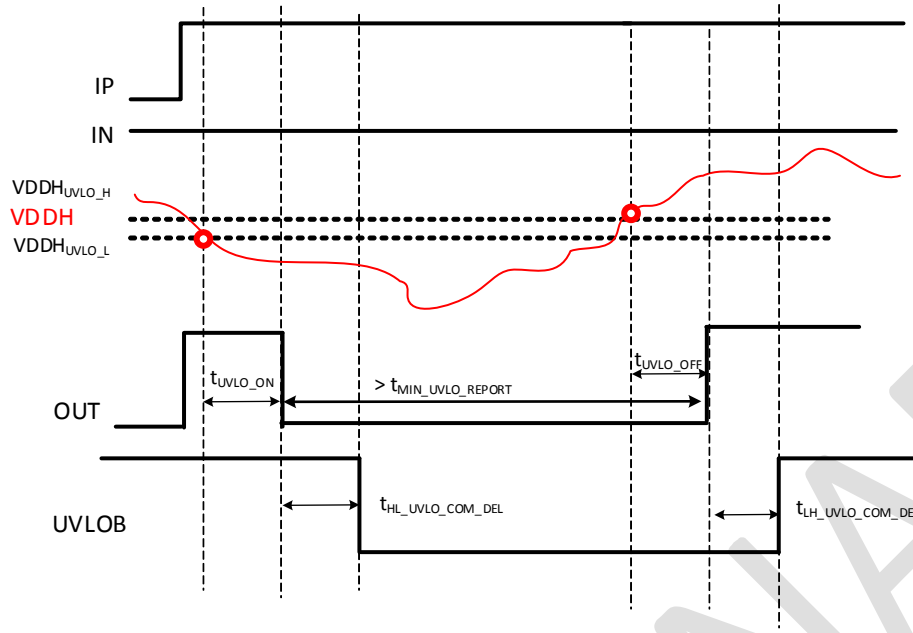


Figure 6 – The SA6880-S during UVLO for time higher than $t_{MIN\_UVLO\_REPORT}$.

When the driver power supply voltage, VDDH, falls below the threshold voltage $VDDH_{UVLO\_L}$ for time smaller than the time t_{UVLO_ON}, the driver is not turned OFF as it is shown in Figure 7. When UVLO is reported and soon after that the driver power supply voltage, VDDH, rises above $VDDH_{UVLO\_H}$, the driver output goes high after time t_{UVLO_OFF}. The report to the low side UVLOB pin is sent after the time $t_{MIN\_UVLO\_REPORT}$ expires, and the pin becomes high after time $t_{HL\_UVLO\_COM\_DEL}$ as shown in Figure 7.

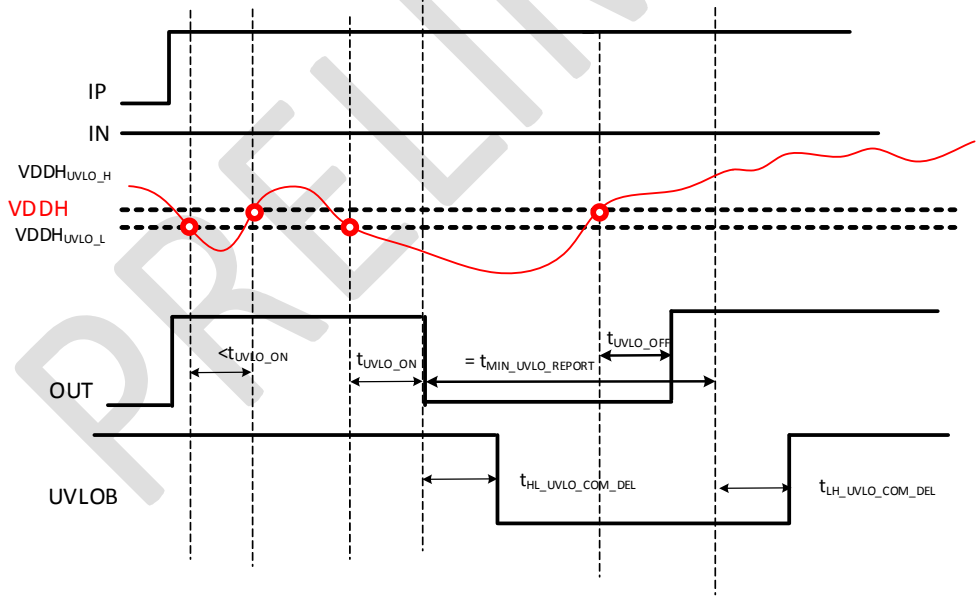


Figure 7 - The SA6880-S during UVLO for time smaller than t_{UVLO_ON} and when the UVLO report is expanded to at least time $t_{MIN\_UVLO\_REPORT}$.

When the SA6880-S is under UVLO condition and VDDH goes high but is not stable, the driver output will not go high until the driver power supply voltage rises above $VDDH_{UVLO\_H}$ for a time longer than t_{UVLO_OFF}. This is shown in Figure 8.

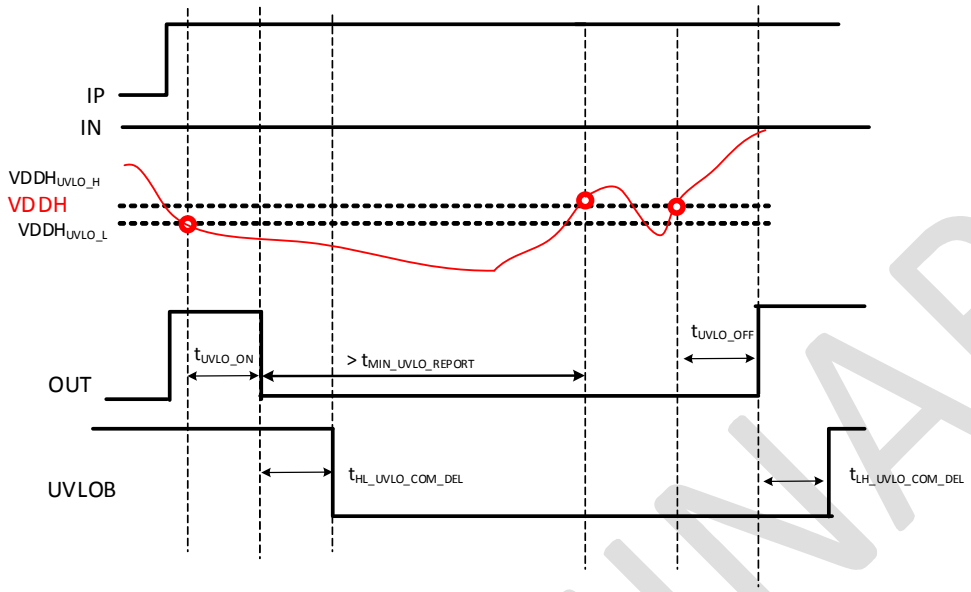


Figure 8 - The SA6880-S under UVLO condition and VDDH goes high but is not stable

6.3 External Protection

6.3.1 Desaturation Protection (DESAT)

The driver has a DESAT input and a de-saturation (over-current) protection function for monitoring the IGBT collector emitter saturation voltage (VCE). The DESAT circuitry must remain disabled for a short time period. The time for the driver to response to DESAT condition is known as blanking time, $t_{DESAT\_BLANKING}$. The blanking time is controlled internally and externally. The blanking time depends on the internal charge current, I_{DESAT_CH}, the DESAT reference threshold voltage, V_{DESAT_TH}, and the DESAT capacitor.
The capacitor, C_5, between the DESAT and VE pins start to charge with current I_{DESAT_CH}. A Zener diode, D_2, is pleased in parallel with the capacitor C_5 to avoid any voltage overshoot between DESAT and VE pins.

When the voltage at DESAT pin becomes higher than V_{DESAT_TH}, soft turn OFF of the IGBT occurs. The capacitor value determines the blanking time $t_{DESAT\_BLANKING}$.

$$t_{DESAT\_BLANKING} = \frac{c_5 V_{DESAT\_TH}}{I_{DEASAT\_CH}}$$

The DESAT pin is connected to the IGBT collector by a diode, D_1, and a resistor R_1 as shown in Figure 9. The diode blocks the voltage across the IGBT during its off state. The diode should be fast, to respond to the fault, and have minimum reverse recovery time to prevent a false trip. For very high IGBT blocking voltages, in the kilovolt range, multiple diodes in series could be used. Multiple diodes can also be used to adjust the actual DESAT threshold voltage.

$$V_{ACTUAL\_DESAT\_TH} = V_{DESAT\_TH} - I_{DESAT\_CH}\, R_1 - nV_F,$$

where n is number of diodes and V_F is a diode forward voltage drop.

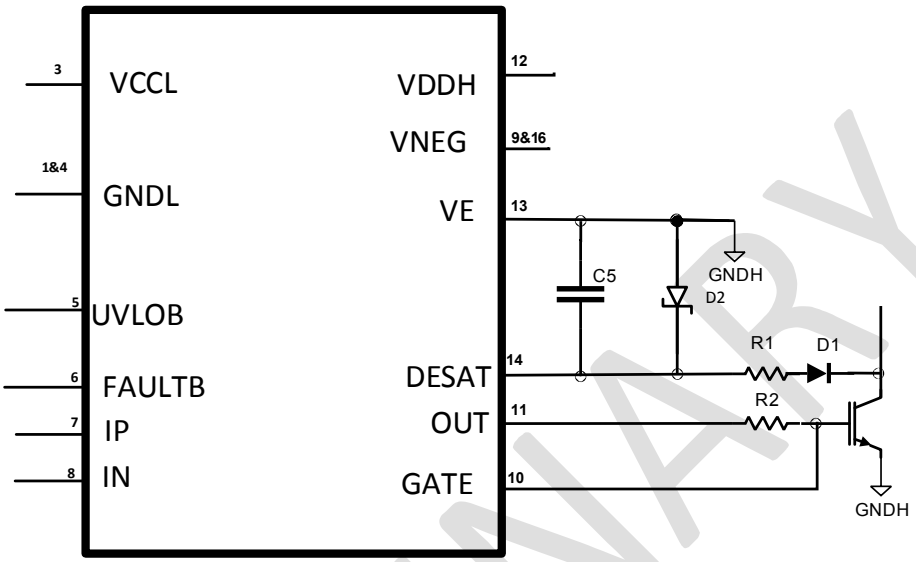


Figure 9 – DESAT circuitry

The propagation delay from DESAT sense to starting soft turn OFF, t_{DESAT_OUT}, is less than 150 ns (max). The soft turn OFF current, $I_{DESAT\_SOFT\_OFF}$ is 53 mA typically. When the GATE voltage becomes equal to V_{CLP_TH}, the GATE pin is shorted to VNEG.

When desaturation protection is activated, the FAULTB pin on the low side should be set to LOW. The time from the DESAT sense and setting the FAULTB pin to LOW, $t_{DESAT\_FAULTB\_LOW}$, is less than 2 µs (typical). During DESAT, the input of the driver is muted. The time from when DESAT exceeds the threshold value to the time the input is muted is t_{DESAT_MUTE}. When the mute time expires, the input signal should be kept LOW for the fault status to return high. This time is $t_{DESAT\_FAULTB\_RESET}$. The time from exceeding the threshold value to 90 % of the GATE voltage and the time from exceeding the threshold value to 10 % of the GATE voltage depends on the gate capacitance, C_{GATE}.

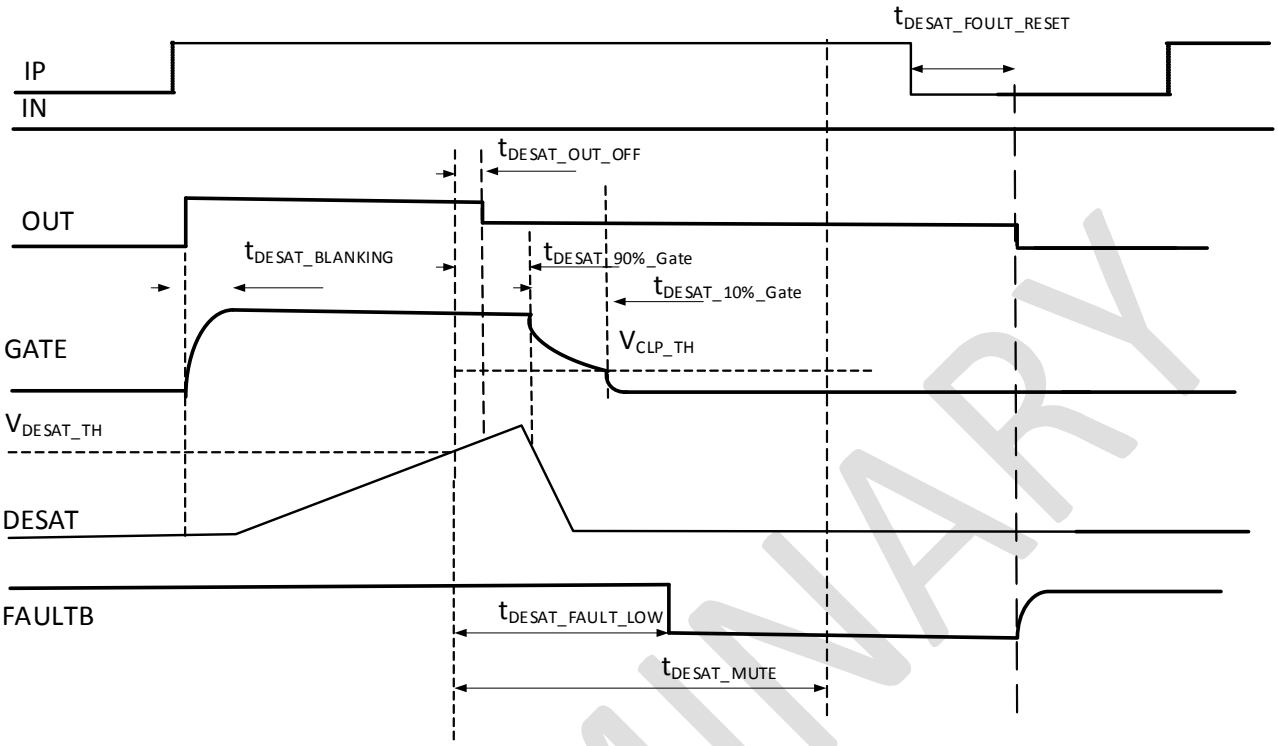


Figure 10- Driver time diagram during DESAT conditions (the timescale is not proportional)

6.3.2 Active Miller clamping

When the IGBT is turned off and the gate voltage is reduced to the Miller clamp threshold voltage, V_{CLP_TH}, the active Miller clamp circuit monitoring the IGBT gate voltage, connects the IGBT gate to the emitter.
The Miller clamp threshold voltage is typically 2.1 V relative to VNEG (max 2.4 V). The clamping current is typically 0.9 A.

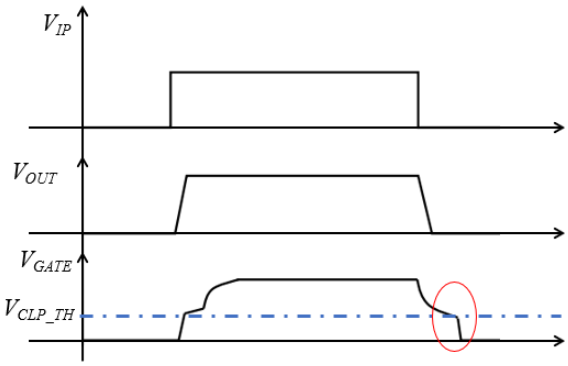


Figure 11- *Voltages on pins IP, OUT and GATE during driver turn ON and OFF.*

7 Isolation

SA6880-S utilizes a magnetically coupled, galvanically isolated, barrier that electrically isolates circuitry between the low side and the high side. The on-chip coreless transformers prevent unwanted AC or DC signals from traveling from one side to the other. They also transmit the switching information between the input chip and output chip and other signals (DESAT and UVLO). The coreless transformer technology provides short propagation delays, excellent delay matching, and strong robustness for driving IGBTs and SiC MOSFETs.

8 Common mode transient immunity

Common mode transient immunity (CMTI) is a key specification parameter of isolated drivers. CMTI is the maximum tolerable rate of the rise or fall of the common mode voltage, V_{CM}. SA6880-S is implemented in an advanced Silicon-on-Insulator high-voltage process (SOI-BCD) which allows the driver to operate latch-up free (by design), even in the presence of large over/under-shoot voltage excursions. As a result, the driver is immune to the noise generated by large dv/dt and di/dt variations during IGBTs or SiC MOSFETs switching.

9 Interlock protection and glitch filtering

The SA6880-S integrates two functions (interlock protection and glitch filtering) to protect from undesired shoot through operation. Figure 12 shows the SA6880-S digital top block diagram. The DEADTIME block is used for interlock protection and GLITCH Filter block for filtering.

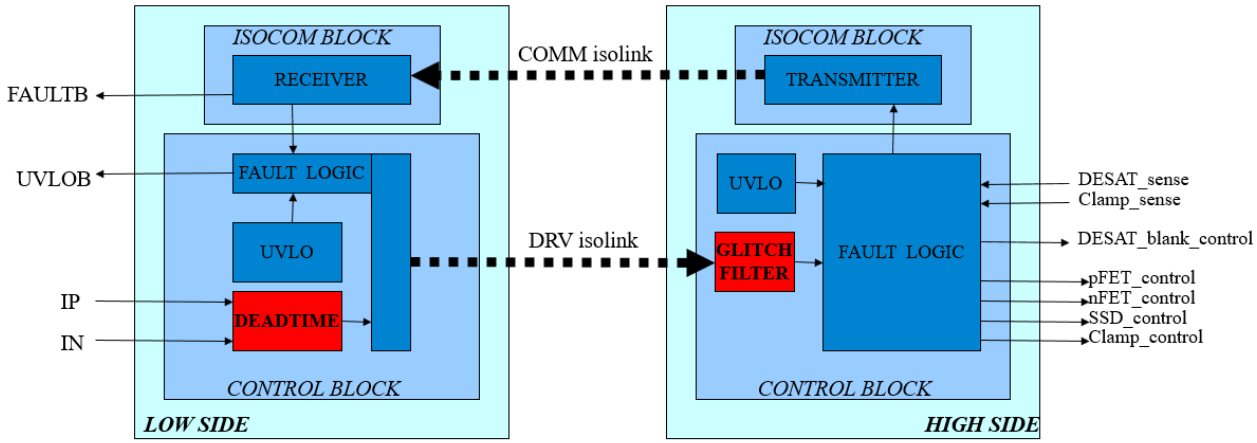


Figure 12 - SA6880-S digital top block diagram

9.1 Interlock protection

IGBTs are mostly used in three-phase applications such as variable-frequency drives, uninterruptible power supply, solar inverters, and other similar inverter applications. To ensure proper operation of an inverter, the switches of an inverter leg should not switch simultaneously. Dead time is used before the transition of high and low-side switch operation to avoid shoot-through. Interlock protection is integrated in SA6880-S drivers to prevent shoot-through. Avoiding shoot-through operation prevents unwanted additional losses or even failure

of power devices. The interlock protection will prevent both switches from being ON if there is an error in calculation of the programmed dead time.
Figure 13 shows one leg of three-phase converter. Each IGBT has its own driver. When the drivers are connected according to Figure 14, a minimum dead time of 0.8 µs will be introduced before the switches change state. This feature prevents a shoot-through condition.

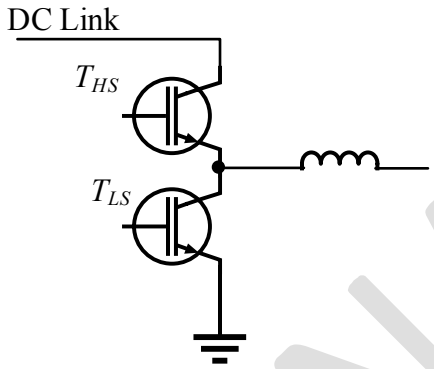


Figure 13 A leg of three-phase inverter

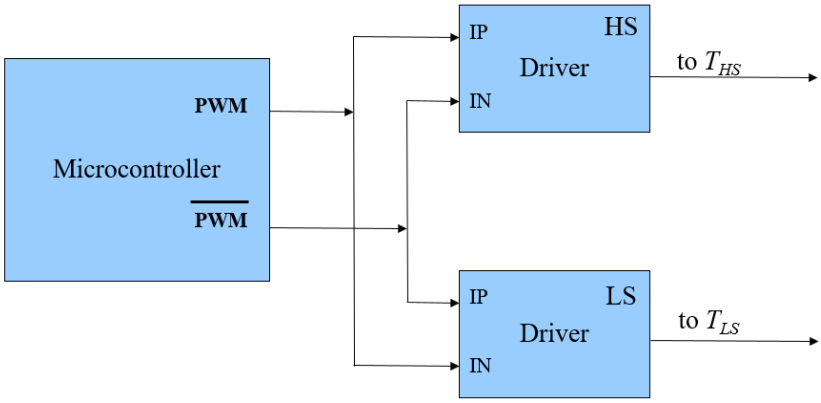


Figure 14 High and low side drivers' connections for interlock protection

Three examples are shown bellow:

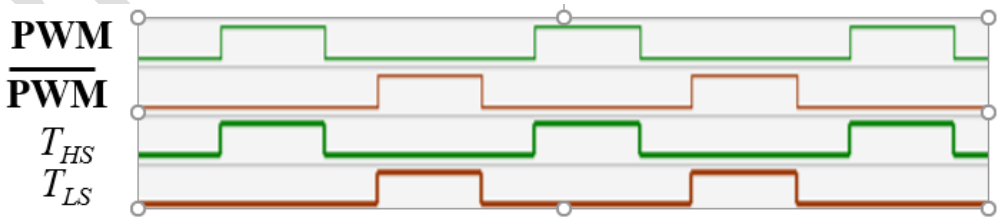


Figure 15 Driver inputs have enough deadtime. Original deadtime from the inputs preserved by the driver.

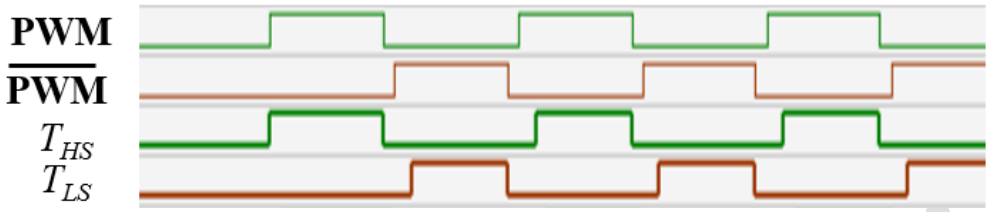


Figure 16 Driver inputs have some deadtime, but less than the minimum deadtime of the driver. Minimum deadtime ensured by the driver.

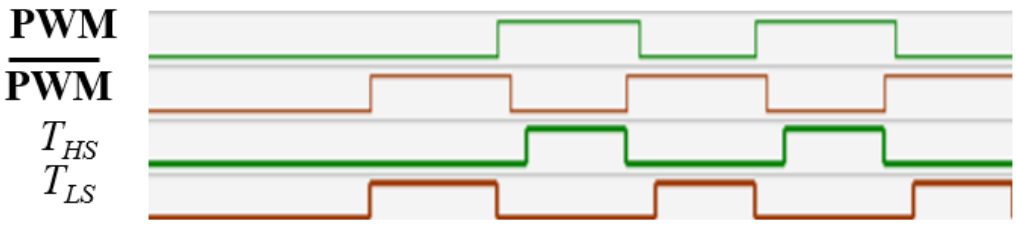


Figure 17 Driver inputs overlapping. Minimum deadtime ensured by the driver.

9.2 Glitch filtering

High-power applications are susceptible to noise from the large voltage and current transients in the power switches. This noise could propagate to the gate drivers' control signals causing the driver to turn ON when it should be OFF. The spike may be so small and insufficient to fully turn ON the power device, due to the power switch input capacitance and gate resistance causing high conduction loss. If in a half-bridge configuration, the two power devices are switching complementary and therefore, shoot-through is a concern if they are accidentally ON at the same time. During shoot-through, high current flows through the devices which can damage the power switches. The SA6880-S has an input glitch filter that rejects the high frequency noise, so the driver output does not see glitches shorter than 30 - 40 ns. This corresponds to a 30 MHz switching frequency, which is significantly higher than the switching frequency in most IGBT or SiC MOSFET –based applications. The glitch filter rejects positive and negative pulses preventing the accidental turning ON or OFF of the switch. The glitch filter integrated within the gate driver improves driver performance in noisy environments and protects the device from possible failure.

Figure 18 shows the input drivers' signals when glitches with 1-clock (20 ns) duration are present. Also, there is no dead time between the input signals. In the output signal the glitches (1) are removed and the dead time is introduced (2).

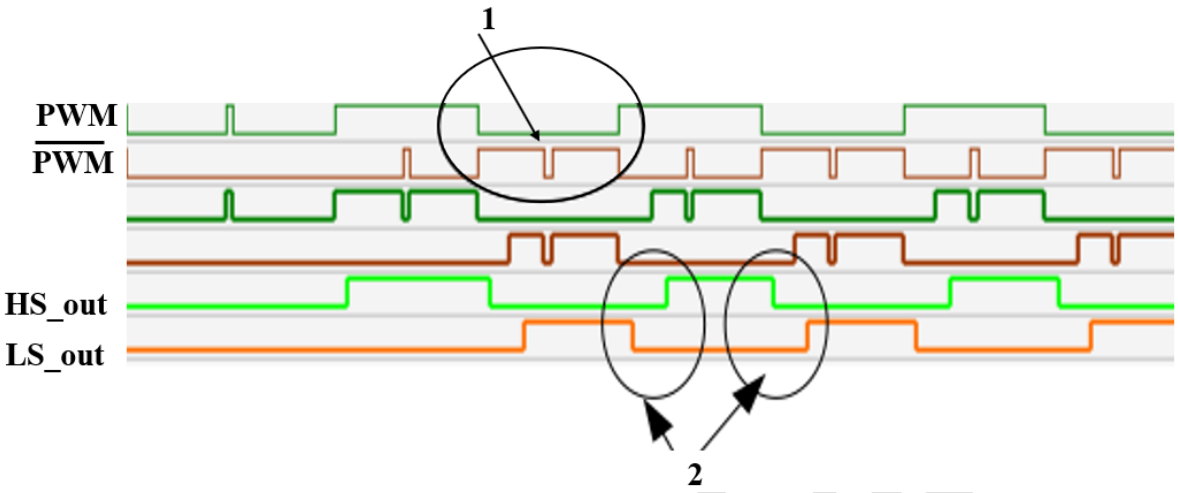


Figure 18 Input and output drivers' signals when 1-clock (20 ns) glitches are present and not dead time of the input signal.

10 SA6880-S - Recommended Application Circuit

Figure 19 shows a recommended application circuit for the SA6880-S.

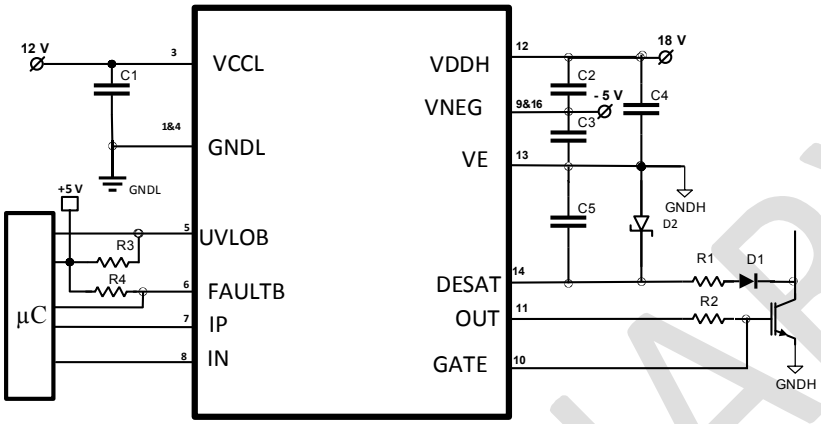


Figure 19- SA6880-S recommended application circuit.

Capacitors C1 and C2 are decoupling capacitors (recommended value = 1 µF). Capacitors C3 and C4 are decoupling capacitors (recommended value = 10 µF). The DESAT circuit includes a high voltage di*ode* (D_1), a 1 kΩ resistor (R_1) and 220 nF capacitor (C_5). Diode D_2 prevents the voltage on the DESAT pin from falling 0.4 V below the voltage on VE pin.

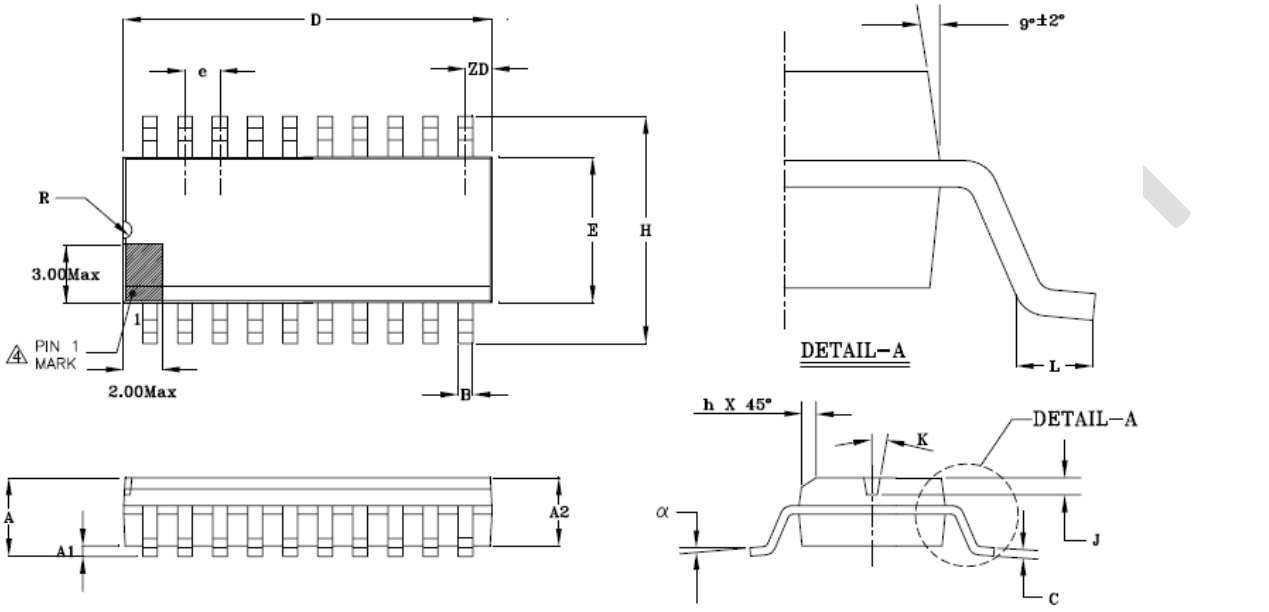
The gate resistor (R_2) limits the gate charge current and indirectly controls the IGBT collector voltage rise and fall times. Its value depends on the IGBT type. The recommended value is 5 Ω.

The pull-up resistors, R4 and R5 ensure the low side outputs are high when no faults are detected. Their recommended value is 3.3 kΩ.

11 Package Outline Drawings

The SA6880-S uses an SOIC16 Wide-Body package as shown below:

SOICW 16LD



SYMBOL	SOIC-16LD	
	MILLIMETERS	
	MIN	MAX
A	2.44	2.64
A1	0.10	0.30
A2	2.24	2.44
B	0.36	0.46
C	0.23	0.32
D	10.11	10.31
E	7.40	7.60
e	1.27 BSC	
H	10.11	10.51
h	0.31	0.71
J	0.53	0.73
K	7° BSC	
L	0.51	1.01
R	0.63	0.89
ZD	0.66 REF	
α	0°	8°

NOTES :

1. LEAD COPLANARITY SHOULD BE 0 TO 0.10MM (.004") MAX.
2. PACKAGE SURFACE FINISHING :
   (2.1) TOP : MATTE (CHARMILLES #18~30).
   (2.2) BOTTOM : SMOOTH OR MATTE (CHARMILLES #12~27).
3. ALL DIMENSIONS EXCLUDING MOLD FLASHES AND END FLASH FROM THE PACKAGE BODY SHALL NOT EXCEED 0.25MM (.010") PER SIDE(D).

⚠ DETAIL OF PIN #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

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SA6880-S