A81805 and A81805-1

40 V, 2.5 A, Synchronous Buck Regulator with Low EMI and 6 µA Quiescent Current

FEATURES AND BENEFITS

- AEC-Q100 Grade 0 qualified
- **V_{IN} Range:** 3.5 to 36 V operating, 40 V transient
- **V_{OUT}:** 3.3 V, ±1.5% accuracy, –40°C to 150°C (5 V for the A81805-1)
- **Up to 2.5 A** of continuous output current
- **High Efficiency:** 92%, 12 V input to 5 V output, 1 A, 2 MHz
- **Integrated Compensation:** Eliminates three external components
- **Low-Power (LP) mode:** 6 µA I_Q from V_{IN} at no load, automatic transition from LP to PWM mode
- **Fixed-Frequency PWM (f_{OSC}):** 400 kHz to 2.5 MHz programmable
- **Synchronizable Switching Frequency (400 kHz to 2.5 MHz):** PLL-based, f_{SYNC} can be above or below f_{OSC}
- **Spread spectrum applied:** Helps to pass CISPR25 class 5
- Internally set Soft-Start
- Accurate ENABLE input threshold
- Open-drain PGOOD output with delay
- Pre-bias startup capable
- Maximized duty cycle at low V_{IN} improves dropout
- Overvoltage, pulse-by-pulse current limit, hiccup mode short-circuit, and thermal protections
- Robust FMEA: pin open/short and component faults

APPLICATIONS

- Infotainment
- Battery-powered systems
- Industrial systems
- Container tracking
- Handheld instruments
- Instrument clusters
- Audio systems
- ADAS

DESCRIPTION

The A81805 is a full-featured, 2.5 A, low EMI, DC-DC regulator designed to satisfy demanding power delivery requirements of automotive and industrial applications. The A81805 and A81805-1 include all the control and protection circuitry to produce a robust 3.3 V or 5 V DC output voltage respectively, with ±1.5% output voltage accuracy over the full operating temperature range.

Fixed-frequency peak current-mode control is employed to ensure rapid response to load and line transients with programmable switching frequency from 400 kHz to 2.5 MHz. Connect the FSET pin to VCC for a 2.2 MHz switching frequency. The A81805 can also synchronize to an external clock applied to the SYNC pin ranging from 400 kHz to 2.5 MHz.

Spread spectrum operation (dithering) is applied, offering lower EMI levels.

Low power (LP) mode maintains the output voltage at no load or very light load conditions while drawing only micro-amps from V_{IN}. No-load input current is a mere 6 µA when operating from a standard 12 V battery. The A81805 automatically transitions between PWM and LP modes.

Integrated loop compensation components simplify the design process while providing fast response to load and line transients.

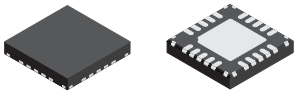
The A81805 has an internally set soft-start and an open-drain power good output.

The accurate ENABLE input has programmable turn-on and turn-off thresholds and a low shutdown current of 1 µA if driven low.

Extensive protection features include pulse-by-pulse current limit, hiccup mode short-circuit protection, BOOT open/short voltage protection, V_{IN} undervoltage lockout, V_{OUT} overvoltage protection, and thermal shutdown.

The A81805 is supplied in a thermally enhanced, 4 mm × 4 mm × 0.75 mm 20-pin wettable flank QFN package (suffix “ES”) with exposed power pad.

PACKAGE



20-contact QFN
4 mm × 4 mm × 0.75 mm
with exposed thermal pad
and wettable flank
(suffix ES)

Not to scale

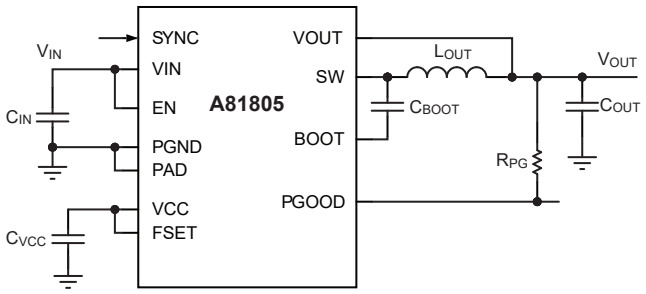


Figure 1: Typical Application Diagram

SELECTION GUIDE

Part Number	V_{OUT} (V)	Package	Packing [1]	Lead Frame
A81805KESJSR	3.3	20-pin 4 mm × 4 mm × 0.75 mm QFN with exposed thermal pad and wettable flank	6000 pieces per 7-inch reel	100% matte tin
A81805KESJSR-1	5			

[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
VIN, EN, PGOOD	V_{IN}, V_{EN}, V_{PGOOD}		–0.3 to 40	V
VOUT	V_{OUT}		-0.3 to 20	V
SW	V_{SW}	Continuous	–0.3 to V_{IN} + 0.3 [3]	V
		V_{IN} ≤ 36 V, t < 50 ns	–1.0, V_{IN} + 2	V
BOOT	V_{BOOT}	Continuous	V_{SW} – 0.3 to V_{SW} + 5.5	V
		t < 1 ms	V_{SW} – 0.3 to V_{SW} + 7.0	V
All other pins			–0.3 to 5.5	V
Operating Junction Temperature	$T_{J(max)}$		–40 to 150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
[3] This voltage is a function of temperature.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [4]	Value	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	37	°C/W
		On Allegro Evaluation Board [5]	31	°C/W
Junction-Case Thermal Resistance	$R_{\theta JC}$	On Allegro Evaluation Board [5]	8	°C/W

[4] Additional thermal information available on the Allegro website.
[5] See Figure 10: PCB Reference Design.

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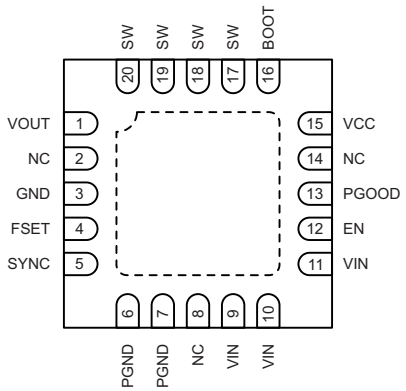
TERMINAL DIAGRAM AND TERMINAL LIST



ES-20 Package Terminals

Terminal List

Number	Name	Function
1	VOUT	Output voltage feedback path for the regulator. Powers the internal LDO when the output voltage level is in regulation. Connect this pin to the output of the regulator.
2	NC	No connect.
3	GND	Analog ground pin.
4	FSET	Switching frequency programming pin. A resistor, R_{FSET}, from this pin to GND sets the switching frequency, f_{SW}. Connect FSET directly to VCC to program a fixed 2.2 MHz (typical) frequency.
5	SYNC	PWM mode switching frequency pin. Applying an external clock (at SYNC pin) forces PWM mode and synchronizes the PWM switching frequency with dither to the external clock.
6, 7	PGND	Power ground pins.
8	NC	No connect.
9, 10, 11	VIN	Input voltage pin. Place a small ceramic bypass capacitor from VIN to GND very close to this pin.
12	EN	ENABLE pin with a hysteretic comparator with an accurate 1.2 V (typical) threshold. Connect EN directly to VIN for “always-on” applications and pull to GND to disable the converter.
13	PGOOD	Power Good open-drain output signal. If the output voltage is out of range (undervoltage or overvoltage), this pin will be asserted low.
14	NC	No connect.
15	VCC	Internal voltage regulator bypass capacitor pin. Connect a 4.7 µF ceramic capacitor from VCC to PGND very close to this pin.
16	BOOT	High-side N-channel MOSFET drive supply pin. Connect a 100 nF ceramic capacitor from BOOT to SW.
17, 18, 19, 20	SW	Regulator switch node output pins. Connect these pins to the power inductor and keep this node small to minimize EMI.
–	PAD	Exposed thermal pad. Connect to PCB PGND plane for best thermal performance.

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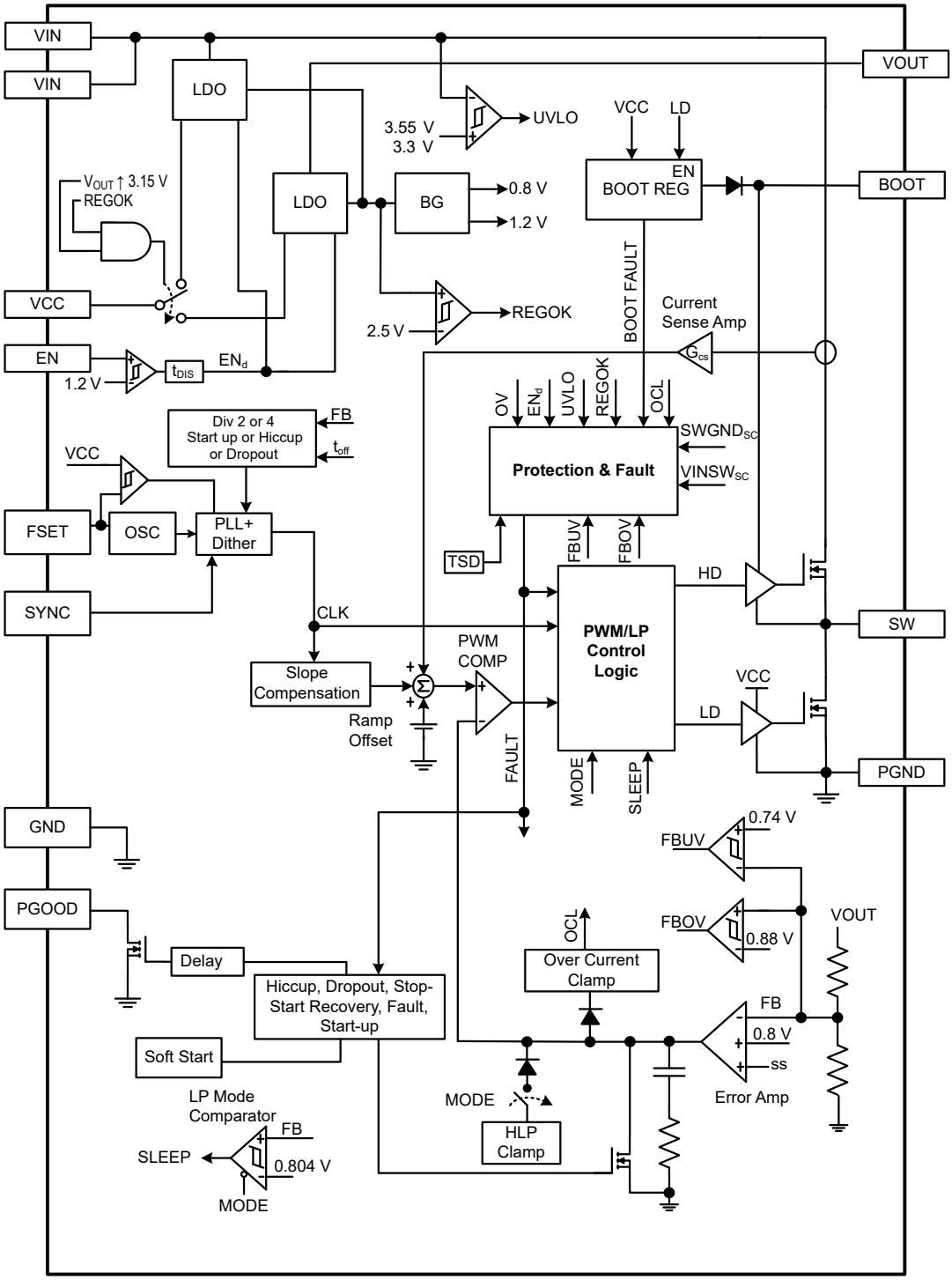
FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS: Valid at 3.5 V ≤ V_{IN} ≤ 36 V, −40°C ≤ T_J ≤ 150°C, unless otherwise specified.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
INPUT SUPPLY						
Input Voltage Range	V_{IN}	V_{IN} must first rise above $V_{UVLO(ON)(MAX)}$	3.5	–	36	V
Undervoltage Lockout (UVLO) Start	$V_{UVLO(ON)}$	V_{IN} rising	3.35	3.55	3.8	V
Undervoltage Lockout (UVLO) Stop	$V_{UVLO(OFF)}$	V_{IN} falling	3.1	3.3	3.5	V
Undervoltage Lockout Hysteresis	$V_{UVLOHYS}$		–	250	–	mV
INPUT SUPPLY CURRENT						
Input Shutdown Current [1]	$I_{IN(SD)}$	V_{IN} = 12 V, V_{EN} = 0 V, V_{SW} = V_{IN}, T_J = 25°C	–	1	2.9	µA
Input Current, PWM Mode [1]	$I_{IN(PWM)}$	V_{IN} = 12 V, V_{EN} = 2 V, no load, no switching	–	5	6.5	mA
3.3 V_{OUT} LP Input Current [1][2]	$I_{LP(3.3V)}$	V_{IN} = 12 V, I_{OUT} = 0 A, T_J = 25°C	–	6	–	µA
		V_{IN} = 12 V, I_{OUT} = 50 µA, T_J = 25°C	–	24.3	–	µA
5.0 V_{OUT} LP Input Current [1][2]	$I_{LP(5.0V)}$	V_{IN} = 12 V, I_{OUT} = 0 A, T_J = 25°C	–	7.5	–	µA
		V_{IN} = 12 V, I_{OUT} = 50 µA, T_J = 25°C	–	40	–	µA
REGULATION ACCURACY						
V_{OUT} Voltage Accuracy	$V_{OUT(ACC)}$	−40°C < T_J < 150°C, V_{IN} = 12 V (A81805)	3.251	3.3	3.349	V
		−40°C < T_J < 150°C, V_{IN} = 12 V (A81805-1)	4.926	5	5.074	V
SWITCHING FREQUENCY AND DITHERING (FSET PIN)						
PWM Switching Frequency	f_{OSC}	FSET connected to VCC	1.98	2.2	2.42	MHz
		R_{FSET} = 14.3 kΩ	1.935	2.15	2.365	MHz
		R_{FSET} = 34 kΩ	0.9	1	1.1	MHz
		R_{FSET} = 71.5 kΩ	450	500	550	kHz
		R_{FSET} = 86.6 kΩ	360	410	460	kHz
		External clock on SYNC pin at $f_{SW(SYNC)}$	–	$f_{SW(SYNC)}$	–	kHz
Dropout Switching Frequency	f_{DROP}		–	f_{OSC} / 2	–	kHz
PWM Frequency Dither Range	$f_{DITH(RNG)}$		–	±5	±6.5	% of f_{OSC}
PWM Dither Modulation Frequency	$f_{DITH(FREQ)}$		–	±0.5	–	% of f_{OSC}
PULSE WIDTH MODULATION (PWM) TIMING AND CONTROL						
Minimum Controllable SW On-Time	$t_{ON(MIN)}$	V_{IN} = 12 V, I_{OUT} = 0.5 A, V_{BOOT} – V_{SW} = 3.3 V, T_J = 25°C	–	45	70	ns
Minimum SW Off-Time	$t_{OFF(MIN)}$	V_{IN} = 12 V, I_{OUT} = 0.5 A, T_J = 25°C	–	70	95	ns
LOW POWER (LP) MODE						
LP Output Voltage Ripple [2][3]	$V_{PP(HLP)}$	LP Mode, 8 V < V_{IN} < 16 V, C_{OUT} = 47 µF	–	–	50	mV
INTERNAL MOSFET PARAMETERS						
High-Side On Resistance	$R_{DSON(HS)}$	T_J = 25°C, V_{IN} = 12 V, V_{BOOT} – V_{SW} = 3.3 V, I_{DS} = 1 A	–	170	200	mΩ
Low-Side On Resistance	$R_{DSON(LS)}$	T_J = 25°C, V_{IN} = 12 V, I_{DS} = 1 A	–	130	160	mΩ
High-Side Leakage Current [1]	$I_{LKG(HS)}$	T_J = 25°C, V_{IN} = 12 V, V_{EN} = 0 V, V_{SW} = 0 V	–	–	3.5	µA
Low-Side Leakage Current [1]	$I_{LKG(LS)}$	T_J = 25°C, V_{IN} = 12 V, V_{EN} = 0 V, V_{SW} = 12 V	–	–	1.5	µA
Gate Drive Non-Overlap Time	t_{NO}	V_{BOOT} – V_{SW} = 3.3 V	–	5	–	ns
Switch Node Rising Slew Rate	SRHS	12 V < V_{IN} < 16 V, V_{BOOT} – V_{SW} = 3.3 V	–	4	–	V/ns

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ELECTRICAL CHARACTERISTICS (continued): Valid at 3.5 V ≤ V_{IN} ≤ 36 V, −40°C ≤ T_J ≤ 150°C, unless otherwise specified.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
MOSFET CURRENT PROTECTION THRESHOLDS						
High-Side Current Limit	$I_{LIM(HS)}$		3.1	3.8	4.5	A
Low-Side Negative Current Limit [4]	$I_{LIM(LSx)}$		–	1.7	–	A
SYNCHRONIZATION INPUT (SYNC PIN)						
Synchronization Frequency Range	$f_{SW(SYNC)}$	R_{FSET} tuned accordingly	0.4	–	2.5	MHz
SYNC Duty Cycle	DC_{SYNC}		20	50	70	%
SYNC Pulse Width	t_{PWSYNC}		80	–	–	ns
SYNC Voltage Thresholds [4]	$V_{SYNC(HI)}$	V_{SYNC} rising	–	1.35	1.5	V
	$V_{SYNC(LO)}$	V_{SYNC} falling	0.8	1.2	–	V
SYNC Hysteresis	$V_{SYNC(HYS)}$	$V_{SYNC(HI)} - V_{SYNC(LO)}$	–	150	–	mV
SYNC Pin Current [1]	I_{SYNC}	V_{SYNC} = 5 V	–	1	–	µA
SOFT-START						
Soft-Start Delay Time [4]	t_{dSS}		–	600	–	µs
Soft-Start Ramp Time [4]	t_{SS}		–	880	–	µs
Soft-Start Frequency Foldback	$f_{SW(SS)}$	0 V < V_{OUT} < 0.825 V, 3.3 V_{OUT} option	–	f_{OSC}/4	–	–
		0.825 V < V_{OUT} < 1.65 V, 3.3 V_{OUT} option	–	f_{OSC}/2	–	–
		1.65 V < V_{OUT}, 3.3 V_{OUT} option	–	f_{OSC}	–	–
		0 V < V_{OUT} < 1.25 V, 5 V_{OUT} option	–	f_{OSC}/4	–	–
		1.25 V < V_{OUT} < 2.5 V, 5 V_{OUT} option	–	f_{OSC}/2	–	–
		2.5 V < V_{OUT}, 5 V_{OUT} option	–	f_{OSC}	–	–
HICCUP MODE						
High-Side Overcurrent Count	HIC_OC		–	120	–	f_{OSC} count
SW Short-to-Ground Count	HIC_SW,GND		–	3	–	f_{OSC} count
BOOT Over/Undervoltaage Count [5]	HIC_{BOOT}		–	120	–	f_{OSC} count
Hiccup Period [2]	t_{HIC}		–	20	–	ms
OUTPUT VOLTAGE PROTECTION THRESHOLDS (V_{OUT}, OV, UV)						
V_{OUT} Overvoltage Threshold in PWM Mode	$V_{OUT(OV)}$	V_{OUT} rising, 3.3 V_{OUT} option	3.45	3.55	3.65	V
		V_{OUT} rising, 5 V_{OUT} option	5.25	5.375	5.5	V
V_{OUT} Overvoltage Hysteresis in PWM Mode	$V_{OUT(OV,HYS)}$	V_{OUT} falling, relative to $V_{OUT(OV)}$, 3.3 V_{OUT} option	–	40	–	mV
		V_{OUT} falling, relative to $V_{OUT(OV)}$, 5 V_{OUT} option	–	94	–	mV
V_{OUT} Undervoltage Threshold in PWM Mode	$V_{OUT(UV)}$	V_{OUT} falling 3.3 V_{OUT} option	2.95	3.05	3.15	V
		V_{OUT} falling, 5 V_{OUT} option	4.47	4.625	4.78	V
V_{OUT} Undervoltage Hysteresis in PWM Mode	$V_{OUT(UV,HYS)}$	V_{OUT} rising, relative to $V_{OUT(UV)}$, 3.3 V_{OUT} option	–	40	–	mV
		V_{OUT} rising, relative to $V_{OUT(UV)}$, 5 V_{OUT} option	–	94	–	mV
V_{OUT} Undervoltage Threshold in LP Mode [2]	$V_{OUT(UV,HLP)}$	V_{OUT} falling, 3.3 V_{OUT} option	2.75	2.9	3.05	V
		V_{OUT} falling, 5 V_{OUT} option	4.15	4.375	4.6	V

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ELECTRICAL CHARACTERISTICS (continued): Valid at 3.5 V ≤ V_{IN} ≤ 36 V, −40°C ≤ T_J ≤ 150°C, unless otherwise specified.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
POWER GOOD OUTPUT (PGOOD PIN)						
PGOOD Startup (SU) Delay	$t_{dPG(SU)}$	Increasing V_{OUT} due to startup	–	30	–	µs
PGOOD Undervoltage (UV) Delay	$t_{dPG(UV)}$	Decreasing V_{OUT}	100	120	–	µs
PGOOD Overvoltage (OV) Delay	$t_{dPG(OV)}$	After overvoltage event	–	310	–	µs
PGOOD Low Output Voltage	$V_{PG(L)}$	I_{PGOOD} = 5 mA	–	200	400	mV
PGOOD Leakage Current [1]	$I_{PG(LKG)}$	V_{PGOOD} = 5.5 V	–	–	2	µA
EN PIN INPUT						
EN High Threshold	$V_{EN(HI)}$	V_{EN} rising	1.14	1.2	1.26	V
EN Input Hysteresis	$V_{EN(HYS)}$	V_{ENHI} – V_{ENLO}	150	200	250	mV
Disable Delay	t_{dDIS}	V_{EN} transitions low to when SW stops	–	155	–	µs
EN Pin Input Current	I_{VEN}	V_{EN} = 5 V	0.8	1.6	2.4	µA
BOOT REGULATOR (BOOT PIN)						
BOOT Charging Frequency	f_{BOOT}		–	f_{OSC}	–	–
BOOT Voltage	V_{BOOT}	V_{IN} = 12 V, V_{BOOT} – V_{SW}	–	3.2	3.66	V
INTERNAL REGULATOR (VCC PIN)						
VCC Voltage	V_{CC}	V_{OUT} = 3.3 V, 3.3 V option	2.85	3.2	3.5	V
		V_{OUT} = 5 V, 5 V option	3.1	3.3	3.66	V
THERMAL SHUTDOWN PROTECTION (TSD)						
TSD Rising Threshold [2]	T_{TSD}	T_J rising, PWM stops immediately	155	170	–	°C
TSD Hysteresis [2]	T_{TSDHYS}	T_J falling, relative to T_{TSD}	–	20	–	°C

[1] Negative current is defined as coming out of the node or pin, positive current is defined as going into the node or pin.
[2] Ensured by design, characterization, and statistical correlation; not production tested.
[3] Validated using component values shown in Table 1: Recommended External Filter Component Values.
[4] Limits ensured by design, characterization, and statistical correlation. Only functionally tested in production.
[5] Only for protection at startup.

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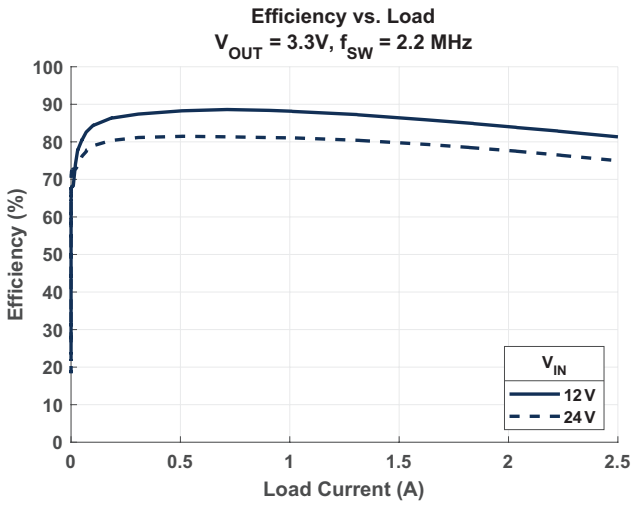
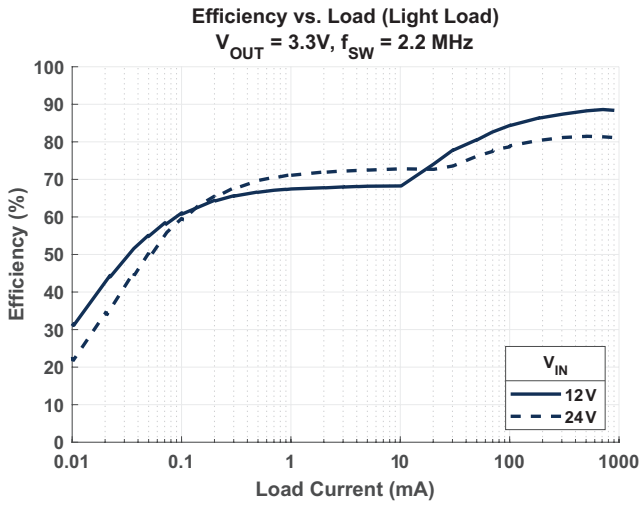
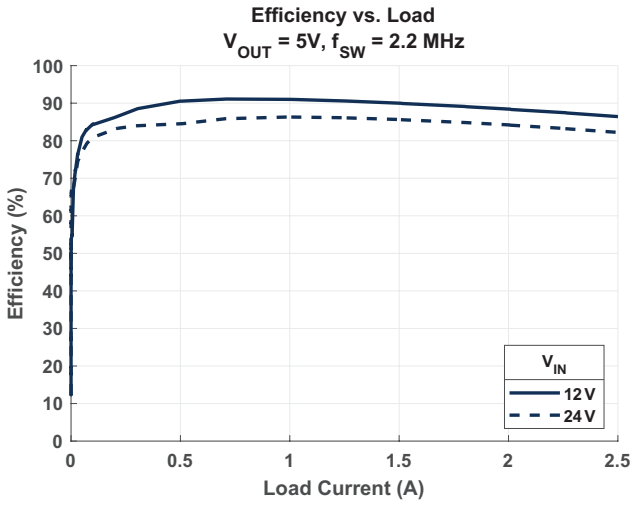
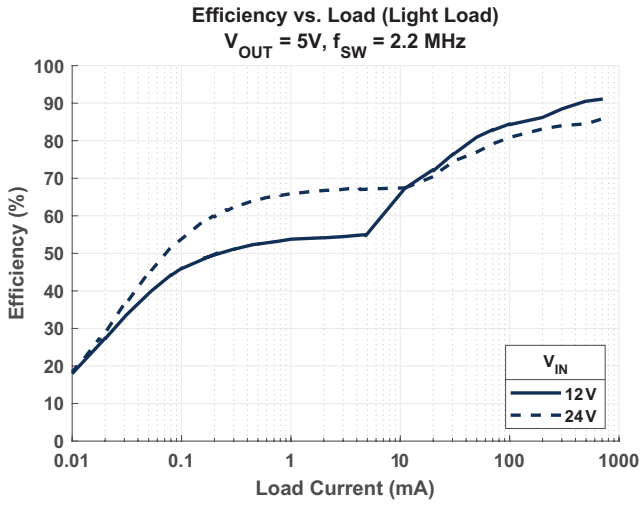
TYPICAL OPERATING CHARACTERISTICS









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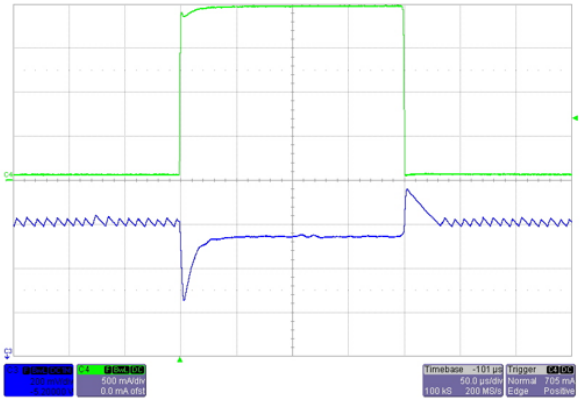
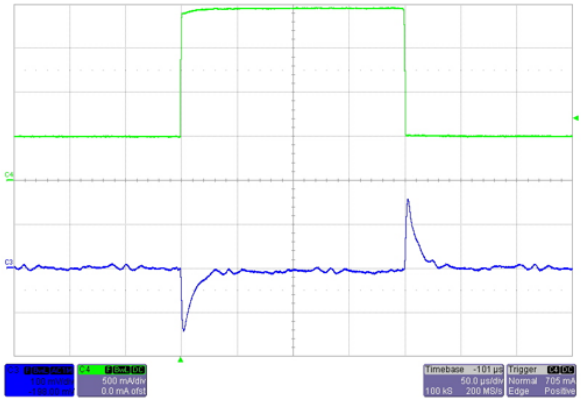
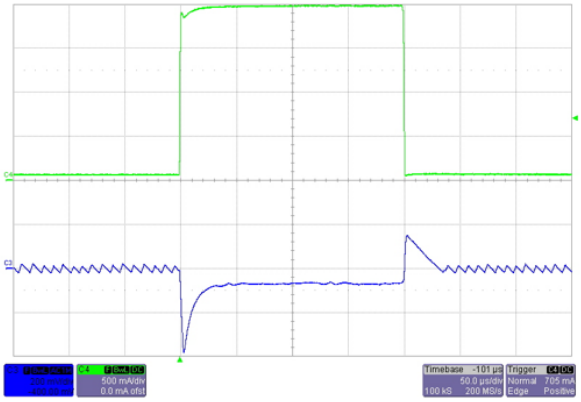
A81805 Load Transient
V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 50 mA – 2 A – 50 mA



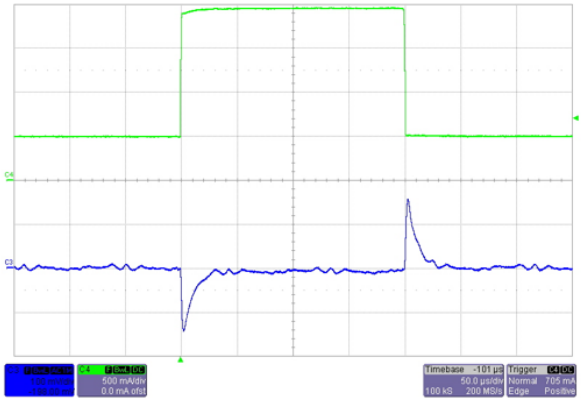
A81805 Load Transient
V_{IN} = 12 V, V_{OUT} = 3.3 V, Load = 500 mA – 2 A – 500 mA



A81805-1 Load Transient
V_{IN} = 12 V, V_{OUT} = 5 V, Load = 50 mA – 2 A – 50 mA



A81805-1 Load Transient
V_{IN} = 12 V, V_{OUT} = 5 V, Load = 500 mA – 2 A – 500 mA



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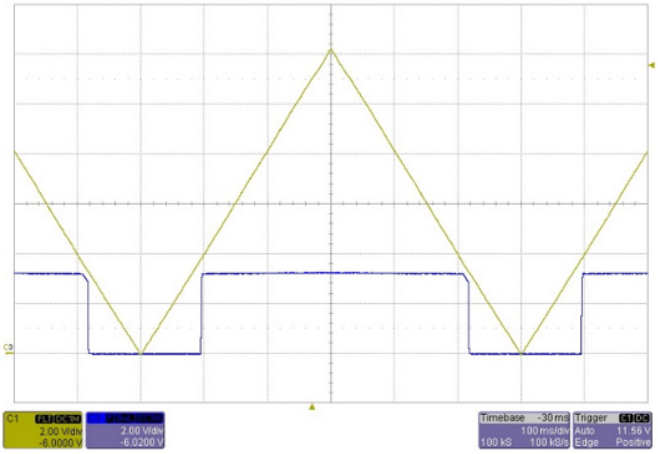
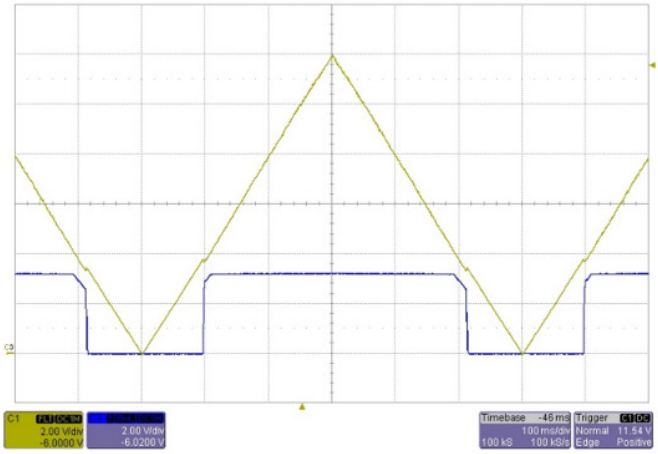
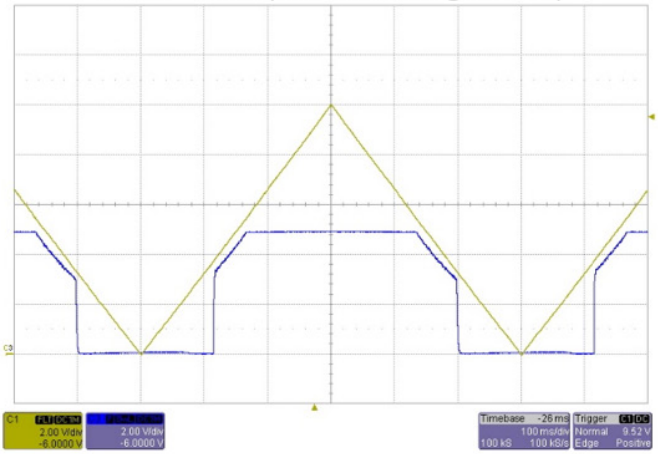
A81805 Startup and Shutdown
V_{IN} = 12 V, V_{OUT} = 3.3 V
R_{LOAD} = 13.2 Ω (250 mA in regulation)



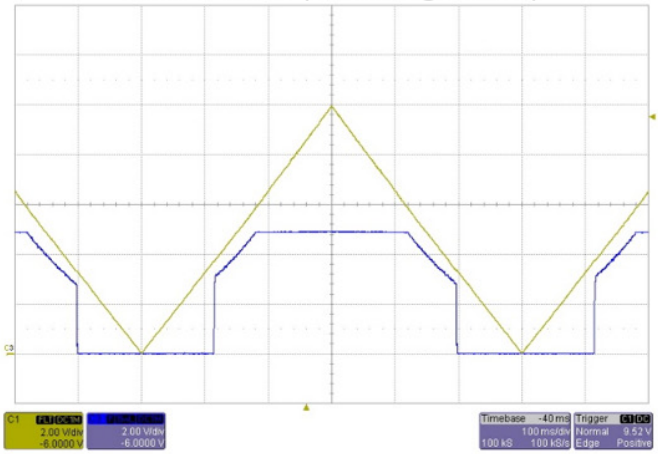
A81805 Startup and Shutdown
V_{IN} = 12 V, V_{OUT} = 3.3 V
R_{LOAD} = 1.65 Ω (2 A in regulation)



A81805-1 Startup and Shutdown
V_{IN} = 12 V, V_{OUT} = 5 V
R_{LOAD} = 20 Ω (250 mA in regulation)



A81805-1 Startup and Shutdown
V_{IN} = 12 V, V_{OUT} = 5 V
R_{LOAD} = 2.5 Ω (2 A in regulation)



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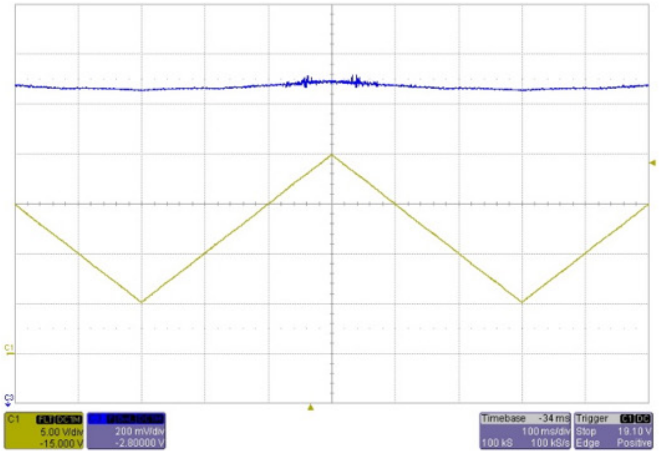
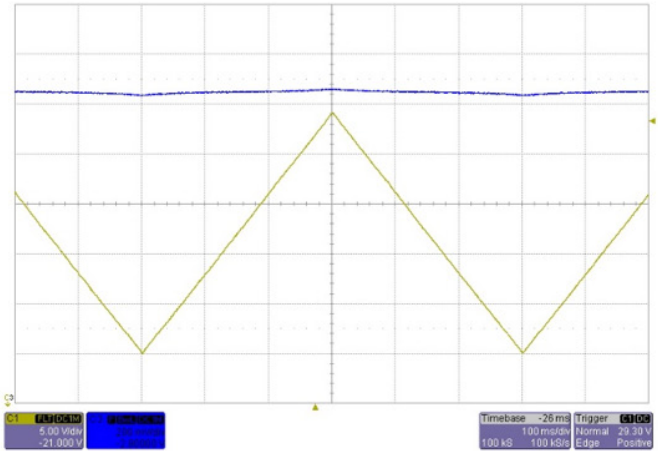
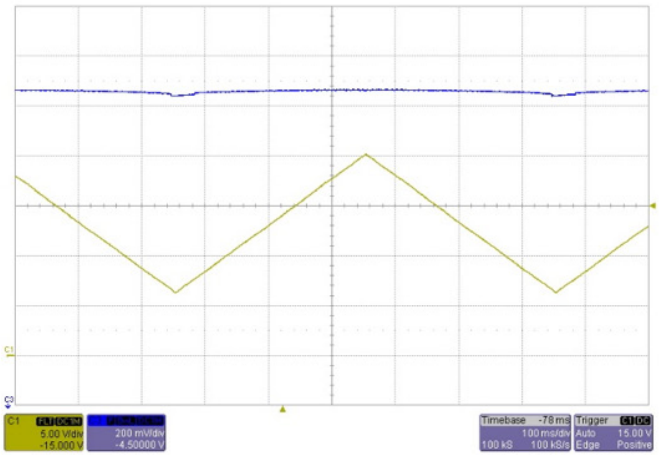
A81805 Line Regulation
V_{IN} = 5 V – 20 V, V_{OUT} = 3.3 V
I_{OUT} = 500 mA



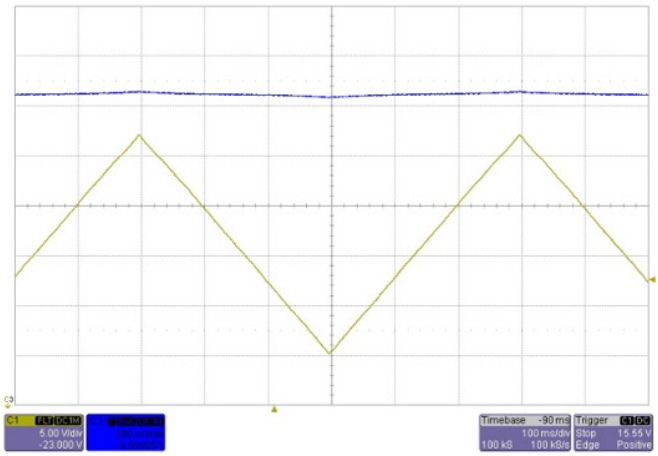
A81805 Line Regulation
V_{IN} = 6 V – 30 V, V_{OUT} = 3.3 V
I_{OUT} = 2 A



A81805-1 Line Regulation
V_{IN} = 6 V – 20 V, V_{OUT} = 5 V
I_{OUT} = 500 mA



A81805-1 Line Regulation
V_{IN} = 8 V – 30 V, V_{OUT} = 5 V
I_{OUT} =2 A



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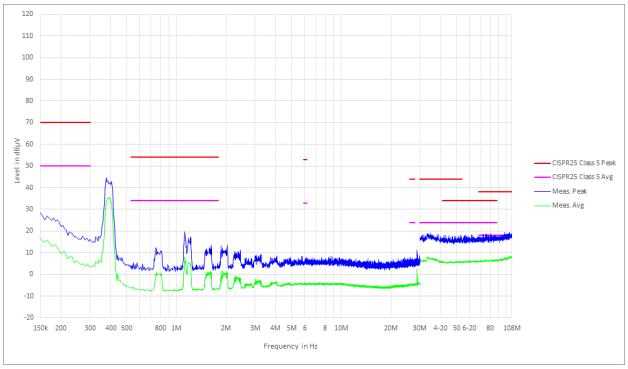
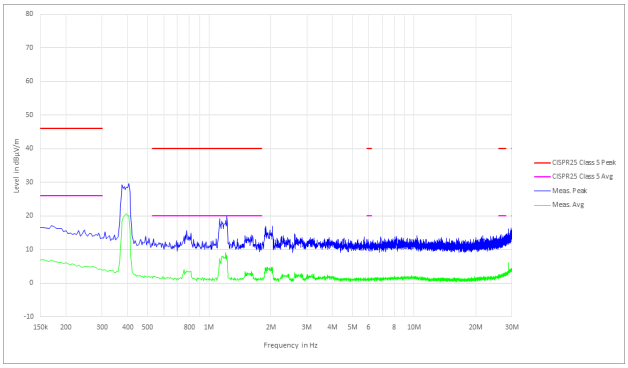
EMI/EMC PERFORMANCE CHARACTERISTICS

EMI test results are obtained using standard A81805 demo board with input EMI filter.
V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} = 400 kHz.

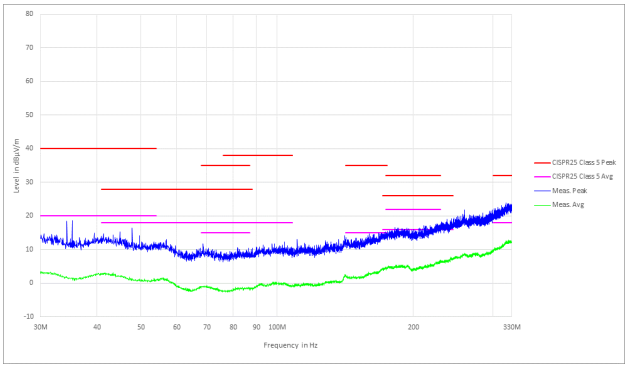
Conducted Emissions



Radiated Emissions (150 kHz – 30 MHz)



Radiated Emissions (30 MHz – 330 MHz)



NOTE: Allegro is not an accredited EMC laboratory. The information presented here is for reference only.

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FUNCTIONAL DESCRIPTION

Overview

The A81805 is a wide input voltage (3.5 to 36 V) synchronous PWM buck regulator that integrates low $R_{DS(on)}$ high-side and low-side N-channel MOSFETs. The A81805 employs peak current mode control to provide superior line and load regulation, cycle-by-cycle current limit, fast transient response, and simple internal compensation. The features of the A81805 include ultra-low I_Q in LP mode, extremely low minimum on-time, maximized duty cycle for low dropout operation, and pre-bias startup capability.

Protection features of the A81805 include VIN undervoltage lockout, cycle-by-cycle overcurrent protection, BOOT overvoltage and undervoltage protection, hiccup mode short-circuit protection, output overvoltage protection, and thermal shutdown. In addition, the A81805 provides open circuit, adjacent pin short circuit, and pin-to-ground short-circuit protections.

Enable

A voltage on EN above the nominal 1.2 V threshold enables the A81805. The EN comparator has a typical hysteresis of 200 mV. Once enabled, if EN decreases below 1 V (typical), the A81805 enters the shutdown state, stops switching, and draws only 1 µA (typical) from V_{IN}.

Internal VCC Regulator

VCC is used as the power supply for internal control circuitry and low-side MOSFET driver. The A81805 consists of two internal low dropout regulators, V_{IN} LDO and V_{OUT} LDO, to generate VCC voltage. V_{IN} LDO is powered from the input voltage to generate 3.3 V for VCC supply during power-up and soft-start. V_{OUT} LDO is powered through the VOUT pin to generate VCC once the converter output is in regulation.

Switching Frequency

The PWM switching frequency of the A81805 is adjustable from 400 kHz to 2.5 MHz by programming the internal clock frequency of the oscillator by connecting an R_{FSET} resistor from the FSET pin to GND. The internal clock has an accuracy of ±10% over the operating temperature range. Figure 2 shows the relationship between the typical switching frequency and R_{FSET} resistor.The A81805 will suspend operation if the FSET pin is shorted to GND or left open.

For a required switching frequency (f_{SW}), the R_{FSET} resistor value can be calculated as follows:

Equation 1:

$$R_{FSET} = \frac{37037}{f_{SW}} - 2.96$$

where f_{SW} is in kHz and R_{FSET} is in kΩ.

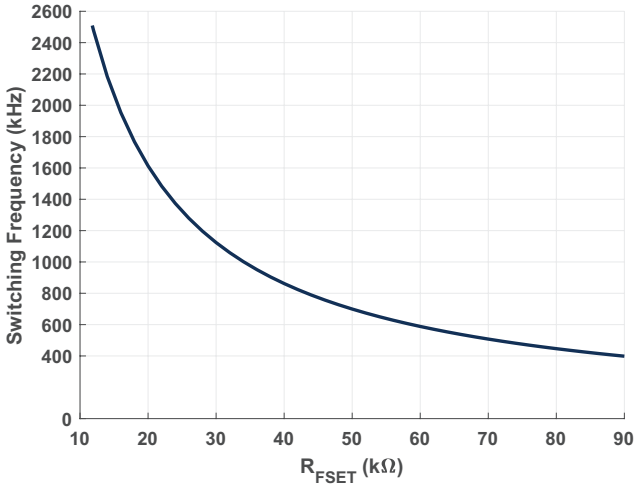

Figure 2: Switching Frequency vs. R_{FSET}

While choosing the PWM switching frequency, the designer should be aware of the minimum controllable on-time, $t_{ON(MIN)}$, of the A81805. If the required on-time of the system is less than the minimum controllable on-time, pulse skipping will occur and the output voltage will have increased ripple. The PWM switching frequency should be calculated using Equation 2, where V_{OUT} is the output voltage, $t_{ON(MIN)}$ is the minimum controllable on-time of the device (see EC table), and $V_{IN(MAX)}$ is the maximum required operational input voltage (not the peak surge voltage).

Equation 2:

$$f_{SW} = \frac{V_{OUT}}{t_{ON(MIN)} \times V_{IN(MAX)}}$$

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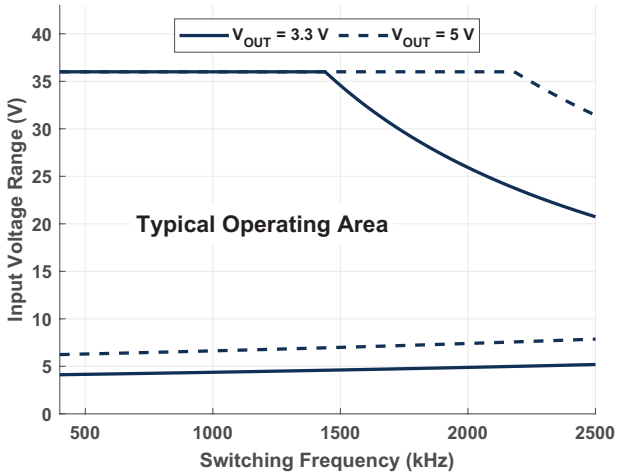

Figure 3: V_{IN} Range Limitation Based On Minimum On and Off Times

Synchronization (SYNC)

The Phase-Locked Loop (PLL) in the A81805 allows its internal oscillator to be synchronized to an external clock applied on the SYNC pin. If the SYNC pin is driven by an external clock, the A81805 will be forced to operate in PWM mode at the synchronized switching frequency and will not enter LP mode. The external clock must satisfy the pulse width, duty cycle, and rise/fall time requirements shown in the Electrical Characteristics table.

If an external clock f_{SYNC} is used for synchronization, the FSET pin must still have a resistor to GND, R_{FSET}, based on Equation 1, to ensure proper slope compensation. The switching frequency, f_{SW}, used to calculate R_{FSET}, should be chosen such that pulse skipping will not occur at the maximum synchronized switching frequency (i.e., $1.5 \times f_{SYNC} < f_{SW}$ in Equation 2).

Frequency Dither

Frequency dither helps to minimize peak emissions by spreading the emissions across a wide range of frequencies. The A81805 provides frequency dither by spreading the switching frequency over ±5% using a triangular modulated wave of 0.5% switching frequency.

The A81805 is capable of adding dither to an external clock applied to the SYNC pin. This unique feature allows the minimizing of EMI even when the device is using external clock.

Table 1: PWM Frequency and Dithering

SYNC	SW Frequency	Dither Frequency Range	Dither Modulation Frequency
Low	f_{OSC}	±0.05 × f_{OSC}	0.005 × f_{OSC}
High	f_{OSC}		
f_{SYNC}	f_{SYNC}	±0.05 × f_{OSC}	0.005 × f_{OSC}

Ultra-Low Quiescent Current Low Power (LP) Mode

When in Low Power (LP) Mode, the A81805 operates with ultra-low quiescent current (I_Q).

The A81805 is in continuous conduction PWM Mode until peak inductor current decreases to $I_{PEAK(LP)}$, 700 mA typ. When peak inductor current falls below $I_{PEAK(LP)}$, the regulation of the output voltage will be managed by the LP comparator, which will monitor the internal feedback node voltage. The reference for the LP comparator is calibrated approximately 0.5% above the PWM regulation point. The transition point from PWM to LP mode is defined by the input voltage, output voltage, and inductor value. The exact operation of A81805 in LP mode is described below.

When voltage on the internal COMP node falls to the voltage corresponding to the Ultra-Low I_Q peak current threshold value, an internal clamp prevents the COMP voltage from falling further. This results in a momentary rise in the internal feedback voltage beyond the LP comparator upper threshold which causes the LP comparator to trip. Once the LP comparator trips, the device enters a coast period during which converter switching is terminated and the associated control circuitry is also shut down. This ensures a very low quiescent current is drawn from the input.

The coast period terminates once the internal feedback voltage falls below the LP comparator lower threshold. The converter will operate at the PWM switching frequency until the voltage at the internal feedback node rises again above the LP comparator threshold. The rate of rise of the output voltage is determined by the input voltage, output voltage, inductor value, output capacitance, and load.

Due to the hysteretic nature of the LP control algorithm, higher output voltage ripple is expected. Typically, output voltage peak-to-peak ripple will be less than 50 mV.

The thermal shutdown (TSD) circuit is disabled in LP mode to further reduce the ultra-low quiescent current, since power dissipation and self-heating in LP mode is very low.

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Low Input Voltage Operation

The A81805 is designed to operate at extremely wide duty cycles to minimize any reduction in output voltage during dropout conditions such as an automotive cold crank. When the A81805 senses the dropout condition, it reduces the switching frequency to extend the duty cycle and regulate the output voltage with a lower input voltage.

Power MOSFETs

The A81805 includes a 170 mΩ, high-side N-channel MOSFET and a 130 mΩ, low-side N-channel MOSFET to provide synchronous rectification. When the A81805 is disabled by pulling the EN input low or by a fault condition, its output stage is tri-stated by turning off both the upper and lower MOSFETs.

BOOT Regulator

The A81805 includes a BOOT regulator to supply the power for a high-side MOSFET gate driver. The voltage across the BOOT capacitor is typically 3.2 V.

Soft-Start (Startup) and Inrush Current Control

The A81805 provides an internal fixed soft-start function to limit inrush current at startup. When the part is enabled, the high-side and low-side MOSFETs will begin switching after t_{dSS}. The output voltage is ramped to the V_{OUT} target level of 3.3 V for the A81805 or 5 V for the A81805-1 during the t_{SS} period.

During startup, PWM switching frequency is reduced to 25% of f_{SW} while V_{OUT} is below 25% of the regulation voltage. When V_{OUT} is between 25% to 50% level, the switching frequency is set to 50% of f_{SW}. When V_{OUT} is above 50% of the regulation voltage, the switching frequency is no longer reduced. The reduced switching frequency is necessary to help improve output regulation and stability when V_{OUT} is very low. During low V_{OUT}, the PWM control loop requires on-time near the minimum controllable on-time and very low duty cycles that are not possible at the nominal switching frequency.

After the soft-start period, t_{SS}, the error amplifier will switch over and begin regulating the output voltage to desired level.

If the A81805 is disabled or a fault occurs, the internal fault latch is set and the soft-start circuit is reset, forcing the converter to go through another soft-start.

Pre-Biased Startup

If the output of the buck regulator is pre-biased at a certain output voltage level upon startup, the A81805 will modify the normal startup routine to prevent discharging the output capacitors. If the output is pre-biased, the voltage at the internal FB node will be non-zero. The device will not start switching until the internal reference to the error amplifier exceeds the FB voltage. Then the error amplifier becomes active and normal startup sequence is followed.

PGOOD Output

The A81805 provides a Power Good (PGOOD) status signal to indicate if the output voltage is within the regulation limits. Since the PGOOD output is an open-drain output, an external pull-up resistor must be used as shown in the applications schematic. PGOOD transitions high when the output voltage, sensed at the internal FB node is within regulation.

During startup, PGOOD signal exhibits an additional delay of $t_{dPG(SU)}$ after the internal FB node voltage reaches the reference voltage, indicating V_{OUT} is in regulation. This delay helps to filter out any glitches on the internal FB node voltage.

The PGOOD output is pulled low if either an output undervoltage or overvoltage condition occurs or the A81805 junction temperature exceeds thermal shutdown threshold (TSD). The PGOOD overvoltage and undervoltage comparators incorporate a small amount of hysteresis to prevent chattering and deglitch filtering ($t_{dPG(UV)}$, $t_{dPG(OV)}$) to eliminate false triggering.

Current Sense Amplifier

The A81805 incorporates a high-bandwidth current sense amplifier to monitor the current through the high-side MOSFET. This current signal is used to regulate the peak current when the high-side MOSFET is turned on. The current signal is also used by the protection circuitry for the cycle-by-cycle current limit and hiccup mode short-circuit protection.

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Pulse Width Modulation (PWM)

The A81805 employs fixed-frequency, peak current-mode control to provide excellent load and line regulation, fast transient response, and simple compensation. A high-speed comparator and control logic are included in the A81805. The inverting input of the PWM comparator is connected to the output of the error amplifier. The non-inverting input is connected to the sum of the current sense signal, the slope compensation signal, and a DC PWM Ramp offset voltage (Ramp Offset).

At the beginning of each PWM cycle, the CLK signal sets the PWM flip-flop, the low-side MOSFET is turned off, the high-side MOSFET is turned on, and the inductor current increases. When the voltage at the non-inverting input of the PWM comparator rises above the error amplifier output COMP, the PWM flip-flop is reset, the high-side MOSFET is turned off, the low-side MOSFET is turned on, and the inductor current decreases. Since the PWM flip-flop is reset, the dominant error amplifier may override the CLK signal in certain situations.

Internal Loop Compensation

The A81805 has internal control loop compensation that ensures adequate stability margins and maintains a high loop gain at DC to achieve excellent output voltage regulation and to obtain a high loop bandwidth for superior transient response.

Slope Compensation

The A81805 incorporates internal slope compensation that ensures stable operation at PWM duty cycles above 50% for a wide range of input/output voltages and switching frequencies. As shown in the functional block diagram, the slope compensation signal is added to the sum of the current sense and PWM Ramp Offset. The relationship between slope compensation and switching frequency is given by Equation 3.

Equation 3:

$$S_E = 1.4 \times f_{SW} - 0.205$$

where f_{SW} is the switching frequency in MHz and S_E is slope compensation in A/µs.

PROTECTION FUNCTIONS AND FAULT HANDLING

The A81805 was designed to satisfy the most demanding automotive and non-automotive applications. The following sections contain a description of each protection feature as well as Table 2 which summarizes the protections and their operation.

Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) comparator in the A81805 monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is below the start threshold ($V_{INUV(ON)}$, V_{IN} rising) or the stop threshold ($V_{INUV(OFF)}$, V_{IN} falling). The UVLO comparator incorporates some hysteresis ($V_{INUV(HYS)}$) to help prevent on-off cycling of the regulator due to resistive or inductive drops in the V_{IN} path during heavy loading or during startup.

Pulse-by-Pulse Peak Current Protection (PCP)

The A81805 monitors the current in the high-side MOSFET. When the peak MOSFET current exceeds the pulse-by-pulse overcurrent limit $I_{LIM(HS)}$, the high-side MOSFET is turned off and the low-side MOSFET is turned on until the start of the next clock pulse from the oscillator. The device includes leading-edge blanking to prevent false triggering of pulse-by-pulse current protection when the high-side MOSFET is turned on.

Overcurrent Protection (OCP) and Hiccup Mode

An OCP counter and hiccup mode circuit protect the buck regulator when the output of the regulator is shorted to ground or when the load is too high. The device asserts the fault state by pulling PGOOD low and stopping switching after HIC_OC switching cycles for an overcurrent condition or HIC_SW,GND cycles if SW is shorted to ground. While the overcurrent protection is active, the device will periodically retry a soft-start every t_{HIC} to check if the short was removed. During the soft-start ramp the OCP hiccup counter is disabled. The A81805 resumes normal operation when the short is removed. A typical hiccup operation during short circuit is shown in Figure 4.

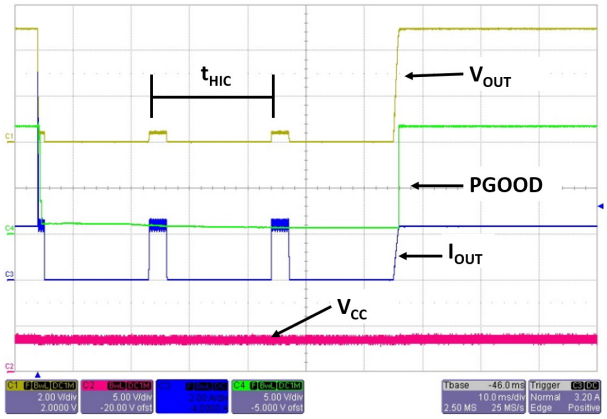

Figure 4: Hiccup Operation During Short Circuit

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Boot Capacitor Protection

The A81805 monitors the voltage across the BOOT capacitor to detect open and short conditions. If an open BOOT capacitor is detected, the regulator pulls PGOOD low and enters hiccup mode, trying to start again with period t_{HIC}. When the open fault is removed, the device exits hiccup mode and returns to normal operation. If the BOOT capacitor is shorted before startup is complete, the regulator will not switch or regulate until the short is removed. If the BOOT capacitor is shorted after startup is complete, the regulator shuts down and must be powercycled after the short is removed to resume normal operation. In both cases, when the BOOT capacitor is shorted, PGOOD is tri-stated and is not asserted low.

Overvoltage Protection (OVP)

The A81805 consists of an always-on overvoltage protection circuit that monitors the voltage on the VOUT pin. During an overvoltage event, the controller tries to reduce the output overvoltage by terminating the high-side MOSFET switching and pulsing the low-side MOSFET for the minimum off-time (t_{OFFmin}) until V_{OUT} returns to regulation. Upon an OVP event, the A81805 waits for the PGOOD overvoltage delay, $t_{dPG(OV)}$, before pulling PGOOD low. If the overvoltage fault is not cleared after $t_{dPG(OV)}$, PGOOD is pulled low and the device continuously attempts to reduce the output overvoltage.

SW Pin Protection

The A81805 protects itself upon a SW pin short to ground. If the SW pin is shorted to ground, there will be a very high current in the high-side MOSFET when it is turned on. The A81805 incorporates internal secondary current protection to detect this unusually high current and turns off the high-side MOSFET if the high current persists for more than two consecutive switching cycles. After turning off the high-side MOSFET, the device enables the hiccup latch and attempts to restart after hiccup latch is cleared. If the short to ground is removed, the regulator will automatically recover; otherwise, the device continues hiccupping.

Pin-to-Ground and Pin-to-Pin Short Protections

The A81805 is designed to satisfy the most demanding automotive applications. For example, the device has been carefully designed to withstand a short-circuit to ground at each pin without causing any damage to the IC.

In addition, the device's pinout is optimized to provide protection against pin-to-pin adjacent short circuits. For example, logic pins and high-voltage pins are separated as much as possible.

Table 2: Summary of A81805 Fault Modes and Operation

Fault Mode	Hiccup	High-Side MOSFET	Low-Side MOSFET	PGOOD	Reset Condition
VIN Undervoltage	No	Off	Off	Low	VIN above UVLO
Output Short / Overcurrent	Yes	Off	Turned On if BOOT Voltage is too low	Low	Short / Overcurrent removed
SW Short-to-GND	Yes	Off	Off	Low	Short removed
BOOT Cap Open	Yes	Off	Off	Low	BOOT capacitor circuit closed
BOOT Cap Shorted – Before Startup Complete	No	Off	Off	Hi-Z	BOOT capacitor short removed
BOOT Cap Shorted – After Startup Complete	No	Off	Off	Hi-Z	BOOT capacitor short removed and power cycle
Output Overvoltage	No	Off	Pulsed with Minimum TOFF	Low	VOUT within operative range
Output Undervoltage	No	Normal Behavior		Low	VOUT within operative range
FSET Short-to-GND or Open	No	Off	Off	Low	FSET shorted removed
Thermal Shutdown	No	Off	Off	Low	Part cools down

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Thermal Shutdown (TSD)

The A81805 monitors internal junction temperature and stops switching if the junction temperature exceeds the Thermal Shutdown Threshold, T_{TSD}. To prepare for a restart, the internal soft-start voltage and the error amplifier output (COMP) are pulled low. Thermal shutdown is a non-latched fault, so the device automatically recovers.

In LP mode, self-heating is minimal due to the low input current and light loading of the converter. To further reduce the quiescent current, thermal shutdown circuitry is disabled in LP mode.

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APPLICATIONS INFORMATION

Component Selection Guidelines

Recommended values for the output inductor, input capacitors, and output capacitors are shown in Table 3. These values are well suited for most applications. The following guidance should be followed if the application requires deviating from these recommended values.

Output Inductor (L_O)

The A81805 incorporates a peak current-mode control technique for closed-loop regulation of the output voltage. Without adequate slope compensation, a peak current-mode-controlled regulator may become unstable when duty cycle is near or above 50%. To stabilize the regulator over the complete range of its operating duty cycle, the A81805 employs an internal slope compensation (S_E) proportional to the switching frequency as described in the Slope Compensation section. Many factors determine the selection of output inductor, such as switching frequency, output/input voltage ratio, transient response, transition to LP mode, and desired ripple current. A larger value inductor will result in less ripple current, which also results in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current.

A good rule of thumb for determining the output inductor is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum output current ($I_{OUT(MAX)}$). The inductance value can be calculated from the following equation:

Equation 4:

$$L_O = \frac{V_{OUT}}{f_{SW} \times \Delta I_{LO}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where ΔI_{LO} is the peak-to-peak inductor ripple current, which is $0.3 \times I_{OUT(MAX)}$.

A second constraint on inductor value arises from the loop stability at duty cycles greater than 50%. Although slope compensation is primarily required to avoid subharmonic oscillations, the inductor value calculated from Equation 5 can critically damp the pole pair at half the switching frequency.

Equation 5:

$$L_O \geq \frac{V_{OUT}}{S_E} \times \left(1 - 0.18 \times \frac{V_{OUT}}{V_{IN(MIN)}}\right)$$

where L_O is output inductance in µH and S_E is external slope compensation.

To avoid dropout, $V_{IN(MIN)}$ must be approximately 1 to 1.5 V above V_{OUT}. Choose an output inductor such that its inductance is greater than the maximum of inductance values calculated in Equation 4 and Equation 5.

The saturation current of the inductor should be higher than the peak current capability of the A81805. Ideally, for output short-circuit conditions, the inductor should not saturate given the peak current limit ($I_{LIM(HS)}$). The output inductor should be sized to not saturate with the peak operating current according to the following equation.

Equation 6:

$$I_{SAT\_LO} > I_{LIM(HS)(MAX)} - \left(\frac{S_E \times t_{ON(MIN)}}{1.15}\right)$$

where $t_{ON(MIN)}$ is the minimum on-time provided in the Electrical Characteristics table.

The typical DC output current capability of the regulator at any given duty cycle (D) is:

Equation 7:

$$I_{OUT(TYP)} > I_{LIM(HS)(TYP)} - \frac{S_E \times D}{f_{SW}} - \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L_O}$$

After an inductor is chosen, it should be tested during output short-circuit conditions. The inductor current should be monitored using a current probe. A good design should ensure neither the inductor nor the regulator are damaged when the output is shorted to ground at maximum input voltage and the highest expected ambient temperature.

Output Capacitors (C_O)

A switching regulator's output capacitor filters the output voltage to provide an acceptable level of ripple and stores energy to help maintain voltage regulation during a load transient. The voltage rating of the output capacitors must support the output voltage with sufficient design margin.

The output voltage ripple (ΔV_{OUT}) is a function of the output capacitor parameters: C_O, ESR_{CO}, and ESL_{CO}.

Equation 8:

$$\Delta V_{OUT} = \Delta I_{LO} \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{CO} + \frac{\Delta I_{LO}}{8 \times f_{SW} \times C_O}$$

The type of output capacitors determines which terms of Equation 10 are dominant. For ceramic output capacitors, ESR_{CO} and ESL_{CO} are

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virtually zero, so the output voltage ripple will be dominated by the third term of Equation 8. The value of C_O can be calculated as:

Equation 9:

$$C_O \geq \frac{\Delta I_{LO}}{8 \times f_{SW} \times \Delta V_{OUT}}$$

Voltage ripple of a regulator using ceramic output capacitors can be reduced by increasing the total capacitance, reducing the inductor current ripple or increasing the switching frequency. For electrolytic output capacitors, the value of capacitance will be relatively high, so the third term in Equation 8 will be very small and the output voltage ripple will be determined primarily by the first two terms:

Equation 10:

$$\Delta V_{OUT} = \Delta I_{LO} \times ESR_{CO} + \frac{V_{IN} - V_{OUT}}{L_O} \times ESL_{CO}$$

Voltage ripple of a regulator using electrolytic output capacitors can be reduced by decreasing the equivalent ESR_{CO} and ESL_{CO} by using a high-quality capacitor, adding more capacitors in parallel, or reducing the inductor current ripple.

As the ESR of some electrolytic capacitors can be quite high, Allegro recommends choosing a quality capacitor for which the ESR or the total impedance is clearly documented in the capacitor datasheet. Also, the ESR of electrolytic capacitors usually increases significantly at cold ambient temperatures, as much as 10 times, which increases the output voltage ripple and may affect the stability of the converter.

The transient response of the regulator depends on the quantity and type of output capacitors. In general, minimizing the ESR of the output capacitance will result in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel or by using higher quality capacitors. At the instant of a fast load transient (high di_O/dt), the change in the output voltage, using electrolytic output capacitors, is:

Equation 11:

$$\Delta V_{OUT} = \Delta I_{LO} \times ESR_{CO} + \frac{di_O}{dt} \times ESL_{CO}$$

When ceramic capacitors are used on the output, the output voltage deviation during load transients depends on the bulk output capacitance along with various other factors. To calculate the bulk ceramic capacitance required, the entire load transient duration can be divided into two stages: large signal and small signal. During large signal load transients, immediately after the transient event, the output voltage deviates from the nominal value due to large mismatch in the load current requirement and the inductor current. The output voltage deviation during this interval is maximum and depends on output inductor, bulk output capacitance, and closed-loop crossover frequency. For designs with higher crossover frequency, the controller typically saturates the duty cycle, i.e., either minimum or maximum. For a chosen output inductor and crossover frequency values, the output voltage deviation can be minimized by increasing the output bulk capacitance. In the case of a buck converter, operating with a low duty cycle, the step-down load transient is more severe and hence the output capacitance should be determined for this scenario. The bulk ceramic output capacitance required is given by:

Equation 12:

$$C_{O(BULK)} \geq \frac{\Delta I_O^2 \times L_O}{2 \times V_{OUT} \times \Delta V_{OUT(SPEC)}}$$

where ΔI_O is the magnitude of the change in the load current, $\Delta V_{OUT(SPEC)}$ is the maximum allowed output voltage deviation during load transient event. Gradually, as the mismatch between the load current and the inductor current becomes small, the output voltage deviation also reduces, resembling a small signal transient event. Eventually, during small signal transient interval, the error amplifier brings the output voltage back to its nominal value. The speed with which the error amplifier brings the output voltage back into regulation depends mainly on the loop crossover frequency. A higher crossover frequency usually results in a shorter time to return to the nominal set voltage.

Output Voltage Ripple – Ultra-Low I_Q LP Mode

After choosing output capacitor(s), it is important to calculate the output voltage ripple ($V_{PP(LP)}$) during ultra-low I_Q LP mode. With ceramic output capacitors, the output voltage ripple in PWM mode is usually negligible, but this is not the case during LP mode.

In LP mode, the peak inductor current during on-time of the high-side switch is limited to $I_{PEAK(LP)}$. Also, in LP mode, the low-side switch is constantly turned off thereby forcing the regulator to operate in Discontinuous Conduction Mode (DCM) in order to reduce switching losses. The LP comparator monitors the output voltage on the internal feedback node and allows the regulator to switch until the internal feedback voltage is greater than 0.5% of its nominal value (0.8 V). When internal feedback voltage is greater than 0.804 V, the A81805 coasts by terminating the switching pulses.

During coasting, the device shuts down most of its internal control circuitry to ensure very low quiescent current is drawn from the input. The number of switching pulses required in LP mode

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to coast the device depend on various factors including input voltage, output voltage, load current, output inductor, and output capacitor. If A81805 starts coasting after a single switching pulse, then the output voltage ripple would be dictated by this single pulse. The peak inductor current without slope compensation (I_{PEAK_L}) is given by:

Equation 13:

$$I_{PEAK\_L} \cong \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times L \times f_{SW}}$$

where I_{PEAK_LP} is the peak inductor current, specified in the Electrical Characteristics table, at which device enters into LP mode. Referring to Figure 1, on-time and off-time calculations are given as:

Equation 14:

$$t_{ON} = \frac{I_{PEAK\_L} \times L_O}{V_{IN} - V_{OUT} - I_{PEAK\_L} \times (R_{DS(ON)HS} + L_{O(DCR)})}$$

Equation 15:

$$t_{OFF} = \frac{I_{PEAK\_L} \times L_O}{V_{OUT}}$$

where $R_{DS(ON)HS}$ is the on-resistance of internal high-side MOSFET and $L_{O(DCR)}$ is the DC resistance of the output inductor, L_O.

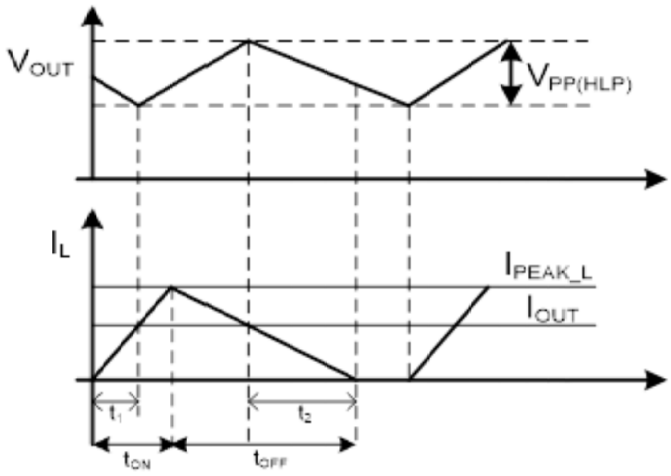

Figure 5: Output Voltage Ripple in LP Mode

During on-time interval, the length of the time for the inductor current to rise from 0 A to I_{OUT} is:

Equation 16:

$$t_1 = \frac{I_{OUT} \times L_O}{V_{IN} - V_{OUT} - I_{PEAK\_L} \times (R_{DS(ON)HS} + L_{O(DCR)})}$$

During off-time interval, the length of the time for the inductor current to fall from I_{OUT} to 0 A is:

Equation 17:

$$t_2 = \frac{I_{OUT} \times L_O}{V_{OUT}}$$

Given the peak inductor current (I_{PEAK_L}) and the rise and fall times (t_{ON} and t_{OFF}) for the inductor current, the output voltage ripple for a single switching pulse can be calculated as follows:

Equation 18:

$$V_{PP(LP)} = \frac{I_{PEAK\_L} \times L_{OUT}}{2 \times C_{OUT}} \times (t_{ON} + t_{OFF} - t_1 - t_2)$$

Input Capacitor Selection (C_{IN})

Three factors should be considered when choosing the input capacitors. First, the capacitors must be chosen to support the maximum expected input surge voltage with adequate design margin. Second, the capacitor RMS current rating must be higher than the expected RMS input current to the regulator. Third, the capacitors must have enough capacitance and a low enough ESR to limit the input voltage dV/dt to much less than the hysteresis of the UVLO circuitry (250 mV nominal) at maximum loading and minimum input voltage. The input capacitors must deliver an RMS current (I_{RMS}) given by:

Equation 19:

$$I_{RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

where D is the duty cycle

Equation 20:

$$D \approx \frac{V_{OUT}}{V_{IN}}$$

Figure 5 shows the normalized input capacitor RMS current versus duty cycle. To use this graph, simply find the operational duty cycle (D) on the x-axis and determine the input/output current multiplier on the y-axis. For example, at a 20% duty cycle, the input/output current multiplier is 0.40. Therefore, if the regulator is delivering 1.0 A of steady-state load current, the input capacitor(s) must support 0.40 × 1.0 A or 0.4 A RMS.

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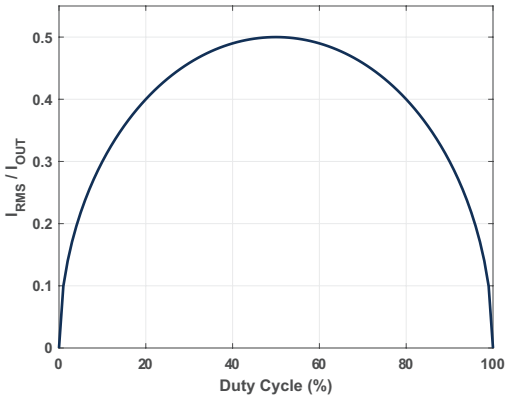

Figure 6: Normalized Input Capacitor Ripple vs. Duty Cycle

The input capacitor(s) must limit the voltage deviations at the VIN pin to significantly less than the device UVLO hysteresis during maximum load and minimum input voltage condition. The following equation allows to calculate the minimum input capacitance required:

Equation 21:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{0.85 \times f_{SW} \times \Delta V_{IN(MIN)}}$$

where $\Delta V_{IN(MIN)}$ is chosen to be much less than the hysteresis of the VIN UVLO comparator ($\Delta V_{IN(MIN)} \leq 150$ mV is recommended), and f_{SW} is the nominal PWM frequency. The D × (1–D) term in Equation 21 has an absolute maximum value of 0.25 at 50% duty cycle.

A good design should consider the DC bias effect on a ceramic capacitor: as the applied voltage approaches the rated value, the capacitance value decreases. This effect is very pronounced with the Y5V and Z5U temperature characteristic devices (as much as 90% reduction), so these types should be avoided. The X5R, X7R, and X8R type capacitors should be the primary choices due to their stability versus both DC bias and temperature.

A ceramic capacitor of 47 nF along with an aluminum electrolytic capacitor is recommended (≥47 µF). The electrolytic capacitor is used to meet load-transient response requirements and to avoid input voltage oscillation due to the negative input impedance of the DC-DC regulator, while the ceramic capacitor is used to bypass high di/dt input ripple current.

Use of EN Pin for Input Undervoltage Protection

EN is input to a hysteretic comparator with an accurate 1.2 V (typical) threshold. A voltage on EN above the nominal 1.2 V threshold enables the A81805. Once enabled, the EN comparator has a typical hysteresis of 200 mV and if EN is lowered below 1.0 V (typical), the A81805 will enter the shutdown state.

This pin can be used to shut the converter down if input voltage falls below desired voltage, as shown in Figure 7.

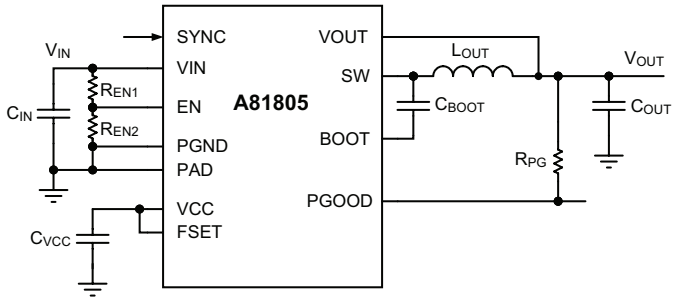

Figure 7: Application Circuit for Setting Input Undervoltage

A voltage divider circuit with two resistors can be used to adjust the enable voltage threshold or undervoltage lockout threshold. Select a convenient value for R_{EN2} and use Equation 22 to calculate R_{EN1} for a rising enable threshold level using the typical value for $V_{EN(HI)}$ of 1.2 V:

Equation 22:

$$R_{EN1} = \frac{V_{INTH(RISE)} - 1.2\ V}{I_{VEN} + \frac{1.2\ V}{R_{EN2}}}$$

where $V_{INTH(RISE)}$ is the desired input voltage threshold to enable the device, and I_{VEN} is the typical enable pin input current.

Use Equation 23 to estimate the falling input voltage threshold level once both resistors are known, using the typical value for $V_{EN(HI)}$ of 1.2 V and typical value of $V_{EN(HYS)}$ of 200 mV.

Equation 23:

$$V_{INTH(FALL)} = V_{ENTH(FALL)} \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}} + (I_{VEN} \times R_{EN1})$$

where $V_{ENTH(FALL)} = V_{EN(HI)} - V_{EN(HYS)}$, typically 1 V.

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APPLICATION SCHEMATIC AND RECOMMENDED EXTERNAL COMPONENTS

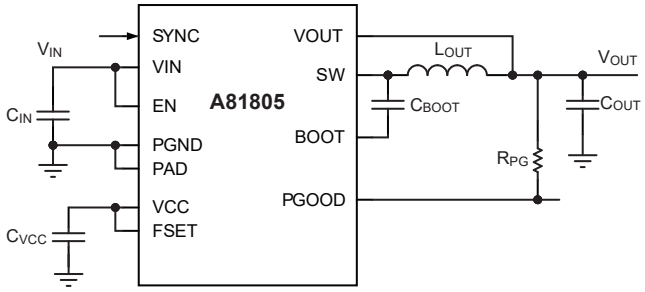

Figure 8: Typical Applications Schematic

Table 3: Recommended External Filter Component Values

Device	V_{OUT}	f_{OSC}	L_O	C_O	$C_{IN(MIN)}$
A81805	3.3 V	2.15 MHz	2.2 µH	2 × 10 µF	1 × 4.7 µF
A81805	3.3 V	400 kHz	8.2 µH	3 × 22 µF	3 × 4.7 µF
A81805-1	5 V	2.15 MHz	2.2 µH	2 × 10 µF	1 × 4.7 µF
A81805-1	5 V	400 kHz	12 µH	1 × 47 µF	3 × 4.7 µF

Components were chosen to maintain LP ripple voltage and minimize voltage droop during LP to PWM changeover.

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PCB LAYOUT GUIDELINES

The A81805 is designed to minimize electromagnetic interference (EMI) when proper PCB layout techniques are adopted. A good PCB layout is also critical for the A81805 to provide clean and stable output voltages. Design guidelines for EMI/EMC-aware PCB layout and minimized thermal impedance are presented below. Figure 9 shows a typical application schematic of a synchronous buck regulator IC with critical power paths/loops.

Place the ceramic input capacitors as close as possible to the VIN pin and PGND pins to minimize the loop area and keep the traces from the VIN pin to these capacitors as short and wide as possible to minimize the impedance. This critical loop is shown as trace 1 in Figure 9. The bulk/electrolytic input capacitor can be located further away from VIN pin. The input capacitors and A81805 IC should be on the same side of the board with traces on the same layer.

The loop from the input supply and capacitors, through the high-side MOSFET, into the output capacitor via the output inductor, and back to ground should be minimized with relatively wide traces.

When the high-side MOSFET is off, free-wheeling current flows from ground through the synchronous low-side MOSFET, as path 2 shown in Figure 9.

Place the output capacitors relatively close to the output inductor (L_O) and the A81805. Ideally, the output capacitors, output inductor, and the A81805 should be on the same layer. Connect the output inductor and the output capacitors with a fairly wide trace. The output capacitors must use a ground plane to make a very low-inductance connection to the PCB GND. These critical connections are shown as trace 3 in Figure 9.

Place the output inductor (L_O) as close as possible to the SW pin with short and wide traces. This critical trace is shown as trace 4 in Figure 9. The voltage at the SW node transitions from approximately 0 V to V_{IN} with a high dv/dt rate. This node is the root cause of many EMI and other noise issues. It is suggested to minimize the SW copper area to minimize the coupling capacitance between SW node and other noise-sensitive nodes; however, the SW node area cannot be too small because it must conduct high current. A ground copper area can be placed underneath the SW node to provide additional shielding.

If an R_{FSET} resistor is used, place it as close as possible to the FSET pin.

The output voltage sense trace should connect to VOUT as close as possible to the load to ensure optimal load regulation.

Place the bootstrap capacitor (C_{BOOT}) near the BOOT pin and keep the routing from this capacitor to the SW polygon as short as possible. This critical trace is shown as trace 5 in Figure 9.

Allegro recommends a 4-layer PCB as shown in Figure 9. Heavier copper layers, reduced material between layers, and a good amount of thermal vias are the keys to improved thermal performance. Use the top layer for routing high-current traces, layer 2 for a solid PGND plane, layer 3 for most other routing, and the bottom layer for solid PGND plane or optionally other components without low-impedance traces constraints—the PGOOD pull-up resistor could be on the bottom layer if desired. Routing on the bottom and top planes interrupts the flow of heat energy from the converter and inductor to the ambient and results in increased board thermal impedance. To the extent possible without compromising the design electrically, routing should be located on layer 3 to optimize the board's ability to dissipate heat.

If a two-layer-only PCB is mandatory, place all the components on the top layer and limit the routing only to the top layer. Use the bottom layer as PGND plane.

When connecting the input and output ceramic capacitors, use multiple vias to the PGND planes and place the vias as close as possible to the pads of the components. Do not use thermal reliefs around the pads for the input and output ceramic capacitors as they increase the impedance of the connections.

To minimize thermal resistance ($R_{\theta JA}$), extend the PGND plane on the top layer as much as possible and use plenty of thermal vias to connect them to the PGND plane in the bottom layer.

To minimize PCB losses and improve system efficiency, the power traces should be as wide as possible.

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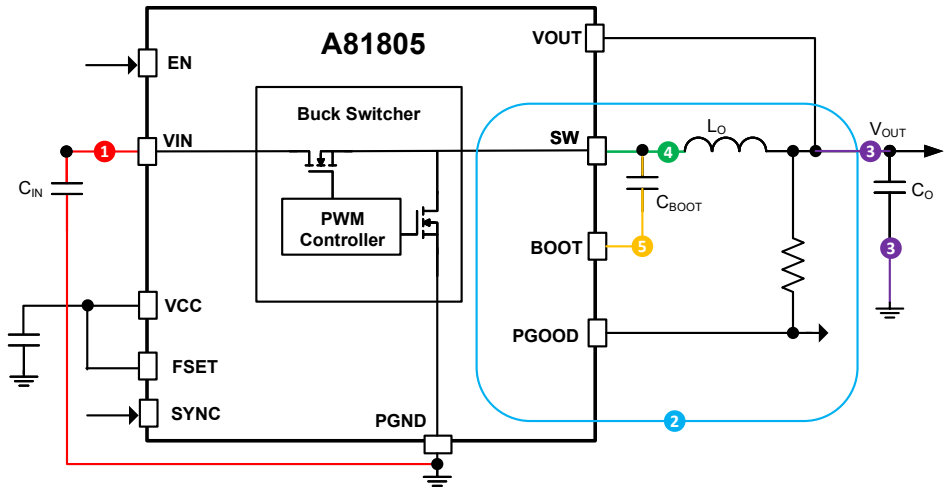

Figure 9: PCB Layout Critical Paths

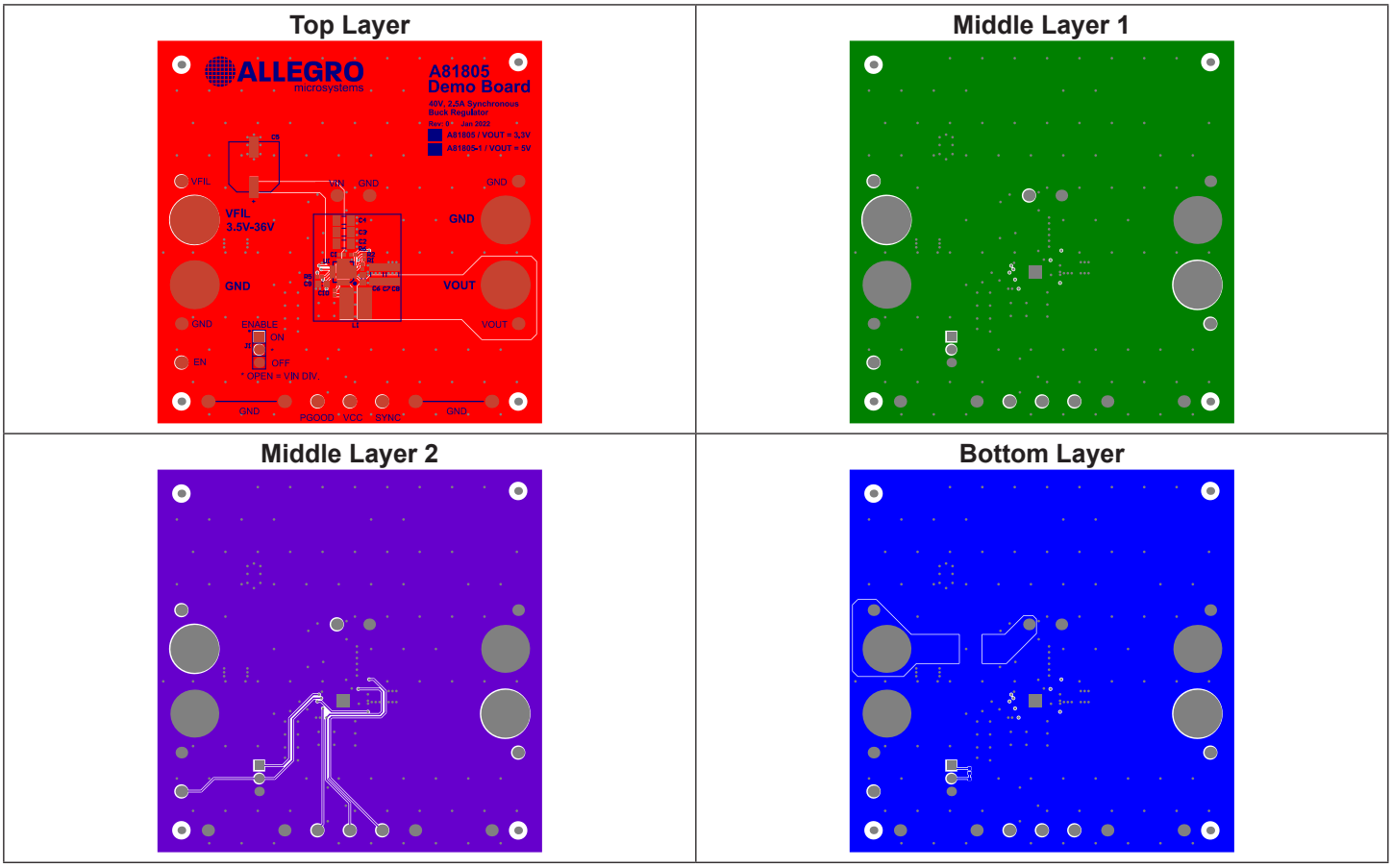

Figure 10: PCB Reference Design

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POWER DISSIPATION AND THERMAL CALCULATIONS

The total power dissipated in the A81805 is the sum of the power dissipated from the V_{IN} supply current (P_{IN}), the power dissipated due to the switching of the high-side power MOSFET (P_{SWH}), the power dissipated due to the conduction of RMS current in the high-side MOSFET (P_{CH}) and low-side MOSFET (P_{CL}), power dissipated due to the low-side MOSFET body diode conduction during the non-overlap time (P_{NO}), and the power dissipated by both high-side and low-side gate drivers (P_{DRIVER}).

The power dissipated from the V_{IN} supply current can be calculated using Equation 24:

Equation 24:

$$P_{IN} = V_{IN} \times I_{IN(PWM)}$$

where V_{IN} is the input voltage, $I_{IN(PWM)}$ is the input quiescent current drawn by the A81805 in PWM mode (see EC table), Q_{GH} and Q_{GL} are the internal high-side and low-side MOSFET gate charges, and f_{SW} is the PWM switching frequency.

The power dissipated by the high-side MOSFET during PWM switching can be calculated using Equation 25:

Equation 25:

$$P_{SWH} = \frac{V_{IN} \times I_{OUT} \times (t_r + t_f) \times f_{SW}}{2}$$

where V_{IN} is the input voltage, I_{OUT} is the regulator output current, f_{SW} is the PWM switching frequency, t_r and t_f are the rise and fall times measured at the switch node.

The exact rise and fall times at the SW node will depend on the external components and PCB layout, so each design should be measured at full load.

The power dissipated in the high-side MOSFET while it is conducting can be calculated using Equation 26:

Equation 26:

$$P_{CH} = I^2_{RMS(H)} \times R_{DS(ON)H} = \frac{V_{OUT}}{V_{IN}} \times \left(I_{OUT} + \frac{\Delta I^2_{LO}}{12}\right) \times R_{DS(ON)H}$$

Similarly, the conduction losses dissipated in the low-side MOSFET while it is conducting can be calculated by Equation 27:

Equation 27:

$$P_{CL} = I^2_{RMS(L)} \times R_{DS(ON)L} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(I^2_{OUT} + \frac{\Delta I^2_{LO}}{12}\right) \times R_{DS(ON)L}$$

where I_{OUT} is the regulator output current, ΔI_{LO} is the peak-to-peak inductor ripple current, $R_{DS(ON)H}$ is the on-resistance of the high-side MOSFET, $R_{DS(ON)L}$ is the on-resistance of the low-side MOSFET.

The power dissipated in the low-side MOSFET body diode during the non-overlap time can be calculated using Equation 28:

Equation 28:

$$P_{NO} = V_{SD} \times I_{OUT} \times 2 \times t_{NO} \times f_{SW}$$

where V_{SD} is the source-to-drain voltage of the low-side MOSFET (typically 0.60 V), and t_{NO} is the non-overlap time.

The power dissipated in the internal gate drivers can be calculated using Equation 29:

Equation 29:

$$P_{DRIVER} = (Q_{GH} + Q_{GL}) \times V_{OUT} \times f_{SW}$$

where V_{GS} is the gate drive voltage.

Finally, the total power dissipated in the A81805 is given by Equation 30:

Equation 30:

$$P_{TOTAL} = P_{IN} + P_{SW} + P_{CH} + P_{CL} + P_{NO} + P_{DRIVER}$$

The average junction temperature (T_J) can be calculated as follows.

Equation 31:

$$T_J = P_{TOTAL} \times R_{\theta JA} + T_A$$

where P_{TOTAL} is the total power dissipated from Equation 30, $R_{\theta JA}$ is the junction-to-ambient thermal resistance (see Thermal Characteristics), and T_A is the ambient temperature.

$R_{\theta JA}$ includes the thermal impedance from junction to case, $R_{\theta JC}$, and the thermal impedance from case to ambient, $R_{\theta CA}$. $R_{\theta CA}$ is generally determined by the amount of copper that is used underneath and around the device on the printed circuit board. See PCB Layout Guidelines section for more details on optimizing the thermal impedance of the board.

The maximum allowed power dissipation depends on how efficiently heat can be transferred from the junction to the ambient air, i.e., minimizing the $R_{\theta JA}$. As with any regulator, there are limits to the amount of heat that can be dissipated before risking thermal shutdown. There are tradeoffs between ambient operating temperature, input voltage, output voltage, output current, switching frequency, PCB thermal resistance, airflow, and other nearby heat sources. Even a small amount of airflow can reduce the junction temperature considerably.

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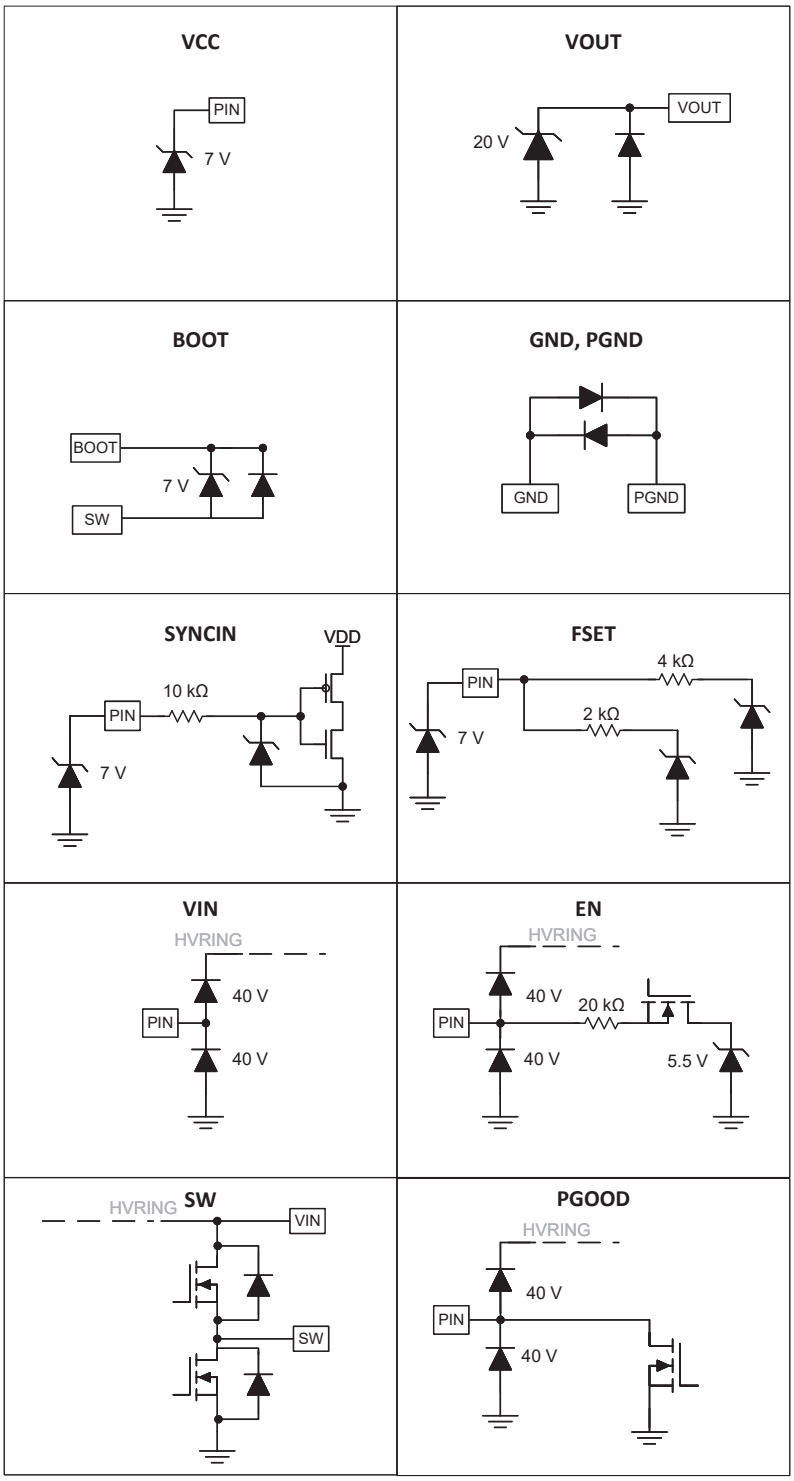
INPUT/OUTPUT STRUCTURES



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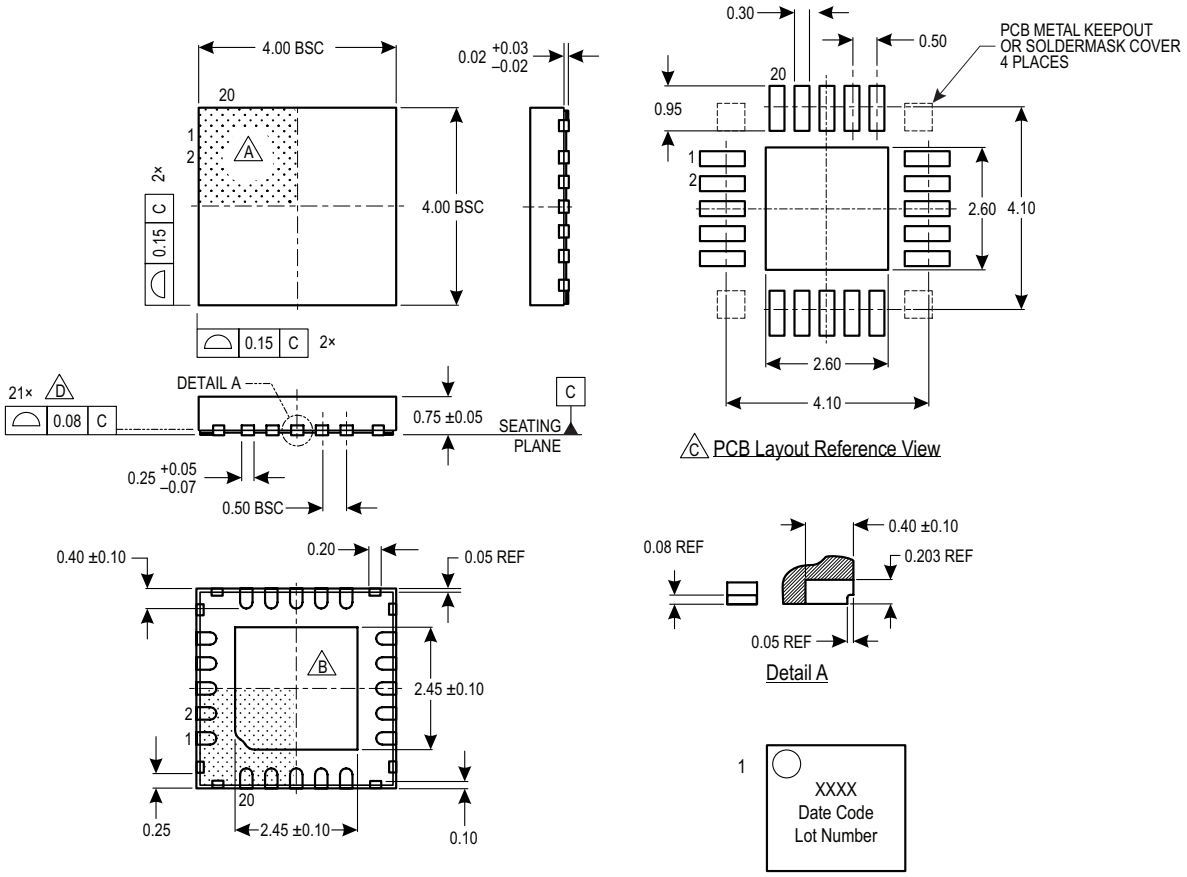
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000222 Rev. 4 or JEDEC MO-220WGGD)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area.

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion).

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-21BM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5).

D Coplanarity includes exposed thermal pad and terminals.

E Branding scale and appearance at supplier discretion.

E Standard Branding Reference View

Lines 1, 2, 3 = 6 characters

Line 1: Part Number
Line 2: 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Pin 1 Dot top left
Center align

Figure 11: 20-Pin 4 mm × 4 mm QFN with exposed thermal pad and wettable flank (suffix ES)

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Revision History

Number	Date	Description
–	February 4, 2022	Initial release
1	February 11, 2022	Updated Features and Benefits (page 1), Terminal Diagram (page 4), VOUT Voltage Accuracy test conditions (page 6), PWM Frequency Dither Range test conditions (page 6), SYNC Voltage Thresholds footnote references (page 7), TSD Hysteresis symbol (page 8); added Startup and Shutdown plots (page 11), Line Regulation plots (page 12); updated EMI/EMC Performance Characteristics plots (page 13), Figure 3 (page 15), Boot Capacitor Protection section (page 18), Table 2 (page 18), Output Inductor section (page 20), Equations 13 and 14 (page 22), Equation 23 (page 23), Power Dissipation section (page 29), and Input/Output Structures (page 28).

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