LM9036 Ultra-Low Quiescent Current Voltage Regulator

Check for Samples: LM9036

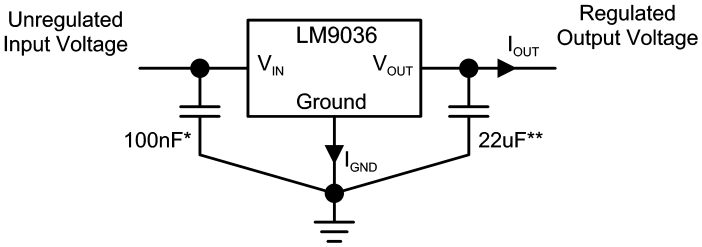
FEATURES

- **Ultra low Ground Pin Current (I_{GND} ≤ 25µA for I_{OUT} = 0.1mA)**
- **Fixed 5V, 3.3V, 50mA Output**
- **Output Tolerance ±5% Over Line, Load, and Temperature**
- **Dropout Voltage Typically 200mV @ I_{OUT} = 50mA**
- **−45V Reverse Transient Protection**
- **Internal Short Circuit Current Limit**
- **Internal Thermal Shutdown Protection**
- **40V Operating Voltage Limit**

DESCRIPTION

The LM9036 ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 25µA Ground Pin current at a 0.1mA load, the LM9036 is ideally suited for automotive and other battery operated systems. The LM9036 retains all of the features that are common to low dropout regulators including a low dropout PNP pass device, short circuit protection, reverse battery protection, and thermal shutdown. The LM9036 has a 40V maximum operating voltage limit, a −40°C to +125°C operating temperature range, and ±5% output voltage tolerance over the entire output current, input voltage, and temperature range.

Typical Application



* Required if regulator is located more than 2″ from power supply filter capacitor.
** Required for stability. Must be rated over intended operating temperature range. Effective series resistance (ESR) is critical, see Electrical Characteristics. Locate capacitor as close as possible to the regulator output and ground pins. Capacitance may be increased without bound.

Connection Diagram

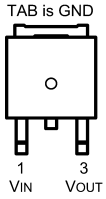


Figure 1. PFM
Top View
Order Number LM9036DT-5.0, LM9036DTX-5.0,
LM9036DT-3.3, LM9036DTX-3.3
See NS Package Number NDP0003B

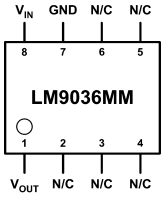


Figure 2. 8 Lead VSSOP
Top View
LM9036MM-3.3, , LM9036MMX-3.3, LM9036MM-5.0, LM9036MMX-5.0
See NS Package Number DGK

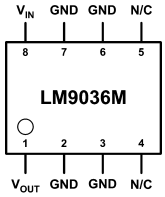


Figure 3. 8 Lead SOIC
Top View
LM9036M-3.3, LM9036MX-3.3, LM9036M-5.0, LM9036MX-5.0
See NS Package Number D

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Input Voltage (Survival)	+55V, −45V
ESD Susceptibility(3)	±1.9kV
Power Dissipation(4)	Internally limited
Junction Temperature (T_{Jmax})	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human body model, 100pF discharge through a 1.5kΩ resistor.
(4) The maximum power dissipation is a function of T_{Jmax}, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the LM9036 will go into thermal shutdown.

Operating Ratings

Operating Temperature Range	−40°C to +125°C
Maximum Input Voltage (Operational)	40V
SOIC-8 (D) θ_{JA}(1)	140°C/W
PFM (NDP0003B) θ_{JA}(1)	125°C/W
PFM (NDP0003B) θ_{JA}(2)	50°C/W
PFM (NDP0003B) θ_{JC}(1)	11°C/W
MSO-8 (DGK) θ_{JA}(1)	200°C/W

(1) Worst case (Free Air) per EIA / JESD51-3.
(2) Typical θ_{JA} with 1 square inch of 2oz copper pad area directly under the ground tab.

Electrical Characteristics - LM9036-5.0

V_{IN} = 14V, I_{OUT} = 10 mA, T_J = 25°C, unless otherwise specified. **Boldface** limits apply over entire operating temperature range

Parameter	Conditions	Min (1)	Typical (2)	Max (1)	Units
Output Voltage (V_{OUT})		4.80	5.00	5.20	V
	5.5V ≤ V_{IN} ≤ 26V, 0.1mA ≤ I_{OUT} ≤ 50mA (3)	**4.75**	**5.00**	**5.25**	
Quiescent Current (I_{GND})	I_{OUT} = 0.1mA, 8V ≤ V_{IN} ≤ 24V		20	25	µA
	I_{OUT} = 1mA, 8V ≤ V_{IN} ≤ 24V		50	100	
	I_{OUT} = 10mA, 8V ≤ V_{IN} ≤ 24V		0.3	0.5	mA
	I_{OUT} = 50mA, 8V ≤ V_{IN} ≤ 24V		2.0	2.5	
Line Regulation (Δ V_{OUT})	6V ≤ V_{IN} ≤ 40V, I_{OUT} = 1mA		10	30	mV
Load Regulation (Δ V_{OUT})	0.1mA ≤ I_{OUT} ≤ 5mA		10	30	mV
	5mA ≤ I_{OUT} ≤ 50mA		10	30	mV
Dropout Voltage (Δ V_{OUT})	I_{OUT} = 0.1mA		0.05	0.10	V
	I_{OUT} = 50mA		0.20	0.40	V
Short Circuit Current (I_{SC})	V_{OUT} = 0V	65	120	250	mA
Ripple Rejection (PSRR)	V_{ripple} = 1V_{rms}, F_{ripple} = 120Hz	−40	−60		dB
Output Bypass Capacitance (C_{OUT})	0.3Ω ≤ ESR ≤ 8Ω 0.1mA ≤ I_{OUT} ≤ 50mA	10	22		µF

(1) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level) and 100% tested.
(2) Typicals are at 25°C (unless otherwise specified) and represent the most likely parametric norm.
(3) To ensure constant junction temperature, pulse testing is used.

Electrical Characteristics - LM9036-3.3

V_{IN} = 14V, I_{OUT} = 10 mA, T_J = 25°C, unless otherwise specified. **Boldface** limits apply over entire operating temperature range

Parameter	Conditions	Min (1)	Typical (2)	Max (1)	Units
Output Voltage (V_{OUT})		3.168	3.30	3.432	V
	5.5V ≤ V_{IN} ≤ 26V, 0.1mA ≤ I_{OUT} ≤ 50mA (3)	**3.135**	**3.30**	**3.465**	
Quiescent Current (I_{GND})	I_{OUT} = 0.1mA, 8V ≤ V_{IN} ≤ 24V		20	25	µA
	I_{OUT} = 1mA, 8V ≤ V_{IN} ≤ 24V		50	100	
	I_{OUT} = 10mA, 8V ≤ V_{IN} ≤ 24V		0.3	0.5	mA
	I_{OUT} = 50mA, 8V ≤ V_{IN} ≤ 24V		2.0	2.5	
Line Regulation (Δ V_{OUT})	6V ≤ V_{IN} ≤ 40V, I_{OUT} = 1mA		10	30	mV
Load Regulation (Δ V_{OUT})	0.1mA ≤ I_{OUT} ≤ 5mA		10	30	mV
	5mA ≤ I_{OUT} ≤ 50mA		10	30	mV
Dropout Voltage (Δ V_{OUT})	I_{OUT} = 0.1mA		0.05	0.10	V
	I_{OUT} = 50mA		0.20	0.40	V
Short Circuit Current (I_{SC})	V_{OUT} = 0V	65	120	250	mA
Ripple Rejection (PSRR)	V_{ripple} = 1V_{rms}, F_{ripple} = 120Hz	−40	−60		dB
Output Bypass Capacitance (C_{OUT})	0.3Ω ≤ ESR ≤ 8Ω 0.1mA ≤ I_{OUT} ≤ 50mA	22	33		µF

(1) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level) and 100% tested.
(2) Typicals are at 25°C (unless otherwise specified) and represent the most likely parametric norm.
(3) To ensure constant junction temperature, pulse testing is used.

Typical Performance Characteristics

Dropout Voltage

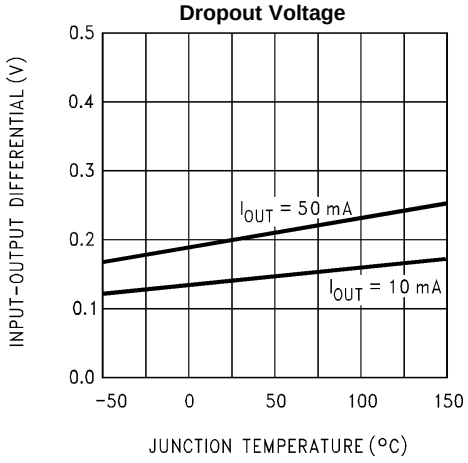


Figure 4.

Quiescent Current

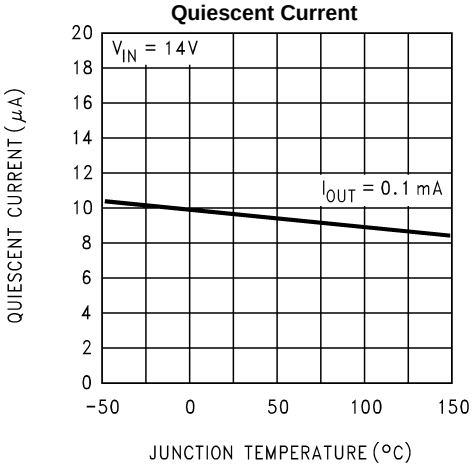


Figure 5.

Quiescent Current

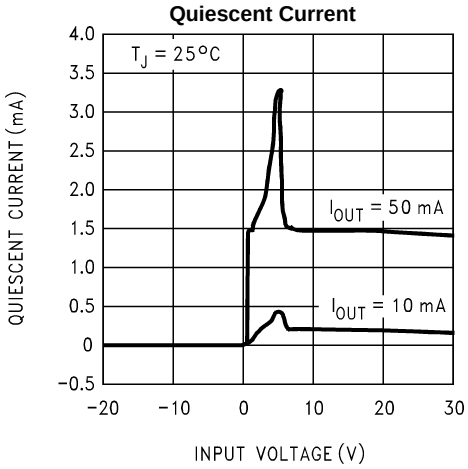


Figure 6.

Quiescent Current

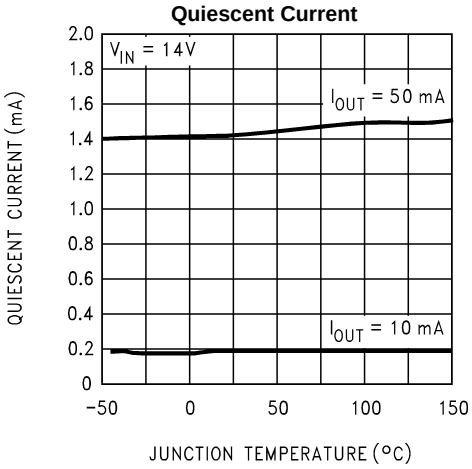


Figure 7.

Peak Output Current

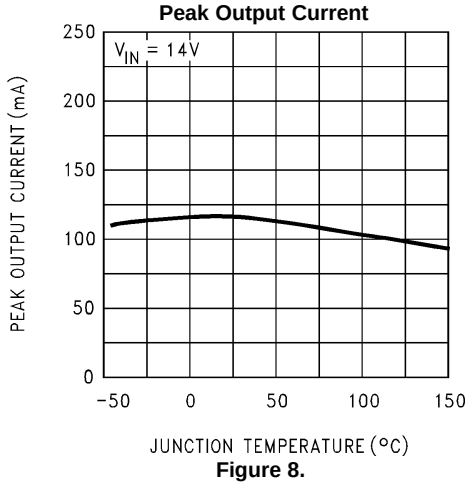


Figure 8.

APPLICATIONS INFORMATION

Unlike other PNP low dropout regulators, the LM9036 remains fully operational to 40V. Owing to power dissipation characteristics of the package, full output current cannot be ensured for all combinations of ambient temperature and input voltage.

The junction to ambient thermal resistance θ_{JA} rating has two distinct components: the junction to case thermal resistance rating θ_{JC}; and the case to ambient thermal resistance rating θ_{CA}. The relationship is defined as: $\theta_{JA} = \theta_{JC} + \theta_{CA}$.

On the PFM package the ground tab is thermally connected to the backside of the die. Adding 1 square inch of 2 oz. copper pad area directly under the ground tab will improve the θ_{JA} rating to approximately 50°C/W.

While the LM9036 has an internally set thermal shutdown point of typically 150°C, this is intended as a safety feature only. Continuous operation near the thermal shutdown temperature should be avoided as it may have a negative affect on the life of the device.

Using the θ_{JA} for a LM9036DT mounted on a circuit board as defined at, see(1), and using the formula for maximum allowable dissipation given in, see(2), for an ambient temperature (T_A) of +85°C, we find that P_{DMAX} = 1.3W. Including the small contribution of the quiescent current I_Q to the total power dissipation, the maximum input voltage (while still delivering 50mA output current) is 29.5V. The LM9036DT will go into thermal shutdown when attempting to deliver the full output current of 50mA, with an ambient temperature of +85°C, and the input voltage is greater than 29.5V. Similarly, with an ambient temperature of 25°C the P_{DMAX} = 2.5W, and the LM9036DT can deliver the full output current of 50mA with an input voltage of up to 40V.

While the LM9036 maintains regulation to 55V, it will not withstand a short circuit above 40V because of safe operating area limitations in the internal PNP pass device. Above 55V the LM9036 will break down with catastrophic effects on the regulator and possibly the load as well. Do not use this device in a design where the input operating voltage may exceed 40V, or where transients are likely to exceed 55V.

(1) Typical θ_{JA} with 1 square inch of 2oz copper pad area directly under the ground tab.
(2) The maximum power dissipation is a function of T_{Jmax}, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{Jmax} - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the LM9036 will go into thermal shutdown.

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM9036DT-5.0/NOPB	ACTIVE	TO-252	NDP	3	75	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LM9036D T-5.0	Samples
LM9036DTX-5.0/NOPB	ACTIVE	TO-252	NDP	3	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	LM9036D T-5.0	Samples
LM9036M-3.3/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6M-3	Samples
LM9036M-5.0/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6M-5	Samples
LM9036MM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KDB	Samples
LM9036MM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KDA	Samples
LM9036MX-3.3/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6M-3	Samples
LM9036MX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6M-5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

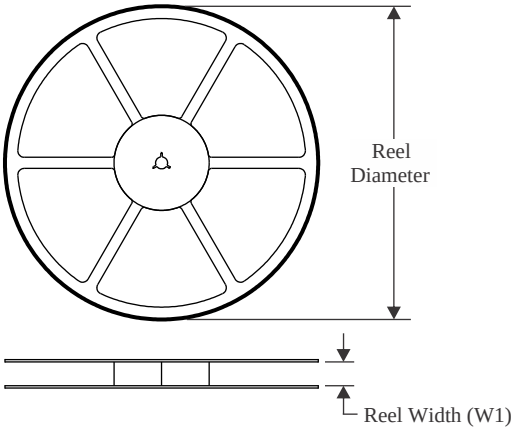
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

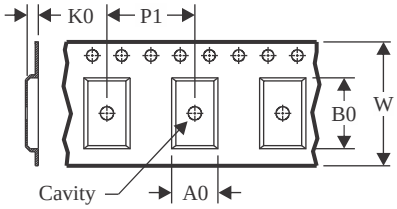
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

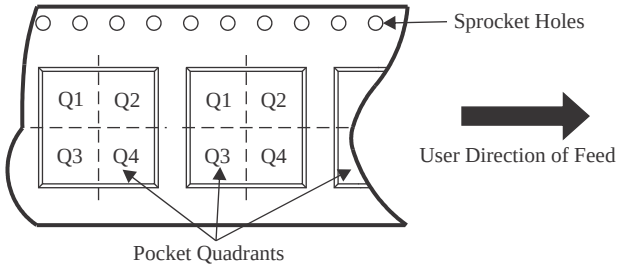


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

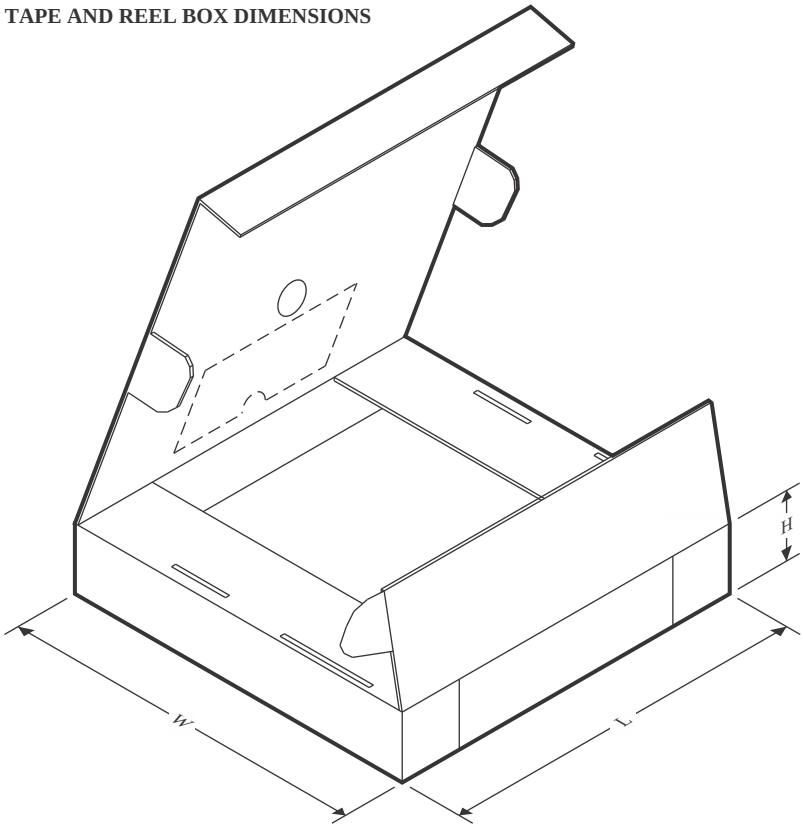
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM9036DTX-5.0/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LM9036MM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036MM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036MX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM9036MX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

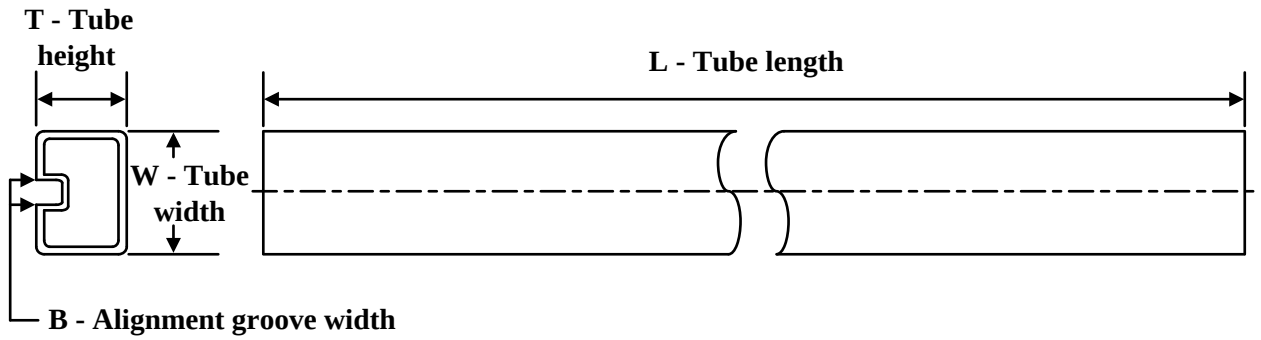
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM9036DTX-5.0/NOPB	TO-252	NDP	3	2500	356.0	356.0	36.0
LM9036MM-3.3/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM9036MM-5.0/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM9036MX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM9036MX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

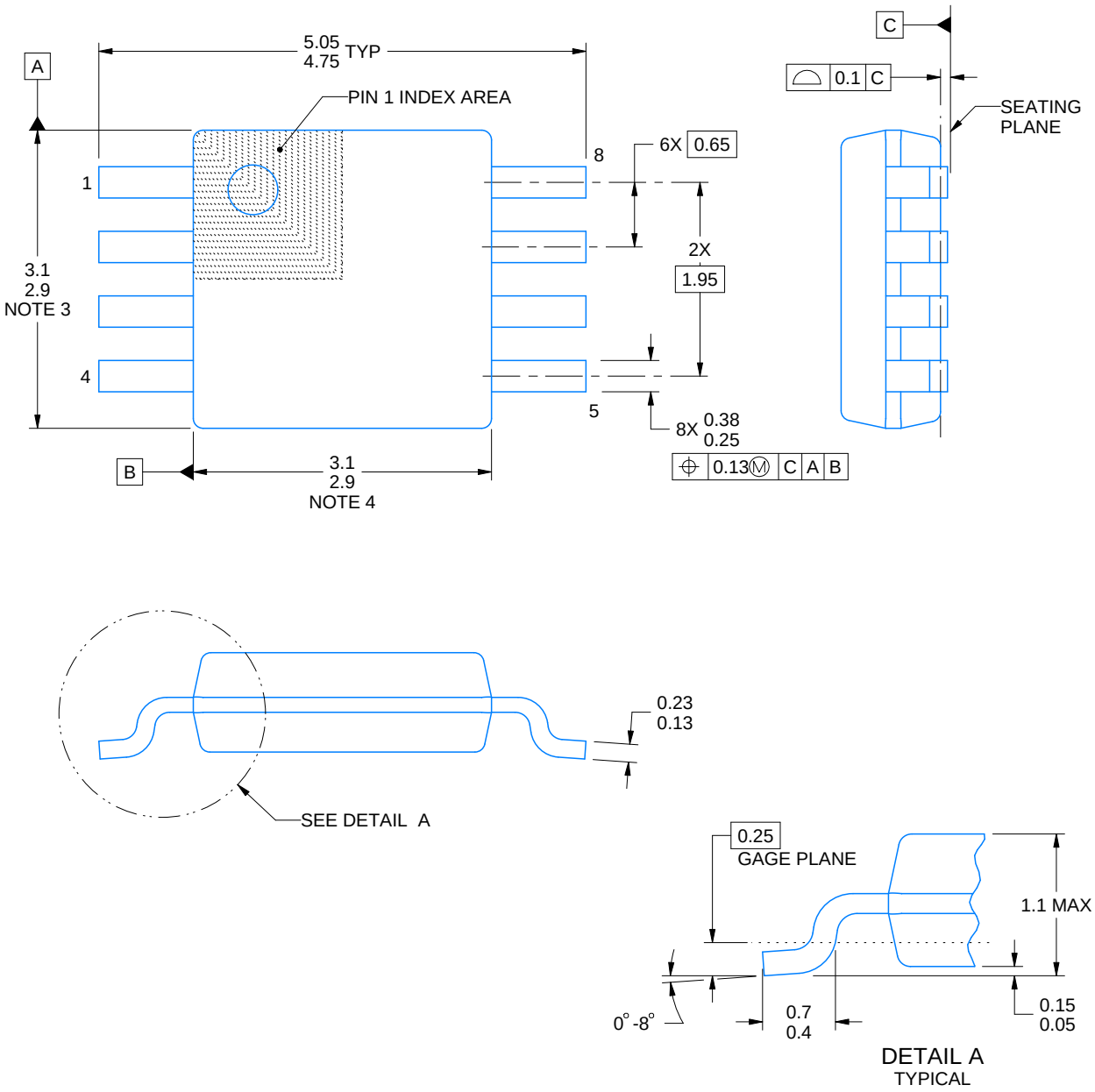
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM9036DT-5.0/NOPB	NDP	TO-252	3	75	508	20	4165.6	3.1
LM9036M-3.3/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM9036M-5.0/NOPB	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

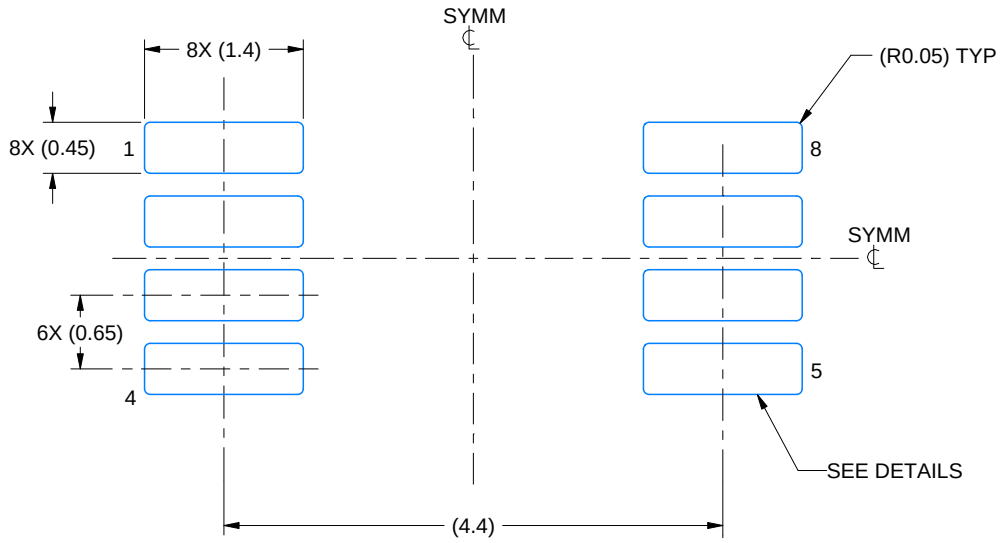
SMALL OUTLINE PACKAGE



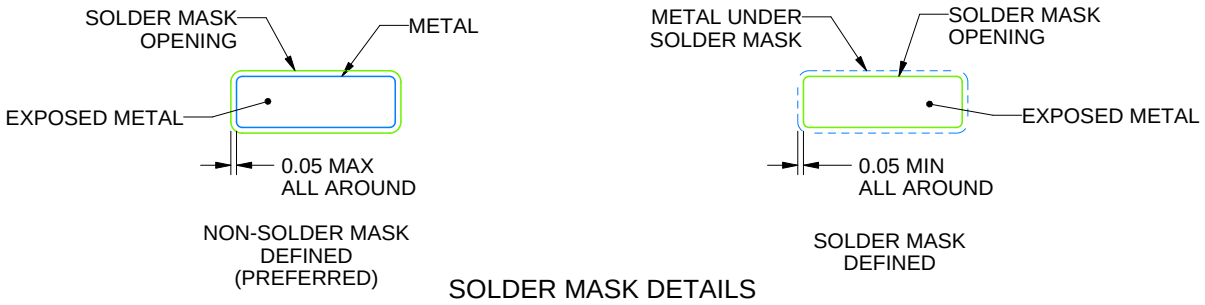
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

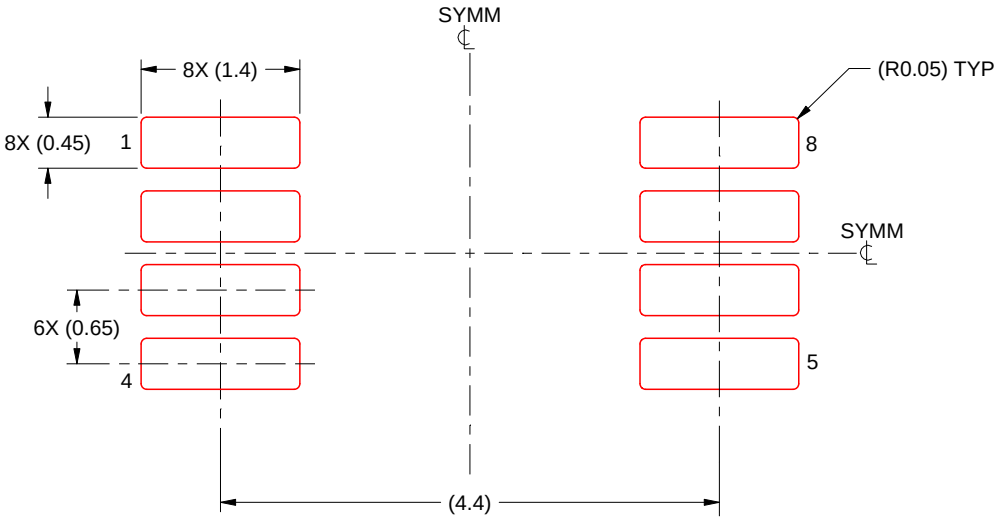


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

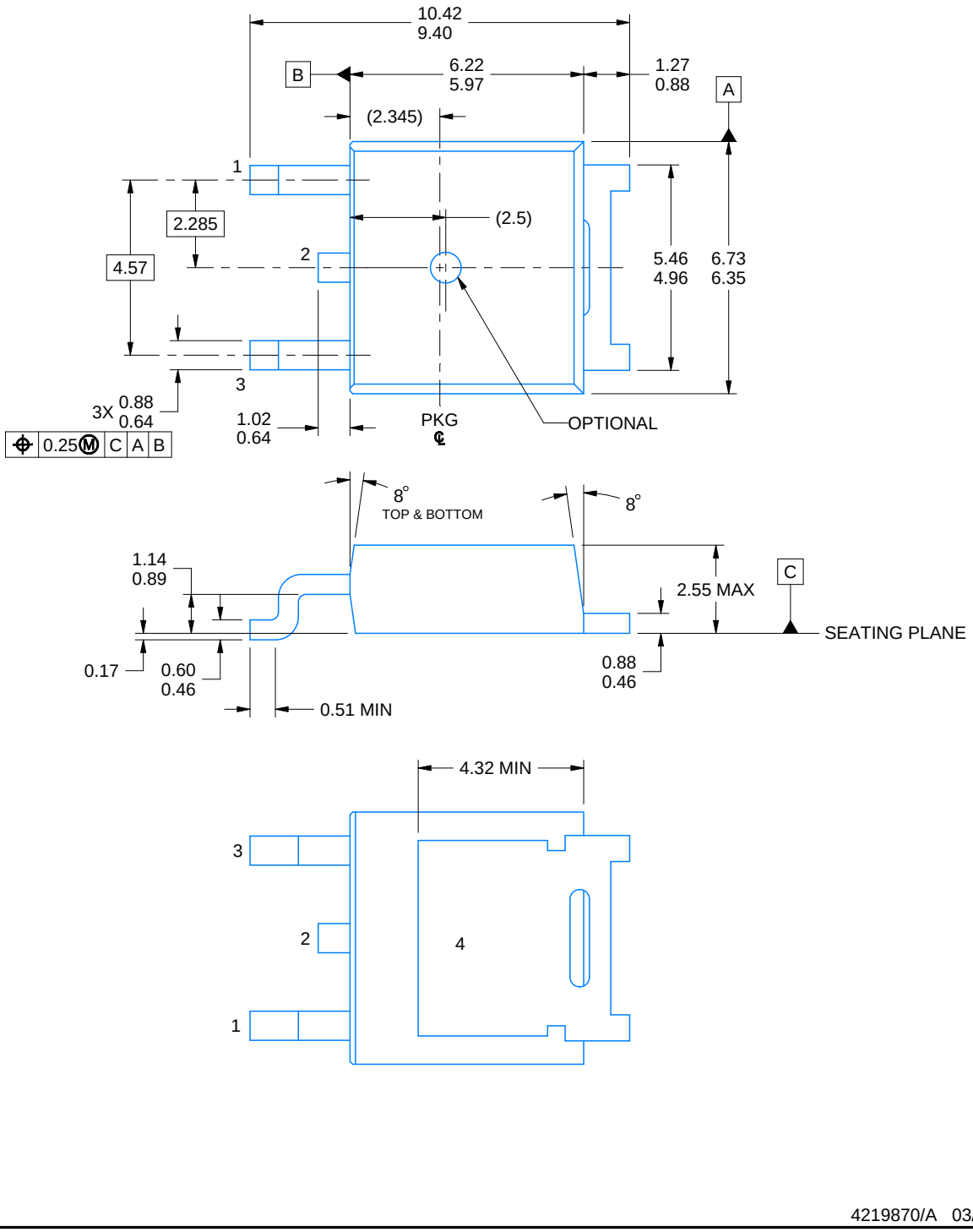
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

NDP0003B

PACKAGE OUTLINE

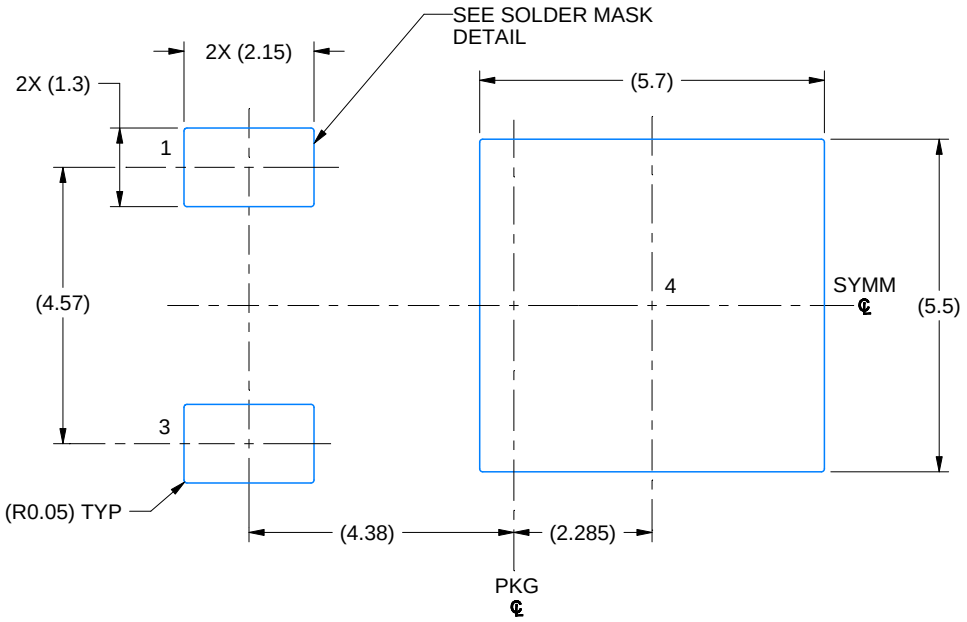
TO-252 - 2.55 mm max height

TRANSISTOR OUTLINE

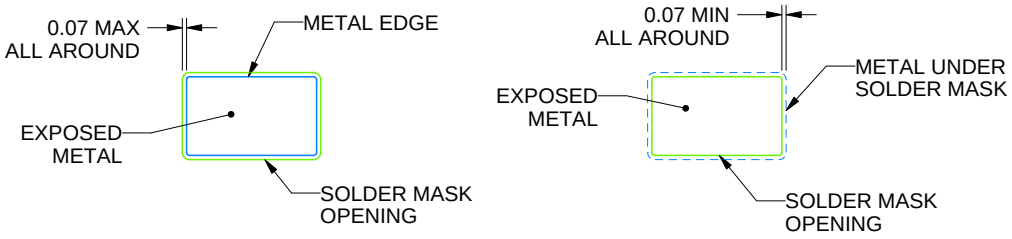


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-252.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

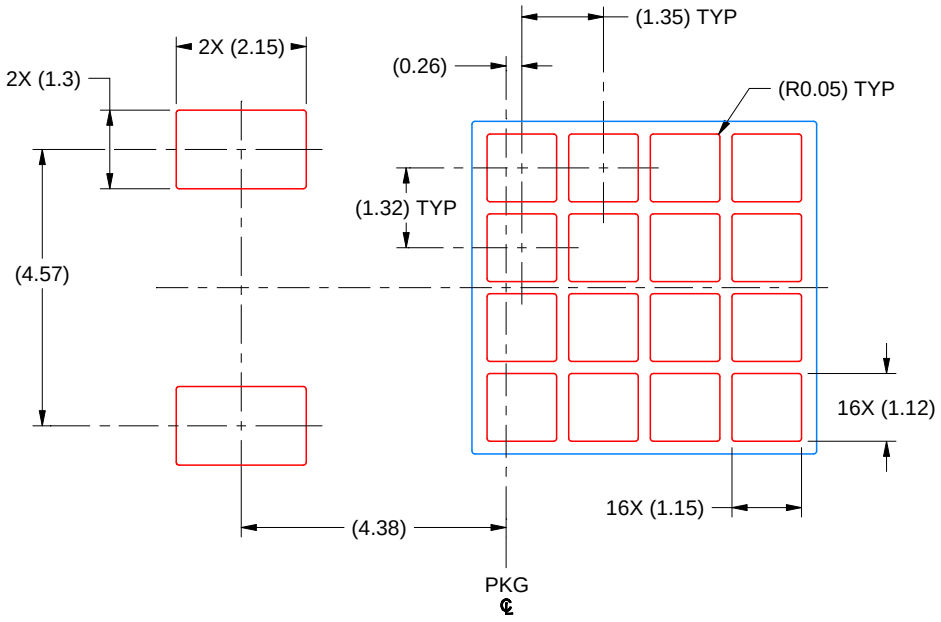


SOLDER MASK DETAIL

4219870/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
5. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

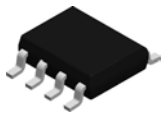


SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 8X

4219870/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

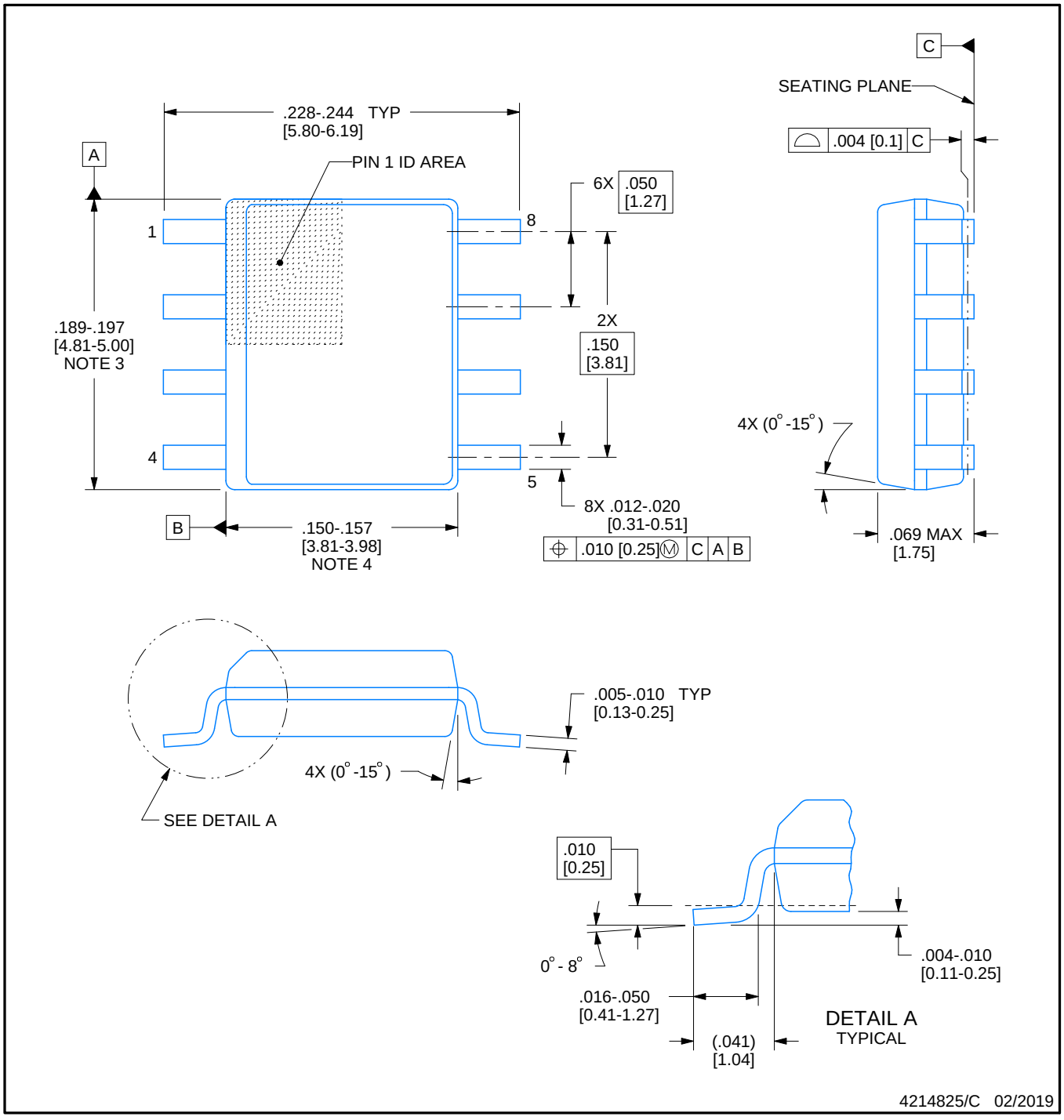


PACKAGE OUTLINE

D0008A

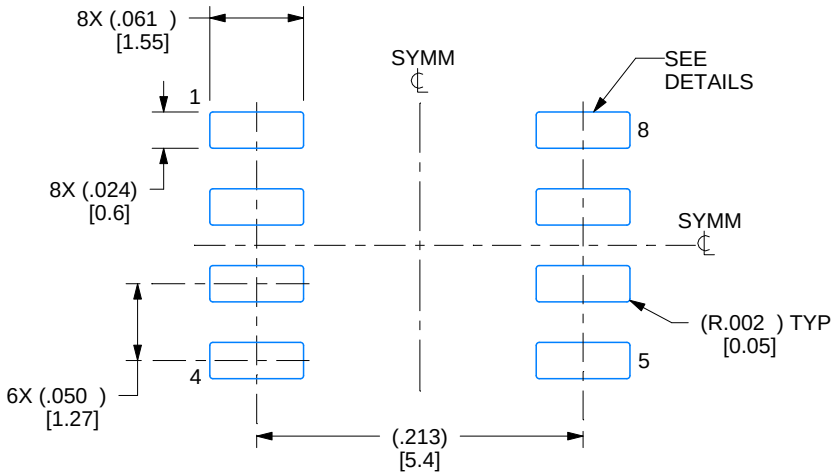
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

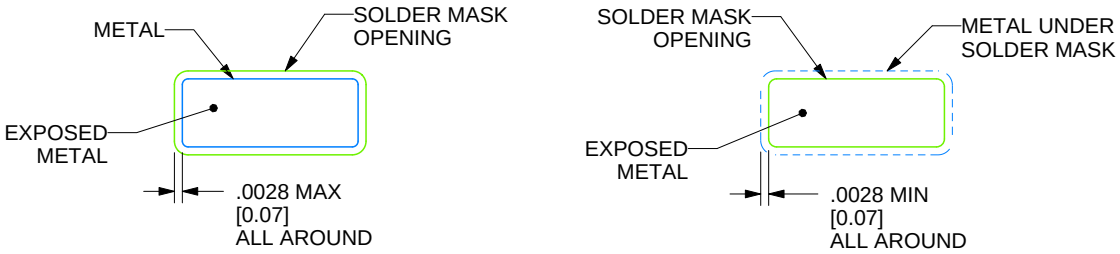


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

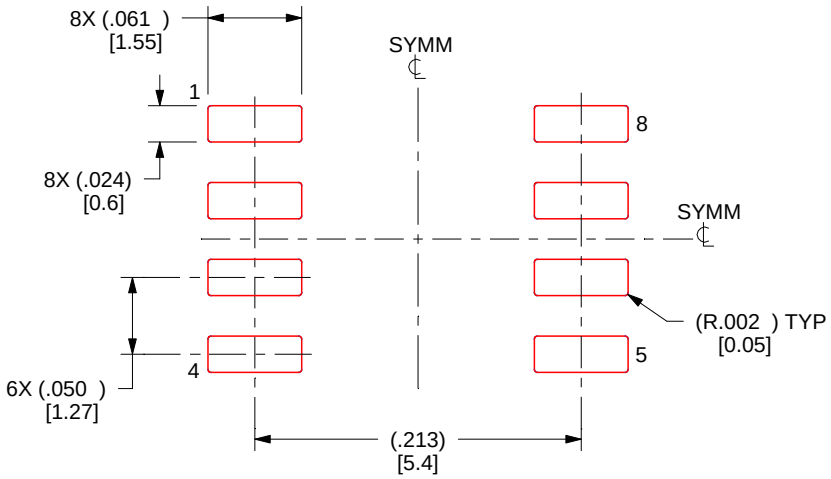
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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