

# N-Channel and P-Channel Enhancement-Mode Dual MOSFET

### **Features**

- · Low Threshold
- · Low On-Resistance
- · Low Input Capacitance
- · Fast Switching Speeds
- · Free from Secondary Breakdown
- · Low Input and Output Leakage
- Independent, Electrically Isolated N-Channel and P-Channel

### **Applications**

- · Medical Ultrasound Transmitters
- · High-Voltage Pulsers
- · Amplifiers
- · Buffers
- · Piezoelectric Transducer Drivers
- · General Purpose Line Drivers
- · Logic-Level Interface

# **General Description**

The TC2320 consists of a high-voltage, low-threshold N-channel and P-channel MOSFET in an 8-Lead SOIC package. This Enhancement-mode (normally-off) transistor uses an advanced vertical DMOS structure and a well-proven silicon gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited for a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance and fast switching speeds are desired.

# **Package Type**



See Table 2-1 for pin information.

# 1.0 ELECTRICAL CHARACTERISTICS

# **Absolute Maximum Ratings†**

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	500
Gate-to-Source Voltage	
Operating Ambient Temperature, T <sub>A</sub>	
Storage Temperature, T <sub>S</sub>	

**† Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

### N-CHANNEL DC AND AC ELECTRICAL CHARACTERISTICS

<b>Electrical Specifications:</b> Unless otherwise noted, $T_A = T_J = +25$ °C.									
Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions			
DC PARAMETER (Note 1)									
Drain-to-Source Breakdown Voltage	BV <sub>DSS</sub>	200	_	_	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 100 μA			
Gate Threshold Voltage	V <sub>GS(th)</sub>	0.6	_	2	V	$V_{GS} = V_{DS}$ , $I_D = 1 \text{ mA}$			
Change in V <sub>GS(th)</sub> with Temperature	$\Delta V_{GS(th)}$	_	_	-4.5	mV/°C	$V_{GS} = V_{DS}$ , $I_D = 1 \text{ mA } (\text{Note 2})$			
Gate Body Leakage Current	I <sub>GSS</sub>		_	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$			
			_	1	μA	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 100V			
		_		10	μA	$V_{GS} = 0V$ , $V_{DS} = Maximum rating$			
Zero-Gate Voltage Drain Current	I <sub>DSS</sub>	1	_	1	mA	$V_{GS} = 0V$ , $T_A = 125$ °C, $V_{DS} = 0.8$ Maximum rating (Note 2)			
On-State Drain Current	1	0.6	_	_	Α	$V_{GS} = 4.5V, V_{DS} = 25V$			
On-State Drain Current	I <sub>D(ON)</sub>	1.2	_		Α	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 25V			
Static Drain-to-Source On-State	R <sub>DS(ON)</sub>	_	_	8	Ω	$V_{GS} = 4.5V, I_D = 150 \text{ mA}$			
Resistance			_	7	Ω	$V_{GS} = 10V, I_D = 1A$			
Change in R <sub>DS(ON)</sub> with Temperature	$\Delta R_{DS(ON)}$	_	_	1	%/°C	$V_{GS} = 4.5V, I_D = 150 \text{ mA } (\text{Note 2})$			
AC PARAMETER (Note 2)									
Forward Transconductance	G <sub>FS</sub>	150	_	_	mmho	V <sub>DS</sub> = 25V, I <sub>D</sub> = 200 mA			
Input Capacitance	C <sub>ISS</sub>	_	_	110	pF	V <sub>GS</sub> = 0V,			
Common Source Output Capacitance	C <sub>OSS</sub>	_	_	60	pF	V <sub>DS</sub> = 25V,			
Reverse Transfer Capacitance	C <sub>RSS</sub>	_	_	23	pF	f = 1 MHz			
Turn-On Delay Time	t <sub>d(ON)</sub>	_	_	20	ns				
Rise Time	t <sub>r</sub>	_	_	15	ns	$V_{DD} = 25V,$			
Turn-Off Delay Time	t <sub>d(OFF)</sub>		_	25	ns	$I_D = 150 \text{ mA},$ $R_{GEN} = 25\Omega$			
Fall Time	t <sub>f</sub>	1	_	25	ns	GLIV			
DIODE PARAMETER									
Diode Forward Voltage Drop	$V_{SD}$		_	1.8	V	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 200 mA ( <b>Note 1</b> )			
Reverse Recovery Time	t <sub>rr</sub>	_	300	_	ns	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 200 mA ( <b>Note 2</b> )			

**Note 1:** Unless otherwise stated, all DC parameters are 100% tested at +25°C. Pulse test: 300 μs pulse, 2% duty cycle.

<sup>2:</sup> Specification is obtained by characterization and is not 100% tested.

# P-CHANNEL DC AND AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $T_A = T_J = +25$ °C.									
Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions			
DC PARAMETER (Note 1)									
Drain-to-Source Breakdown Voltage	BV <sub>DSS</sub>	-200	_	_	V	$V_{GS} = 0V$ , $I_D = -2 \text{ mA}$			
Gate Threshold Voltage	V <sub>GS(th)</sub>	-1	_	-2.4	V	$V_{GS} = V_{DS}$ , $I_D = -1$ mA			
Change in V <sub>GS(th)</sub> with Temperature	$\Delta V_{GS(th)}$	_	_	4.5	mV/°C	$V_{GS} = V_{DS}$ , $I_D = -1 \text{ mA } (\text{Note 2})$			
Gate Body Leakage	$I_{GSS}$		1	-100	nA	$V_{GS} = \pm 20V$ , $V_{DS} = 0V$			
		ı		-10	μA	V <sub>GS</sub> = 0V, V <sub>DS</sub> = Maximum rating			
Zero-Gate Voltage Drain Current	I <sub>DSS</sub>	l		-1	mA	$V_{GS} = 0V$ , $T_A = 125$ °C, $V_{DS} = 0.8$ Maximum rating (Note 2)			
On-State Drain Current	1	-0.25	-0.7		Α	$V_{GS} = -4.5V, V_{DS} = -25V$			
On-State Drain Current	I <sub>D(ON)</sub>	-0.75	-2.1	_	Α	$V_{GS} = -10V, V_{DS} = -25V$			
Static Drain-to-Source On-State	_	_	10	15	Ω	$V_{GS} = -4.5V$ , $I_D = -100$ mA			
Resistance	R <sub>DS(ON)</sub>		8	12	Ω	$V_{GS} = -10V$ , $I_D = -200$ mA			
Change in R <sub>DS(ON)</sub> with Temperature	$\Delta_{RDS(ON)}$			1.7	%/°C	V <sub>GS</sub> = -10V, I <sub>D</sub> = -200 mA ( <b>Note 2</b> )			
AC PARAMETER (Note 2)									
Forward Transconductance	G <sub>FS</sub>	100	250	_	mmho	$V_{DS} = -25V$ , $I_{D} = -200$ mA			
Input Capacitance	C <sub>ISS</sub>	_	75	125	pF	V <sub>GS</sub> = 0V,			
Common-Source Output Capacitance	C <sub>OSS</sub>		20	85	pF	$V_{DS} = -25V$ ,			
Reverse Transfer Capacitance	$C_{RSS}$	_	10	35	pF	f = 1 MHz			
Turn-On Delay Time	t <sub>d(ON)</sub>			10	ns				
Rise Time	t <sub>r</sub>		_	15	ns	V <sub>DD</sub> = –25V, I <sub>D</sub> = –0.75A,			
Turn-On Delay Time	t <sub>d(OFF)</sub>			20	ns	$R_{GEN} = 25\Omega$			
Fall Time	t <sub>f</sub>	_	_	15	ns	GLIN =			
DIODE PARAMETER									
Diode Forward Voltage Drop	$V_{SD}$	_	_	-1.8	V	$V_{GS} = 0V, I_{SD} = -0.5A $ (Note 1)			
Reverse Recovery Time	t <sub>rr</sub>	_	300	_	ns	$V_{GS} = 0V, I_{SD} = -0.5A (Note 2)$			

**Note 1:** Unless otherwise stated, all DC parameters are 100% tested at +25°C. Pulse test: 300 μs pulse, 2% duty cycle.

# **TEMPERATURE SPECIFICATIONS**

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions			
TEMPERATURE RANGE									
Operating Ambient Temperature	T <sub>A</sub>	-55	_	+150	°C				
Storage Temperature	T <sub>S</sub>	-55	_	+150	°C				
PACKAGE THERMAL RESISTANCE									
8-lead SOIC	$\theta_{\sf JA}$	_	101	_	°C/W	Note 1			
N-4- 4- 4 f 0" 4" DOD									

Note 1: 1 oz., four-layer, 3" x 4" PCB

<sup>2:</sup> Specification is obtained by characterization and is not 100% tested.

# **TC2320**

# 2.0 PIN DESCRIPTION

Table 2-1 shows the description of pins in TC2320. Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	SN	Source N-channel
2	GN	Gate N-channel
3	SP	Source P-channel
4	GP	Gate P-channel
5	DP	Drain P-channel
6	DP	Drain P-channel
7	DN	Drain N-channel
8	DN	Drain N-channel

# 3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 and Figure 3-2 illustrate the switching waveforms and test circuits for TC2320.

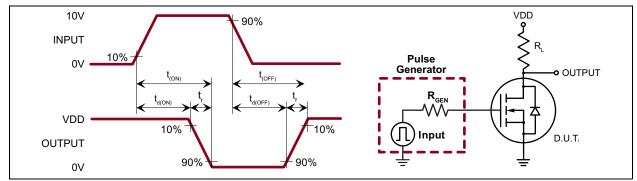


FIGURE 3-1: N-Channel Switching Waveforms and Test Circuit.

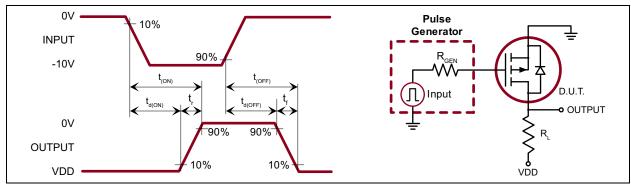


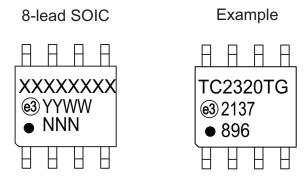
FIGURE 3-2: P-Channel Switching Waveforms and Test Circuit.

TABLE 3-1: PRODUCT SUMMARY

BV <sub>DS</sub>	<sub>S</sub> /BV <sub>DGS</sub> (V)	R <sub>DS(ON)</sub> (Maximum) (Ω)				
N-Channel	P-Channel	N-Channel	P-Channel			
200	-200	7	12			

### 4.0 PACKAGING INFORMATION

# 4.1 Package Marking Information



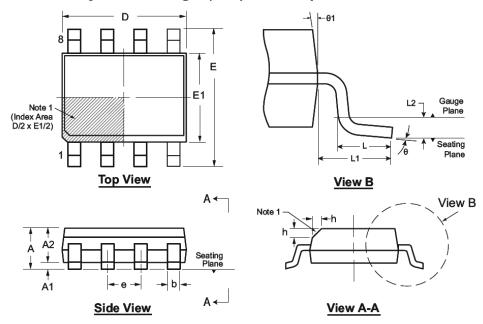
Legend: XX...X Product Code or Customer-specific information
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code

By-free JEDEC® designator for Matte Tin (Sn)
This package is Pb-free. The Pb-free JEDEC designator (a)
can be found on the outer packaging for this package.

te: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

# 8-Lead SOIC (Narrow Body) Package Outline (LG/TG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbo	I	Α	A1	A2	b	D	E	E1	е	h	L	L1	L2	θ	θ1
	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*		0.25	0.40			<b>0</b> o	5º
Dimension (mm)	NOM	-	-	-	-	4.90	6.00	3.90	1.27 BSC	-	-	1.04 REF	0.25 BSC	-	-
()	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*	230	0.50	1.27		230	8º	15º

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
\* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

# **TC2320**

NOTES:

# APPENDIX A: REVISION HISTORY

# Revision A (June 2017)

- Converted Supertex Doc# DSFP-TC2320 to Microchip DS20005708A
- Changed packaging format
- Changed the packaging quantity of the 8-lead SOIC TG package from 2000/Reel to 3300/Reel
- Made minor text changes throughout the document

# Revision B (March 2021)

- Corrected the On-State Drain Current  $V_{DS}$  condition and changed the value from -5V to -25V
- Made minor text changes throughout the document

# PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Example: PART NO. XXPackage Device Media Type Environmental a) TC2320TG-G: N-Channel and P-Channel Options Enhancement-Mode Dual MOSFET, 8-lead SOIC, 3300/Reel N-Channel and P-Channel Enhancement-Mode Dual MOSFET TC2320 Device: 8-lead SOIC Package: TG Environmental: G Lead (Pb)-free/RoHS-compliant Package Media Type: (blank) 3300/Reel for a TG Package

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ISBN: 978-1-5224-7842-3



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