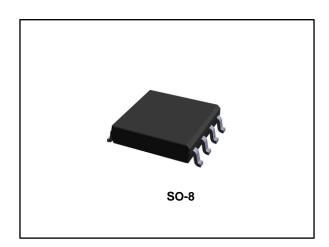
LCDP1521S



Dual line programmable transient voltage suppressor for SLIC protection

Datasheet - production data



Features

- Dual line programmable transient voltage suppressor with separated gates
- Wide negative firing voltage range:
 V_{Gn} = -175 V max.
- Low dynamic switching voltages:
 V_{FP} and V_{DGL}
- Low gate triggering current: I_{GT} = 5 mA max
- Peak pulse current: I_{PP} = 40 A (5/310 μs)
- Holding current: $I_H = 150$ mA min.

Benefits

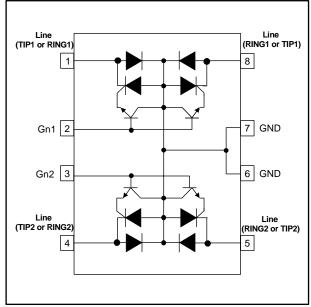
- A Trisil™ is not subject to ageing and provides a fail safe mode in short circuit for a better protection.
- Trisils are used to help equipment to meet various standards such as UL1950, IEC 60950 / CSA C22.2, UL1459 and TIA-968-A (formerly FCC part 68).
- Trisils have UL94 V0 resin approved (Trisils are UL497B approved file: E136224).

Description

This device has been especially designed to protect 2 new high voltage, as well as classical SLICs, against transient overvoltages.

Positive overvoltages are clamped by 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to -VBAT through the gate. Separated gates allow the SLICs to be supplied by two different voltages.

Figure 1: Functional diagram



Characteristics LCDP1521S

1 Characteristics

Table 1: Standards compliance

Standard	Peak surge voltage (V)	Voltage waveform	Required peak current (A)	Current waveform	Minimum serial resistor to meet standard (Ω)
GR-1089 Core	2500	2/10 µs	500	2/10 μs	20
First level	1000	10/1000 µs	100	10/1000 µs	30
GR-1089 Core Second level	5000	2/10 μs	500	2/10 µs	40
GR-1089 Core Intra-building	1500	2/10 μs	100	2/10 µs	0
ITU-T-K20/K21	6000	10/700	150	5/310 µs	110
	1500	10/700 μs	37.5		0
ITU-T-K20 (IEC	ITU-T-K20 (IEC 8000		ESD contact discharge		0
61000-4-2)	15000	1/60 ns	ESD air d	0	
IEC 61000-4-5	4000	10/700 μs	100	5/310 µs	60
IEC 61000-4-5	4000	1.2/50 µs	100	8/20 μs	5
TIA-968-A,	1500	10/160 µs	100	10/160 µs	26
lightning surge type A	800	10/560 µs	200	10/560 µs	19
TIA-968-A, lightning surge type B	1000	9/720 µs	25	5/320 μs	0

Table 2: Thermal resistances

Symbol	Parameter	Value	Unit
R _{th(j-a)}	Junction to ambient	170	°C/W

LCDP1521S Characteristics

Table 3: Absolute ratings ((0 °C < T_j < 70 °C, unless otherwise specified))

Symbol		Value	Unit			
		Telcordia GR-1089- CORE Issue 6, May 2011, section 4	10/1000 µs	25		
		TIA-968-A, lightning surge type A	10/560 µs	30	A	
		ITU-T K20/21/44/45, (10/700 µs open circuit voltage waveshape)	5/310 μs	40		
I _{pp}	Peak pulse current ⁽¹⁾	TIA-968-A, lightning surge type A	10/160 µs	45		
		IEC 61000-4-5, (1.2/50 μ s open circuit waveshape) with 10 Ω	2/40 μs	85		
		ITU-T K20/21/44/45, (1.2/50 µs open circuit voltage waveshape)	8/20 μs	90		
		Telcordia GR-1089- CORE Issue 6, (2/10 μs open circuit waveshape)	2/10 μs	100		
			t = 0.2 s	5		
I _{TSM}	Non repetitive surge peak on-state current		t = 1 s	3.5	Α	
ITSM	(50 Hz sinusoidal) ⁽¹⁾		t = 2 s	3	A	
	(00112011001001)		t = 15 mn	1.3		
V _{GN}	Negative battery voltage range			-175	V	
T _{stg}	Storage junction temper		°C			
Tj	Maximum operating junction temperature -55 to + 150					
TL	Maximum temperature	for soldering during 10 s		260	°C	

Notes:

⁽¹⁾The rated current values may be applied either to the Ring to GND or to the Tip to GND terminal pairs. Additionally, the four terminal pairs may have their rated current values applied simultaneously (in this case the GND terminal current will be four times the rated current value of an individual terminal pair)

Characteristics LCDP1521S

Figure 2: Electrical characteristics (definitions)

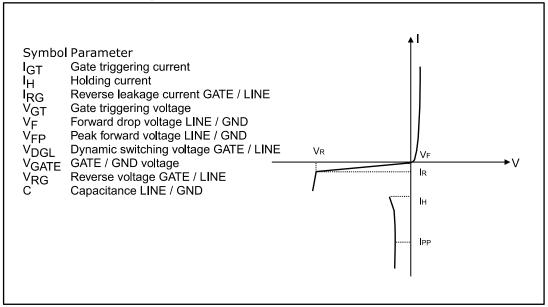
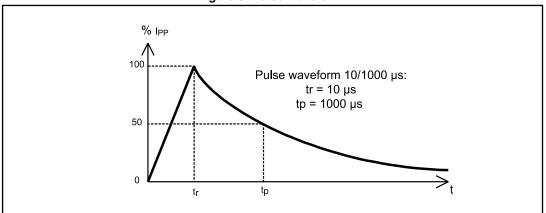


Figure 3: Pulse waveform



LCDP1521S Characteristics

Table 4: Parameters (T_j = 25 °C unless otherwise specified)

Symbol	Test conditions	Min.	Тур.	Max.	Unit	
lgт	V _{LINE} = -48 V		0.05		5	mA
lн	V _{Gn} = -48 V		150			mA
V _{GT}	at I _{GT}				2.5	V
I _{RG}	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$				5 50	μA
V _{DGL} (1)	V_{Gn} = -48 V, 10/700 µs, 1.5 kV, R_S = 0 Ω , I_{PP} = 37.5 A				5	V
VF	I _F = 1 A	t = 500 μs			2	V
V _{FP}	10/700 μs, 1.5 kV, R _S = 0 Ω, I _{PP} = 37.5 A				8	V
I _R	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$				5 50	μΑ
С	V _{LINE} = -50 V, V _{RMS} = 1 V, f = 1 MHz V _{LINE} = -2 V, V _{RMS} = 1 V, f = 1 MHz			18 35		pF

Notes:

Table 5: Recommended gate capacitance

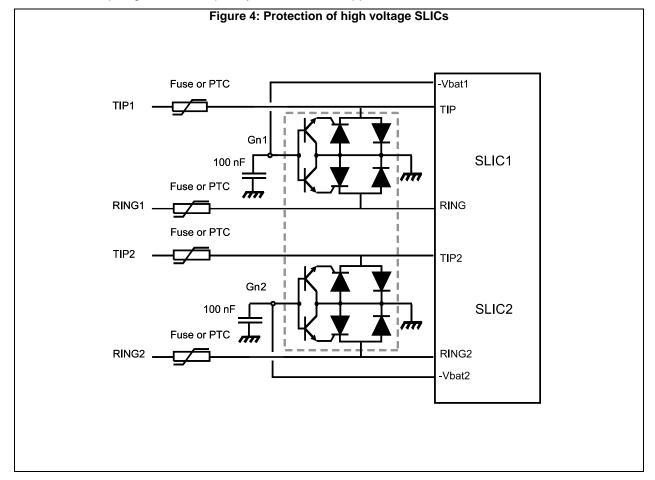
Symbol	Component	Min.	Тур.	Max.	Unit
C _G	Gate decoupling capacitance		220	-	nF

 $[\]ensuremath{^{(1)}}\xspace$ The oscillations with a time duration lower than 50 ns are not taken into account.

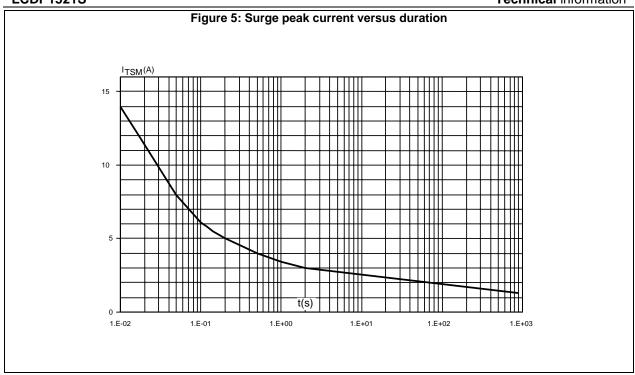
Technical information LCDP1521S

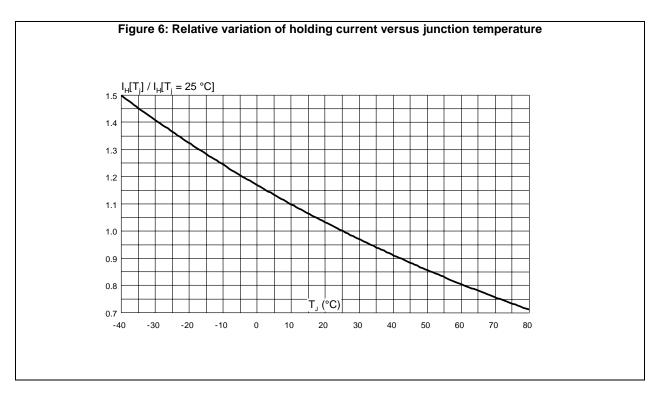
2 Technical information

The LCDP1521S is particularly optimized for the new telecom applications such as the fiber in the loop, the WLL, the remote central office. In this case, the operating voltages are smaller than in the classical system. This makes the high voltage SLICs particularly suitable. The schematics of *Figure 4: "Protection of high voltage SLICs"* shows the topologies most frequently used for these applications.



LCDP1521S Technical information





Package information LCDP1521S

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

3.1 SO-8 package information

Figure 7: SO-8 package outline

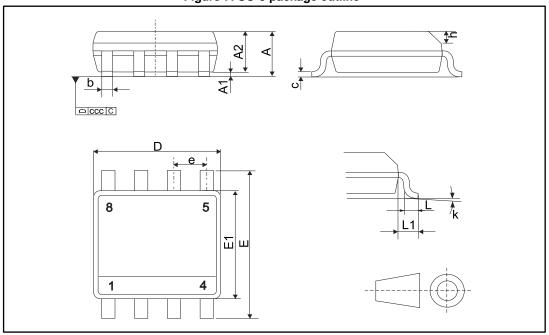


Table 6: SO-8 package mechanical data

	Dimensions							
Ref.	Millimeters			Inches				
	Min.	Тур.	Max.	Min.	Тур.	Max.		
А			1.75			0.069		
A1	0.1		0.25	0.004		0.010		
A2	1.25			0.049				
b	0.31		0.51	0.012		0.020		
С	0.10		0.25	0.004		0.010		
D	4.80	4.90	5.00	0.189	0.193	0.197		
Е	5.80	6.00	6.20	0.228	0.236	0.244		
E1	3.80	3.90	4.00	0.150	0.154	0.157		
е		1.27			0.050			
h	0.25		0.50	0.010		0.020		
L	0.40		1.27	0.016		0.05		
L1		1.04			0.041			
k°	0		8	0		8		
ccc			0.10			0.004		

LCDP1521S Package information

Figure 8: Footprint recommendations, dimensions in mm (inches)

Figure 9: Marking layout (refer to ordering information table for marking)

Chamfer indicates pin 1

XXXXXX

XXXXXX: Marking ZZ: Manufacturing location Y: Year WW: week

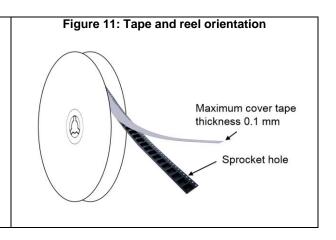
Figure 10: Package orientation in reel

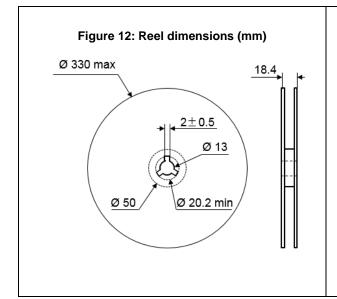
Pin 1

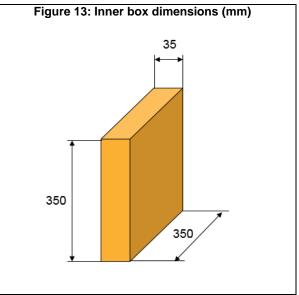
Pin 1

Taped according to EIA-481

Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package







Package information LCDP1521S

Figure 14: Tape and reel outline

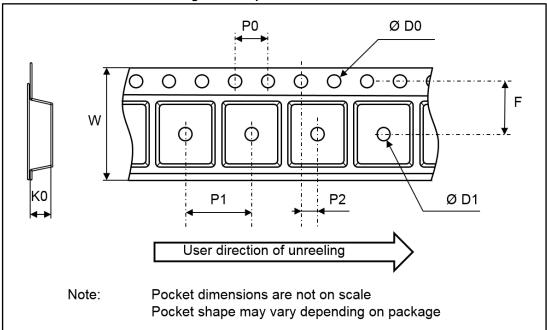


Table 7: Tape and reel mechanical data

	Dimensions						
Ref.	Millimeters						
	Min.	Тур.	Max.				
P0	3.9	4	4.1				
P1	7.9	8	8.1				
P2	1.95	2	2.05				
ØD0	1.45	1.5	1.6				
ØD1	1.6						
F	5.45	5.5	5.55				
K0	2.5	2.6	2.7				
W	11.7	12	12.3				

LCDP1521S Package information

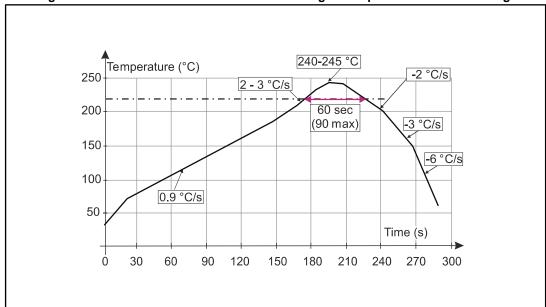


Figure 15: ST ECOPACK® recommended soldering reflow profile for PCB mounting



Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

Ordering information LCDP1521S

4 Ordering information

Figure 16: Ordering information scheme

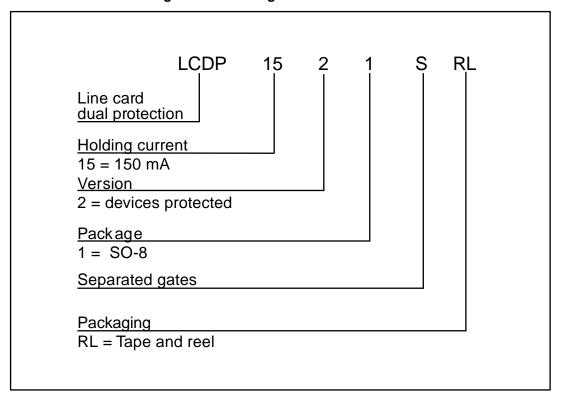


Table 8: Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
LCDP1521SRL	DP152S	SO-8	0.08 g	2500	Tape and reel

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
24-Sep-2009	1	First issue.
23-Feb-2012	2	Standardized nomenclature for Gn and Gp.
20-May-2015	3	Updated Table 3 and package view.
02-Jul-2015	4	Updated package information.
08-Jul-2015	5	Updated Figure 7.
01-Oct-2016	6	Updated Section 6: "Characteristics" and Section 8.1: "SO-8 package information". Minor format changes.
09-Feb-2017 7 Updated Figure 7: "SO-8 package outline".		Updated Figure 7: "SO-8 package outline".

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