TOSHIBA Field-Effect Transistor Silicon N Channel MOS Type

SSM6N40TU

- Power Management Switch Applications
- High-Speed Switching Applications
- 4 V drive
- N-ch 2-in-1
- Low ON-resistance:

 $R_{on} = 182m\Omega \text{ (max)} (@V_{GS} = 4 \text{ V})$ $R_{on} = 122m\Omega \text{ (max)} (@V_{GS} = 10 \text{ V})$

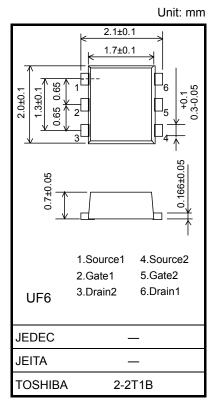
Absolute Maximum Ratings (Ta = 25 °C) (Q1, Q2 Common)

Characteristic		Symbol	Rating	Unit	
Drain-source voltage		V _{DSS}	30	V	
Gate-source voltage		V _{GSS}	±20	V	
Drain current	DC	۱ _D	1.6	A	
	Pulse	I _{DP}	3.2		
Drain power dissipation		P _D (Note1)	500	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	–55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note1: Mounted on an FR4 board. (total dissipation) (25.4 mm \times 25.4 mm \times 1.6 mm, Cu Pad : 645 mm^2)



Weight: 7.0mg (typ.)

Electrical Characteristics (Ta = 25°C) (Q1,Q2 Common)

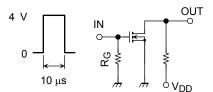
Char	racteristics	Symbol	Test Conditions	Min	Тур.	Max	Unit
Drain-source breakdown voltage	V (BR) DSS	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	30	_	_	- V	
	V (BR) DSX	$I_{D} = 1 \text{ mA}, V_{GS} = -20 \text{ V}$	15	_			
Drain cutoff currer	nt	I _{DSS}	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	_		1	μA
Gate leakage curr	rent	I _{GSS}	$V_{GS} = \pm 16$ V, $V_{DS} = 0$ V	_	—	±1	μA
Gate threshold vo	ltage	V _{th}	$V_{DS} = 5 \text{ V}, \text{ I}_{D} = 1 \text{ mA}$	1.0		2.6	V
Forward transfer a	admittance	Y _{fs}	$V_{DS} = 5 \text{ V}, \text{ I}_{D} = 1 \text{A}$ (Note 2)	1.9	3.7		S
Drain-source ON-resistance	D	$I_D = 1 \text{ A}, V_{GS} = 10 \text{ V}$ (Note 2)	_	96	122	mΩ	
	R _{DS (ON)}	$I_D = 0.5 \text{ A}, V_{GS} = 4 \text{ V}$ (Note 2)	_	130	182		
Input capacitance	1	C _{iss}		_	180	_	
Output capacitance		C _{oss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	_	34	_	pF
Reverse transfer	capacitance	C _{rss}		_	27	_	1
Total Gate Charge Gate–Source Charge		Qg		_	5.1	_	nC
		Q _{gs}	V _{DS} = 15 V, I _D = 1.6 A, V _{GS} = 10 V	_	3.9	_	
Gate-Drain Charge		Q _{gd}			1.2		
Switching time	Turn-on time	t _{on}	V_{DD} = 15 V, I _D = 0.5 A V _{GS} = 0 to 4 V, R _G = 10 Ω		9.5		- ns
	Turn-off time	t _{off}		_	9.0	_	
Drain-source forw	ard voltage	V _{DSF}	$I_D = -1.6 \text{ A}, V_{GS} = 0 \text{ V}$ (Note 2)	_	-0.8	-1.2	V

Note 2: Pulse test

Switching Time Test Circuit

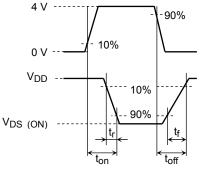
(a) Test Circuit

(b) V_{IN}

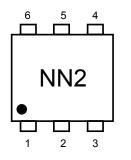


$$\begin{split} V_{DD} &= 15 \text{ V} \\ R_G &= 10 \ \Omega \\ \text{Duty} &\leq 1\% \\ V_{IN} \colon t_r, \ t_f < 5 \ \text{ns} \\ \text{Common Source} \\ Ta &= 25^\circ\text{C} \end{split}$$

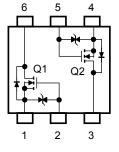
(c) V_{OUT}



Marking



Equivalent Circuit (top view)



Notice on Usage

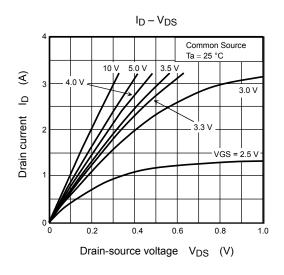
 V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D = 1 mA for this product. For normal switching operation, $V_{GS (on)}$ requires a higher voltage than V_{th} and $V_{GS (off)}$ requires a lower voltage than V_{th} . (The relationship can be established as follows: $V_{GS (off)} < V_{th} < V_{GS (on)}$.)

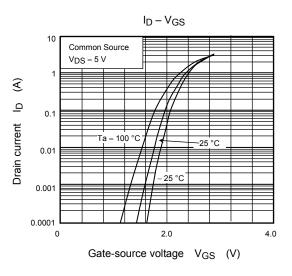
Take this into consideration when using the device.

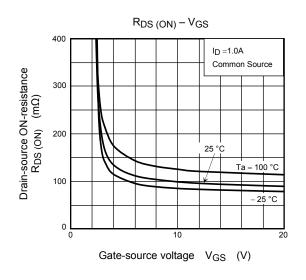
Handling Precaution

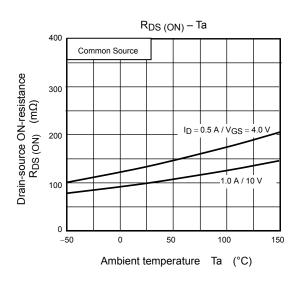
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

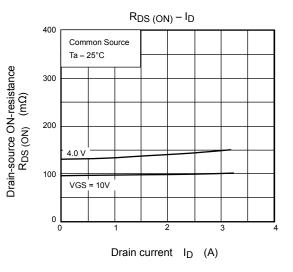
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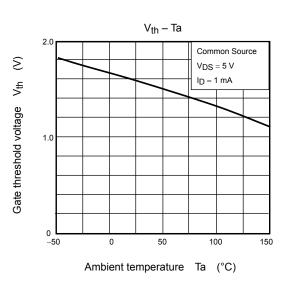




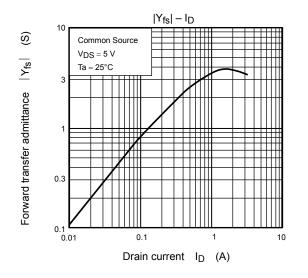


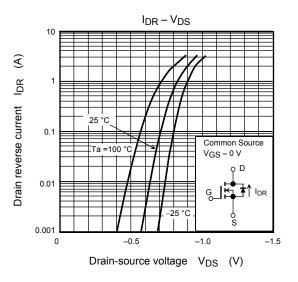


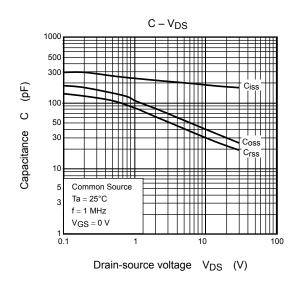


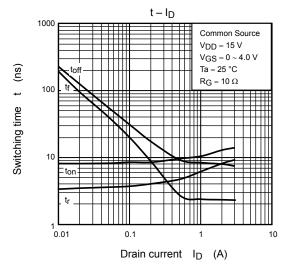


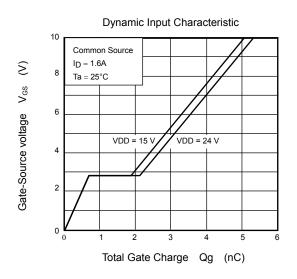
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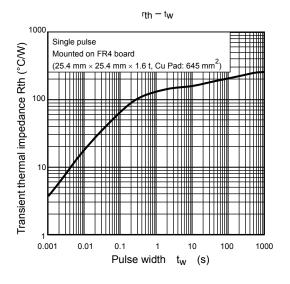


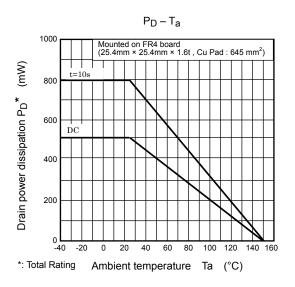






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