14-Bit, 40 MSPS Dual Analog-to-Digital Converter

ADW12001

FEATURES

Integrated dual 14-bit ADC
Single 3 V supply operation: 2.7 V to 3.6 V
Differential input with 500 MHz, 3 dB bandwidth
Flexible analog input: 1 V p-p to 2 V p-p range
Offset binary or twos complement data format
Clock duty cycle stabilizer
Output datamux option

APPLICATIONS

Ultrasound equipment
Direct conversion or IF sampling receivers
WB-CDMA, CDMA2000, WiMAX
Battery-powered instruments
Hand-held scopemeters
Low cost digital oscilloscopes

GENERAL DESCRIPTION

The ADW12001 is a dual, 3 V, 14-bit, 40 MSPS analog-to-digital converter (ADC). It features dual high performance sample-and-hold amplifiers (SHAs) and an integrated voltage reference. The ADW12001 uses a multistage differential pipelined architecture with output error correction logic to provide 14-bit accuracy and to guarantee no missing codes over the full operating temperature. The wide bandwidth differential SHA allows for a variety of user-selectable input ranges and offsets, including single-ended applications. It is suitable for various applications, including multiplexed systems that switch full-scale voltage levels in successive channels and for sampling inputs at frequencies well beyond the Nyquist rate.

Dual single-ended clock inputs are used to control all internal conversion cycles. A duty cycle stabilizer is available and can compensate for wide variations in the clock duty cycle, allowing the converter to maintain excellent performance. The digital output data is presented in either straight binary or twos complement format. Out-of-range signals indicate an overflow condition, which can be used with the most significant bit to determine low or high overflow.

FUNCTIONAL BLOCK DIAGRAM

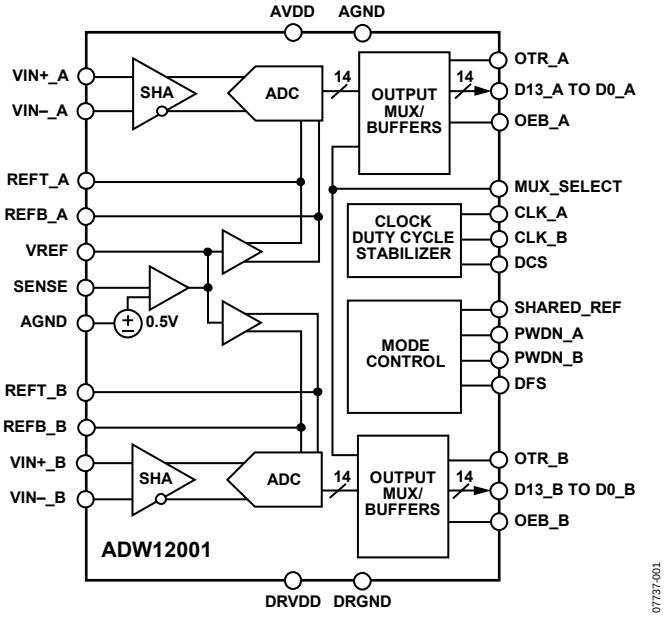

Figure 1.

Fabricated on an advanced CMOS process, the ADW12001 is available in a Pb-free, space saving, 64-lead LFCSP and is specified over the industrial temperature range (−40°C to +115°C).

PRODUCT HIGHLIGHTS

1. Pin compatible with the AD9238, 12-bit 40 MSPS ADC.
2. Low power consumption: 40 MSPS = 330 mW.
3. Typical channel isolation of 85 dB @ f_{IN} = 10 MHz.
4. The clock duty cycle stabilizer maintains performance over a wide range of clock duty cycles.
5. Multiplexed data output option enables single port operation from either Data Port A or Data Port B.

Rev. 0

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REVISION HISTORY

1/09—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, maximum sample rate, CLK_A = CLK_B; A_{IN} = −0.5 dBFS differential input, 1.0 V internal reference, T_{MIN} to T_{MAX}, DCS enabled, unless otherwise noted.

Table 1.

		25°C			115°C			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	14			14			Bits
ACCURACY								
No Missing Codes Guaranteed	Full	14			14			Bits
Offset Error	25°C		±0.2	±1.3		±0.2	±1.3	% FSR
Gain Error[1]	Full		±0.3	±2.4		±0.5	±2.5	% FSR
Differential Nonlinearity (DNL)[2]	Full		±0.65			±0.7		LSB
	25°C		±0.6	±1.0		±0.65	±1.0	LSB
Integral Nonlinearity (INL)[2]	Full		±2.7			±2.8		LSB
	25°C		±2.3	±4.5		±2.4	±4.5	LSB
TEMPERATURE DRIFT								
Offset Error	Full		±2			±2		ppm/°C
Gain Error[1]	Full		±12			±12		ppm/°C
INTERNAL VOLTAGE REFERENCE								
Output Voltage Error (1 V Mode)	Full		±5	±35		±5	±35	mV
Load Regulation @ 1.0 mA	Full		0.8			0.8		mV
Output Voltage Error (0.5 V Mode)	Full		±2.5			±2.5		mV
Load Regulation @ 0.5 mA	Full		0.1			0.1		mV
INPUT REFERRED NOISE								
Input Span = 1 V	25°C		2.1			2.1		LSB rms
Input Span = 2.0 V	25°C		1.05			1.05		LSB rms
ANALOG INPUT								
Input Span = 1.0 V	Full		1			1		V p-p
Input Span = 2.0 V	Full		2			2		V p-p
Input Capacitance[3]	Full		7			7		pF
REFERENCE INPUT RESISTANCE	Full		7			7		kΩ
POWER SUPPLIES								
Supply Voltages								
AVDD	Full	2.7	3.0	3.6	2.7	3.0	3.6	V
DRVDD	Full	2.25	3.0	3.6	2.25	3.0	3.6	V
Supply Current								
IAVDD[2]	Full		110			115		mA
IDRVDD[2]	Full		10			11		mA
PSRR	Full		±0.01			±0.01		% FSR
POWER CONSUMPTION								
DC Input[4]	Full		330			350		mW
Sine Wave Input[2]	Full		360	400		315	412	mW
Standby Power[5]	Full		7.0			7.0		mW

Parameter	Temp	25°C Min	25°C Typ	25°C Max	115°C Min	115°C Typ	115°C Max	Unit
MATCHING CHARACTERISTICS								
Offset Error (Nonshared Reference Mode)	25°C		±0.19	±1.56		±0.25	±1.74	% FSR
Offset Error (Shared Reference Mode)	25°C		±0.19	±1.56		±0.25	±1.74	% FSR
Gain Error (Nonshared Reference Mode)	25°C		±0.07	±1.43		±0.07	±1.47	% FSR
Gain Error (Shared Reference Mode)	25°C		±0.01	±0.06		±0.01	±0.10	% FSR

[1] Gain error and gain temperature coefficients are based on the ADC only (with a fixed 1.0 V external reference).
[2] Measured at the maximum clock rate with a low frequency sine wave input and approximately 5 pF loading on each output bit.
[3] Input capacitance refers to the effective capacitance between one differential input pin and AVSS. Refer to Figure 18 for the equivalent analog input structure.
[4] Measured with dc input at the maximum clock rate.
[5] Standby power is measured with the CLK_A and CLK_B pins inactive (that is, set to AVDD or AGND).

AC SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, maximum sample rate, CLK_A = CLK_B; A_{IN} = −0.5 dBFS differential input, 1.0 V external reference, T_{MIN} to T_{MAX}, DCS enabled, unless otherwise noted.

Table 2.

		25°C			115°C			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)								
f_{IN} = 2.4 MHz	Full							
	25°C	72.8	73.4		70.0	72.5		dB
f_{IN} = 19.6 MHz	Full							
	25°C	72.3	72.9		70.5	71.8		dB
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)								
f_{IN} = 2.4 MHz	Full							dB
	25°C	72.0	73.0		69.5	72.0		dB
f_{IN} = 19.6 MHz	Full							dB
	25°C	71.0	72.3		69.5	71.5		dB
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 2.4 MHz	Full					11.6		Bits
	25°C	11.7	11.8					Bits
WORST HARMONIC (SECOND or THIRD)								
f_{IN} = 2.4 MHz	Full					86.0		dBc
	25°C	77.5	86.0		77			dBc
f_{IN} = 19.6 MHz	Full							dBc
	25°C	76.0	84.0					dBc
						85		dBc
					75			dBc
WORST OTHER SPUR (NONSECOND or THIRD)								
f_{IN} = 2.4 MHz	Full		88.0			84		dBc
	25°C	83.5	89.0					dBc
f_{IN} = 19.6 MHz	Full		88.0			85		dBc
	25°C	82.6	88.5					dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 2.4 MHz	Full		85.0		84	92		dBc
	25°C	77.5	86.0		77.5	86.0		dBc
f_{IN} = 19.6 MHz	Full		83.0		85	90		dBc
	25°C	76.0	84.0					dBc
CROSSTALK	Full		−85.0			−85.0		dB

DIGITAL SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, maximum sample rate, CLK_A = CLK_B; A_{IN} = −0.5 dBFS differential input, 1.0 V internal reference, T_{MIN} to T_{MAX}, DCS enabled, unless otherwise noted.

Table 3.

		25°C/115°C			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Unit**
LOGIC INPUTS					
High Level Input Voltage	Full	2.0			V
Low Level Input Voltage	Full			0.8	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	−10		+10	µA
Input Capacitance	Full		2		pF
LOGIC OUTPUTS[1]					
High Level Output Voltage	Full	DRVDD − 0.05			V
Low Level Output Voltage	Full			0.05	V

[1] Output voltage levels measured with capacitive load only on each output.

SWITCHING SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, maximum sample rate, CLK_A = CLK_B; A_{IN} = −0.5 dBFS differential input, 1.0 V internal reference, T_{MIN} to T_{MAX}, DCS enabled, unless otherwise noted.

Table 4.

Parameter	Temp	Min	Typ	Max	Unit
SWITCHING PERFORMANCE					
Maximum Conversion Rate	Full	40			MSPS
Minimum Conversion Rate	Full			1	MSPS
CLK Period	Full	25.0			ns
CLK Pulse Width High[1]	Full	8.8			ns
CLK Pulse Width Low[1]	Full	8.8			ns
DATA OUTPUT PARAMETER					
Output Delay[2] (t_{PD})	Full	2	3.5	6	ns
Pipeline Delay (Latency)	Full		7		Cycles
Aperture Delay (t_A)	Full		1.0		ns
Aperture Uncertainty (t_J)	Full		0.5		ps rms
Wake-Up Time[3]	Full		2.5		ms
OUT-OF-RANGE RECOVERY TIME	Full		2		Cycles

[1] This model has a duty cycle stabilizer circuit that, when enabled, corrects for a wide range of duty cycles (see Figure 16).
[2] Output delay is measured from clock 50% transition to data 50% transition with a 5 pF load on each output.
[3] Wake-up time is dependent on the value of the decoupling capacitors; typical values shown with 0.1 µF and 10 µF capacitors on REFT and REFB.

Timing Diagram

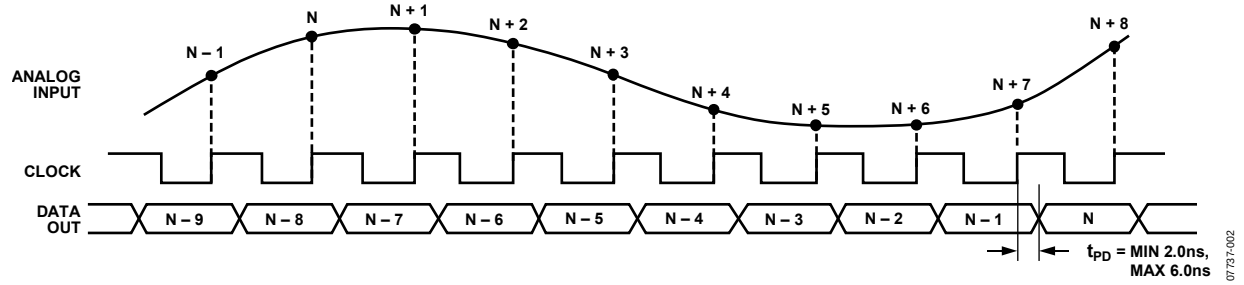


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter[1]	Rating
Electrical	
AVDD to AGND	−0.3 V to +3.9 V
DRVDD to DRGND	−0.3 V to +3.9 V
AGND to DRGND	−0.3 V to +0.3 V
AVDD to DRVDD	−3.9 V to +3.9 V
Digital Outputs CLK_A, CLK_B, DCS, MUX_SELECT, SHARED_REF to DRGND	−0.3 V to DRVDD + 0.3 V
OEB, DFS to AGND	−0.3 V to AVDD + 0.3 V
VIN±_A, VIN±_B to AGND	−0.3 V to AVDD + 0.3 V
VREF to AGND	−0.3 V to AVDD + 0.3 V
SENSE to AGND	−0.3 V to AVDD + 0.3 V
REFB_A, REFB_B, REFT_A, REFT_B to AGND	−0.3 V to AVDD + 0.3 V
PDWN_A, PDWN_B to AGND	−0.3 V to AVDD + 0.3 V
Environmental[2]	
Operating Temperature Range	−45°C to +115 °C
Junction Temperature	150°C
Lead Temperature (10 sec)	300°C
Storage Temperature Range	−65°C to +150°C

[1] Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied.

[2] Typical thermal impedances: 64-lead LFCSP, θ_{JA} = 26.4°C/W with heat slug soldered to the ground plane. These measurements were taken on a 4-layer board in still air, in accordance with EIA/JESD51-7.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
64-Lead LFCSP	26.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

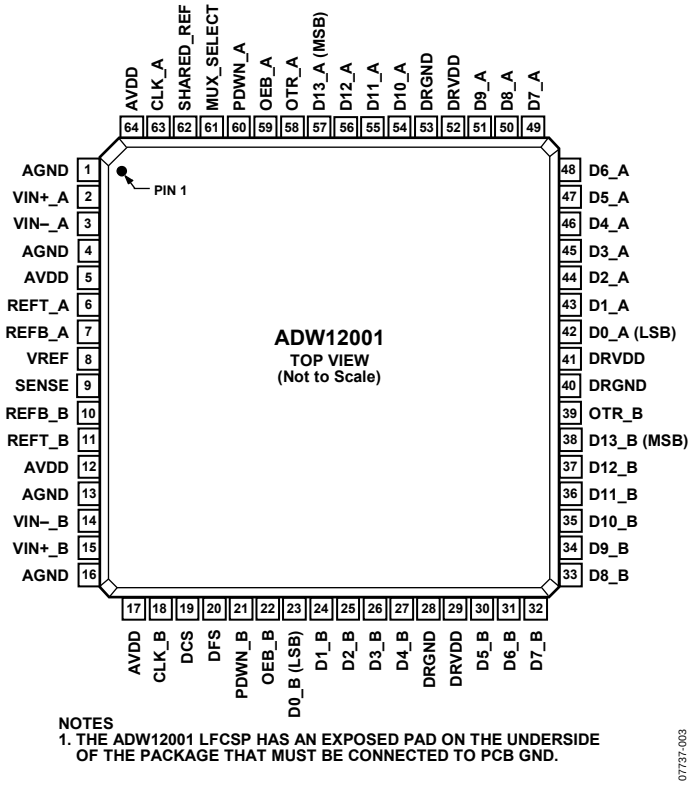


Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 13, 16	AGND	Analog Ground.
2	VIN+_A	Analog Input Pin (+) for Channel A.
3	VIN−_A	Analog Input Pin (−) for Channel A.
5, 12, 17, 64	AVDD	Analog Power Supply.
6	REFT_A	Differential Reference (+) for Channel A.
7	REFB_A	Differential Reference (−) for Channel A.
8	VREF	Voltage Reference Input/Output.
9	SENSE	Reference Mode Selection.
10	REFB_B	Differential Reference (−) for Channel B.
11	REFT_B	Differential Reference (+) for Channel B.
14	VIN−_B	Analog Input Pin (−) for Channel B.
15	VIN+_B	Analog Input Pin (+) for Channel B.
18	CLK_B	Clock Input Pin for Channel B.
19	DCS	Enable Duty Cycle Stabilizer (DCS) Mode.
20	DFS	Data Output Format Select Pin. Low for offset binary, high for twos complement.
21	PDWN_B	Power-Down Function Selection for Channel B. Logic 0 enables Channel B. Logic 1 powers down Channel B (outputs static, not high-Z).
22	OEB_B	Output Enable Pin for Channel B. Logic 0 enables Data Bus B. Logic 1 sets outputs to high-Z.
23 to 27	D0_B (LSB) to D4_B	Channel B Data Output Bits.
30 to 37	D5_B to D12_B	Channel B Data Output Bits.
38	D13_B (MSB)	Channel B Data Output Bits.
28, 40, 53	DRGND	Digital Output Ground.

Pin No.	Mnemonic	Description
29, 41, 52	DRVDD	Digital Output Driver Supply. Must be decoupled to DRGND with a minimum 0.1 µF capacitor. Recommended decoupling is 0.1 µF capacitor in parallel with 10 µF capacitor.
39	OTR_B	Out-of-Range Indicator for Channel B.
42 to 51	D0_A (LSB) to D9_A	Channel A Data Output Bits.
54 to 56	D10_A to D12_A	Channel A Data Output Bits.
57	D13_A (MSB)	Channel A Data Output Bits.
58	OTR_A	Out-of-Range Indicator for Channel A.
59	OEB_A	Output Enable Pin for Channel A. Logic 0 enables Data Bus A. Logic 1 sets outputs to high-Z.
60	PDWN_A	Power-Down Function Selection for Channel A. Logic 0 enables Channel A. Logic 1 powers down Channel A (outputs static, not high-Z).
61	MUX_SELECT	Data Multiplexed Mode. See Data Format section for how to enable; high setting disables output data multiplexed mode.
62	SHARED_REF	Shared Reference Control Pin. Low for independent reference mode, high for shared reference mode.
63	CLK_A	Clock Input Pin for Channel A.
EP		Exposed Pad. This part has an exposed pad on the underside of the package that must be connected to PCB GND.

TERMINOLOGY

Aperture Delay
SHA performance measured from the rising edge of the clock input to when the input signal is held for conversion.

Aperture Jitter
The variation in aperture delay for successive samples, which is manifested as noise on the input to the ADC.

Integral Nonlinearity (INL)
Deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 14-bit resolution indicates that all 16,384 codes must be present over all operating ranges.

Offset Error
The major carry transition should occur for an analog value ½ LSB below VIN+ = VIN−. Offset error is defined as the deviation of the actual transition from that point.

Gain Error
The first code transition should occur at an analog value ½ LSB above negative full scale. The last transition should occur at an analog value 1½ LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Temperature Drift
The temperature drift for zero error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection
The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

Total Harmonic Distortion (THD)
The ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal, expressed as a percentage or in decibels relative to the peak carrier signal (dBc).

Signal-to-Noise and Distortion (SINAD) Ratio
The ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in dB.

Effective Number of Bits (ENOB)
Using the following formula:

$$ENOB = (SINAD - 1.76)/6.02$$

ENOB for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Signal-to-Noise Ratio (SNR)
The ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in dB.

Spurious-Free Dynamic Range (SFDR)
The difference in dB between the rms amplitude of the input signal and the peak spurious signal.

Nyquist Sampling
When the frequency components of the analog input are below the Nyquist frequency ($f_{CLOCK}/2$), this is often referred to as Nyquist sampling.

IF Sampling
Due to the effects of aliasing, an ADC is not limited to Nyquist sampling. Higher sampled frequencies are aliased down into the first Nyquist zone (dc – $f_{CLOCK}/2$) on the output of the ADC. The bandwidth of the sampled signal should not overlap Nyquist zones and alias onto itself. Nyquist sampling performance is limited by the bandwidth of the input SHA and clock jitter (jitter adds more noise at higher input frequencies).

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product.

Out-of-Range Recovery Time
The time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale or from 10% below negative full scale to 10% below positive full scale.

Crosstalk
Coupling onto one channel being driven by a (−0.5 dBFS) signal when the adjacent interfering channel is driven by a full-scale signal. Measurement includes all spurs resulting from both direct coupling and mixing components.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD, DRVDD = 3.0 V, T = 25°C, A_{IN} differential drive, full scale = 2 V, unless otherwise noted.

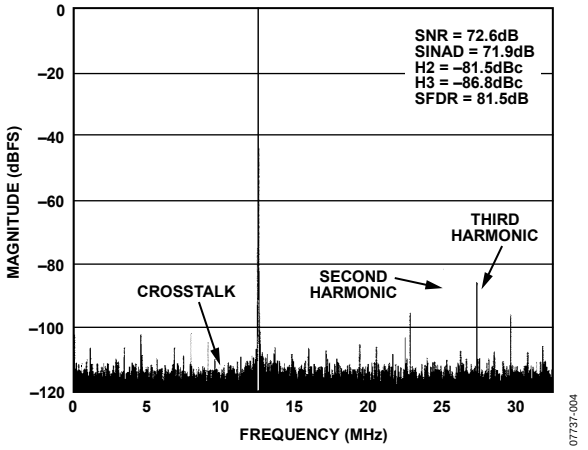


Figure 4. Single-Tone FFT of Channel A Digitizing f_{IN} = 12.5 MHz While Channel B Is Digitizing f_{IN} = 10 MHz

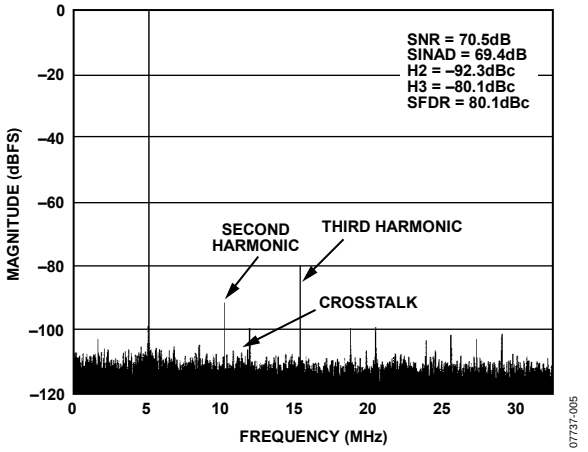


Figure 5. Single-Tone FFT of Channel A Digitizing f_{IN} = 70 MHz While Channel B Is Digitizing f_{IN} = 76 MHz

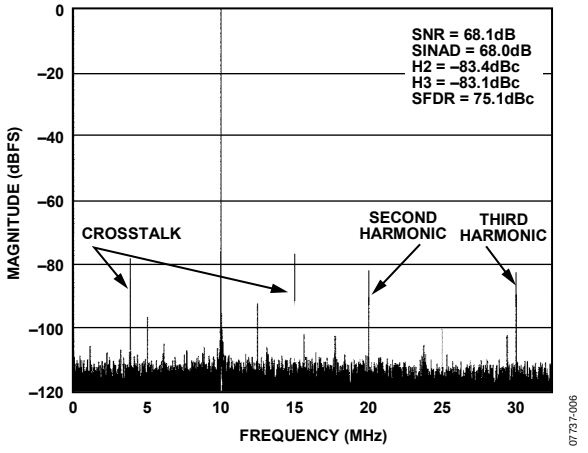


Figure 6. Single-Tone FFT of Channel A Digitizing f_{IN} = 120 MHz While Channel B Is Digitizing f_{IN} = 126 MHz

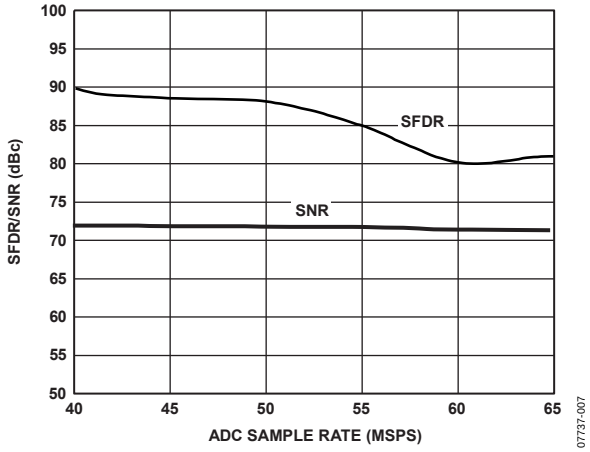


Figure 7. Single-Tone SFDR/SNR vs. FS with f_{IN} = 20 MHz

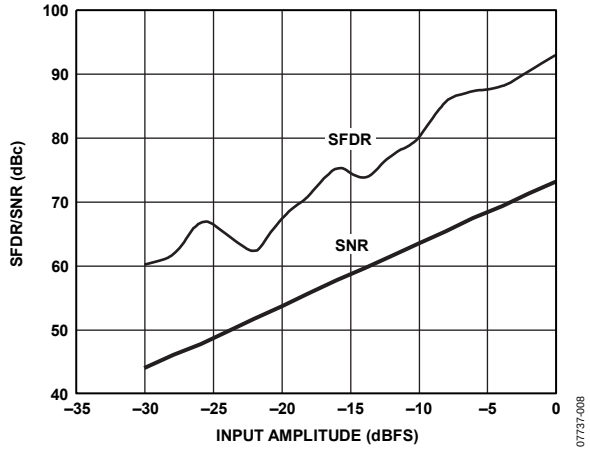


Figure 8. Single-Tone SFDR/SNR vs. A_{IN} with f_{IN} = 20 MHz

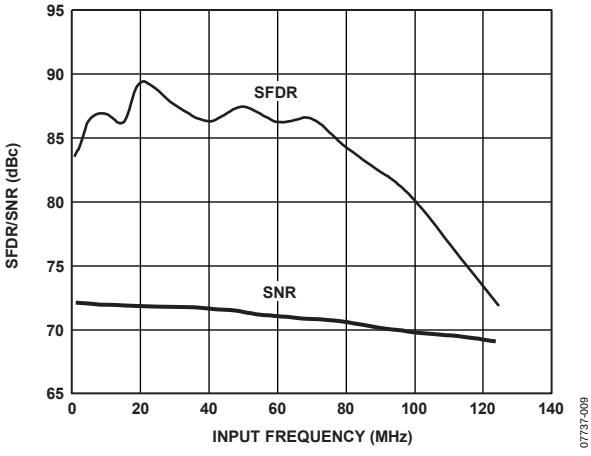


Figure 9. Single-Tone SFDR/SNR vs. f_{IN}

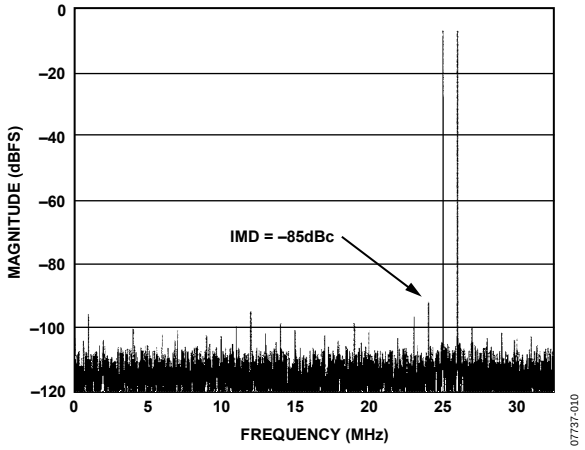


Figure 10. Dual-Tone FFT with f_{IN1} = 39 MHz and f_{IN2} = 40 MHz

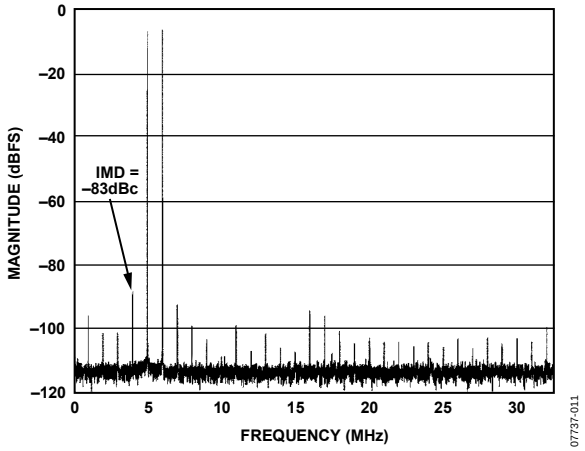


Figure 11. Dual-Tone FFT with f_{IN1} = 70 MHz and f_{IN2} = 71 MHz

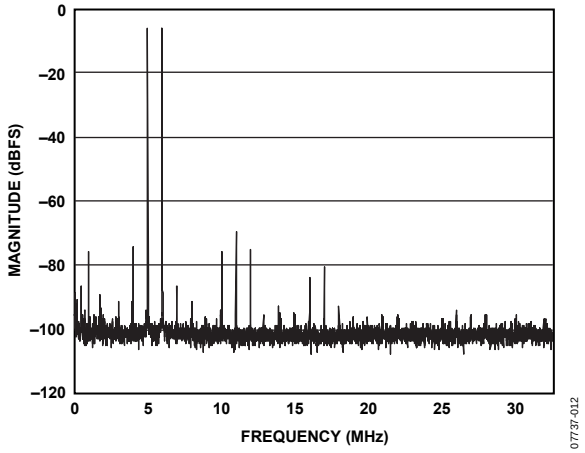


Figure 12. Dual-Tone FFT with f_{IN1} = 200 MHz and f_{IN2} = 201 MHz

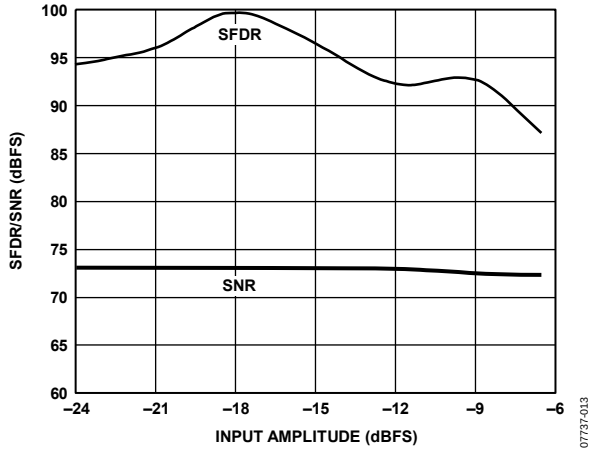


Figure 13. Dual-Tone SFDR/SNR vs. A_{IN} with f_{IN1} = 45 MHz and f_{IN2} = 46 MHz

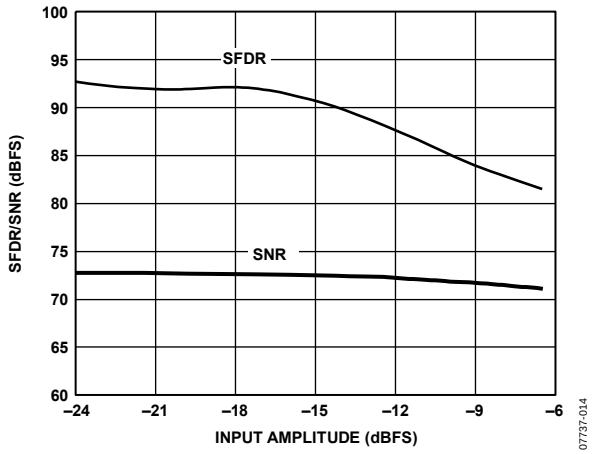


Figure 14. Dual-Tone SFDR/SNR vs. A_{IN} with f_{IN1} = 70 MHz and f_{IN2} = 71 MHz

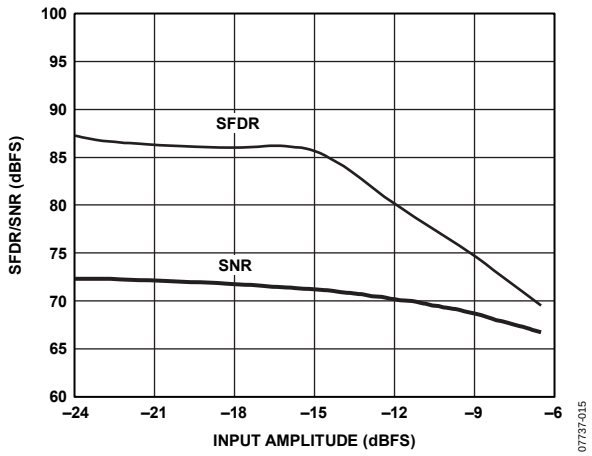


Figure 15. Dual-Tone SFDR/SNR vs. A_{IN} with f_{IN1} = 200 MHz and f_{IN2} = 201 MHz

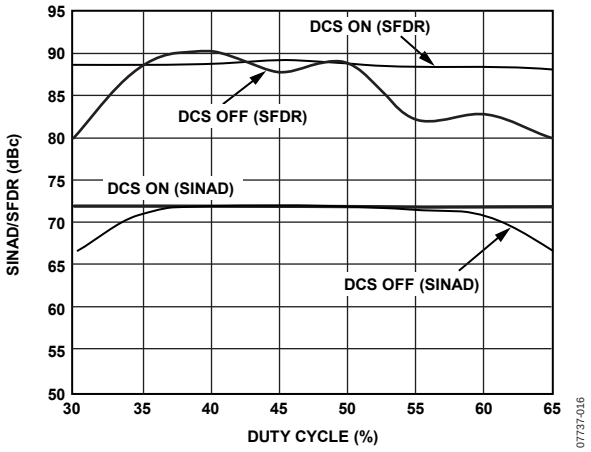


Figure 16. SINAD/SFDR vs. Clock Duty Cycle

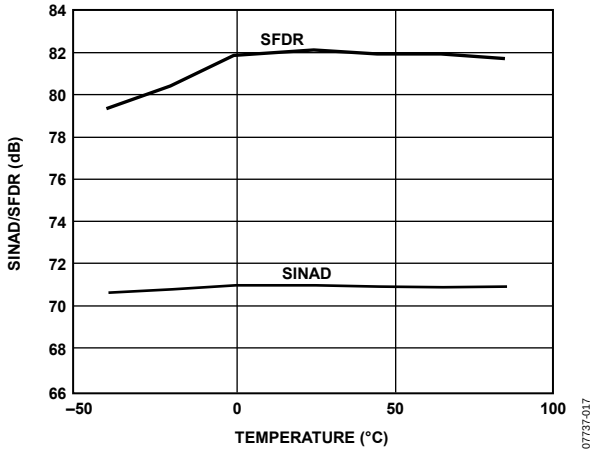


Figure 17. SINAD/SFDR vs. Temperature with f_{IN} = 32.5 MHz

EQUIVALENT CIRCUITS

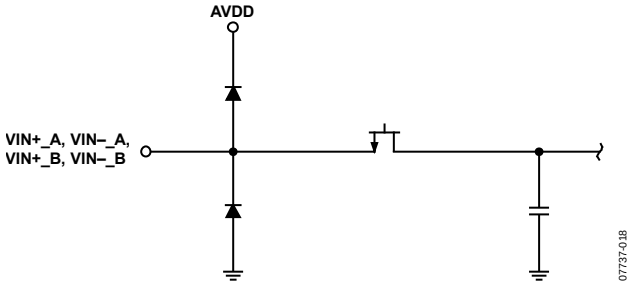


Figure 18. Equivalent Analog Input Circuit

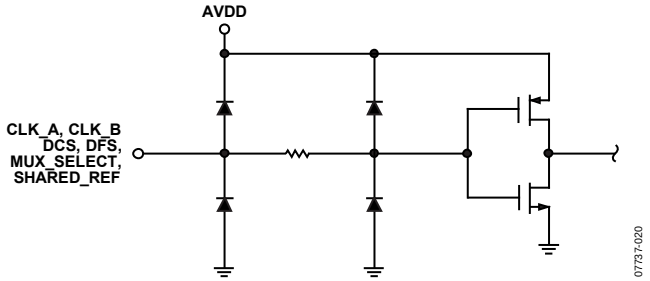


Figure 20. Equivalent Digital Input Circuit

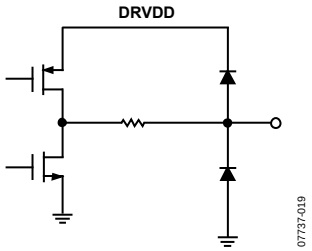


Figure 19. Equivalent Digital Output Circuit

THEORY OF OPERATION

The ADW12001 consists of two high performance ADCs that are based on the AD9235 converter core. The dual ADC paths are independent, except for a shared internal band gap reference source, VREF. Each of the ADC paths consists of a proprietary front-end SHA followed by a pipelined switched capacitor ADC. The pipelined ADC is divided into three sections, consisting of a 4-bit first stage, followed by eight 1.5-bit stages, and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined through the digital correction logic block into a final 12-bit result. The pipelined architecture permits the first stage to operate on a new input sample, whereas the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the respective clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC and a residual multiplier to drive the next stage of the pipeline. The residual multiplier uses the flash ADC output to control a switched capacitor digital-to-analog converter (DAC) of the same resolution. The DAC output is subtracted from the input signal of the stage, and the residual is amplified (multiplied) to drive the next pipeline stage. The residual multiplier stage is also called a multiplying DAC (MDAC). One bit of redundancy is used in each one of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be configured as ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing.

ANALOG INPUT

The analog input to the ADW12001 is a differential switched capacitor SHA designed for optimum performance while processing a differential input signal. The SHA input accepts inputs over a wide common-mode range. An input common-mode voltage of midsupply is recommended to maintain optimal performance.

The SHA input is a differential switched capacitor circuit. In Figure 21, the clock signal alternatively switches the SHA between sample mode and hold mode. When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. Also, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application. In IF under sampling applications, any shunt capacitors should be removed. In combination with the driving source impedance, they limit the input bandwidth. For the best dynamic performance, match the source impedances driving VIN+ and VIN− such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC.

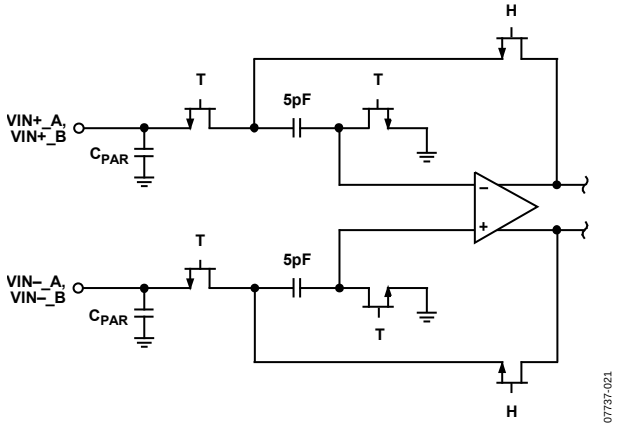


Figure 21. Switched Capacitor Input

An internal differential reference buffer creates positive and negative reference voltages, REFT and REFB, respectively, that define the span of the ADC core. The output common mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as:

$$REFT = ½(AVDD + V_{REF})$$

$$REFB = ½(AVDD + V_{REF})$$

$$Span = 2 \times (REFT - REFB) = 2 \times V_{REF}$$

These equations show that the REFT and REFB voltages are symmetrical around the midsupply voltage and, by definition, the input span is twice the value of the V_{REF} voltage.

The internal voltage reference can be pin-strapped to fixed values of 0.5 V or 1.0 V or adjusted within the same range as discussed in the Internal Reference Connection section. Maximum SNR performance is achieved with the ADW12001 set to the largest input span of 2 V p-p. The relative SNR degradation is 3 dB when changing from 2 V p-p mode to 1 V p-p mode.

The SHA may be driven from a source that keeps the signal peaks within the allowable range for the selected reference voltage. The minimum and maximum common-mode input levels are defined as

$$VCM_{MIN} = V_{REF}/2$$

$$VCM_{MAX} = (AVDD + V_{REF})/2$$

The minimum common-mode input level allows the ADW12001 to accommodate ground referenced inputs. Although optimum performance is achieved with a differential input, a single-ended source may be driven into VIN+ or VIN−. In this configuration, one input accepts the signal, while the opposite input is set to midscale by connecting it to an appropriate reference. For

example, a 2 V p-p signal may be applied to VIN+, while a 1 V reference is applied to VIN–. The ADW12001 then accepts an input signal varying between 2 V and 0 V. In the single-ended configuration, distortion performance may degrade significantly as compared to the differential case. However, the effect is less noticeable at lower input frequencies.

Differential Input Configurations

Optimum performance is achieved while driving the ADW12001 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8138 is easily set to AVDD/2, and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

At input frequencies in the second Nyquist zone and above, the performance of most amplifiers is not adequate to achieve the true performance of the ADW12001. This is especially true in IF under sampling applications where frequencies in the 70 MHz to 200 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration, as shown in Figure 22.

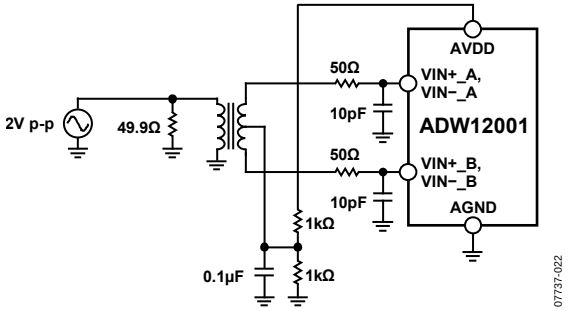


Figure 22. Differential Transformer Coupling

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz, and excessive signal power can also cause core saturation, which leads to distortion.

Single-Ended Input Configuration

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration, there is a degradation in SFDR and distortion performance due to the large input common-mode swing. However, if the source impedances on each input are matched, there should be little effect on SNR performance.

CLOCK INPUT AND CONSIDERATIONS

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The ADW12001 provides separate clock inputs for each channel. The optimum performance is achieved with the clocks operating at the same frequency and phase. Clocking the channels asynchronously may degrade performance significantly. In some applications, it is desirable to skew the clock timing of adjacent channels. The separate clock inputs of the ADW12001 allow for clock timing skew (typically ±1 ns) between the channels without significant performance degradation.

The ADW12001 contains two clock duty cycle stabilizers, one for each converter, that retime the nonsampling edge, providing an internal clock with a nominal 50% duty cycle. When proper track-and-hold times for the converter are required to maintain high performance, maintaining a 50% duty cycle clock is particularly important in high speed applications. It may be difficult to maintain a tightly controlled duty cycle on the input clock on the PCB (see Figure 16). DCS can be enabled by tying the DCS pin high.

The duty cycle stabilizer uses a delay-locked loop to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately 2 µs to 3 µs to allow the DLL to acquire and settle to the new rate.

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{IN}) due only to aperture jitter (t_J) can be calculated as

$$SNR = 20 \times \log\left[\frac{1}{\left(2 \times \pi \times f_{IN} \times t_j\right)}\right]$$

In the equation, the rms aperture jitter, t_J, represents the root-sum square of all jitter sources, which includes the clock input, analog input signal, and ADC aperture jitter specification. Under sampling applications are particularly sensitive to jitter.

For optimal performance, especially in cases where aperture jitter may affect the dynamic range of the ADW12001, it is important to minimize input clock jitter. The clock input circuitry should use stable references; for example, use analog power and ground planes to generate the valid high and low digital levels for the ADW12001 clock input. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

POWER DISSIPATION AND STANDBY MODE

The power dissipated by the ADW12001 is proportional to its sampling rates. The digital (DRVDD) power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit. The digital drive current can be calculated by

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLOCK} \times N$$

where N is the number of bits changing and C_{LOAD} is the average load on the digital pins that changed.

The analog circuitry is optimally biased so that each speed grade provides excellent performance while affording reduced power consumption. Each speed grade dissipates a baseline power at low sample rates that increases with clock frequency.

Either channel of the ADW12001 can be placed into standby mode independently by asserting the PDWN_A or PDWN_B pins.

It is recommended that the input clock(s) and analog input(s) remain static during either independent or total standby, which results in a typical power consumption of 1 mW for the ADC. Note that if DCS is enabled, it is mandatory to disable the clock of an independently powered-down channel. Otherwise, significant distortion results on the active channel. If the clock inputs remain active while in total standby mode, typical power dissipation of 12 mW results.

The minimum standby power is achieved when both channels are placed into full power-down mode (PDWN_A = PDWN_B = high). Under this condition, the internal references are powered down. When either or both of the channel paths are enabled after a power-down, the wake-up time is directly related to the recharging of the REFT and REFB decoupling capacitors and to the duration of the power-down. Typically, it takes approximately 5 ms to restore full operation with fully discharged 0.1 µF and 10 µF decoupling capacitors on REFT and REFB.

A single channel can be powered down for moderate power savings. The powered-down channel shuts down internal circuits, but both the reference buffers and shared reference remain powered on. Because the buffer and voltage reference remain powered on, the wake-up time is reduced to several clock cycles.

DIGITAL OUTPUTS

The ADW12001 output drivers can be configured to interface with 2.5 V or 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies that may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fanouts may require external buffers or latches.

The data format can be selected for either offset binary or twos complement. See the Data Format section for more information.

TIMING

The ADW12001 provides latched data outputs with a pipeline delay of seven clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal. Refer to Figure 2 for a detailed timing diagram.

The internal duty cycle stabilizer can be enabled on the ADW12001 using the DCS pin. This provides a stable 50% duty cycle to internal circuits.

Minimize the length of the output data lines and the loads placed on them to reduce transients within the ADW12001. These transients can detract from the dynamic performance of the converter. The lowest typical conversion rate of the ADW12001 is 1 MSPS. At clock rates below 1 MSPS, dynamic performance may degrade.

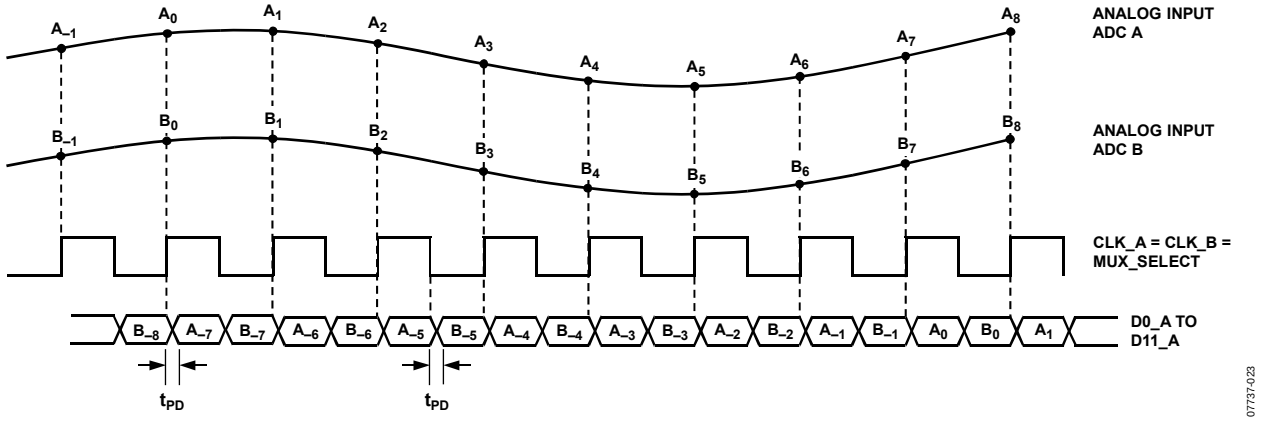


Figure 23. Multiplexed Data Format Using the Channel A Output and the Same Clock Tied to CLK_A, CLK_B, and MUX_SELECT

DATA FORMAT

The ADW12001 data output format can be configured for either twos complement or offset binary. This is controlled by the data format select pin (DFS). Connecting DFS to AGND produces offset binary output data. Conversely, connecting DFS to AVDD formats the output data as twos complement.

The output data from the dual ADCs can be multiplexed onto a single 14-bit output bus. The multiplexing is accomplished by toggling the MUX_SELECT bit, which directs channel data to the same or opposite channel data port. When MUX_SELECT is logic high, the Channel A data is directed to the Channel A output bus, and the Channel B data is directed to the Channel B output bus. When MUX_SELECT is logic low, the channel data is reversed, that is, the Channel A data is directed to the Channel B output bus, and the Channel B data is directed to the Channel A output bus. By toggling the MUX_SELECT bit, multiplexed data is available on either of the output data ports.

If the ADCs run with synchronized timing, this same clock can be applied to the MUX_SELECT pin. Any skew between CLK_A, CLK_B, and MUX_SELECT can degrade ac performance. It is recommended to keep the clock skew <100 ps. After the MUX_SELECT rising edge, either data port has the data for its respective channel; after the falling edge, the data of the alternate channel is placed on the bus. Typically, the other unused bus is disabled by setting the appropriate OEB higher to reduce power consumption and noise. Figure 23 shows an example of multiplex mode. When multiplexing data, the data rate is two times the sample rate. Note that both channels must remain active in this mode and that each power-down pin of the channel must remain low.

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the ADW12001. The input range can be adjusted by varying the reference voltage applied to the ADW12001, using either the internal reference with different external resistor configurations or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly. If the ADC is being driven differentially through a transformer, the reference voltage can be used to bias the center tap (common-mode voltage).

The shared reference mode allows the user to connect the references from the dual ADCs together externally for superior gain and offset matching performance. If the ADCs are to function independently, the reference decoupling can be treated independently and can provide superior isolation between the dual channels. To enable shared reference mode, the SHARED_REF pin must be tied high and the external differential references must be externally shorted. (REFT_A must be externally shorted to REFT_B, and REFB_A must be shorted to REFB_B.)

Internal Reference Connection

A comparator within the ADW12001 detects the potential at the SENSE pin and configures the reference into four possible states, which are summarized in Table 8. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 24), setting VREF to 1 V. Connecting the SENSE pin to VREF switches the reference amplifier output to the SENSE pin, completing the loop and providing a 0.5 V reference output. If a resistor divider is connected, as shown in Figure 25, the switch is again set to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output defined as

$$V_{REF} = 0.5 \times (1 + R2/R1)$$

In all reference configurations, REFT and REFB drive the ADC core and establish its input span. The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

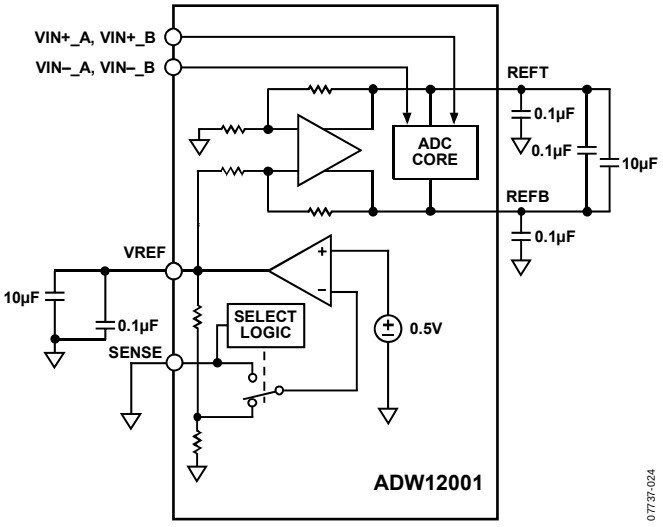


Figure 24. Internal Reference Configuration

Table 8. Reference Configuration Summary

Selected Mode	SENSE Voltage	Resulting V_{REF} (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A[1]	2 × External Reference
Internal Fixed Reference	V_{REF}	0.5	1.0
Programmable Reference	0.2 V to V_{REF}	0.5 × (1 + R2/R1)	2 × V_{REF} (See Figure 25)
Internal Fixed Reference	AGND to 0.2 V	1.0	2.0

[1] N/A means not applicable.

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or to improve thermal drift characteristics. When multiple ADCs track one another, a single reference (internal or external) may be necessary to reduce gain matching errors to an acceptable level. A high precision external reference may also be selected to provide lower gain and offset temperature drift. Figure 26 shows the typical drift characteristics of the internal reference in both 1 V and 0.5 V modes. When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7 kΩ load. The internal buffer still generates the positive and negative full-scale references, REFT and REFB, for the ADC core. The input span is always twice the value of the reference voltage; therefore, the external reference must be limited to a maximum of 1 V. If the internal reference of the ADW12001 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 27 depicts how the internal reference voltage is affected by loading.

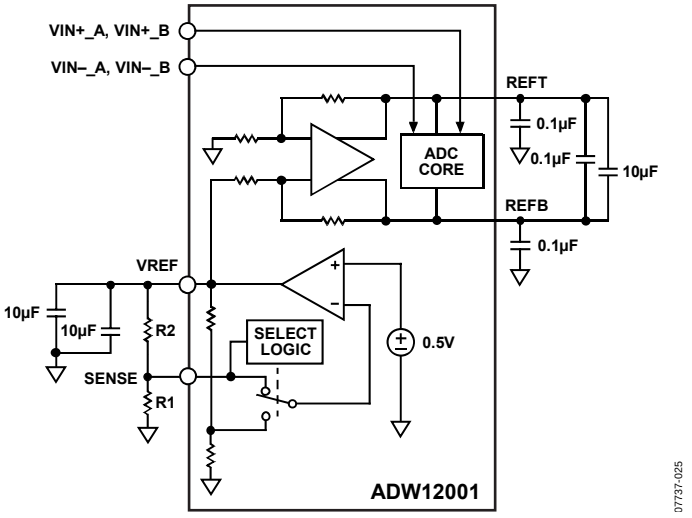


Figure 25. Programmable Reference Configuration

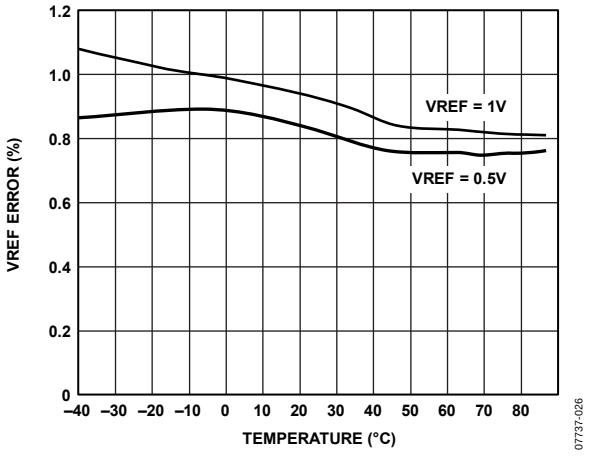


Figure 26. Typical VREF Drift

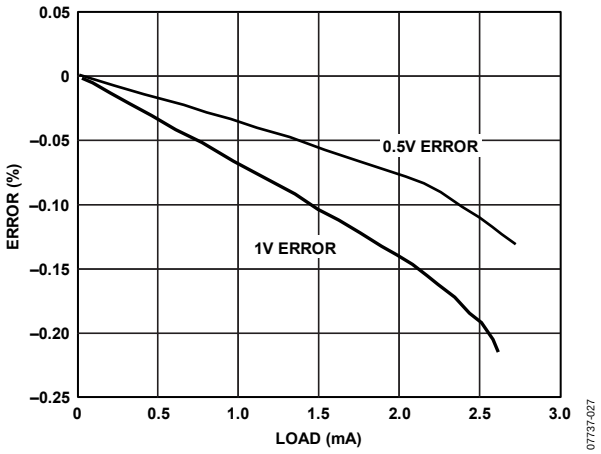


Figure 27. VREF Accuracy vs. Load

THERMAL CONSIDERATIONS

The ADW12001 LFCSP has an integrated heat slug that improves the thermal and electrical properties of the package when locally attached to a ground plane at the PCB. A thermal (filled) via array to a ground plane beneath the part provides a path for heat to escape the package, lowering junction temperature. Improved electrical performance also results from the reduction in package parasitics due to proximity of the ground plane. The recommended array consists of 0.3 mm vias on a 1.2 mm pitch. θ_{JA} = 26.4°C/W with this recommended configuration. Soldering the slug to the PCB is a requirement for this package.

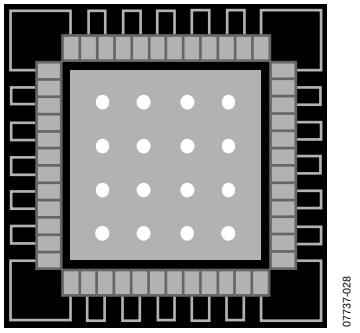
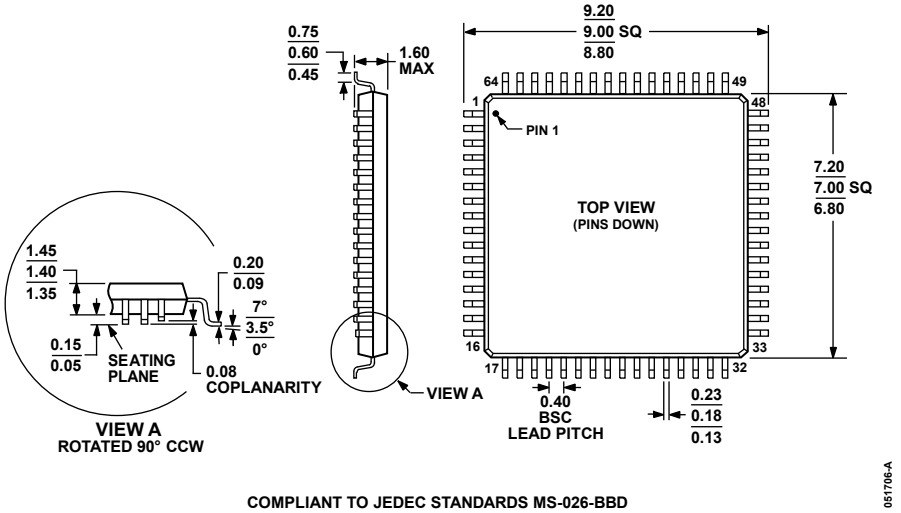


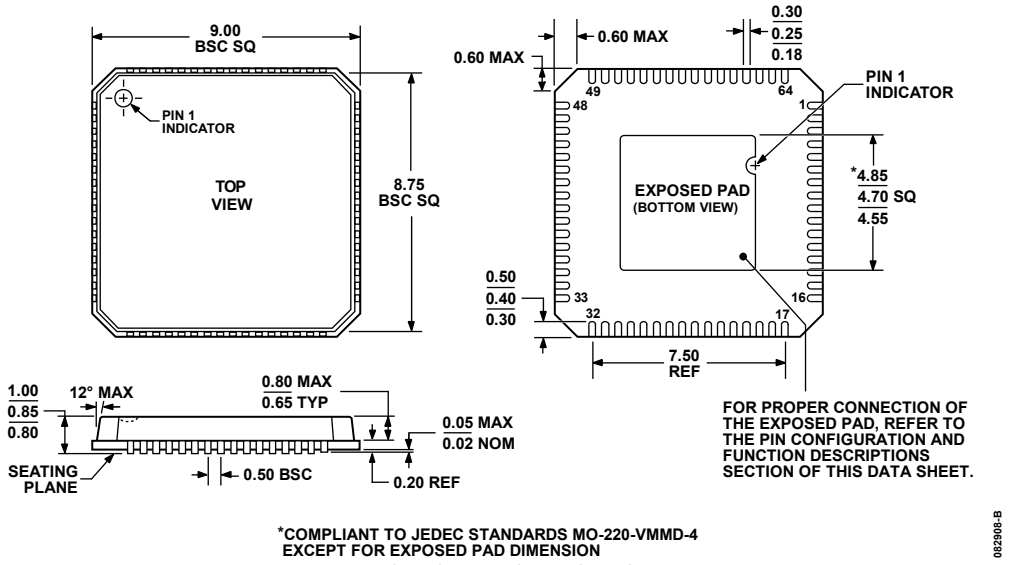
Figure 28. Thermal Via Array

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BBD

Figure 29. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-1)
Dimensions shown in millimeters (mm)



*COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4
EXCEPT FOR EXPOSED PAD DIMENSION

Figure 30. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-1)
Dimensions shown in millimeters (mm)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADW12001BCPZ-40[1]	−40°C to +115°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-1
ADW12001BCPZRL-40[1]	−40°C to +115°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-1
ADW12001BSTZ-40[1]	−40°C to +115°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-1
ADW12001BSTZRL-40[1]	−40°C to +115°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-1

[1] Z = RoHS Compliant Part.

NOTES

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NOTES

D07737-0-1/09(0)

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Analog Devices Inc.:

AD9248BCPZ-65 AD9248BCPZRL-65 AD9248BSTZ-20 AD9248BCPZ-20 AD9248BSTZ-40 AD9248BSTZ-65 AD9248BCPZ-40 AD9248BCPZRL-40