Reference design guide

Automotive front light LED reference design with SEPIC topology

Design overview

This Infineon reference design guide describes a detailed implementation of an automotive front light high beam/low beam combination using the flexible multi-topology DC-DC controller TLD5099EP of the LITIX™ Power family in current controlled buck-boost SEPIC configuration. One single DC-DC channel is used to drive the high beam and low beam. The high beam can be activated in conjunction with the low beam or the low beam can be activated standalone. This represents a cost saving approach especially suitable for entry level LED headlamps. A PWM dimming feature enables furthermore control of brightness and enables derating in extreme operating conditions. State of the art diagnosis is provided as well as transient robustness. Compliant EMC performance is verified according to the CISPR25 standard. Thermal performance information is given and discussed.

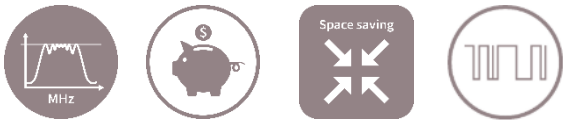
Highlighted components

- TLD5099EP Multi-topology DC-DC controller from the LITIX™ Power family
- IPD60N10S4L OptiMOS™ -T2 as power stage switching MOSFET
- IPD50P04P4L-11 OptiMOS™ -P2 as reverse battery protection MOSFET

Applications

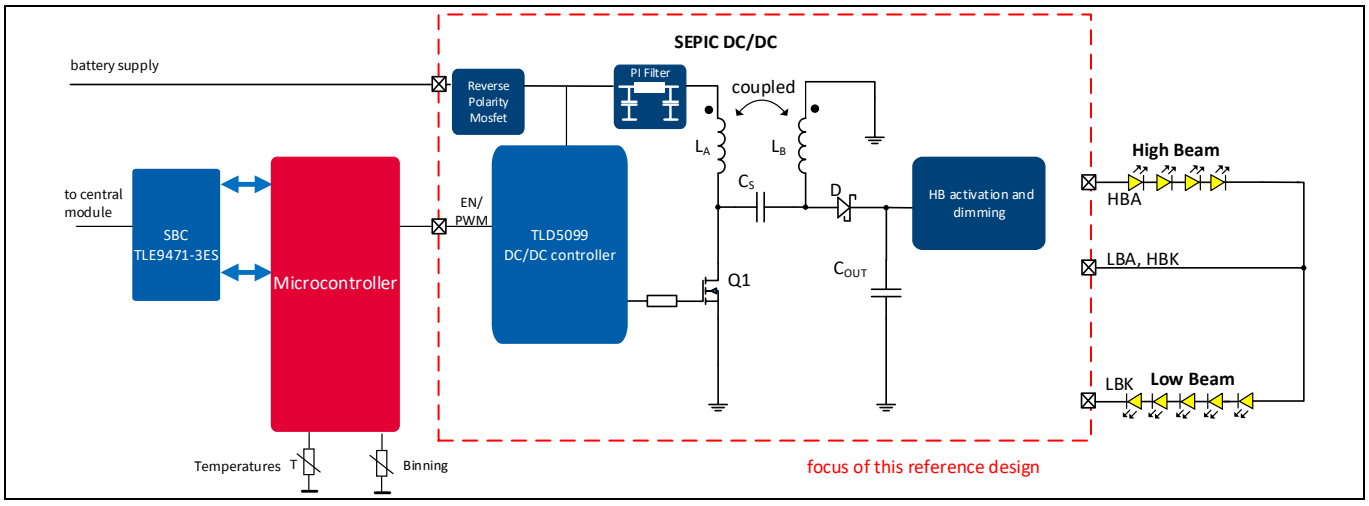
- Automotive front light
- High beam, low beam
- Daytime running light, turn indicator
- Motorcycle headlamp

Highlighted design aspects



EMC tested | Cost optimized | Space saving | Transient pulse tested

Block diagram



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1 System description

This reference design describes a solution for the illumination light functions of an automotive LED headlamp with 25 W to 30 W (depending on the cooling effort) output power. It is considered that this design can be scaled to the needs of a motorcycle headlamp where the output power is typically lower than 25 W to 30 W. For front light LED designs neither the number of LEDs per light function nor the current per LED is standardized but typically the required output power is higher than for exterior rear lighting. Typically, DC-DCs are used as drivers for front light systems to keep the power losses within an acceptable range and to allow the output voltage to be higher than the battery supply. The TLD5099EP design, being a DC-DC boost controller that supports boost and buck-boost topologies was used for this design.

Traditional car headlamp LED designs for high-beam + low-beam consider a maximum power higher than 30 W, however, today this feature is unnecessary to fulfill the requirements for the light output of an LED headlamp. The key is to use highly efficient automotive LEDs with sufficient cooling that enables front light designs with a reduced number of LEDs.

State of the art LEDs that are available on the market today offer highly luminous flux values with >100 lm/W under real application conditions.

Two examples for LEDs for HB/LB are: Nichia NCSW170D and OSRAM Black Flat S where a typical luminous flux of >300 lm at I_F=1000 mA is expected. Using highly efficient LEDs in combination with a direct topology DC-DC such as TLD5099EP a compact design with few external components and low power losses can be achieved. In the following sections the system design for TLD5099EP with coupled coil and a shorting switch for high-beam and low-beam is described. A heatsink (metal ECU) that would significantly improve the heat conduction was not considered as this is specific for each ECU design and all measurements were done with 5 LEDs for low beam and 4 LEDs for high beam.

1.1 Design specifications

Table 1 Design specifications

Parameter	Symbol	Values			Unit	Comment
		Min.	Typ.	Max.		
System parameters						
Input voltage	V_{IN}	8	13.5	16	V	
Transient input voltage	$V_{IN,Tran}$	4.5		35	V	Min. value due to cranking, max. value due to load dump
LED forward voltage	$V_{F,LED}$	2.75	3	3.4	V	LED: OSRAM OSLON® Compact PL KW CELNM1.TG
LED forward voltage of binning class	$V_{F,LED,BIN}$	2.75		3.00	V	LED forward voltage of specific binning class (15)
Output voltage	V_{OUT}	5 x $V_{F,LED,BIN,min}$ = 13.75 V		9 x $V_{F,LED,BIN,max}$ = 27 V	V	LB active: 5 x LED LB and HB active: 9 x LED
LED current	I_{LED}		900		mA	Regulated
LED current ripple	ΔI_{LED}			200	mA	Peak to peak current ripple in LED string
Reverse input voltage	V_{RP}			-14	V	Input voltage in reverse polarity situation
Switching frequency	f_{SW}		310		kHz	Switching frequency of the SEPIC power stage
Dimming frequency	f_{DIM}		500		Hz	PWM dimming frequency

System description

Parameter	Symbol	Values			Unit	Comment
		Min.	Typ.	Max.		
Thermal						
Operating temperature	T_A	-40	25	105	°C	Derating needs to be applied
Transient immunity						
Jumpstart				Functional class A		
Load dump				Functional class A		
Start pulses				Functional class B/C		Cold and hot pulses
Reverse polarity				Functional class C		
Electromagnetic compatibility						
Conducted emissions				Class V to Class III		CISPR25, 150 kHz - 108 MHz
Radiated emissions				Class V		CISPR25, 30 MHz - 1 GHz

2 System design

The system design follows the design specifications and can be divided in four main subsystem which are:

- TLD5099EP multi-topology DC-DC controller
- SEPIC power stage and input filter
- HB activation, PWM dimming and output filter
- Reverse polarity and input protection

The PCB with the TLD5099EP is depicted in Figure 1 and a simplified block diagram of the overall system is depicted in Figure 2. A reverse polarity and input protection circuit ensures that no destructive events occur during transient disturbances along the supply line and in a reverse polarity situation. The TLD5099EP multi-topology DC-DC controller drives and monitors the SEPIC power stage. The power stage provides the output power to the LED strings and is configured for current control mode. To provide EMC compliance according to CISPR25 for conducted and radiated emissions a PI-filter is placed at the input and a common mode choke is placed at the output. The HB activation circuit provides the possibility to drive only the LB or a combination of LB and HB. Furthermore, PWM dimming is also implemented to regulate the intensity of the LED string and to achieve a derating strategy under extreme operating conditions.

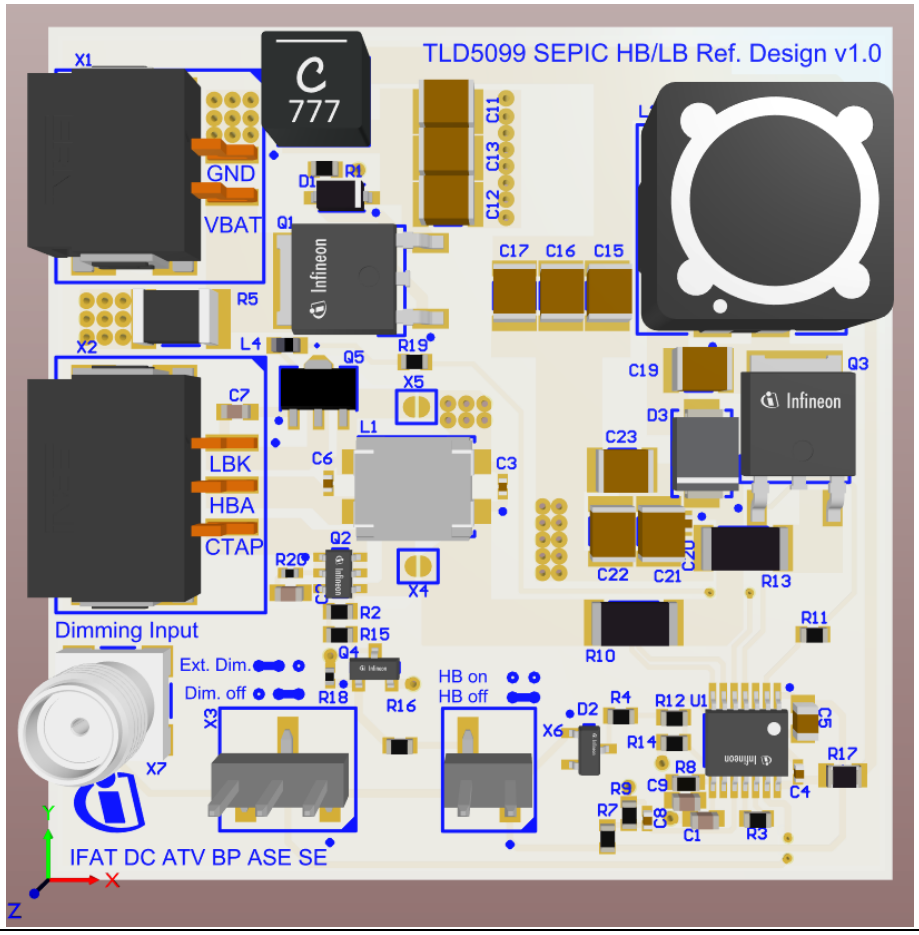


Figure 1 TLD5099EP SEPIC HB/LB reference design PCB

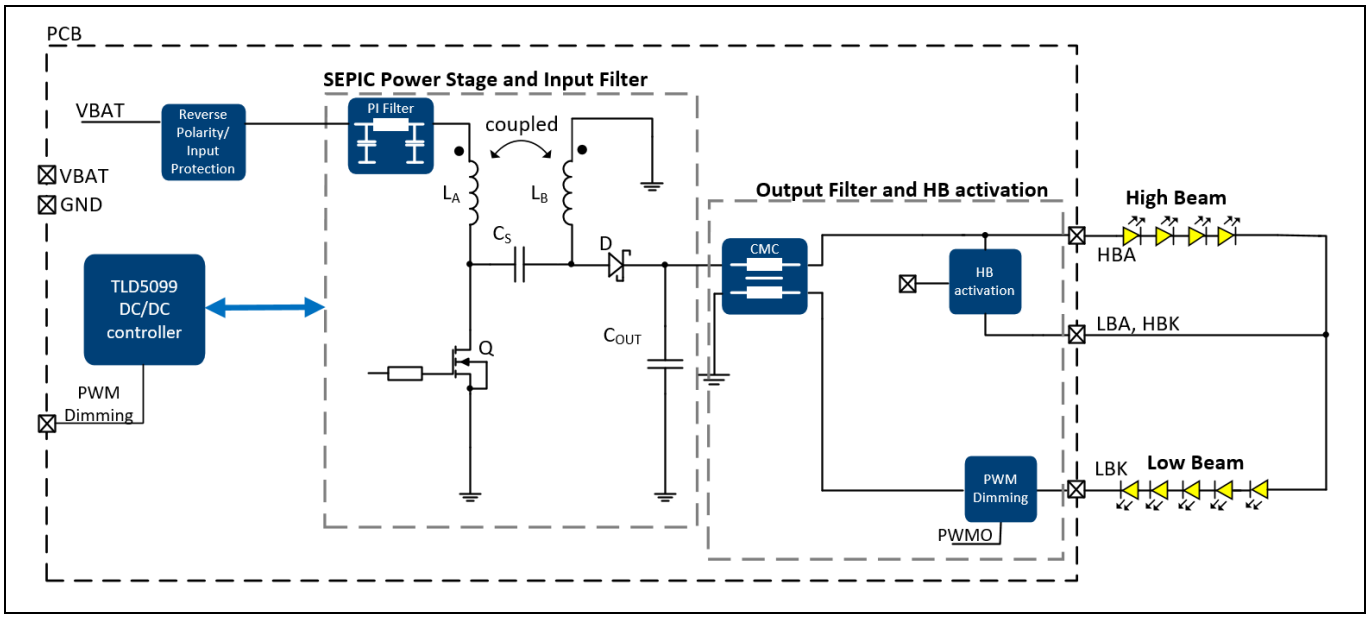


Figure 2 TLD5099EP SEPIC HB/LB reference design block diagram

2.1 TLD5099EP constant current controller

The TLD5099EP is an automotive qualified multi-topology DC-DC controller with built in diagnosis and protection features. The controller IC operates in an asynchronous topology, driving a low side n-channel power MOSFET from an internal 5 V linear regulator. In order to configure the power stage switching frequency, either the implemented oscillator with spread spectrum modulator, or an external clock source can be used. Below Table 2 summarizes the key product parameters.

Table 2 TLD5099EP main parameters

Parameter	Symbol	Range
Nominal supply voltage range	V_{IN}	8 V to 34 V
Extended supply voltage range	V_{IN}	4.5 V to 45 V
Switching frequency range	f_{FREQ}	100 kHz to 500 kHz oscillator frequency adjustment range 250 kHz to 500 kHz synchronization frequency capture range
Maximum duty cycle	$D_{max,fixed}$	91% fixed frequency mode
	$D_{max,sync}$	88% synchronization mode
Gate driver peak sourcing current	$I_{SWO,SRC}$	380 mA (typical)
Gate driver peak sinking current	$I_{SWO,SNK}$	550 mA (typical)

In the following section, the functions of the TLD5099EP will be explained briefly, in order to give guidance for proper partitioning. Figure 3 shows a block diagram of the TLD5099EP and Figure 4 shows the controller IC with its external circuitry. Before defining the SEPIC power stage, the protection features and configuration possibilities of the device will be discussed in the following sections.

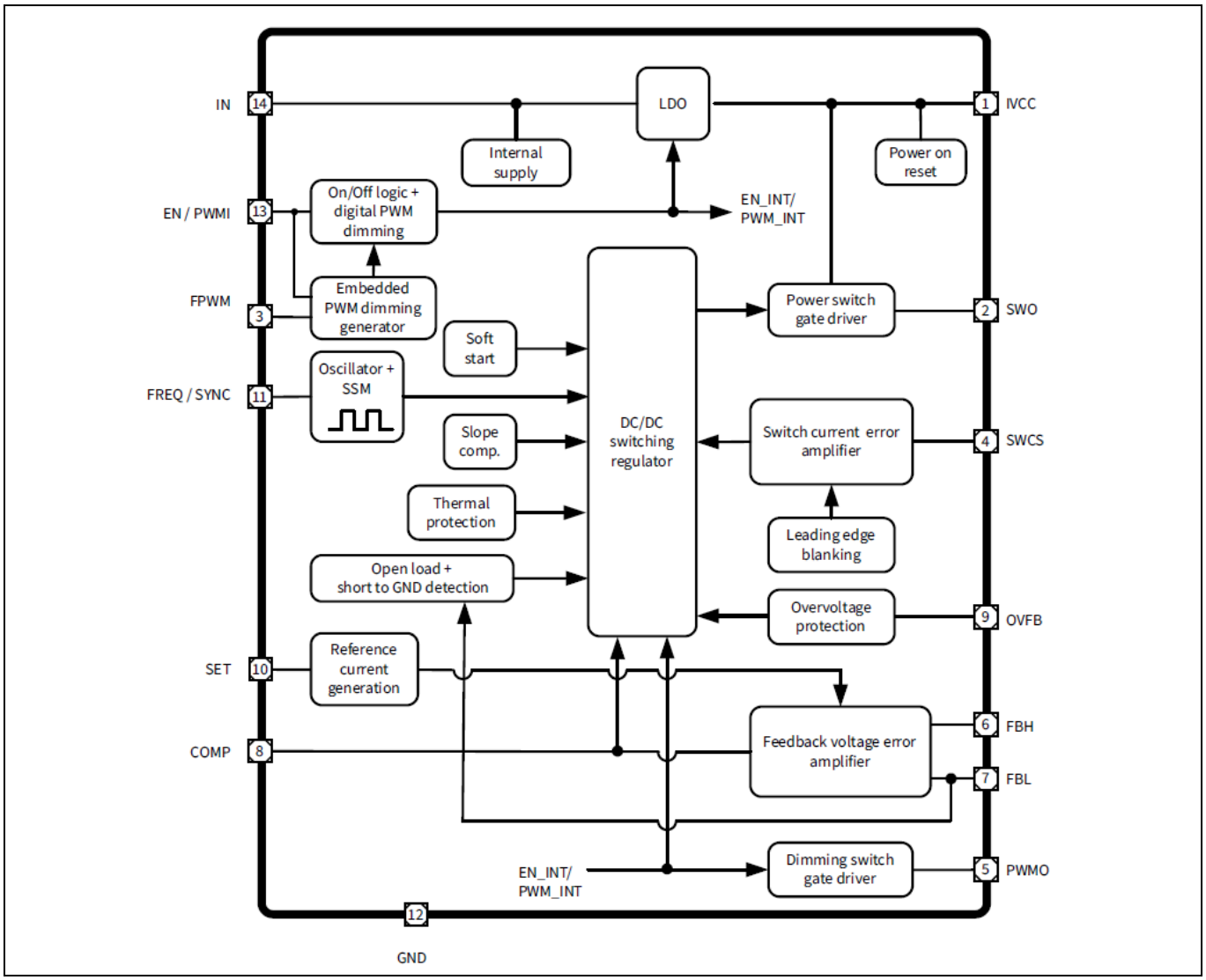


Figure 3 TLD5099EP block diagram [1]

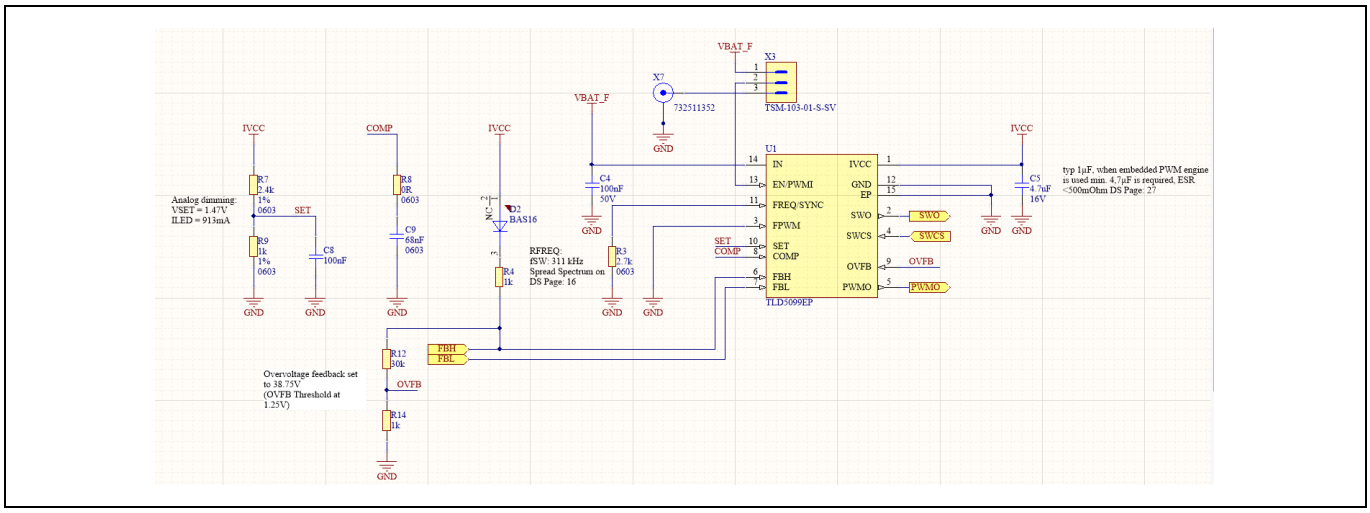


Figure 4 TLD5099EP schematic with external components

2.1.1 Power supply

The TLD5099EP is powered by a reverse polarity protected supply voltage at the IN pin. In order to start-up the device, the input voltage must exceed the threshold of $V_{IN,on}$ = 4.85 V. Additionally, the voltage applied to the EN/PWMI pin must be above $V_{EN/PWMI,ON}$ = 3 V during startup. In the configuration given in Figure 4, an input undervoltage shutdown occurs at voltages below $V_{IN\_off(min)}$ = 3.5 V. This threshold is defined by the minimum rating of the IN pin at decreasing input voltage. Using the three-pin jumper X3, the EN/PWMI pin can either be supplied by the reverse polarity protected input voltage, or by applying an external PWM signal via the SMA-Connector X7. Therefore, an external PWM signal is used for the PWM dimming feature. More details on the PWM dimming feature and how the EN/PWMI pin needs to be connected in case the embedded PWM engine is used is given in Chapter 2.1.5. Once the supply voltages are above their undervoltage thresholds, the internal linear regulator delivers 5 V with up to 90 mA (max.) to the gate drivers. An external capacitor with an ESR below $R_{IVCC,ESR}$ = 0.5 Ω must be placed close to the IVCC pin for stability and buffering purposes. According to the datasheet, a typical ceramic capacitor C_{IVCC} = 1 µF is proposed. If embedded PWM dimming is used, the capacitance needs to be increased to C_{IVCC} = 4.7 µF.

2.1.2 Switching frequency & spread spectrum

As listed in Table 2, the frequency of the internal oscillator can be configured in the range from 100 kHz to 500 kHz. This is done by connecting an external resistor R_{FREQ} between the FREQ pin and ground. The range of usable resistor values is divided into two sections. In Figure 5 below, it is seen that low resistor values activate the spread spectrum modulation, while higher resistances set the switching frequency without modulation.

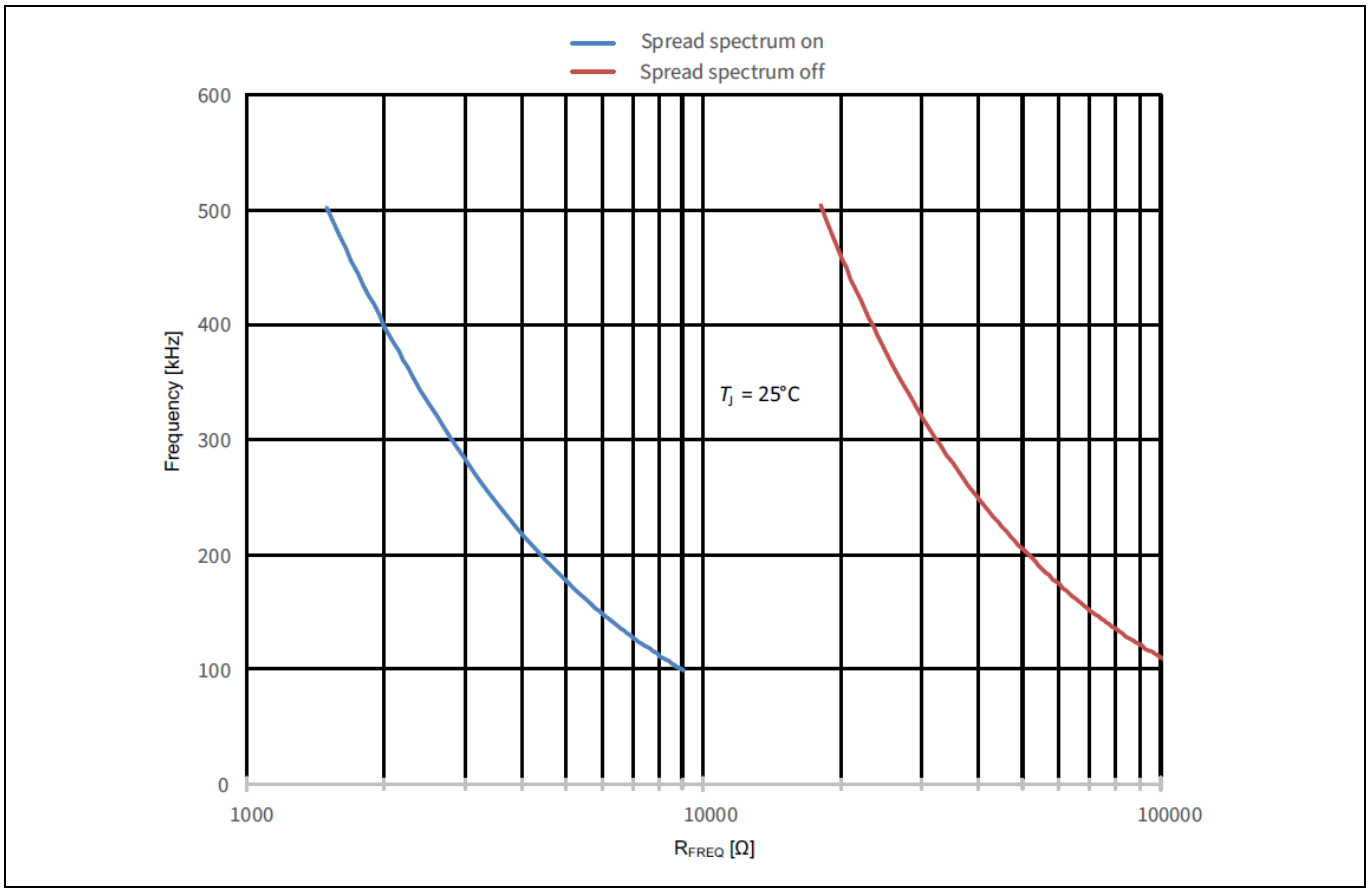


Figure 5 TLD5099EP switching frequency versus R_{FREQ} [1]

As the spread spectrum modulation helps to improve the EMC performance, the resistor is chosen such that the modulation is activated. While the modulation frequency is fixed to f_{FM} = 7 kHz, the modulation depth varies with 15% of f_{SW}. The required resistance to configure a spread spectrum modulated switching frequency of f_{SW} = 310 kHz, which is defined in the design specification and is determined by using Eq. 1.

$$R_{FREQ,SSMon} = \frac{1}{(600 * 10^{-12} * f_{SW})^{0.943}} - 600 = \frac{1}{(600 * 10^{-12} * 310\ kHz)^{0.943}} - 600 = 2.69\ k\Omega \quad \text{Eq. 1}$$

Due to the off-the-shelf availability of the resistor, a resistance of R_{FREQ} = 2.7 kΩ is used in the application. This deviation leads to the real switching frequency calculated in Eq. 2.

$$f_{SW} = \frac{\left(\frac{1}{R_{FREQ,SSMon} + 600}\right)^{\frac{1}{0.943}}}{600 * 10^{-12}} = \frac{\left(\frac{1}{2.7\ k\Omega + 600}\right)^{\frac{1}{0.943}}}{600 * 10^{-12}} = 309.5\ kHz \quad \text{Eq. 2}$$

To operate without spread spectrum modulation, the resistor calculated in Eq. 3 may be used.

$$R_{FREQ,SSMoff} = \frac{1}{(340 * 10^{-12} * f_{SW})^{1.13}} = \frac{1}{(340 * 10^{-12} * 310\ kHz)^{1.13}} = 31.2\ k\Omega \quad \text{Eq. 3}$$

2.1.3 Output current configuration

The controlled output current of the TLD5099EP is set via a sensing resistor in the output path of the converter. Based on the design specification, a load current of I_{OUT} = 0.9 A is desired for this application. This requirement is fulfilled in two steps. Firstly, the nominal output current is set to I_{OUT} = 1 A, before using the analog dimming feature to fine-tune the current. The feedback resistor R_{FB}, represented by R10 in Figure 11, is calculated as given in Eq. 4.

$$R_{FB} = \frac{V_{REF}}{I_{OUT}} = \frac{0.3\ V}{1\ A} = 0.3\ \Omega \quad \text{Eq. 4}$$

The maximum power loss of the shunt resistor is calculated in Eq. 5.

$$P_{RFB} = R_{FB} * {I_{OUT}}^2 = 0.3\ \Omega * (0.9\ A)^2 = 243\ mW \quad \text{Eq. 5}$$

To avoid overheating of the resistor, the WSL2010R3000FEA18 with a power rating of 1 W is considered.

In the second step, the analog dimming feature is used to reduce the nominal output current to the desired value of I_{OUT} = 0.9 A. To do so, the voltage level across the SET pin has to be configured accordingly. Figure 6 visualizes the relationship between V_{SET} and the controller feedback reference voltage V_{REF}. It is seen, that the reference voltage can be varied linearly based on a V_{SET} in the range between 100 mV and 1.6 V. In case the analog dimming is not needed, the SET pin must be connected to IVCC or an external voltage supply higher than 1.6 V.

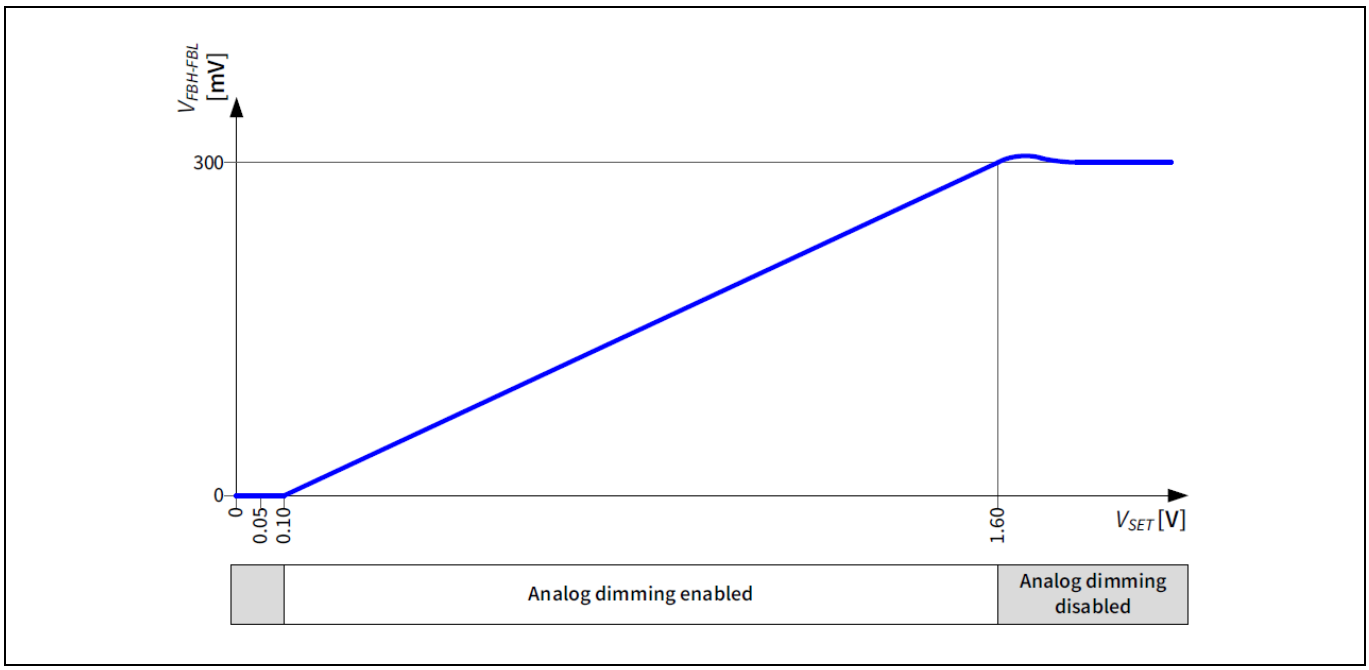


Figure 6 Reduction of V_{REF} via V_{SET} [1]

To reduce the set nominal output current to the desired I_{OUT} = 0.9 A, an analog dimming of 90% is necessary. For this purpose, the controller feedback reference voltage has to be lowered to 270 mV. The corresponding SET voltage is calculated using Eq. 6.

Eq. 6

$$V_{SET} = 5 * R_{FB} * I_{OUT} + 0.1\,V \rightarrow 5 * 0.3\,\Omega * 0.9\,A + 0.1\,V = 1.45\,V$$

This voltage level can easily be supplied to the SET pin using a resistor divider with reference to IVCC. By choosing R_{SET2} = 1 kΩ, R_{SET1} can be determined with Eq. 7. It is recommended to use a tolerance of ± 1% when choosing the SET resistor to increase accuracy.

$$R_{SET1} = \frac{V_{IVCC} * R_{SET2}}{V_{SET}} - R_{SET2} = \frac{5\,V * 1\,k\Omega}{1.45\,V} - 1\,k\Omega = 2.448\,k\Omega$$

Eq. 7

$$\rightarrow chosen = 2.4\,k\Omega$$

Due to the deviation from the ideal R_{SET1} resistance, the resulting output current is as in below Eq. 8.

$$V_{SET} = V_{IVCC} * \frac{R_{SET2}}{R_{SET1} + R_{SET2}} = 5\,V * \frac{1\,k\Omega}{2.4\,k\Omega + 1\,k\Omega} = 1.47\,V$$

$$I_{OUT} = \frac{V_{SET} - 0.1\,V}{5 * R_{FB}} = \frac{1.47\,V - 0.1\,V}{5 * 0.3\,\Omega} = 0.913\,A$$

Eq. 8

2.1.4 Switch current sense

Besides the sensing resistor for the output current, one further resistor is required for the current mode control loop and the switch current limitation. The so called R_{SWCS}, which is represented by R13 in Figure 11, limits the current through the n-channel MOSFET to a certain value.

The maximum voltage across the sensing resistor must not reach the threshold of $V_{SWCS,min}$ = 125 mV. As this condition must not only be valid for the steady state, but also for the transition phase, the current limit is set 25% above the actual switch peak current as safety margin. Using the peak current calculated in Chapter 2.2.2, the resistance is determined in Eq. 9.

$$R_{SWCS} = \frac{V_{SWCS,min}}{1.25 * I_{Q,peak}} = \frac{125\ mV}{1.25 * 5.13\ A} \approx 18\ m\Omega \qquad \text{Eq. 9}$$

The maximum power loss of the shunt resistor is calculated in Eq. 10.

$$P_{RSWCS} = R_{SWCS} * {I_{Q,RMS}}^2 = 18\ m\Omega * (3.92\ A)^2 = 0.277\ W \qquad \text{Eq. 10}$$

To avoid overheating of the resistor, the WSL2010R0180FEA18 with a power rating of 1 W is considered.

2.1.5 PWM dimming

The PWM dimming feature is used to modulate the average current in the load to a desired value. This feature is useful for brightness control and to implement derating strategies in extreme operating conditions. The output current which was set is not modified in amplitude but is modulated with a lower PWM frequency (100 Hz to 500 Hz) by an additional dimming MOSFET. The modulation can be done in two different ways which are external PWM dimming or embedded PWM dimming. In this reference design the external PWM dimming approach is used. In this case, the FPWM pin is also connected to GND because this is necessary only for embedded PWM dimming.

2.1.5.1 External PWM dimming

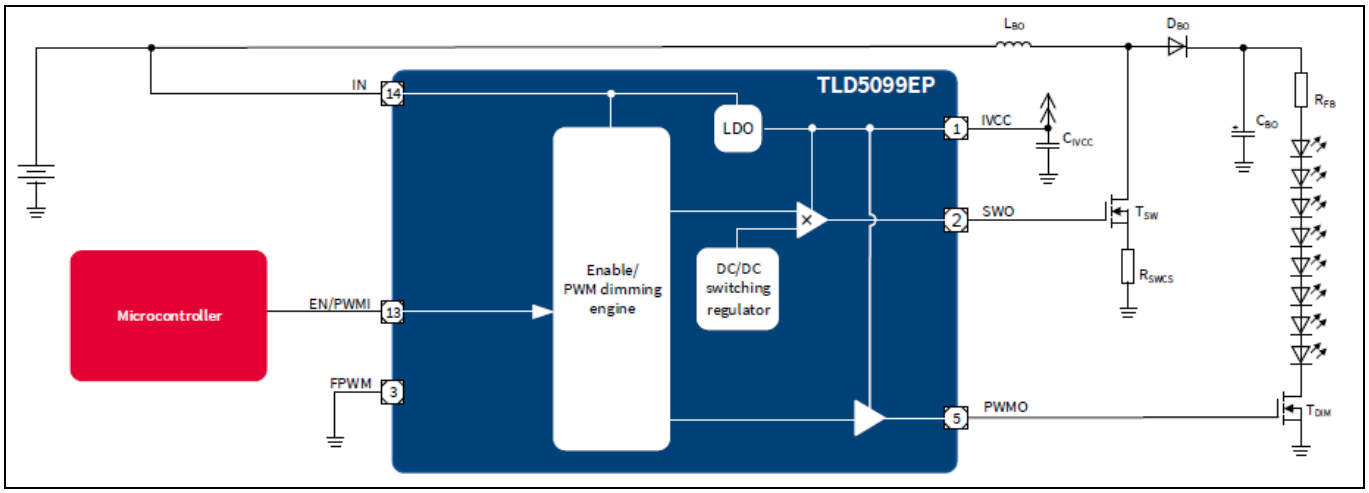


Figure 7 TLD5099EP simplified application circuit for external PWM dimming [1]

The concept of the external PWM dimming is shown in Figure 7. An external source (e.g. microcontroller) is used to implement the PWM dimming. In case a constant logic high signal is present at the EN/PWMI pin no PWM dimming is used. However, if a PWM is applied in the range of 100 Hz to 500 Hz by the external source, the PWM

dimming feature is activated. When the PWM dimming is active, the device differentiates between enable off and PWM dimming signal by requiring the signal at the EN/PWMI pin to stay low for the $t_{EN,OFF,DEL,typ}$ = 10 ms which corresponds to 100 Hz.

2.1.5.2 Embedded PWM dimming

In case no external source is in place to provide a PWM signal to achieve the PWM dimming one can also use the internal embedded PWM engine of the device. Figure 8 depicts the concept. A voltage divider at the EN/PWMI pin is used to provide a specific voltage which correlates to a specific DC. Furthermore, a capacitor is used at the FPWM pin to set the PWM frequency (100 Hz to 500 Hz).

Note: *If the internally generated voltage V_{IVCC} is used to power the voltage divider at the EN/PWMI pin, a specific startup circuit is necessary. This startup circuit is necessary because the EN/PWMI needs to have a voltage above $V_{EN/PWMI,ON}$ = 3 V during startup that the internal LDO can start to operate, as discussed in Chapter 2.1.1.*

For more details regarding embedded PWM dimming and the startup circuit please refer to the product datasheet [1].

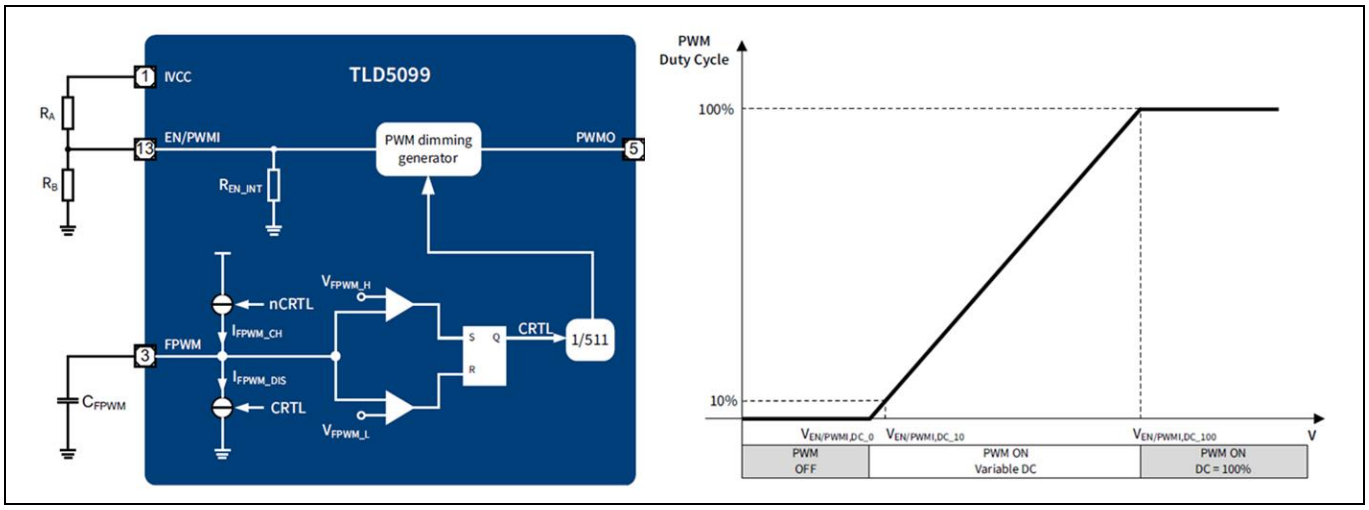


Figure 8 TLD5099EP embedded PWM engine [1]

2.1.6 Compensation network

The compensation network consisting of a serial RC-network determines the stability of the control loop. In order to select the proper values for the given partitioning, a calculation sheet is used. Under consideration of every possible input and output voltage condition, the best fitting component values were chosen. Figure 9 represents the Bode plot of the controller at typical input voltage and activated high beam. The compensation network which ensures a stable system over the whole operational range is
R_{COMP} = 0 Ω and C_{COMP} = 68 nF.

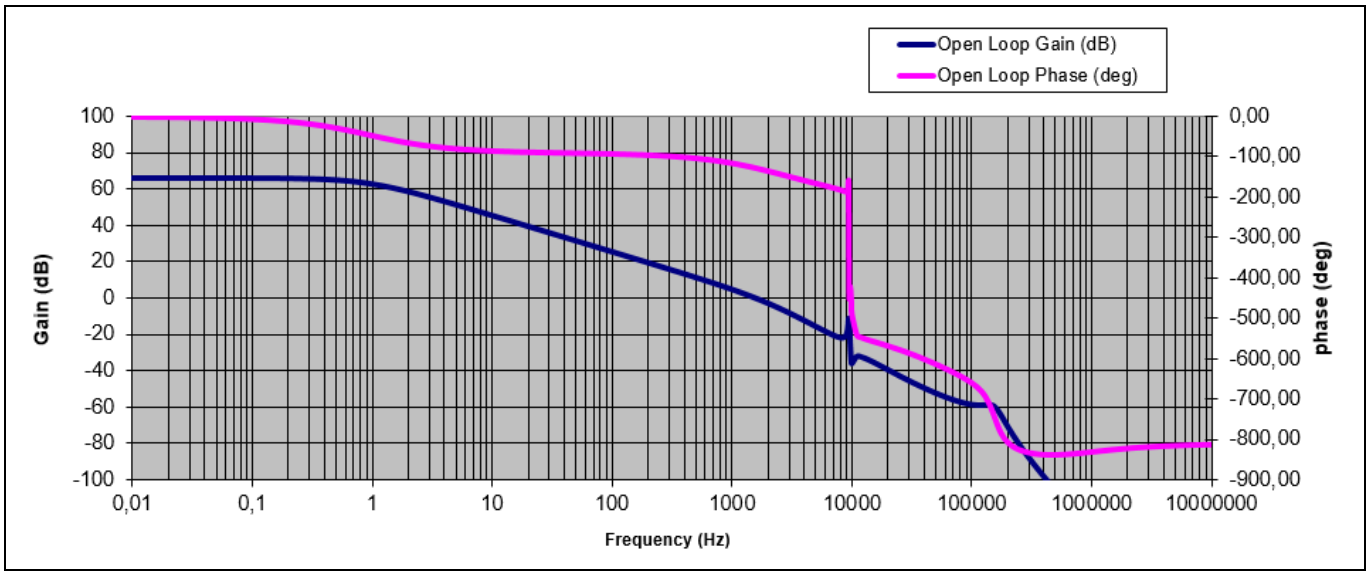


Figure 9 TLD5099EP Bode plot with C_{COMP} = 68 nF and HB active at typical input voltage

2.1.7 Overvoltage protection

The output overvoltage protection feature helps to avoid too high voltage levels during an open load condition. In the case of the considered application, the maximum output voltage occurs when the HB and the LB is active. In Figure 10, the temperature dependency of the LED forward voltage is shown.

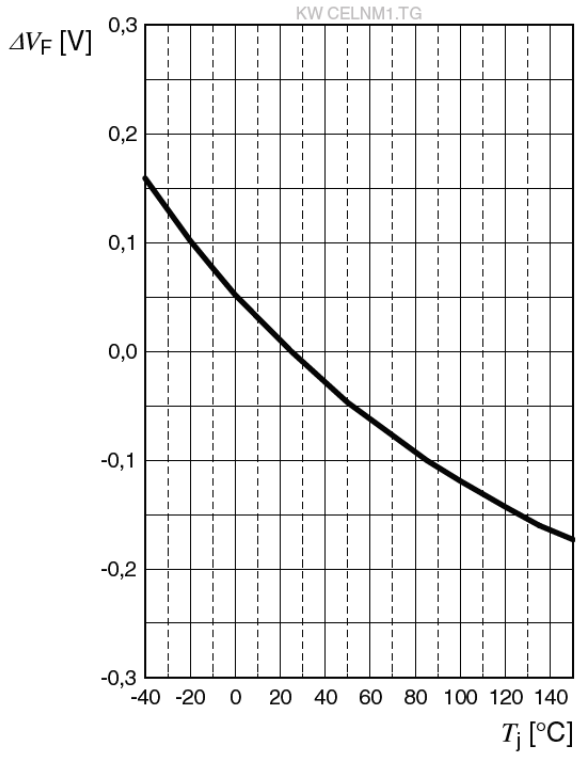


Figure 10 Temperature dependency of the LED forward voltage [2]

It is seen, that the forward voltage increases by up to 0.16 V per LED at negative temperatures. The output voltage at negative temperature of -40°C is calculated in Eq. 11. In this case the maximum possible forward voltage $V_{F,LED,max}$ for every LED is considered.

$$V_{OUT,neg40} = \#LEDs * V_{F,LED,max} + \#LEDs * \Delta V_F = 9 * 3.4\ V + 9 * 0.16\ V = 32.04\ V \quad \textit{Eq. 11}$$

An overvoltage fault is triggered, once the voltage at the OVFB pin reaches $V_{OVFB,TH,typ}$ = 1.25 V. By using a resistor divider and selecting the lower resistor as R_{OVL} = 1 kΩ, the upper resistor R_{OVH} can be calculated using Eq. 12. Including a safety margin, the overvoltage threshold is selected as 38 V.

$$R_{OVH} = \frac{V_{OUTOV} * R_{OVL}}{V_{OVFB,TH,typ}} - R_{OVL} = \frac{38\ V * 1\ k\Omega}{1.25\ V} - 1\ k\Omega = 29.4\ k\Omega \quad \textit{Eq. 12}$$

$$\rightarrow chosen = 30\ k\Omega$$

Due to the slightly higher resistance, the actual overvoltage threshold increases as given in Eq. 13.

$$V_{OUTOV} = V_{OVFB,TH,typ} * \frac{R_{OVH} + R_{OVL}}{R_{OVL}} = 1.25\ V * \frac{30\ k\Omega + 1\ k\Omega}{1\ k\Omega} = 38.75\ V \quad \textit{Eq. 13}$$

Once this threshold is reached, the TLD5099EP will stop the switching activities, until the voltage at the OVFB pin decreases by the hysteresis value $V_{OVFB,HYS,min}$ = 50 mV.

2.2 SEPIC power stage and input filter

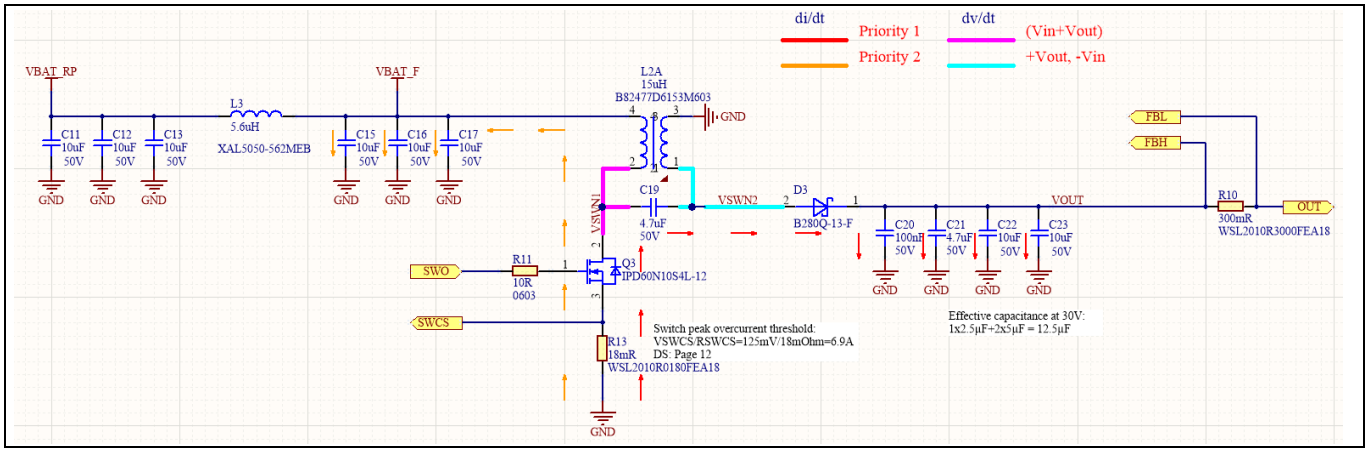


Figure 11 Power stage and input filter schematic

As given in the system description, the target of this design is to drive a combination of LB and HB LEDs based on the SEPIC topology. The SEPIC topology offers a buck-boost behavior which is beneficial to stabilize the varying input voltage from a battery supply in a car. Furthermore, it has an inherent short to GND protection due to the SEPIC coupling capacitor compared for example to the classical boost converter topology. However, there are also drawbacks related to the SEPIC topology as for example higher current/voltage stress on the active components and the need for two inductors or one coupled inductor. Therefore, thermal design considerations are extremely important when designing a SEPIC power stage. The operating current and voltage waveforms for the main components of the SEPIC power stage can be seen in Figure 12 and Figure 13.

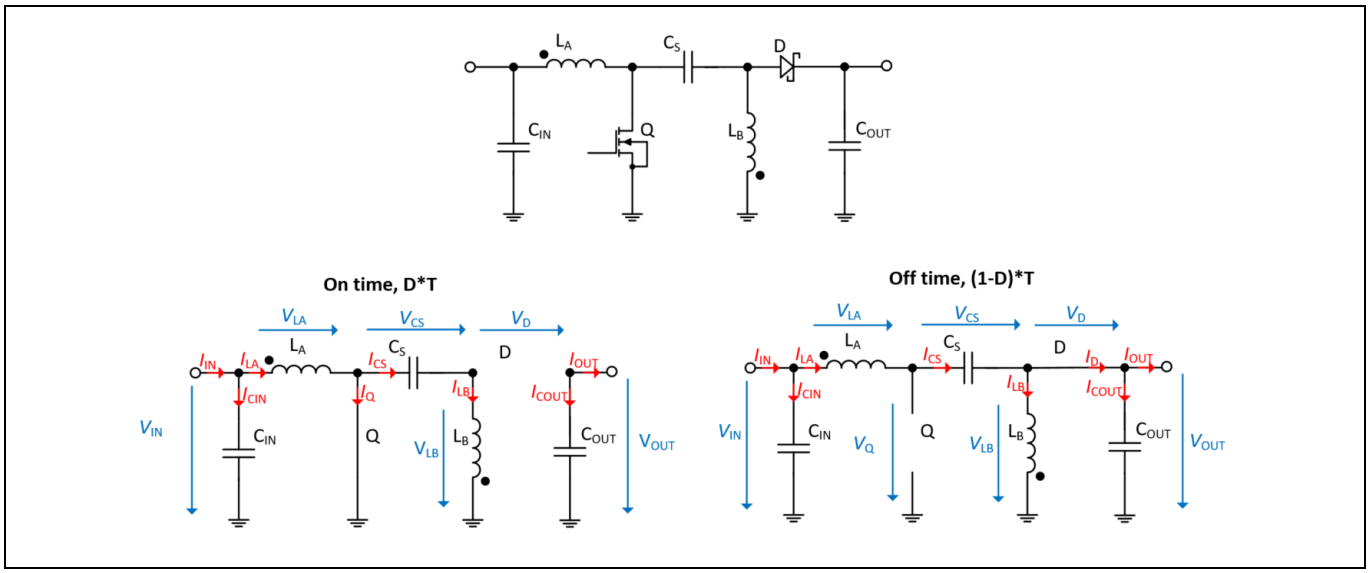


Figure 12 SEPIC power stage during on and off time

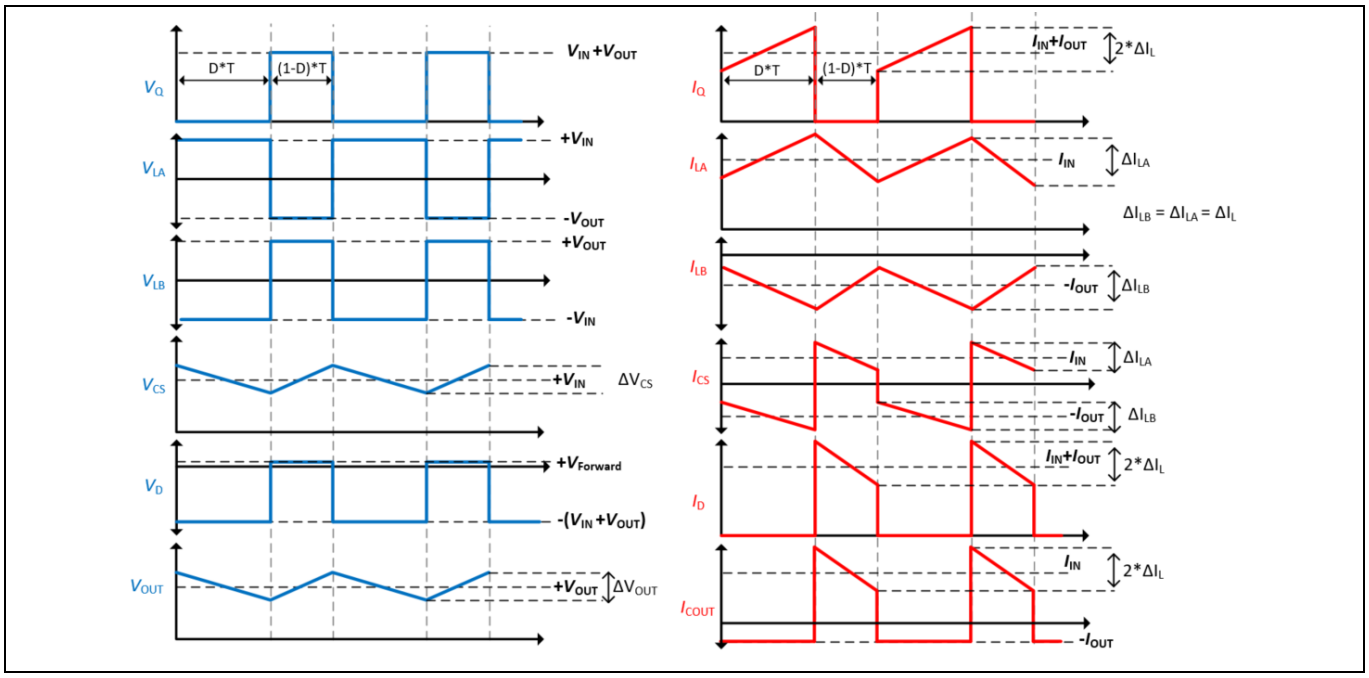


Figure 13 SEPIC power stage voltage and current waveforms in steady state and CCM

2.2.1 Passive components

One of the fundamental parameters of every switched mode power supply is the DC with which the MOSFET is driven. In case of the SEPIC topology, this parameter is as given in Eq. 14. The diode forward voltage V_D is also impacting the DC due to the asynchronous topology. However, a Schottky diode is used and the effect of the forward voltage drop is considered as small compared to the input and output voltage and is therefore neglected in the calculations.

$$D = \frac{V_{OUT} + (V_D)}{V_{IN} + V_{OUT} + (V_D)} \quad \text{Eq. 14}$$

While the maximum duty cycle occurs at $V_{IN,min}$, the minimum duty cycle is computed considering $V_{IN,max}$. As the output voltage of the converter changes depending on the HB activation, the number of operating points is doubled. Referring to the V_{IN} and V_{OUT} voltage levels given in Table 1, four extreme operating points can be calculated. Table 3 summarizes the resulting duty cycles.

Table 3 Duty cycle variation with respect to V_{IN} and V_{OUT}

	$V_{IN,max}$ = 16 V	**$V_{IN,min}$ = 8 V**	**$V_{IN,typ}$ = 13.5 V**
$V_{OUT,max}$ = 27 V	62.8%	77.1%	66.6%
$V_{OUT,min}$ = 13.75 V	46.2%	63.2%	50.4%

In the following calculation steps, these operating points are used to determine the power stage components. Based on an assumed converter efficiency of η = 85%, the maximum input current is calculated. As seen in Eq. 15, the maximum input current $I_{IN,max}$ occurs at $V_{IN,min}$ and $V_{OUT,max}$.

$$\eta = \frac{V_{OUT.max} * I_{OUT}}{V_{IN,min} * I_{IN,max}} \rightarrow I_{IN,max} = \frac{I_{OUT}}{\eta} * \frac{V_{OUT,max}}{V_{IN,min}} \quad \text{Eq. 15}$$

$$I_{IN,max} = \frac{0.9\ A}{0.85} * \frac{27\ V}{8\ V} = 3.57\ A$$

The inductor size depends on the allowed current ripple ΔI_L. When defining the peak-to-peak value of the ripple, the target is to ensure CCM operation. However, the TLD5099EP can also operate and control the power stage in DCM but one has to keep in mind that the transfer function on the power stage will change and could cause instability. A typical proposal is to select 20% of the maximum input current as allowed inductor current ripple. Using the previously calculated maximum input current results in the ripple given in Eq. 16.

$$\Delta I_L = 0.2 * I_{IN,max} = 0.2 * 3.57\ A = 0.714\ A \quad \text{Eq. 16}$$

With the current ripple calculated in Eq. 16, the required inductor can be determined. One must consider, that for a coupled inductor, approximately half the inductance value compared to uncoupled coils can be assumed due to mutual inductance and a coupling factor of approximately one. The minimum required coupled inductor value is calculated in the following Eq. 17.

$$L_{Coupled} \geq \frac{1}{2} * \frac{V_{IN,min} * D_{max}}{\Delta I_L * f_{SW}} \geq \frac{1}{2} * \frac{8\ V * 0.771}{0.714\ A * 310\ kHz} \quad \text{Eq. 17}$$

$$L_{Coupled} \geq 13.9\ \mu H \rightarrow 15\ \mu H\ chosen$$

As already mentioned previously, it is recommended to ensure that the CCM is guaranteed in the different operating points of the converter. The transition to the DCM occurs when the ΔI_L ripple exceeds double the output current. Using Eq. 18, the ΔI_L at varying DC can be determined.

$$\Delta I_L = \frac{V_{IN} * D}{2 * L_{Coupled} * f_{SW}} \quad \text{Eq. 18}$$

Due to the fact, that the inductor current ripple is proportional to the DC, only the operating cases at maximum output voltage were considered for the calculations summarized in Table 4. It is seen, that CCM is given over the complete static input voltage range.

Table 4 Ripple current with respect to input voltage

	$V_{IN,max}$ = 16 V		$V_{IN,min}$ = 8 V		$V_{IN,typ}$ = 13 V	
$V_{OUT,max}$ = 27 V	Duty cycle	62.8%	Duty cycle	77.1%	Duty cycle	66.6%
	ΔI_L	1.08 A	ΔI_L	0.66 A	ΔI_L	0.93 A

With the calculated current ripples, the peak currents through both inductors can be determined. The peak current in inductor L_A is given by the maximum input current plus half the current ripple. In case of L_B the maximum output current plus half the current ripple is considered. As the maximum input current occurs at minimum input voltage, a ripple of ΔI_L = 0.66 A is considered in Eq. 19.

$$I_{LA,peak} = I_{IN,max} + \frac{\Delta I_L}{2} = 3.63\ A + \frac{0.69\ A}{2} = 3.98\ A$$

$$I_{LB,peak} = I_{OUT} + \frac{\Delta I_L}{2} = 0.9\ A + \frac{0.69\ A}{2} = 1.25\ A$$

Eq. 19

To avoid saturation effects, the inductor saturation current should be approximately 20% higher than the peak current. For the selection of the inductor, the components from Table 5 were compared. From this comparison, the 15 µH coupled coil TDK B82477D6 was selected.

Table 5 Possible candidates for the main coupled inductor

Manuf.	Series	Induct.	Shielded	RMS curr. (both wind.)	Sat. curr.	DCR	Max. temp	PCB area
Coilcraft	MSD1260T	22 µH	Yes	1.76 A[1)]	5.02 A[2)]	116 mΩ	165°C	151 mm²
Coilcraft	MSD1260T	15 µH	Yes	2.06 A[1)]	5.8 A[2)]	85 mΩ	165°C	151 mm²
Coilcraft	MSD1278	22 µH	Yes	1.99 A[1)]	6.8 A[2)]	96 mΩ	165°C	151 mm²
Coilcraft	MSD1278	15 µH	Yes	2.3 A[1)]	9.1 A[2)]	72 mΩ	165°C	151 mm²
TDK	B82477D4	22 µH	Yes	2.8 A[3)]	4.5 A	70 mΩ	150°C	156 mm²
TDK	B82477D4	15 µH	Yes	3.25 A[3)]	5.5 A[5)]	52.5 mΩ	150°C	156 mm²
TDK	B82477D6	15 µH	Yes	4.92 A[3)]	8.7 A[5)]	29.6 mΩ	150°C	156 mm²
Vishay	IHCL-4040DZ	22 µH	Yes	2.5 A[1)]	4.75 A[4)]	177 mΩ	155°C	108 mm²
Vishay	IHCL-4040DZ	15 µH	Yes	3.3 A [1)]	6 A [4)]	110 mΩ	155°C	108 mm²

1) Current applied to both windings simultaneously which causes a 40°C temperature rise
2) 30% drop of inductance, current in both windings simultaneously
3) Current which can be applied (sum of both windings) up to 105°C ambient
4) 20% drop of inductance, current in both windings simultaneously
5) 10% drop of inductance, current in both windings simultaneously

The forward current through the LED string will vary depending on the output voltage ripple. In order to select the proper output capacitor, firstly the maximum allowed voltage ripple has to be defined. It depends on the transresistance of the LED chain in the operating point and the maximum allowed peak to peak current ripple in the LED string. The resistance is determined using the forward current graph shown in Figure 14.

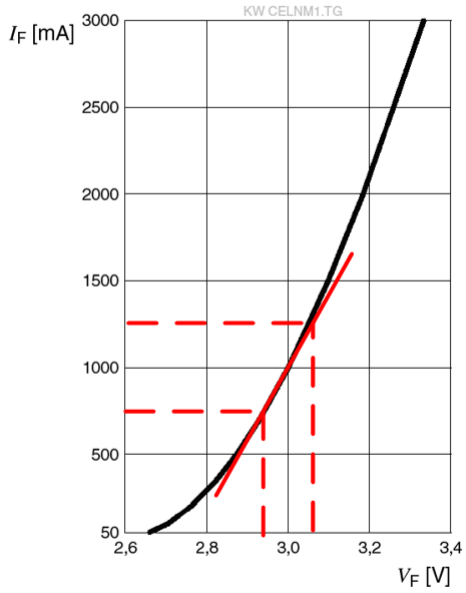


Figure 14 I/V curve from the load LED OSRAM OSLON® Compact PL, KW CELNM1.TG [2]

From the read values, the transresistance is calculated in Eq. 20.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} = \frac{3.05 - 2.95}{1.25 - 0.75} = 200\ m\Omega \qquad \textit{Eq. 20}$$

The maximum output voltage ripple, computed in Eq. 21, distributes equally over the number of LEDs. Here, the worst case occurs when only the five LB LEDs are active.

$$\Delta V_{LED} = \frac{\Delta V_{OUT}}{\#LEDs} = R_{LED} * \Delta I_{LED} \rightarrow \Delta V_{OUT} = \#LEDs * R_{LED} * I_{LED} \qquad \textit{Eq. 21}$$

$$\Delta V_{OUT} = 5 * 200\ m\Omega * 200\ mA = 200\ mV$$

Based on the output voltage ripple requirements, the output capacitor can be calculated. During the on-time, the output capacitor needs to provide the output current. ESR considerations should be included if they have a relevant contribution. In this case ceramic capacitors will be used in parallel which offers very low ESR. The worst-case output current ripple occurs at maximum duty cycle. These parameters, including the switching frequency, are required to calculate the output capacitor using Eq. 22.

$$C_{OUT} \geq \frac{I_{OUT} * D_{max}}{(\Delta V_{OUT} - \cancel{\Delta V_{OUT_{ESR}}}) * f_{SW}}$$

$$C_{OUT} \geq \frac{0.9\ A * 0.771}{(0.2\ V) * 310\ kHz} \geq 11.2\ \mu F \qquad \textit{Eq. 22}$$

$$\rightarrow\ chosen\ 1\ x\ 4.7\ \mu F + 2\ x\ 10\ \mu F = 24.7\ \mu F \rightarrow effective\ @30V \approx 12.5\ \mu F$$

The chosen output capacitors are:

- 1x 4.7 µF, X7R, 50 V (GCM32ER71H475KA55)
- 2x 10 µF (GCM32EC71H106KA03)

These capacitors sum up in total to nominal 24.7 µF. However, when considering the DC-bias effect of multilayer ceramic capacitors the effective capacitance drops to approximately half the nominal value which is shown in Figure 15, where the blue line corresponds to 0 V DC-bias and the green line to 30 V DC-bias [3]

Note: *The DC-bias effect reduces the nominal capacitance at the output capacitors approximately to the half value (@ 30 V output voltage). Switching from a 50 V rated capacitor to for example a 100 V capacitor does not significantly improve the DC-bias effect.*

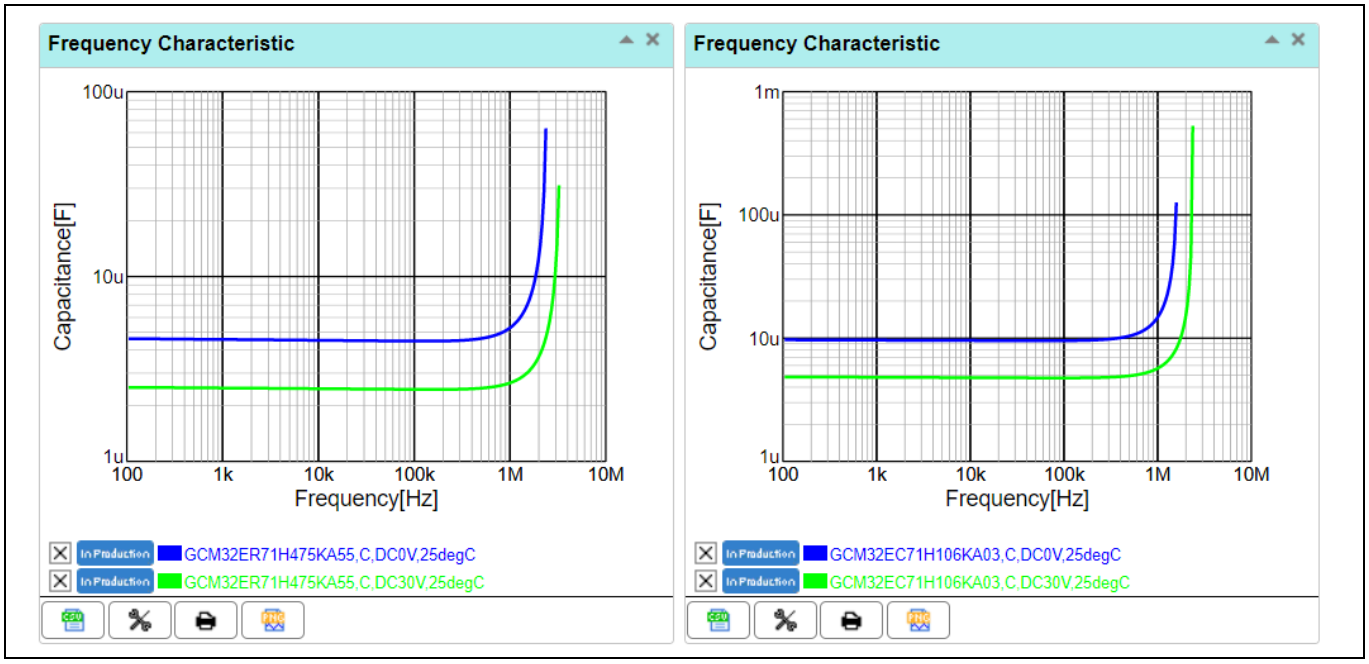


Figure 15 DC-bias effect on output capacitors [3]

The ripple current rating of the output capacitor can be calculated using Eq. 23. During the on-time, the negative output current and during the OFF-time, the input current flows into the output capacitor. Here, the worst case occurs at minimal input voltage, thus maximal input current. Since low ESR ceramic capacitors are used in parallel, the ripple current rating of the capacitors is sufficient.

$$I_{COUT,RMS} = \sqrt{\frac{-I_{OUT}{}^2}{T} * \int_0^{D_{max}*T} d_t + \frac{I_{IN,max}{}^2}{T} * \int_{D_{max}*T}^{T} d_t}$$

$$= \sqrt{-I_{OUT}{}^2 * D_{max} + I_{IN,max}{}^2 * (1 - D_{max})} \qquad \text{Eq. 23}$$

$$I_{COUT,RMS} = \sqrt{-0.9\ A^2 * 0.771 + 3.57\ A^2 * (1 - 0.771)} = 1.88\ A$$

One of the key components of the SEPIC topology is the coupling capacitor C_S which has to further provide the input voltage during the switching activities. A reasonable maximal peak to peak voltage variation across the C_S would be 10% of the minimum input voltage. During the on-time, the negative output current flows through the coupling capacitor. The capacitance is calculated using Eq. 24.

$$C_S \geq \frac{I_{OUT} * D_{max}}{0.1 * V_{IN,min} * f_{SW}} \geq \frac{0.9\ A * 0.771}{0.1 * 8\ V * 310\ kHz} \geq 2.79\ \mu F$$
$$\rightarrow chosen = 4.7\ \mu F \qquad \textit{Eq. 24}$$

The RMS current through the coupling capacitor is given in Eq. 25.

$$I_{CS,RMS} = \sqrt{{I_{OUT}}^2 * D_{max} + {I_{IN,max}}^2 * (1 - D_{max})} \qquad \textit{Eq. 25}$$
$$= \sqrt{0.9\ A^2 * 0.771 + 3.57\ A^2 * (1 - 0.771)} = 1.88\ A$$

When selecting the capacitor component between the switching node and the output, one must consider the voltage rating. The maximum voltage levels across the coupling capacitor is shown in Figure 13. The static and transient case is shown in Eq. 26.

$$V_{CS,max} = V_{IN,max} = 16\ V$$
$$V_{CS,\max\_trans} = V_{IN,Trans\_max} = 35\ V \qquad \textit{Eq. 26}$$

2.2.2 Switching MOSFET

The switching MOSFET in the SEPIC topology faces high current and voltage stress as it can be seen in the current and voltage waveforms in Figure 13. Peak current and voltage requirements can be calculated using equation Eq. 27.

$$I_{Q,peak} = I_{IN,max} + I_{OUT} + \Delta I_L = 3.57\ A + 0.9\ A + 0.66\ A = 5.13A$$
$$V_{Q,peak} = V_{IN,max} + V_{OUT,max} = 16\ V + 27\ V = 43\ V \qquad \textit{Eq. 27}$$
$$V_{Q1,peak,Trans} = V_{IN,Trans,max} + V_{OUT,max} = 35\ V + 27\ V = 62\ V$$

Power MOSFETs in switching converters suffer from different loss mechanisms. The most dominating ones are the conduction losses, switching losses and reverse recovery losses due to the switching diode. Switching and conduction losses will be discussed analytically. Reverse recovery losses are not included in the analytical calculations but will be considered in a simulation presented in Chapter 2.2.2.1.

2.2.2.1 Switching losses

Switching losses are usually the dominant losses in switching converters. The switching losses increase with switching frequency, peak current and voltage during the switching event and decrease with faster slew rates. However, faster slew rates also have a negative impact on EMC performance, thus a compromise between switching losses and switching slew rates has to be made. In a SEPIC converter, the stress on the power MOSFET is especially high, since the peak voltage during the switching transient is approximately V_{IN} plus V_{OUT}. Furthermore, the peak current during the switching transient is I_{IN} plus I_{OUT}. Therefore, an appropriate analysis of the switching losses and thermal design is crucial for the switching MOSFET.

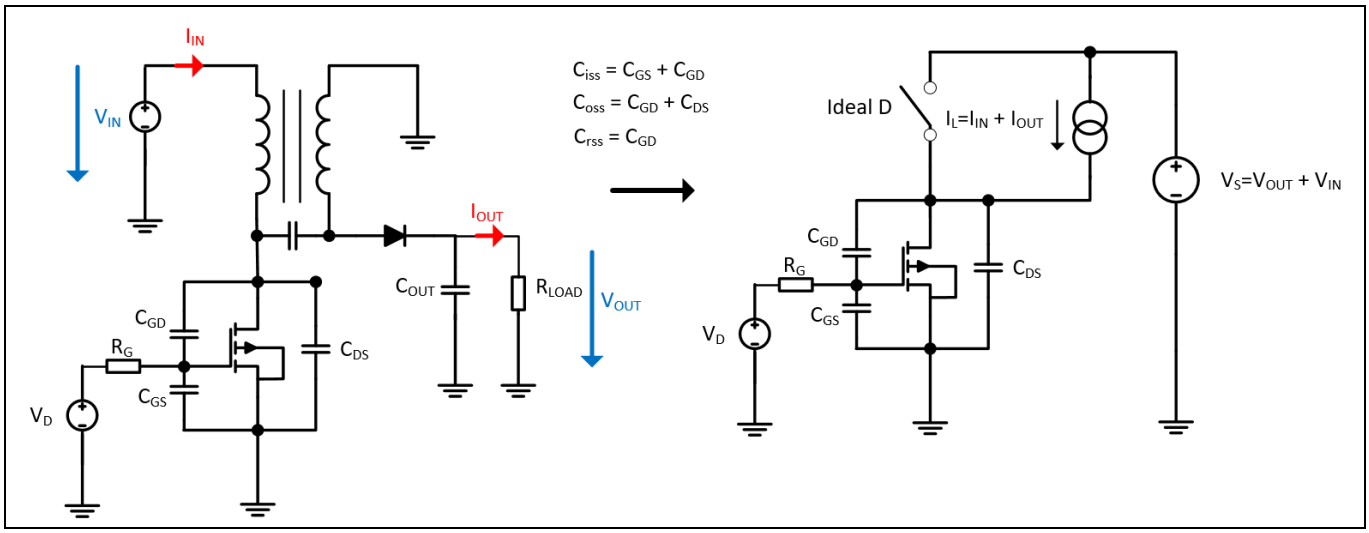


Figure 16 Equivalent circuit switching losses

Power MOSFETs have parasitic capacitances which determine the switching behavior. Figure 16 depicts a circuit which represents what occurs in a hard-switched converter. For simplicity the diode can be replaced with an ideal diode and the inductor can be replaced with a current source. The voltage source is modeled with a magnitude of V_{IN} plus V_{OUT} and the load current as I_{IN} plus I_{OUT} which gives a reasonable approximation. Refer to Figure 13 for the current and voltage waveforms on the switching MOSFET. The switching process can be separated into four phases and is shown for a turn-on.

Phase 1, $t_0 \le t \le t_1$:

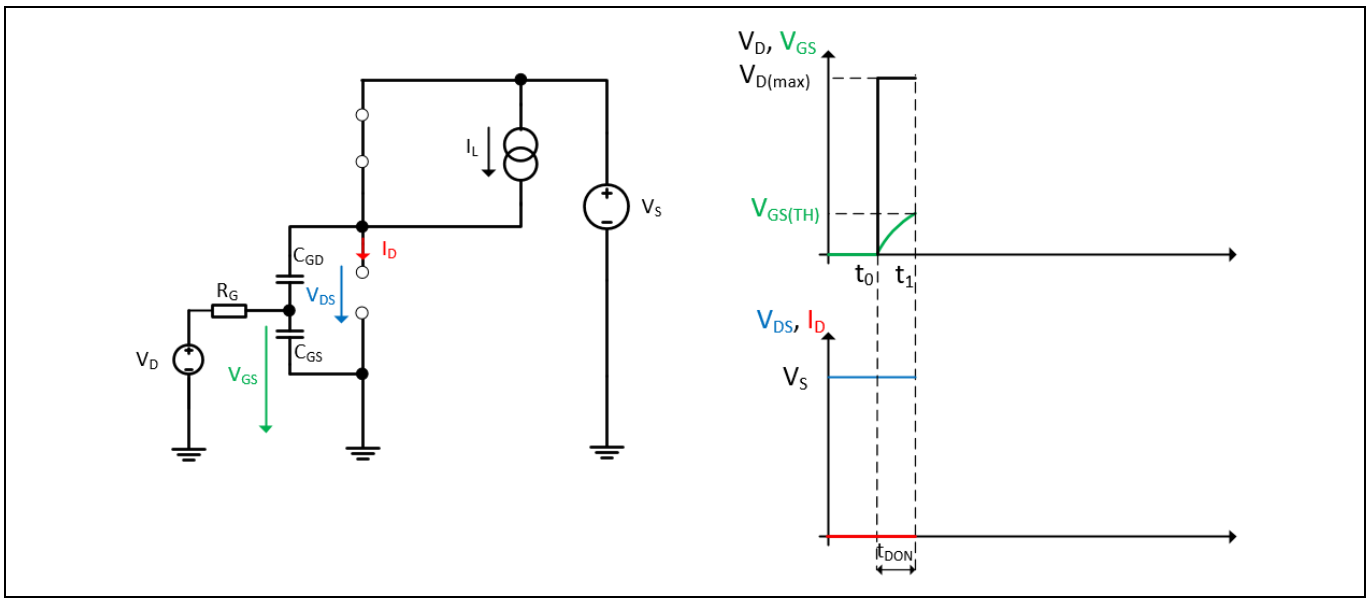


Figure 17 Power MOSFET turn-on transition – Phase 1

During phase 1, which is depicted in Figure 17, the diode conducts and the load current flows through the diode. At time t_0 the gate drive voltage $V_{D(max)}$ is applied to the gate of the MOSFET. In this moment V_{GS} starts to rise. V_{GS} rises until the threshold voltage $V_{GS(TH)}$ is reached where the MOSFET begins to conduct. During this time interval, the drain source voltage is clamped by the ideal diode to the supply voltage and the drain current is zero.

Phase 2, $t_1 \le t \le t_2$:

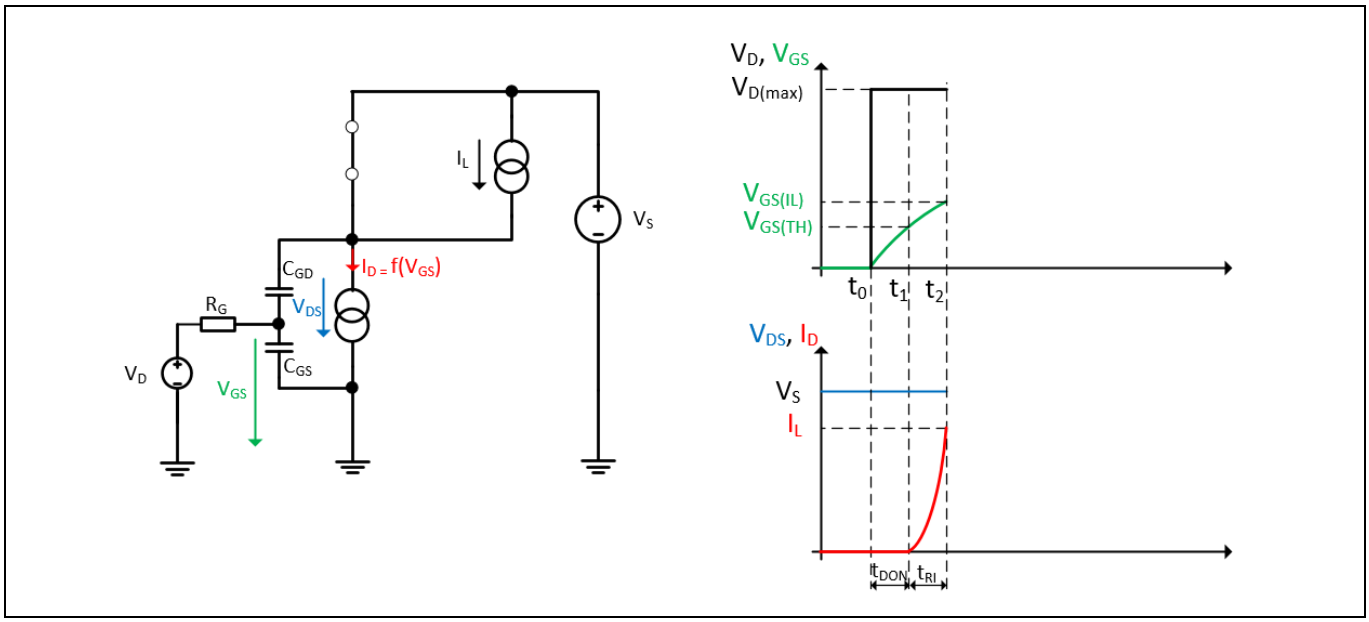


Figure 18 Power MOSFET turn-on transition – Phase 2

During phase 2, which is depicted in Figure 18, the current in the drain source channel in the MOSFET rises. The drain current is a function of the applied V_{GS}. The V_{GS} rises until the drain current reaches the level of the load current. Until that moment the ideal diode still clamps the drain source voltage to the supply voltage since current is flowing through the diode. Delay time (t_{DON}) is the time it takes from when the drive voltage is applied to the gate of the MOSFET (t_0) until the current starts to flow (t_1). The time where the drain current starts to flow (t_1) until the load current is reached (t_2) is called current rise time (t_{RI}).

Phase 3, $t_2 \le t \le t_3$:

During phase 3, which is shown in Figure 19, all the load current is now flowing through the MOSFET, thus the diode is turned off. Therefore, the drain source voltage can start to decrease.

Note: Reverse recovery effects would be visible at this stage and would manifest itself in an increase of the drain current above the load current level. This would provide the reverse recovery charge which is necessary so that the switching diode is able to turn off (= reverse recovery effect)

The potential on the drain of the MOSFET starts to fall. A consequence of a negative voltage slope at the drain is that C_{rss} capacitor needs to be charged by the gate driver. The gate charge-current flows through C_{rss} to provide the necessary charge. As a consequence, the gate source voltage cannot increase and stays constant. This is the so called “Miller Plateau”. The gate charge current is constant during that time since V_D and V_{GS} are constant. Therefore, the assumption would be that the drain source voltage decreases linearly. However, the slope is observed to be steepest at t2 and flattens out to t3. This is due to the fact that the reverse transfer capacitance C_{rss} is nonlinear. C_{rss} decreases with increasing drain source voltage. Therefore, at time t_2, C_{rss} is at a minimum since V_{DS} is at a maximum thus, the slope is steepest at t_2.

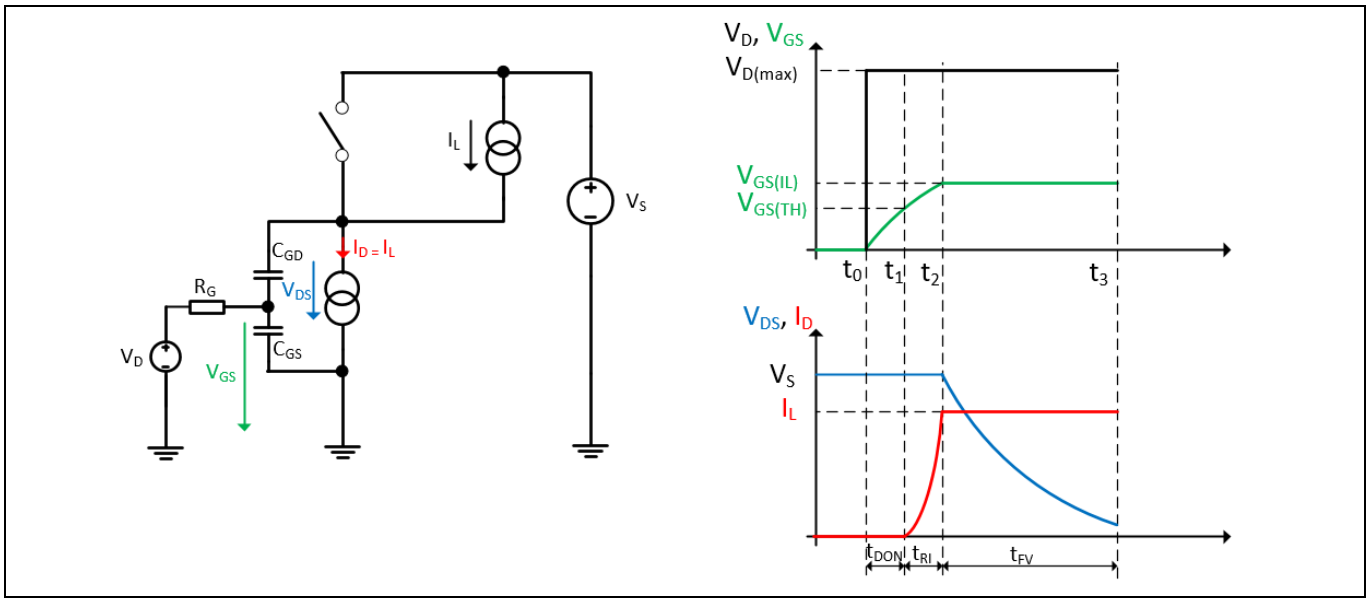


Figure 19 Power MOSFET turn-on transition – Phase 3

Phase 4, $t_3 \le t \le t_4$:

During phase 4, which is shown in Figure 20, the gate source voltage finally can increase further since the reverse transfer capacitance C_{rss} is fully charged and the gate charge current is used to further increase the gate source voltage. In this phase the on-state resistance is further reduced until the gate is charged up to the gate drive voltage V_D. The to the load current times the on-state resistance. When the MOSFET is fully switched on, the drain source voltage reduces to the equivalent of $I_L * R_{DS(ON)}$.

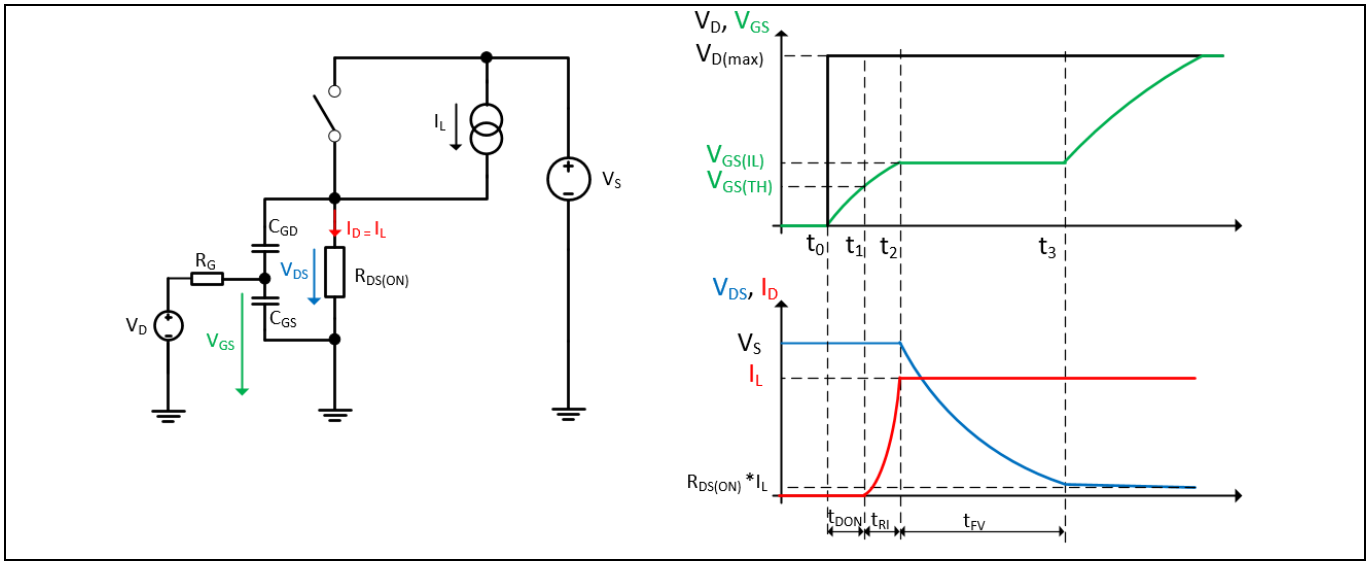


Figure 20 Power MOSFET turn-on transition – Phase 4

It can be concluded that the total switching losses can be approximated using the following formula.

$$P_{SW} = V_S * I_L * \frac{t_{RI} + t_{FV} + t_{FI} + t_{RV}}{2} * f_{SW} \qquad \text{Eq. 28}$$

This formula implies a triangular area formed by V_S and I_L which is an overestimation since the drain source voltage and drain current does not decrease/increase linearly due to the voltage dependent reverse transfer capacitance C_{rss} and the quadratic relationship between V_{GS} and I_D, thus leads to overestimated switching losses. Another challenge is to calculate the switching times.

$$t_{RI} = R_G * C_{iss} * \ln\left(\frac{V_D - V_{GS(TH)}}{V_D - V_{GS(IL)}}\right)$$

$$t_{FV} = R_G * C_{rss} * \frac{V_S}{V_D - V_{GS(IL)}}$$

$$t_{FI} = R_G * C_{iss} * \ln\left(\frac{V_{GS(IL)}}{V_{GS(TH)}}\right)$$

$$t_{RV} = R_G * C_{rss} * \frac{V_S}{V_{GS(IL)}}$$

Eq. 29

The four switching times can be calculated using Eq. 29.

The following parameters are required for the calculations:

- R_G … Gate resistance
- C_{iss} … Input capacitance (C_{gd} + C_{gs})
- V_D… Gate drive voltage
- $V_{GS(IL)}$ … Plateau voltage (Miller plateau)
- $V_{GS(TH)}$ … Gate source threshold voltage
- V_S … Drain source voltage during switching event
- C_{rss} … Reverse transfer capacitance (C_{gd})

Some parameters which are necessary to calculate the switching times vary in relation to the drain source voltage, have possible large spread or are difficult to extract from the datasheet. For this design firstly, an analytical calculation of the switching losses and conduction losses is given and secondly, it is compared to a simulation done in SPICE. For this design the Infineon OptiMOS™ –T2 power transistor IPD60N10S4L-12 was selected. Another possible candidate for the switching MOSFET could be also the OptiMOS™ –5 power transistor IAUC28N08S5L230. Table 6 summarizes the most important parameters of the IPD60N10S4L-12 power MOSFET:

Table 6 IPD60N10S4L-12 OptiMOS™-T2 n-channel power transistor parameters [4]

Parameter	Min.	Typ.	Max.	comment
V_{GS}	-16 V	–	16 V	Maximum gate source voltage
V_{DS}	–	–	100 V	Maximum drain source voltage
T_J	-55°C	–	175°C	Operating temperature range
$V_{GS(TH)}$	1.1 V	1.6 V	2.1 V	Gate source threshold voltage (logic level)
$R_{DS(ON)}$	–	12.3 mΩ	15 mΩ	Drain source on state resistance (T_J = 25°C)
C_{iss}	–	2440 pF	3170 pF	Input capacitance
$C_{rss(effective)}$	–	175 pF	–	Extracted from plot $C_{rss} = f(V_{DS})$ -> mean value
$V_{plateau}$	–	2.6 V	–	Extracted from plot $I_D = f(V_{GS})$ @ $I_{IN,max} + I_{OUT}$

Parameter	Min.	Typ.	Max.	comment
$R_{th(JA)}$	–	–	62 K/W	Thermal resistance from junction to ambient, minimal footprint

The OptiMOS™ –T2 power transistor IPD60N10S4L-12 offers sufficient drain source voltage capability which was calculated in Eq. 27. Furthermore a logic level device was selected due to the fact that the gate drive voltage sourced by the TLD5099EP is 5 V. For switching transistors the parasitic capacitances are very important because they determine the switching behavior. When choosing a higher value of $R_{DS(ON)}$ the parasitic capacitances usually reduce in value because less active area is needed. Thus a compromise between switching losses and conduction losses must be made when choosing the switching MOSFET. Another important factor is the thermal performance which is mostly influenced by the package of the device. All these parameters influencing the decision on choosing the MOSFET.

With following parameters of the OptiMOS™ –T2 power transistor IPD60N10S4L-12 the switching times can be approximated:

- R_G … 10 Ω
- C_{iss} … 3170 pF
- V_D… 5 V
- $V_{GS(IL)}$ … 2.6 V
- $V_{GS(TH)}$ … 2.1 V
- V_S … $V_{IN,min} + V_{OUT,max}$ = 35 V
- C_{rss} … 175 pF

$$t_{RI} = R_G * C_{iss} * \ln\left(\frac{V_D - V_{GS(TH)}}{V_D - V_{GS(IL)}}\right) = 10\,\Omega * 3170\,pF * \ln\left(\frac{5\,V - 2.1\,V}{5\,V - 2.6\,V}\right) = 2.8\,ns$$

$$t_{FV} = R_G * C_{rss} * \frac{V_S}{V_D - V_{GS(IL)}} = 10\,\Omega * 175\,pF * \frac{35\,V}{5\,V - 2.6\,V} = 26\,ns$$

$$t_{FI} = R_G * C_{iss} * \ln\left(\frac{V_{GS(IL)}}{V_{GS(TH)}}\right) = 10\,\Omega * 3170\,pF * \ln\left(\frac{2.6\,V}{2.1\,V}\right) = 3.2\,ns$$

$$t_{RV} = R_G * C_{rss} * \frac{V_S}{V_{GS(IL)}} = 10\,\Omega * 175\,pF * \frac{35\,V}{2.6\,V} = 24\,ns$$

Eq. 30

It can be seen that the current rise/fall times are much shorter than the voltage rise/fall times thus, the voltage rise/fall times have a higher contribution to the switching losses. With the known switching times the switching losses can be calculated using Eq. 31.

$$P_{Q,SW} = \left(V_{IN,min} + V_{OUT,max}\right) * \left(I_{IN,max} + I_{OUT}\right) * \frac{t_{RI} + t_{FV} + t_{FI} + t_{RV}}{2} * f_{SW} =$$
$$(8\,V + 27\,V) * (3.57\,A + 0.9\,A) * \frac{2.8\,ns + 26\,ns + 3.2\,ns + 24\,ns}{2} * 310\,kHz = 1.36\,W$$

Eq. 31

2.2.2.2 Conduction losses

Conduction losses can be calculated by multiplying the squared RMS current through the MOSFET with its $R_{DS(ON)}$. Since the $R_{DS(ON)}$ of a MOSFET increases with increasing temperature, the maximum $R_{DS(ON)}$ at maximum

junction temperature can be used for the calculation. The RMS current in the switching MOSFET can be calculated using Eq. 32.

$$I_{Q,RMS} = \sqrt{\frac{1}{T}\int_0^T I_{Q1}^2 * d_t} \approx \sqrt{\frac{1}{T} * \int_0^{D_{max}*T} \left(I_{IN,max} + I_{OUT}\right)^2 * d_t} \approx \left(I_{IN,max} + I_{OUT}\right) * \sqrt{D_{max}} \quad \text{Eq. 32}$$

$$I_{Q,RMS} \approx \left(I_{IN,max} + I_{OUT}\right) * \sqrt{D_{max}} = (3.57 + 0.9) * \sqrt{0.771} = 3.92\ A$$

The conduction losses can be calculated using Eq. 33.

$$P_{Q,C} = I_{Q,RMS}^2 * R_{DS(on),max} = 3.92^2 * 0.02 = 307\ \text{mW} \quad \text{Eq. 33}$$

The total losses found by analytical calculation can then be calculated using Eq. 34:

$$P_{Q,total} = P_{Q,C} + P_{Q,SW} = 0.307 + 1.36 = 1.67\ W \quad \text{Eq. 34}$$

2.2.2.3 Simulated losses

It can be concluded that the switching losses dominate the conduction losses. The calculations in Chapter 2.2.2.2 give an estimation of the total losses and show their influencing parameters. However, a practical approach would be to simulate the losses using SPICE simulation and the MOSFET simulation models provided by Infineon. Furthermore, here also reverse recovery losses can be included. Figure 21 shows the setup to simulate the losses in the switching MOSFET. The main components of the SEPIC power stage are modeled. The simulated circuit operates at following operating conditions:

- Approximately output power of 25 W
- Duty cycle of 77.1%
- Input voltage of 8 V
- Gate drive voltage of 5 V
- Gate drive sourcing current limited to 380 mA
- Gate drive sinking current limited to 550 mA
- Junction temperature of 120°C

These operating conditions represent a worst-case scenario. Furthermore, the current capability of the gate driver implemented in the TLD5099EP is also modeled.

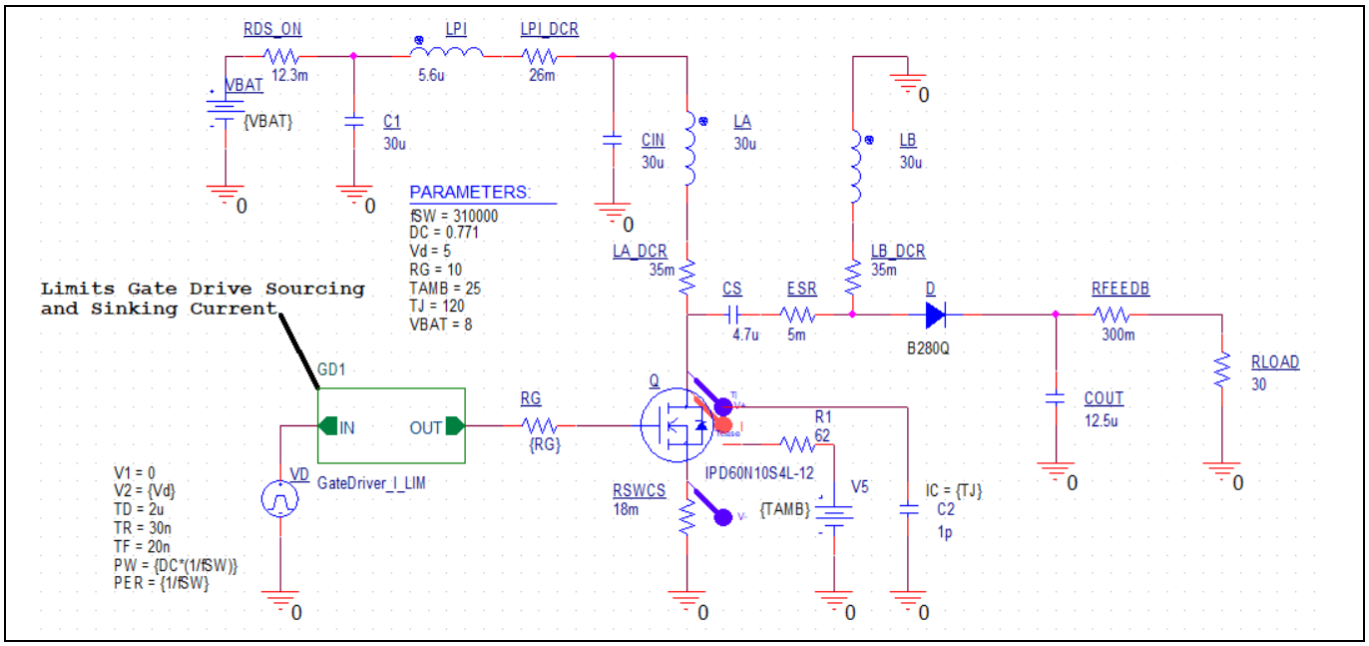


Figure 21 SPICE simulation setup for total losses in switching MOSFET

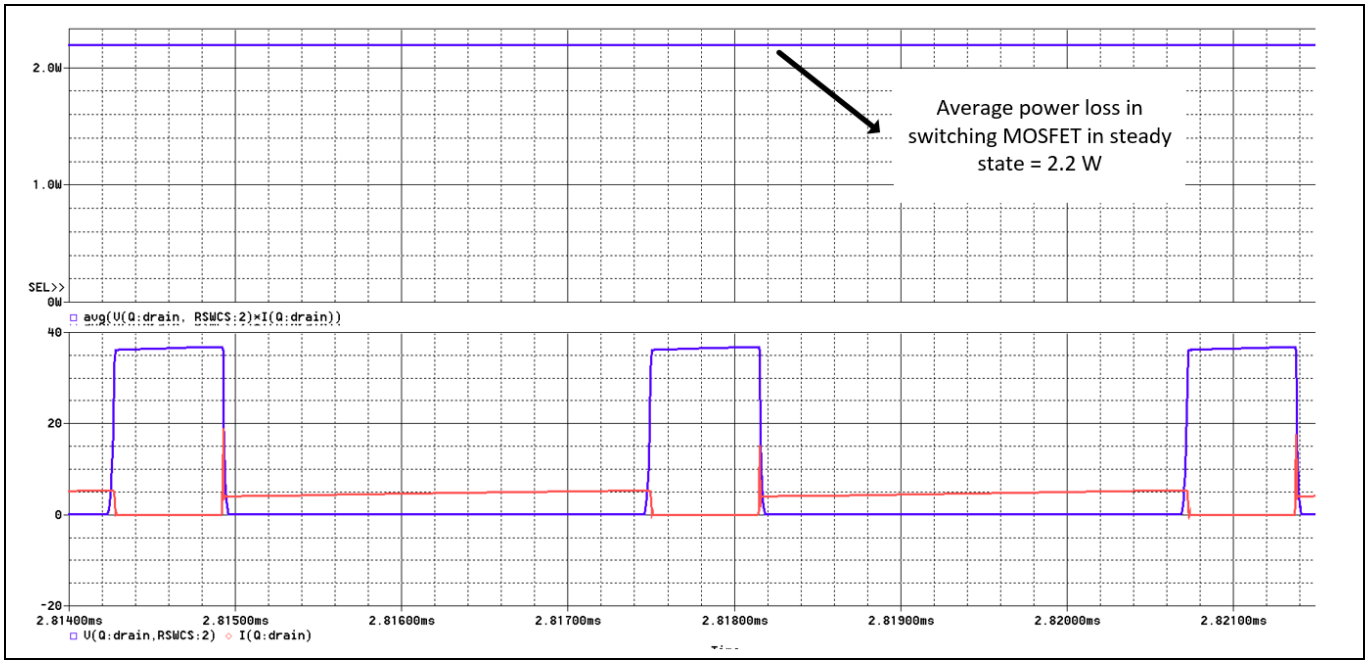


Figure 22 Simulated total losses in switching MOSFET

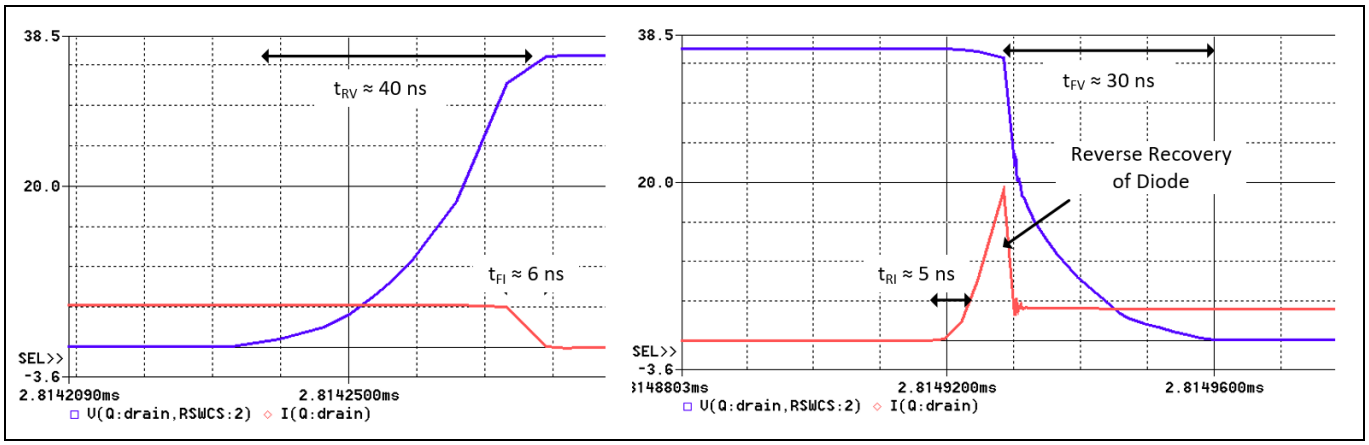


Figure 23 Simulated turn off and turn on transitions

It can be observed in Figure 22 that the simulated total losses are around 2.2 W which is around 0.5 W higher than the analytic calculated results.

This can be mainly explained due to:

- the nonlinear voltage slopes during transition which are due to the nonlinearity of the reverse transfer capacitance, which are assumed to be linear in the analytic switching losses calculation. This results in lower simulated losses than analytic calculated losses
- the included reverse recovery losses generated during turn-on of the MOSFET (t_{FV}) which can be clearly seen in Figure 23. These losses increase the simulated losses compared to the analytic calculation
- the difference in analytic and simulated switching times

2.2.2.4 Thermal considerations

To give a prediction of the thermal performance of the switching MOSFET one can monitor the junction temperature of the switching MOSFET in the simulation. However, this would lead to very long simulation times because the time constant of the thermal circuit is much greater than the switching activities. Another approach would be to use the average power dissipation in the device and use the thermal resistance parameters given in the datasheet to calculate a prediction of the temperature of the device. Thermal resistance in the system depends on a number of circumstances such as PCB layout, stackup, amongst others are namely, nearby components, ambient temperature however, it is still possible to do an estimation.

Usually derating strategies are applied when the input voltage or ambient temperature deviate from typical operating conditions of the module. Therefore, the total losses in the switching MOSFET for $V_{IN,typ}$ will be used for thermal calculations. Following the same approach for the simulations as depicted in Figure 21 the losses in the switching MOSFET for $V_{IN,typ}$ can be found to be 1.5 W. With a thermal resistance of 62 K/W, which is the maximum value for minimal footprint attachment to the PCB, an ambient temperature of 75°C, where typically derating starts to apply, the following junction temperature can be estimated.

$$T_{J,Q} = T_{AMB} + P_{Q,total} * R_{TH,JA,max} = 75\,°C + 1.5\,W * 62\frac{K}{W} = 168\,°C \qquad \textit{Eq. 35}$$

Although the calculated maximum junction is near the maximum junction temperature of the MOSFET which is 175°C, this is with worst-case thermal resistance without any additional cooling elements. Usually this application uses heatsinks thus will improve the thermal behavior.

2.2.3 Switching diode

The switching diode in the SEPIC topology faces high current and voltage stress as can be seen in the current and voltage waveforms in Figure 13. Peak current and voltage requirements can be calculated using equation Eq. 36.

$$I_{D,peak} = I_{IN,max} + I_{OUT} + \Delta I_L = 3.57\ A + 0.9\ A + 0.66\ A = 5.13\ A$$
$$V_{D,peak} = -\left(V_{IN,max} + V_{OUT,max}\right) = -(16\ V + 27\ V) = -43\ V \qquad \text{Eq. 36}$$
$$V_{D,peak,Trans} = -\left(V_{IN,Trans,max} + V_{OUT,max}\right) = -(35\ V + 27\ V) = -62\ V$$

For this design the high voltage switching Schottky diode B280Q from Diodes Incorporated was selected which comprises the following key parameters:

Table 7 B280Q high voltage Schottky diode parameters

Parameter	Min.	Typ.	Max.	Comment
V_R	–	80 V	–	Working peak reverse voltage
I_O	–	–	2.0 A	Average rectified output current
V_F	–	–	0.79 V	Forward voltage drop
T_J	-65°C	–	150°C	Operating temperature range

The average rectified forward current in the switching diode can be found by using Eq. 37.

$$I_{DAVG} = \frac{1}{T} * \int_{D_{max}}^{T} \left(I_{IN,max} + I_{OUT}\right) * d_t = \frac{1}{T} * \left(I_{IN,max} + I_{OUT}\right) * T * (1 - D_{max}) \qquad \text{Eq. 37}$$
$$I_{D,AVG} = \left(I_{IN,max} + I_{OUT}\right) * (1 - D_{max}) = (3.57 + 0.9) * (1 - 0.771) = 1.024\ A$$

The worst-case power loss in the diode can be calculated using the average rectified forward current times the maximum forward voltage drop of the diode:

$$P_D = I_{D,AVG} * V_D = 1.024\ A\ * 0.8\ V = 819\ mW \qquad \text{Eq. 38}$$

2.2.4 Input filter

The input filter in a switched mode power supply is usually required to pass EMC requirements, e.g. CISPR25 Class V limits, and is designed mainly to damp noise in the lower frequency range. The input filter design must already provide enough damping at the first harmonic of the switching frequency. As filter topology, the PI-filter structure is selected. To achieve best performance, the capacitance on each side of the filter structure should be distributed equally, which results in wider low impedant frequency range. The output capacitors of the PI-filter serves as input capacitors to the SEPIC power stage.

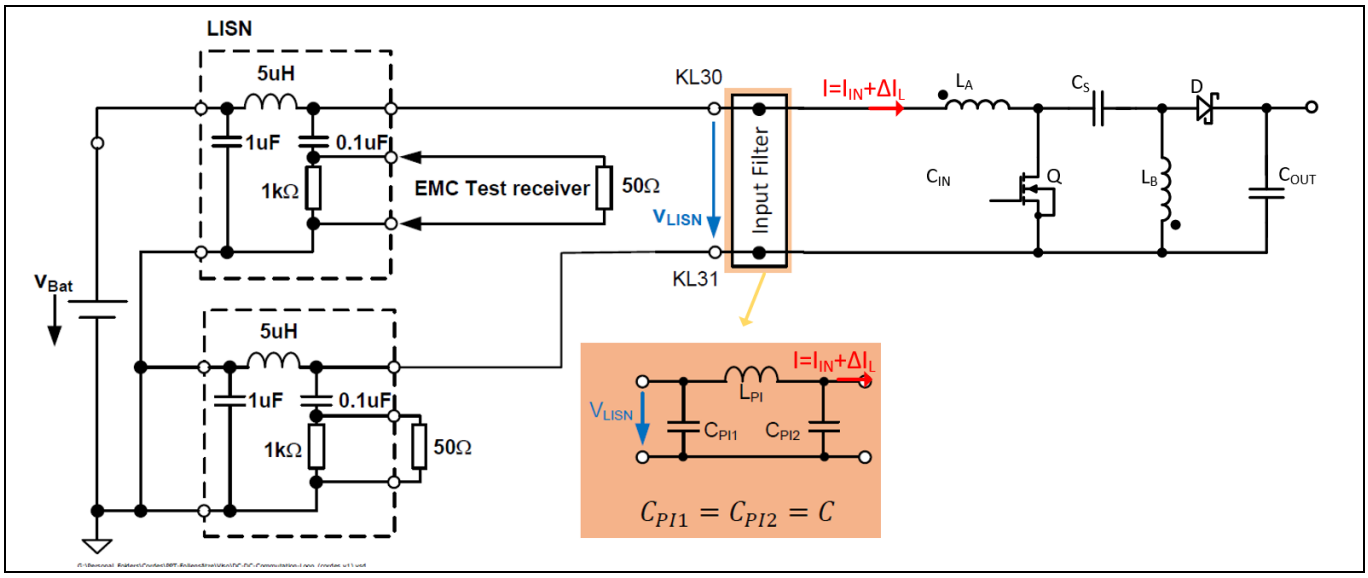


Figure 24 EMC measurement setup with input filter and LISN

Service / Band	Frequency MHz	Levels in dB(µV)														
		Class 5			Class 4			Class 3			Class 2			Class 1		
		Peak	Quasipeak	Average	Peak	Quasipeak	Average	Peak	Quasipeak	Average	Peak	Quasipeak	Average	Peak	Quasipeak	Average
BROADCAST																
LW	0,15 to 0,30	70	57	50	80	67	60	90	77	70	100	87	80	110	97	90
MW	0,53 to 1,8	54	41	34	62	49	42	70	57	50	78	65	58	86	73	66
SW	5,9 to 6,2	53	40	33	59	46	39	65	52	45	71	58	51	77	64	57
FM	76 to 108	38	25	18	44	31	24	50	37	30	56	43	36	62	49	42
TV Band I	41 to 88	34	–	24	40	–	30	46	–	36	52	–	42	58	–	48

Figure 25 Limits conducted emissions CISPR25

Figure 24 depicts EMC measurement setup with input filter and LISN. The AC part of the input current of the converter, which is the inductor current ripple ΔI_L, can be related to a voltage variation on the supply side of the PI-filter. This voltage variation is called V_{LISN}. This voltage variation is directly measured by the EMC receiver via the Line Impedance Stabilization Network (LISN). The relation between ripple current ΔI_L and the voltage variation at the EMC receiver V_{LISN} can be found by the filter impedance. The value V_{LISN} represents the limit at the first harmonic and must not be exceeded. In this design the specific standard CISPR25 is used. The limits for conducted emissions from components and modules are depicted in Figure 25. Since a switched mode power supply is a continuous and small band disturber the average and peak detector will measure approximately the same amplitude, thus the average limit must be applied since this is the lower limit. At the MW band starting at 530 kHz the limit for the average detector is 34 dBµV which is 50 µV which can be used as V_{LISN} for the calculations.

A step by step instruction for calculating the PI-filter elements is given:

1) Calculate input current ripple: → $\Delta I_L = 0.93\ A\ (@V_{IN,typ})$
2) Select value for PI-filter inductor, for example: → $L_{PI} = 5.6\ \mu H$
3) Calculate required minimum capacitance: $C = \sqrt{\frac{\Delta I_L}{V_{LISN}} * \frac{1}{\omega^3 * L_{PI}}} = \sqrt{\frac{0.93}{50\mu} * \frac{1}{(2*\pi*310000)^3 * 10\mu}} = 15.9\ \mu F$
4) Select next available capacitor: → $C_{PI} \geq C \rightarrow C_{PI} = 3x10\mu F \approx 30\mu F$
5) Calculate PI-filter resonance frequency: $f_{PI,res} = \frac{1}{2*\pi*\sqrt{\frac{L_{PI}*C_{PI}}{2}}} = \frac{1}{2*\pi*\sqrt{\frac{5.6\mu*30\mu}{2}}} = 17.3\ kHz$
6) Check that the resonance frequency of the PI-filter is at least 1 decade lower than the switching frequency: $\frac{f_{SW}}{f_{PI,res}} \geq 10 \rightarrow \frac{300k}{17.3k} \approx 17$
7) Verify filter behavior by emission test. If emission is above the limit line increase capacitor or inductor:
   → $L_{needed} = L_{existing} * 10^{\frac{\Delta dB}{20}}$ → $C_{needed} = C_{existing} * 10^{\frac{\Delta dB}{40}}$

$$Z_{Filter} = \frac{V_{LISN}}{\Delta I_L} \approx \frac{1}{-j\omega^3 C^2 L} \rightarrow C \approx \frac{1}{\sqrt{-j\omega^3 L * Z_{Filter}}} \approx \sqrt{\frac{\Delta I_L}{V_{LISN}} * \frac{1}{\omega^3 * L}} \quad \text{Eq. 39}$$

2.3 High beam activation, PWM dimming and output filter

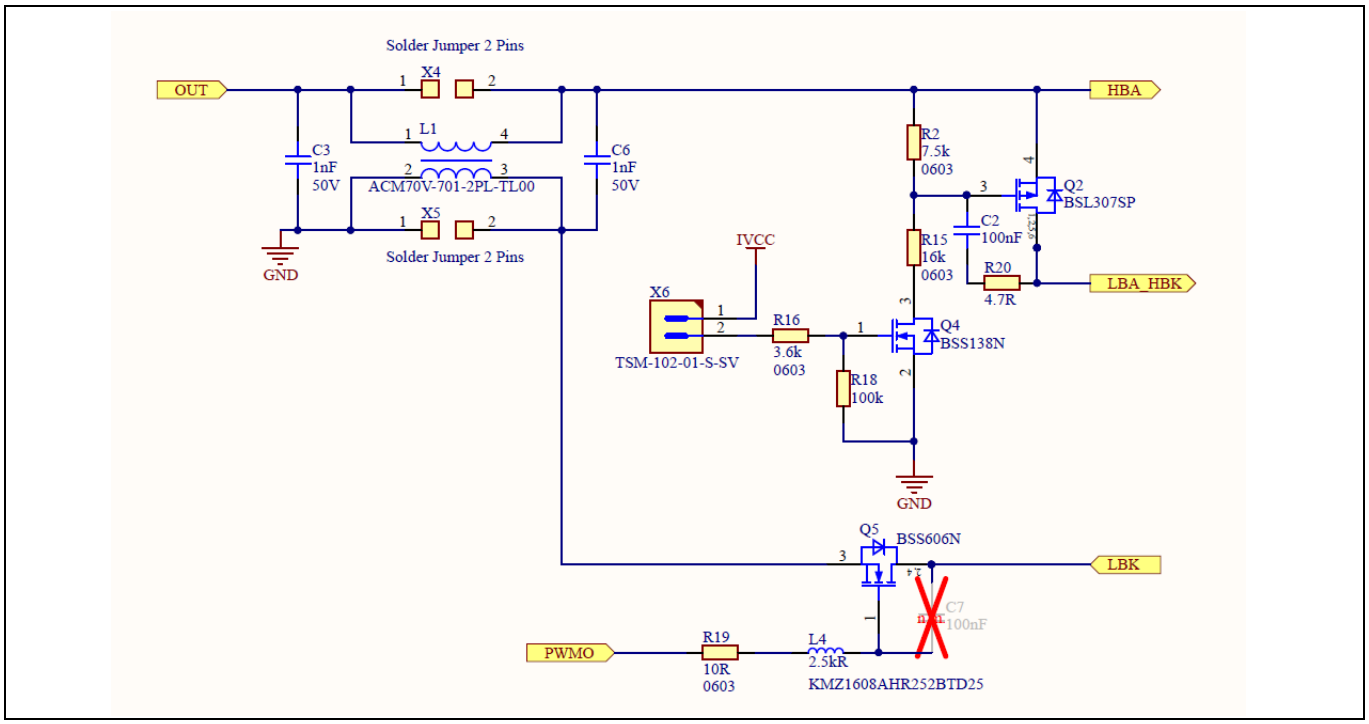


Figure 26 Schematic HB activation, PWM dimming and output filter

As already discussed, one DC-DC channel should drive two light functions, the HB and the LB. In a normal driving situation only the LB would be active. In certain situations, the HB is activated additionally. The activation is accomplished using a circuit given in Figure 26. When jumper X6 is open the small signal p-channel MOSFET BSL307SP Q2 is off since Q4 is not conducting, thus the high beam is activated because it is not

shorted by Q2. Vice versa, when the jumper X6 is closed, the HB turns off accordingly. The reverse transfer capacitance C_{rss} of Q2 is increased by placing an additional capacitor C2 between the gate and the drain of the device. This will increase the voltage rise and fall times to a couple of milliseconds to decrease current overshoot during the transient between activating and deactivating the high beam, see Figure 44. Q5 is used as PWM dimming MOSFET and is controlled by the TLD5099EP.

Furthermore, a CMC is used at the output to damp common mode noise originating mainly by capacitive coupling with the reference plane. The CMC is placed at the output since a lower current rating is required and therefore saves cost. The common mode and differential mode impedance of the CMC is depicted in Figure 27.

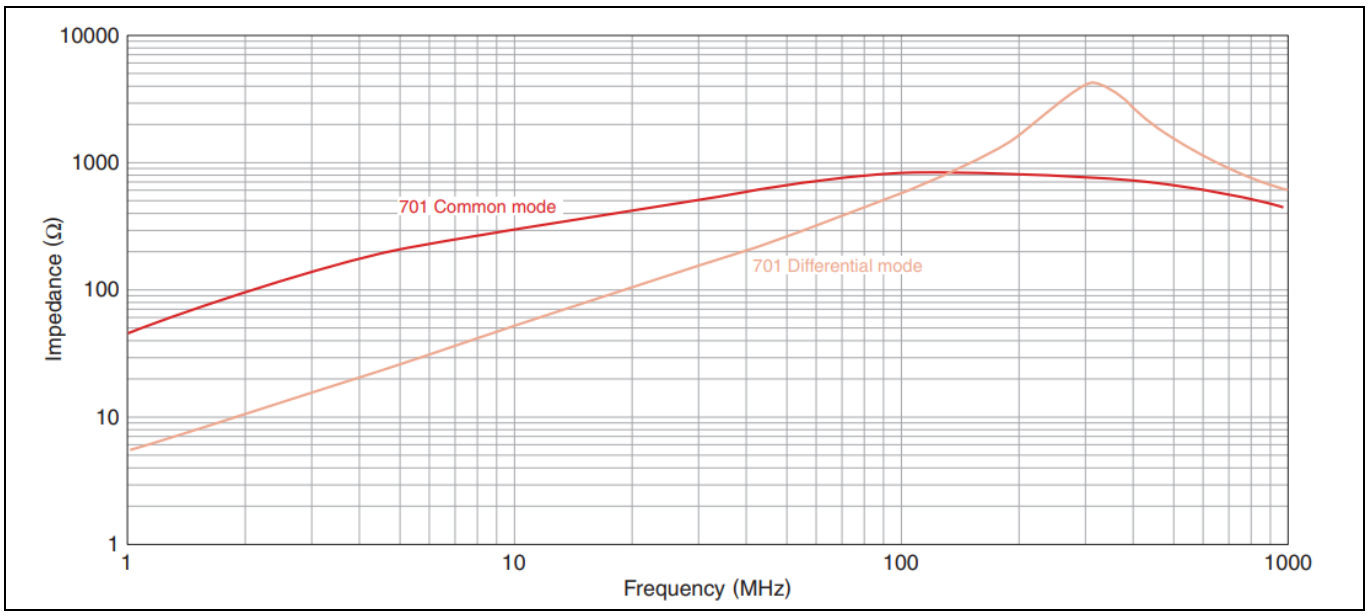


Figure 27 Common mode and differential mode impedance vs. frequency for ACM70V-701-2PL-TL00 [5]

2.4 Reverse polarity and input protection

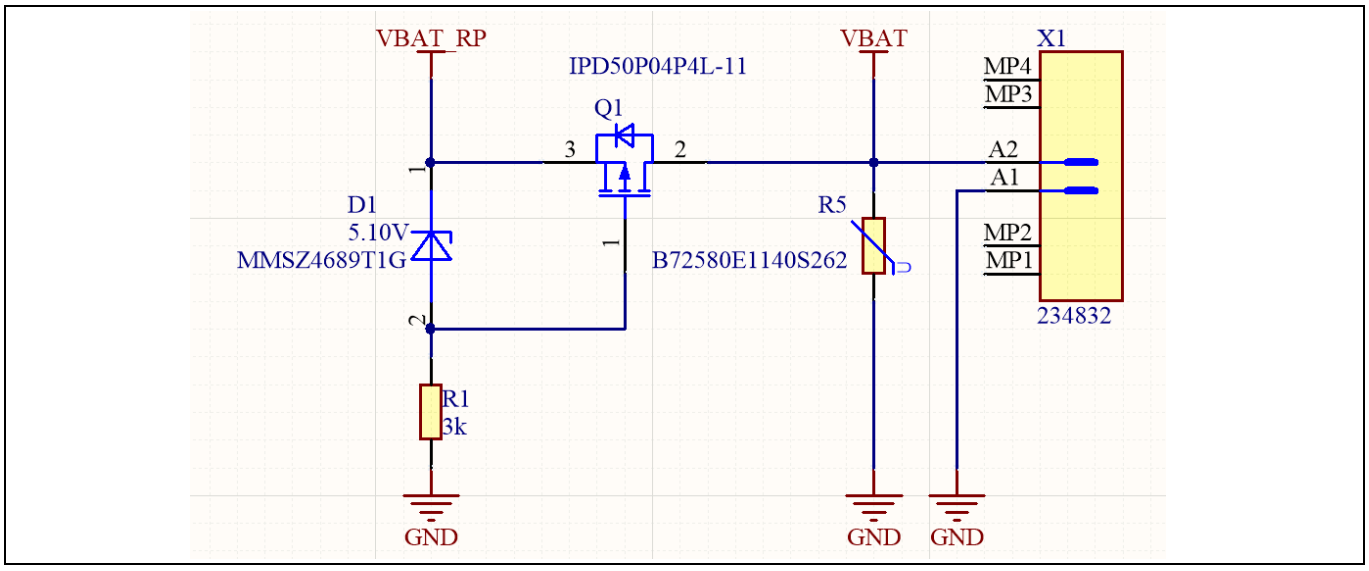


Figure 28 Reverse polarity and input protection circuit

Systems in the automotive environment face challenging requirements. Several international or OEM specific standards are in place, with which the system design needs to comply. The reverse polarity and input protection circuit protects the downstream electronics mainly against transients along the supply line. Figure 29 depicts some possible transients along the battery supply line. Depending on the specific standard or requirements of the OEM the size and shape of these transients vary.

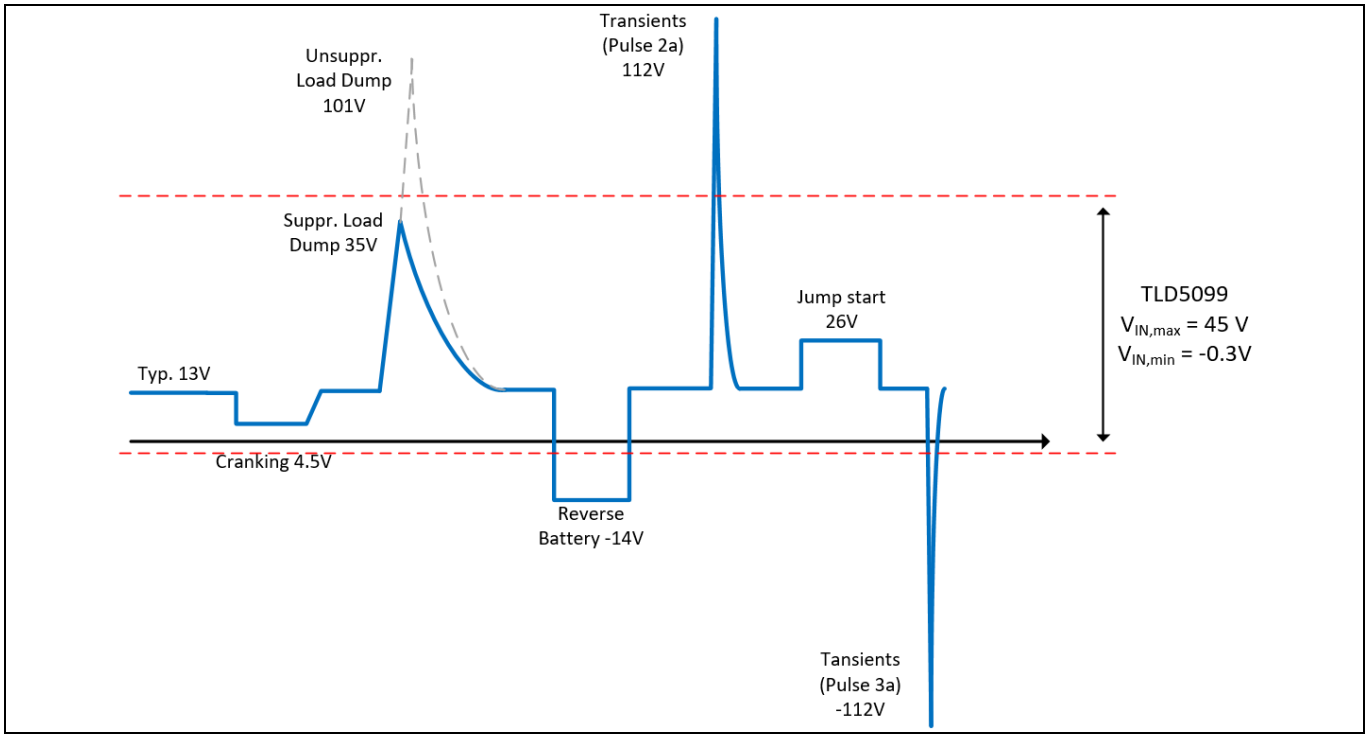


Figure 29 Transients along the supply line in an automotive battery supply

As an example, the maximum input voltage range of the TLD5099EP is marked. It can be seen that for reverse polarity; unsuppressed load dump and transients originating from inductive switching, that additional protection circuitry is necessary. However, the input filter will also damp these pulses to a certain degree. It can be concluded that for the reverse polarity case a protection circuit must be implemented, since this is a static case. For a possible unsuppressed load dump and transients due to inductive switching a TVS diode is typically used. The input protection therefore should ensure a maximum voltage present for the downstream electronics ranging from 0 V up to 40 V. The protection level of 0 V to 40 V originates from the present downstream electronic components' ratings with a safety margin. However, devices like the TLD5099EP can also withstand certain pulses without any additional protection.

2.4.1 Ceramic transient voltage suppressor

As input protection a CTVS from TDK (CT1812S14BAUTOG) got selected. These devices are voltage dependent resistors with a symmetrical V/I characteristic whose resistance decreases with increasing voltage. Connected in parallel with the electronic circuit that is to be guarded, the CTVS threshold value prevent any further rise in the transient overvoltage. The main advantages of CTVS are:

- No temperature derating up to 150°C
- Excellent surge current handling capability
- Low response time
- Bidirectional characteristic

Table 8 Important parameters CTVS CT1812S14BAUTOG

$V_{RMS,max}$	$V_{DC,max}$	W_{max}	W_{LD} (10 pulses)	$P_{diss,max}$	$V_{clamp,max}$
14 V	16 V	2400 mJ	6000 mJ	15 mW	40 V

Table 8 summarizes the most important parameters of the CTVS CT1812S14BAUTOG. A step by step explanation how to select the right CTVS is given in the following section based on a load dump pulse with a peak voltage of 35 V and a source impedance of 1 Ω.

Step 1) Maximum operating voltage $V_{RMS,max}$ and $V_{DC,max}$

To obtain a low protection level (clamping voltage), an operating voltage $V_{DC,max}$ close to the maximum operating voltage should be selected. Maximum DC operating voltage for this design is 16 V.

Step 2) Maximum surge current $I_{Surge,max}$

The maximum surge current in the device is dependent on the applied test pulse and the source impedance. Figure 30 depicts the transformation of the surge pulse.

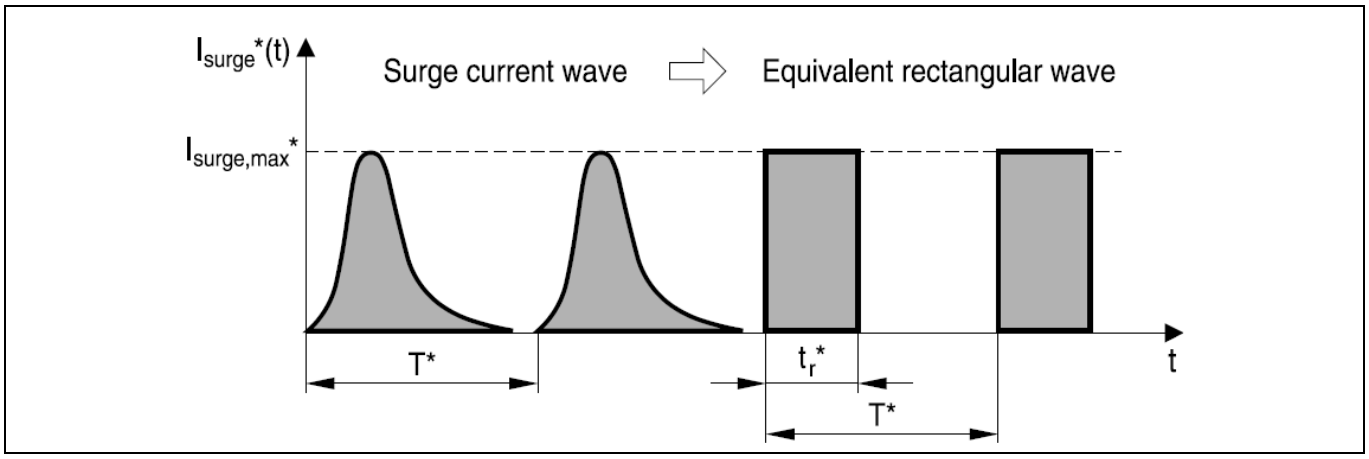


Figure 30 Equivalent rectangular surge current

A practical approach to determine the equivalent rectangular wave for a specific transient pulse would be a SPICE simulation, where TDK provides simulation models for the CTVS.

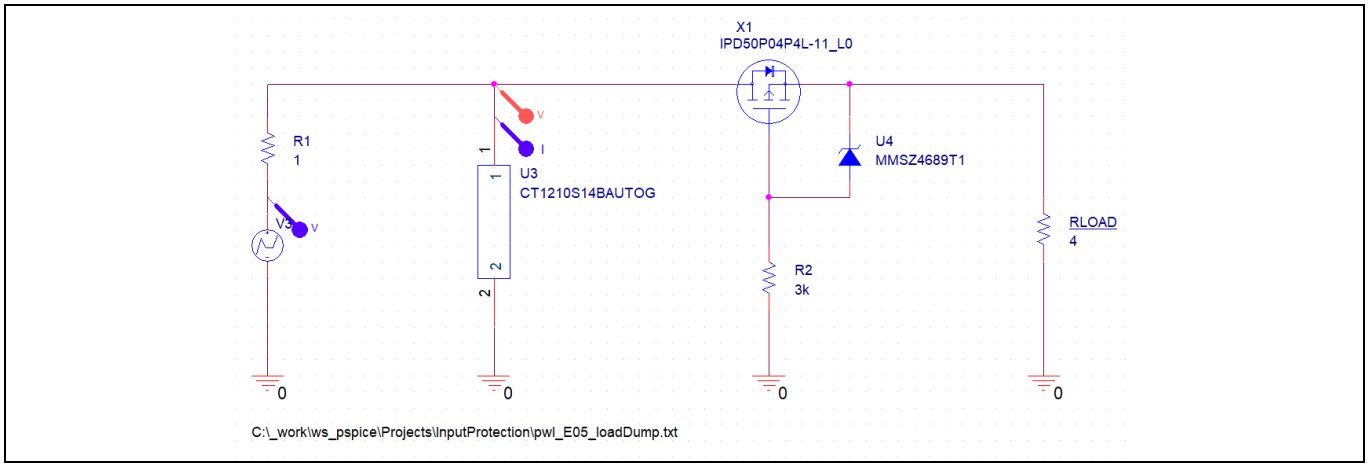


Figure 31 SPICE simulation reverse polarity and input protection

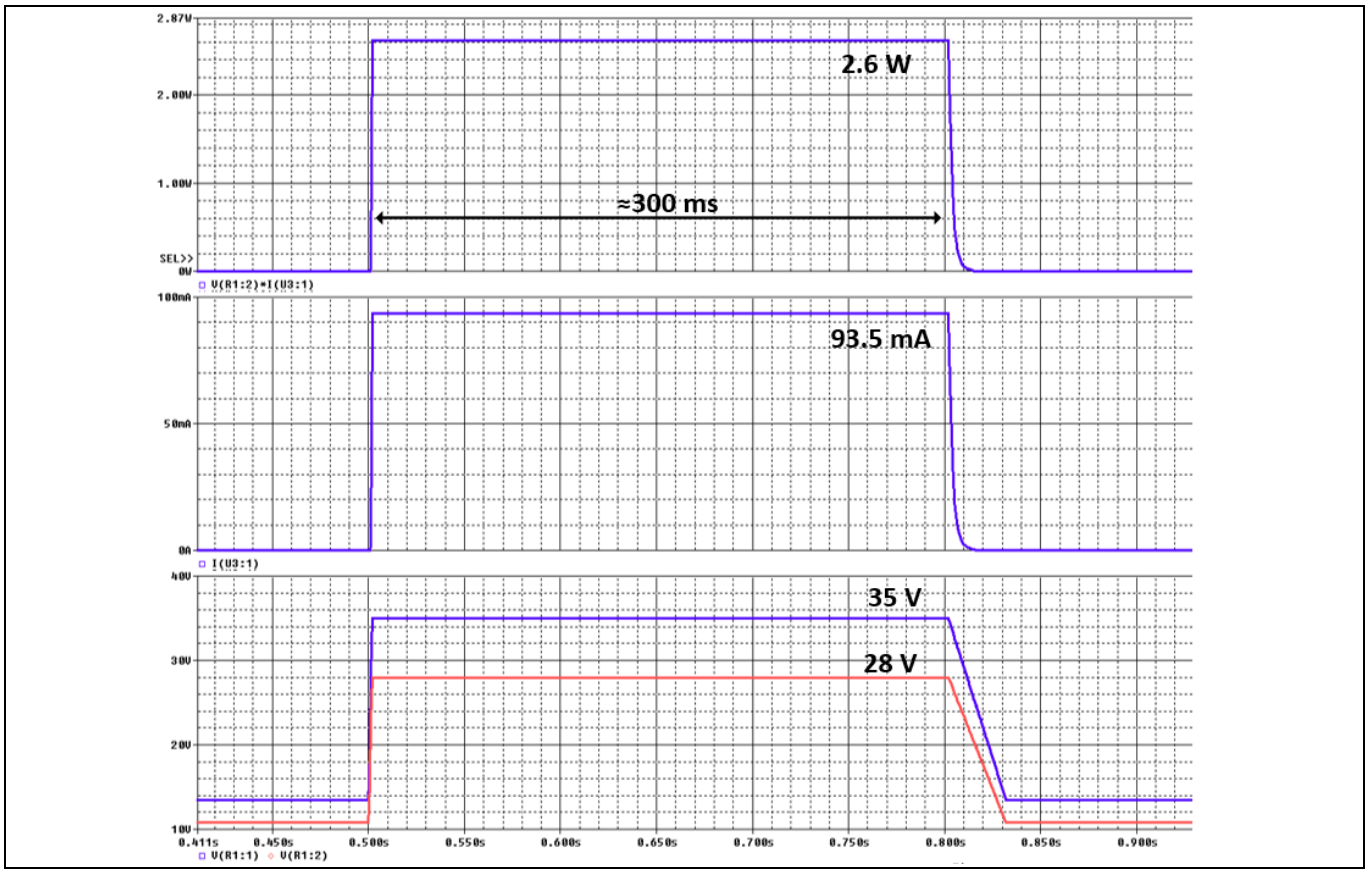


Figure 32 CTVS surge current for a load dump pulse with 35 V peak voltage

Figure 32 depicts the simulation results for the surge current of a load dump pulse with a peak voltage of 35 V and a source impedance of 1 Ω for the chosen CTVS (CT1812S14BAUTOG). It can be seen that for this test pulse the surge current is approximately in a rectangular shape and therefore needs no transformation. From the simulation $I_{Surge,max}$ = 93.5 mA and t_r = 300 ms can be determined.

When the equivalent rectangular wave is known (t_r and $I_{surge,max}$) a graph is given from which the maximum ratings can be seen which is shown for the chosen CTVS (CT1812S14BAUTOG) in Table 8. Although the time scale ends at 10 ms one can interpolate up to 300 ms and conclude that 93.5 mA will be below the maximum rating.

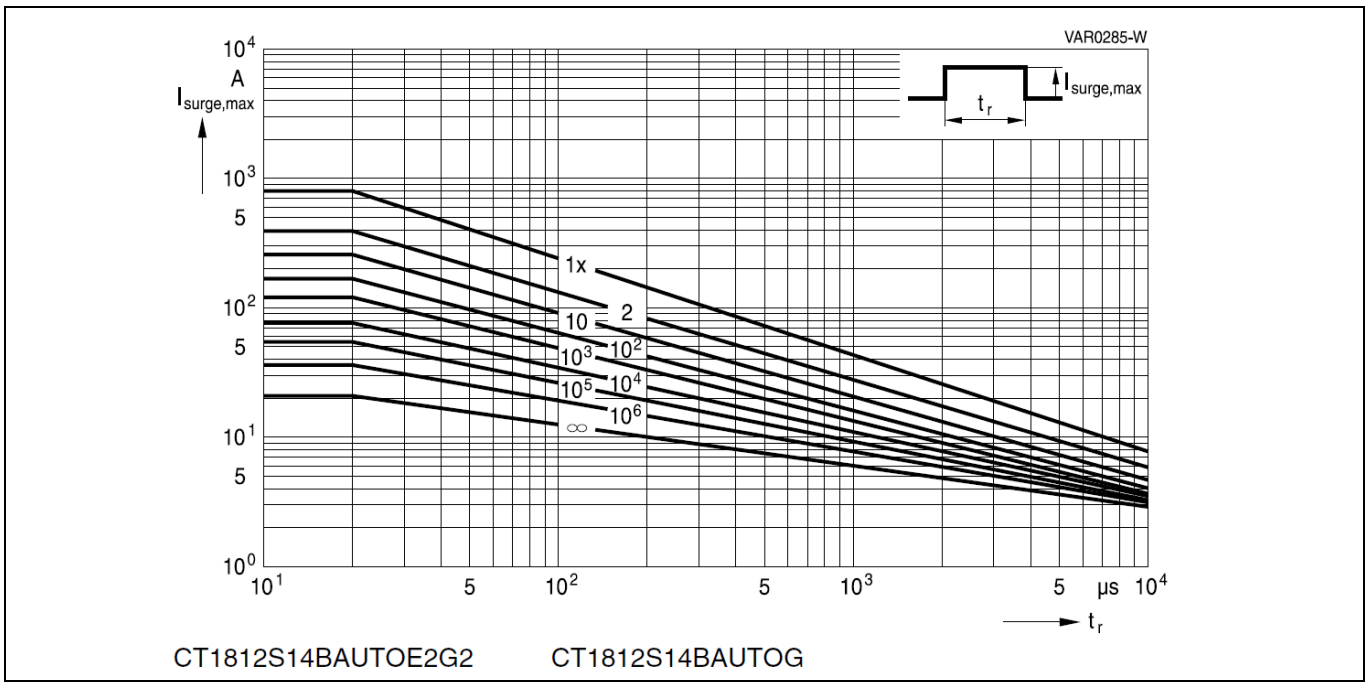


Figure 33 CTVS surge current vs. surge time

Step 3) Maximum energy absorption W_{max}

When a surgent current flows there will be energy absorption in the CTVS. The amount of energy to be absorbed can be calculated by Eq. 40.

$$W = \int_{t_0}^{t_1} v(t) * i(t) * dt \qquad \textit{Eq. 40}$$

From the simulation the energy absorption in the CTVS can be found. The absorbed energy must be smaller than W_{max} given in Table 8.

$$W = 2.6\,W * 300\,ms = 780\,mJ \leq W_{max} \qquad \textit{Eq. 41}$$

Step 4) Average power dissipation $P_{diss,max}$

If a periodic energy absorption is present at the CTVS, an average power dissipation can be calculated using Eq. 42, which is not the case for the load dump pulse.

$$P_{diss} = \frac{V_{surge} * I_{surge} * t_r}{T} \leq P_{diss,max} \qquad \textit{Eq. 42}$$

Step 5) Maximum protection level (clamping voltage) $V_{clamp,max}$

The maximum possible voltage rise in the event of a surge current is checked by simulation or with V/I curves as depicted in Figure 34. By simulation, a clamping voltage for the load dump pulse of 28 V can be observed.

Higher voltage transients will increase the surge current and therefore also the clamping voltage although they usually incorporate much less energy.

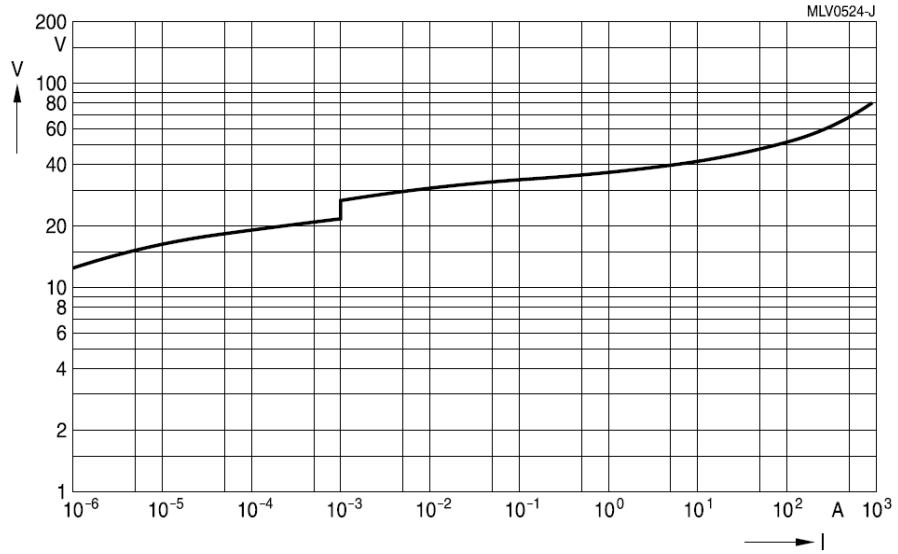


Figure 34 CTVS V/I curves to determine clamping voltage

2.4.2 Reverse polarity protection

The implemented reverse polarity protection is based on the OptiMOS™ –P2 P-channel power transistor IPD50P04L-11. Table 9 summarizes the most important parameters of the power transistor.

Table 9 IPD50P04L-11 OptiMOS-P2 P-channel power transistor parameters

Parameter	Min.	Typ.	Max.	Comment
V_{GS}	-16 V	–	+ 5 V	Maximum gate source voltage
V_{DS}	-40 V	–	–	Drain source breakdown voltage
T_J	-55°C	–	175°C	Operating temperature range
$V_{GS(TH)}$	-1.2 V	-1.7 V	-2.2 V	Gate source threshold voltage (logic level)
$R_{DS(ON)}$	–	12.3 mΩ	17.2 mΩ	V_{GS} = -4.5 V, I_D = -30 A
$R_{th(JA)}$	–	–	40 K/W	Thermal resistance from junction to ambient

Related to Figure 28, the Zener diode D1 gets forward biased in a reverse polarity situation and therefore turns off the MOSFET since a positive V_{GS} is applied which is the forward voltage drop of D1. In reverse polarity, the approximate value of the reversed input voltage is present over the drain source channel of Q1. The breakdown voltage of the drain source channel is -40 V as given in Table 9. Thus, every increase above -40 V will lead to an avalanche breakdown. However, since the CTVS is bidirectional and if it is assured that the clamped voltage for every transient input pulse does not exceed -40 V, Q1 is protected. In normal operation, a negative V_{GS} is applied by the Zener voltage of D1, thus turning on Q1.

The worst-case losses in the reverse polarity MOSFET Q1 can be calculated using Eq. 43. Considering the worst-case losses, thermal considerations can be neglected.

$$P_{RP} = I_{IN,max}^2 * R_{DS(ON)} \approx 3.57^2 * 17.2\,m\Omega = 219\,mW \qquad \textit{Eq. 43}$$

2.5 Layout considerations

2.5.1 Layer stackup

The layer stackup is depicted in Figure 35. It is a two-layer design where the bottom layer serves as a common GND plane and the top layer is used as a routing layer.

Board Stack Report

Stack Up		Layer Stack			
Layer	Board Layer Stack	Name	Material	Thickness	Constant
1		Top Paste			
2		Top Overlay			
3		Top Solder	Solder Resist	0,020mm	3,5
4		L1_Top	Copper	0,071mm	
5		Dielectric	Core-FR4	1,476mm	4,5
6		L2_Bot	Copper	0,071mm	
7		Bottom Solder	Solder Resist	0,020mm	3,5
8		Bottom Overlay			
9		Bottom Paste			
	Height : 1,658mm				

Figure 35 Layer stackup

2.5.2 General recommendations

General recommendations for a good layout are listed below and focus mainly on EMC performance and signal integrity:

- **Use only one common GND plane**
  - As far as possible, avoid splits and discontinuities in the GND plane as much as possible
  - Place vias not too close to each other so that no slot in the GND plane arises
  - If routing on the GND plane is necessary, try to reduce the trace length/slot as much as possible
- **Control return currents**
  - For frequencies of around > 10 kHz the return current follows the path of least impedance
  - This is usually directly underneath the signal trace if no discontinuity is present
  - For higher frequency signals provide a short signal path with no discontinuities in the return path
- **Keep all current loops with high di/dt as small as possible**
  - This will reduce the parasitic loop inductance and therefore differential mode radiation
- **Keep all areas with high dv/dt as small as possible**
  - This will reduce the parasitic capacitance and therefore common mode noise due to capacitive coupling

- **Avoid vias/layer changes in high frequency signals as far as possible**
  - This reduces the loop inductance
- **Provide a return current path if a layer change is necessary**
  - Mainly important for multilayer PCBs
  - Place stitching vias or place stitching capacitors (not so effective in the higher frequency range, mainly dependent on the package size)
- **Place all connectors to the PCB close together, e.g. on one side**
  - This avoids possible common mode radiations by reducing GND shift between connectors
- **Do not route signals underneath power inductors**
  - This avoids coupling of electromagnetic energy into signals

Figure 36 shows the GND layer in blue. A solid GND plane is ensured with two short signal routings which were necessary but kept as small as possible and do not discontinue high frequency signal return paths. One can also clearly see that the GND plane is not placed underneath the output CMC which violates the above-mentioned recommendation. However, this has the reason that higher frequency common mode noise cannot bypass the CMC by parasitic capacitive coupling which usually starts at around 30 MHz and upwards.

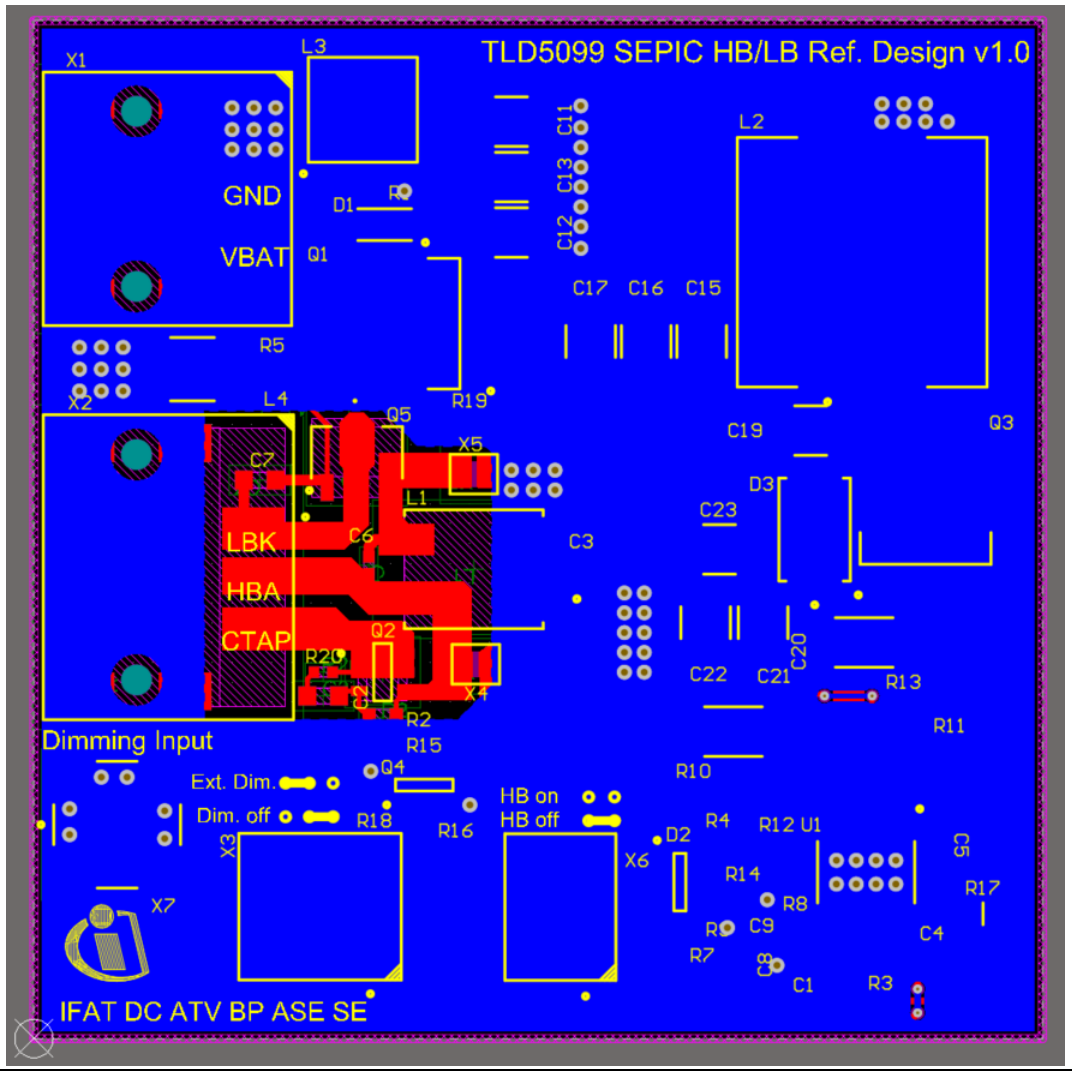


Figure 36 Layout GND layer

2.5.3 Power stage and input filter

The power stage and input filter are by far the most critical sub circuits when it comes to layout for EMC and thermal performance, thus special care has to be taken. Especially in the power stage the tradeoff between thermal and EMC performance becomes most obvious. Here thermal performance would require to separate the components and use large copper planes to maximize cooling effects. However, EMC performance usually requires the exactly opposite with closely arranged components and small copper planes. Figure 37 depicts the critical di/dt loops and dv/dt nodes.

The most critical di/dt loop is the current commutation loop formed by R13, Q3, C19, D3 and the output capacitors C20, C21, C22 and C23. The second di/dt loop where attention is required is the input loop formed by R13, Q3, L2 and input capacitors C17, C16, C15. The input loop is not as critical as the commutation loop because the current is kept fairly constant due to the inductance involved (can be also seen in Figure 13), therefore reducing di/dt. Especially when it comes to the commutation loop the loop size needs to be as small as possible and a solid GND plane should be placed underneath it. Furthermore, high dv/dt nodes can be identified by SWN1 and SWN2. These nodes need to be as small as possible for good EMC performance. However, especially VSWN1 is also important for thermal aspects because it is the drain connection of the switching MOSFET Q3. In the datasheet of the MOSFET a maximal thermal resistance $R_{TH,JA}$ of 40 K/W is given for a 6 cm² cooling area on the drain connection and 62 K/W is given in case only the minimal footprint is used. Clearly this layout does not provide 6 cm² copper area for the drain connection and is therefore optimized for EMC performance.

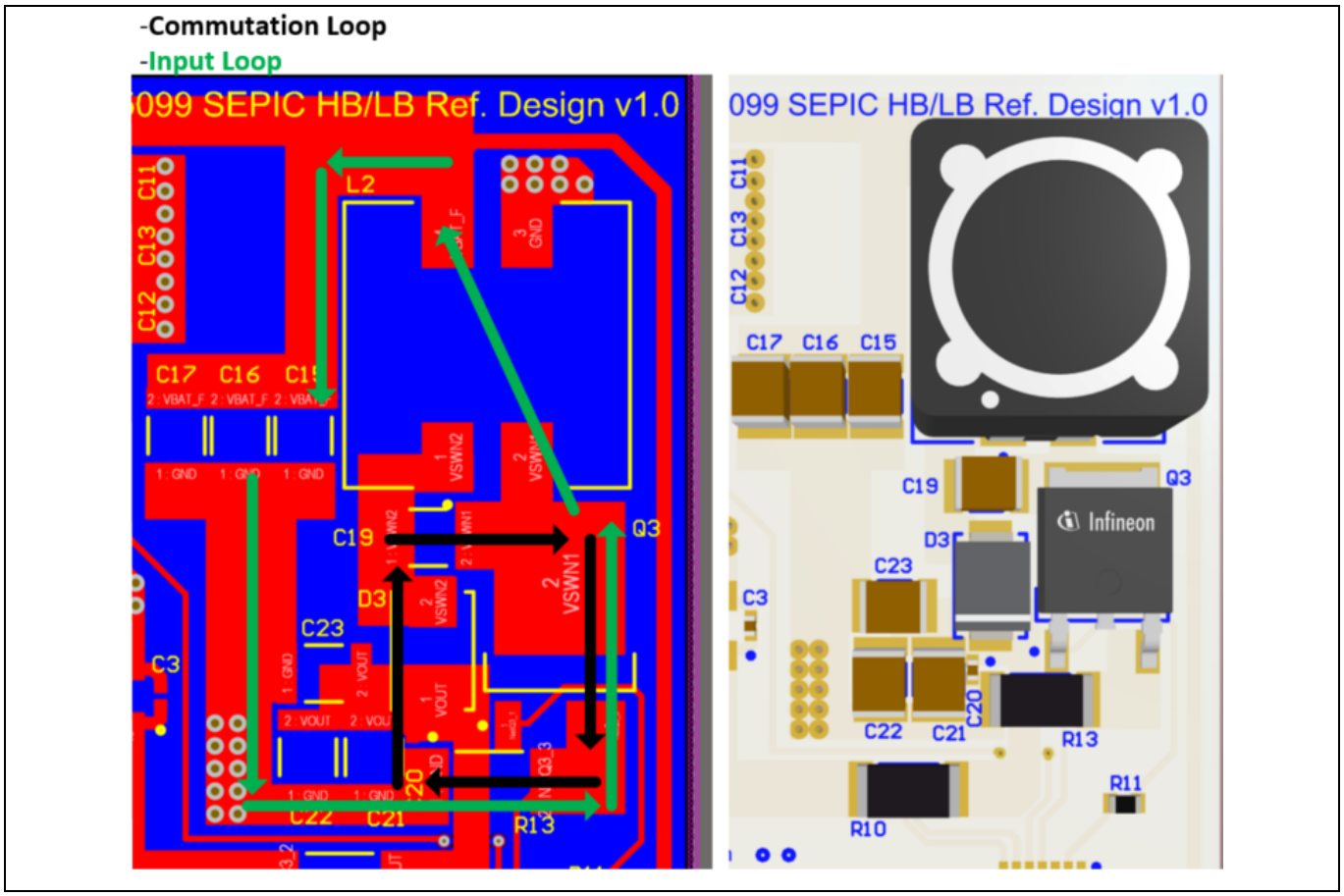


Figure 37 Layout power stage

Another layout design hint for the input filter arrangement is that the distance between the main coupled inductor and the input filter inductor should have around two times the diameter of the main coupled inductor. This ensures low mutual coupling between these two components. See Figure 38.

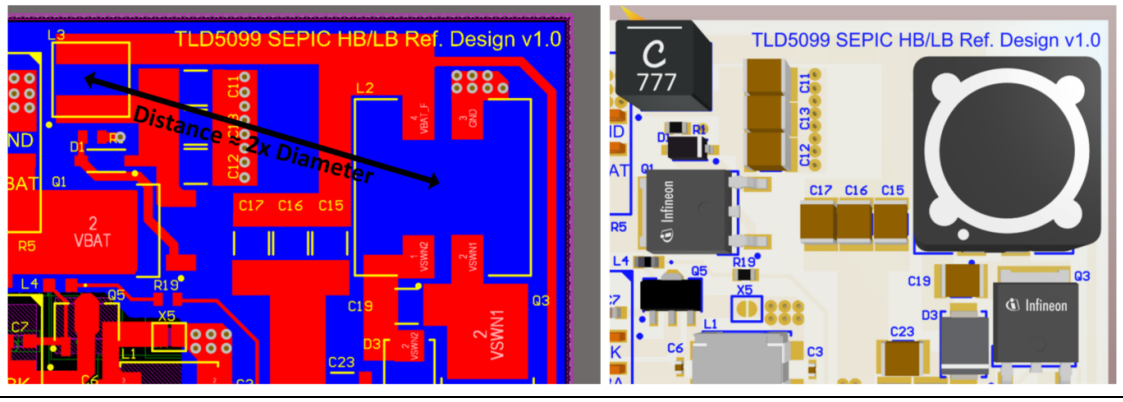


Figure 38 Distance between power inductors

2.5.4 TLD5099EP

The most critical signals regarding the layout of the TLD5099EP are the gate signal of the switching MOSFET Q3, the current sense signal of the output current shunt R10 and the placement of the decoupling capacitors. The gate signal is routed without any layer change and with a solid GND plane underneath it to provide a good current return path. The current sense feedback of the output shunt is done as a differential pair with a small length and without any layer change providing low inductance and good signal integrity. The decoupling capacitors C4 and C5 are placed very close to their respective pins to provide a low inductance power source. The compensation network components C9 and R8 are also placed near to their respective pins. Furthermore, thermal vias are placed in the exposed pad of the TLD5099EP providing a good thermal conductivity to the GND plane to decrease self-heating.

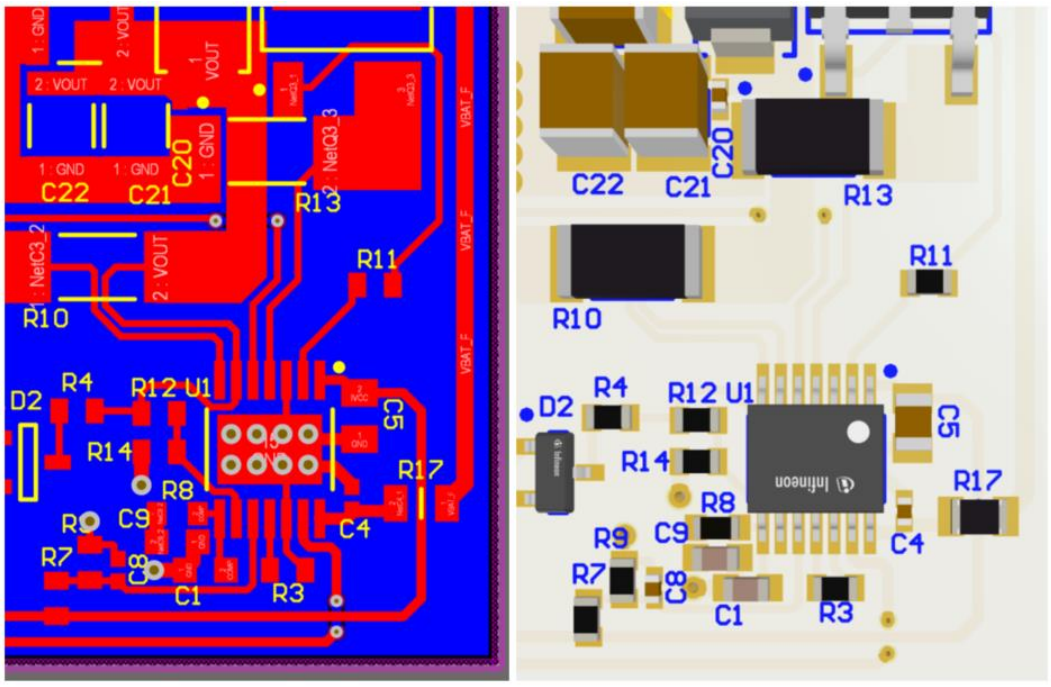


Figure 39 Layout TLD5099EP

3 System performance

As the system design was introduced in the previous chapter, now the system performance is discussed based on measurement results on the actual system. Besides the basic performance view, some transient immunity tests are performed.

3.1 General operating characteristics

The voltage and current measurement points for the general operating characteristics are shown in Figure 40. Voltages are measured with respect to GND.

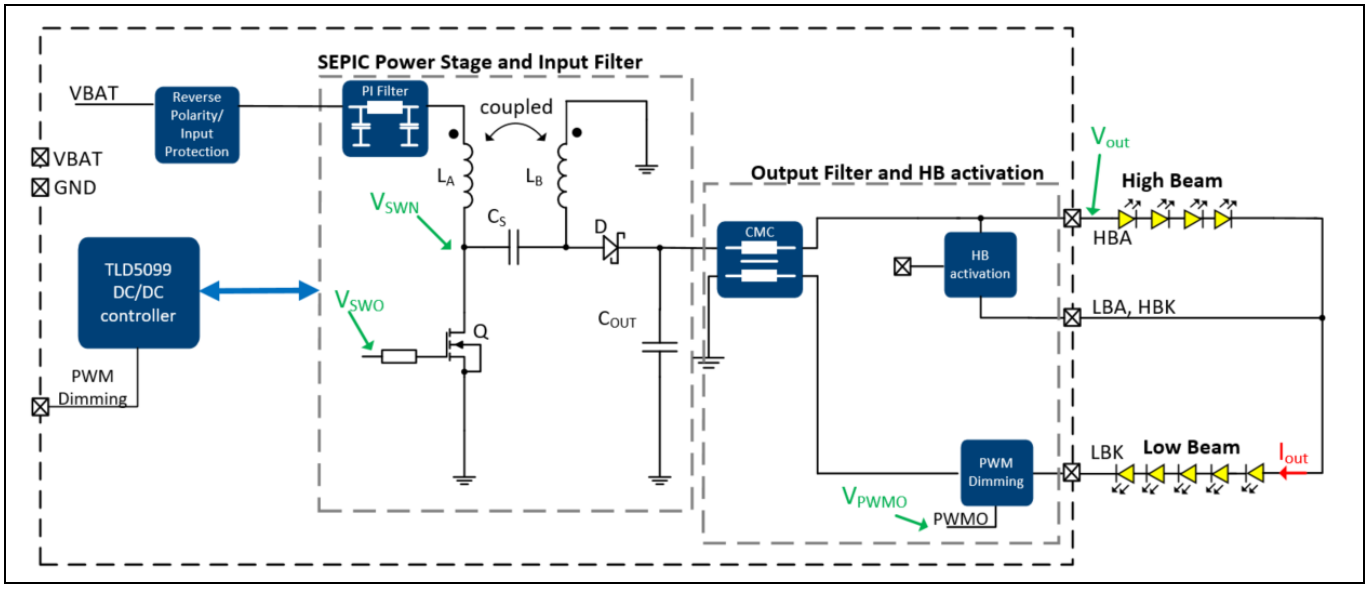


Figure 40 Voltage and current measurement points

The following setup is used in the documented test results.

- V_{BAT} = 13 V
- Compensation network = 68 nF
- CMC active
- Gate resistance 10 Ω
- Spread spectrum activated
- HB activated

3.1.1 Output voltage and current

With activated high beam, an output voltage of 27 V can be measured. The output current is regulated to around 900 mA. Figure 41 shows the output current and voltage with activated high beam. A current ripple of 50 mA can be observed which is due to the output voltage ripple caused by the switching frequency as discussed in Chapter 2.2.1. Furthermore, a low frequency ripple caused by the spread spectrum feature is seen.

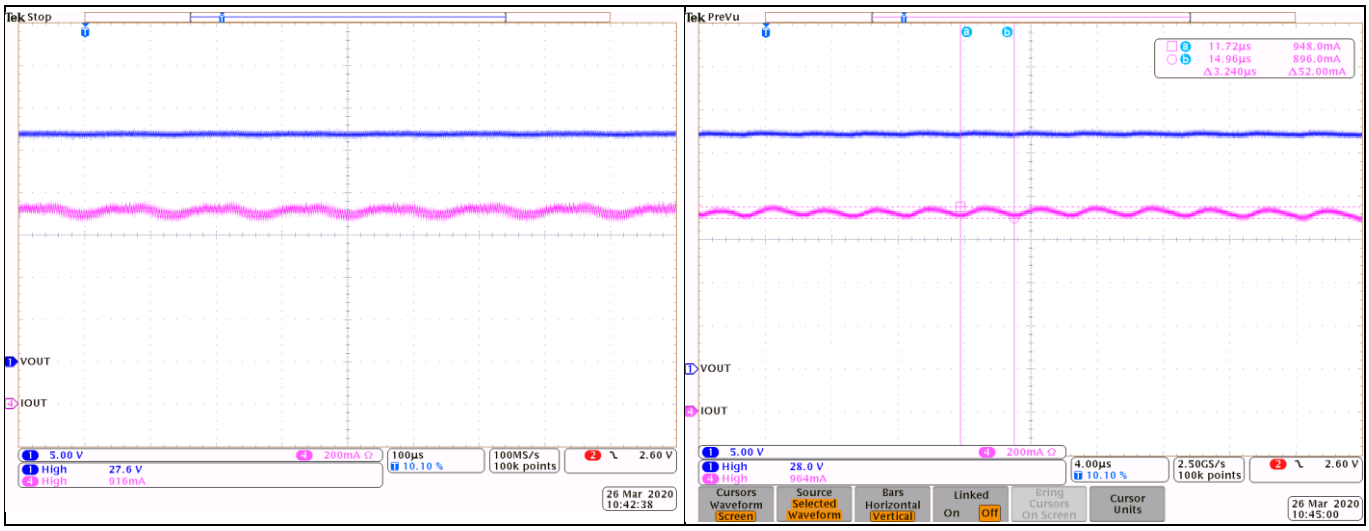


Figure 41 Output voltage and output current with HB on

3.1.2 Switching node

The switching node waveforms are shown below in Figure 42. The switching node voltage amplitude is approximately the sum of the input voltage plus output voltage. Due to the spread spectrum feature, the measured switching frequency deviates from the calculated one.

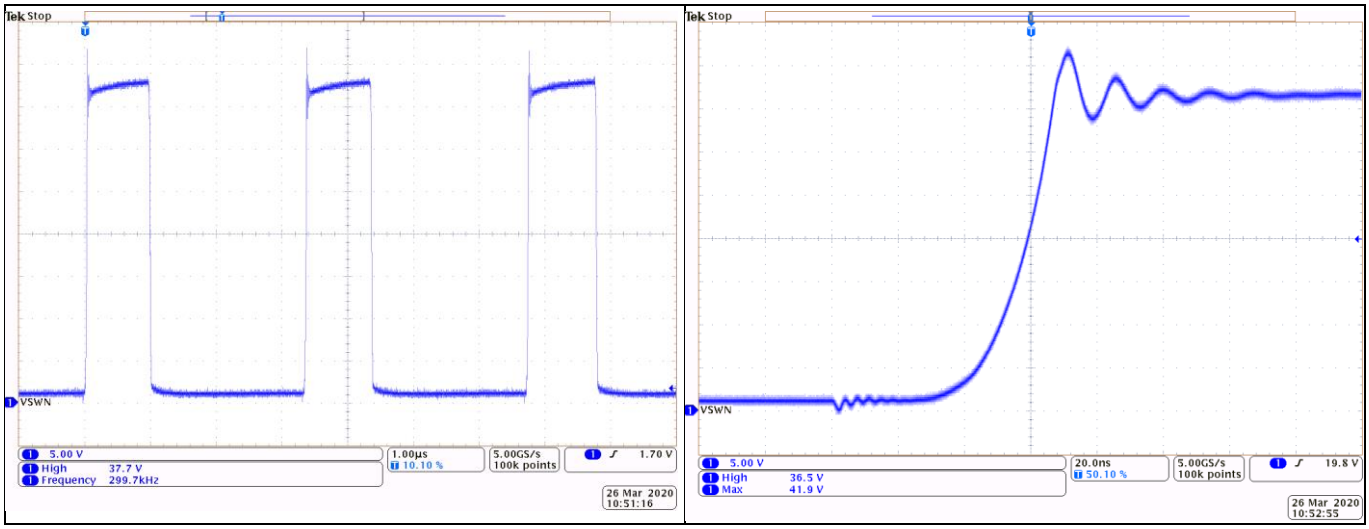


Figure 42 Switching node with HB on

3.1.3 PWM dimming

Figure 43 depicts the condition when PWM dimming is used. A dimming frequency of 500 Hz and a duty cycle of 50 % is used. It can be seen that the switching MOSFET as well as the PWM MOSFET is turned off when PWM dimming is active.

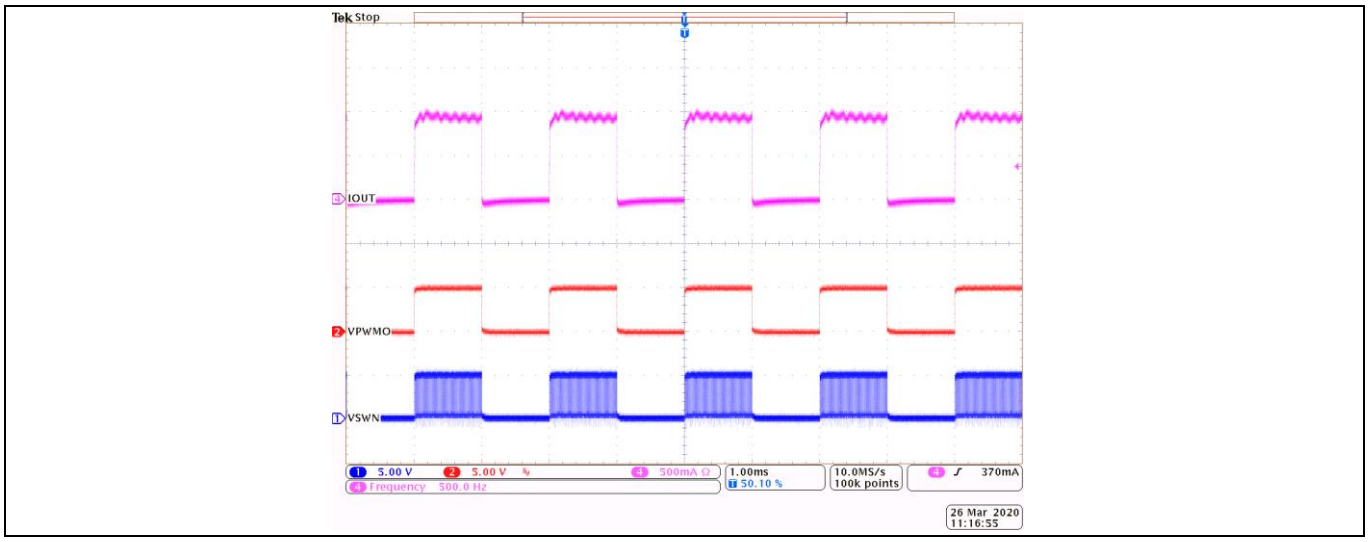


Figure 43 PWM dimming with 50% duty cycle

3.1.4 High beam activation

During the activation and deactivation of the high beam, the output load and consequently the output voltage changes. This change can cause a current overshoot in the LED string if the voltage slew rate is too fast. Especially when switching the high beam off, the output transition is done from a higher output voltage to a lower value. Therefore, the stored charge in the output capacitors can cause a current overshoot and thus must be reduced slowly. As discussed, the transition time should be in the order of milliseconds as a good reference. Figure 44 depicts a turn-on and turn-off transition of the high beam. During turn-off, a current overshoot with a peak value of 1.09 A can be observed which is in an acceptable range.

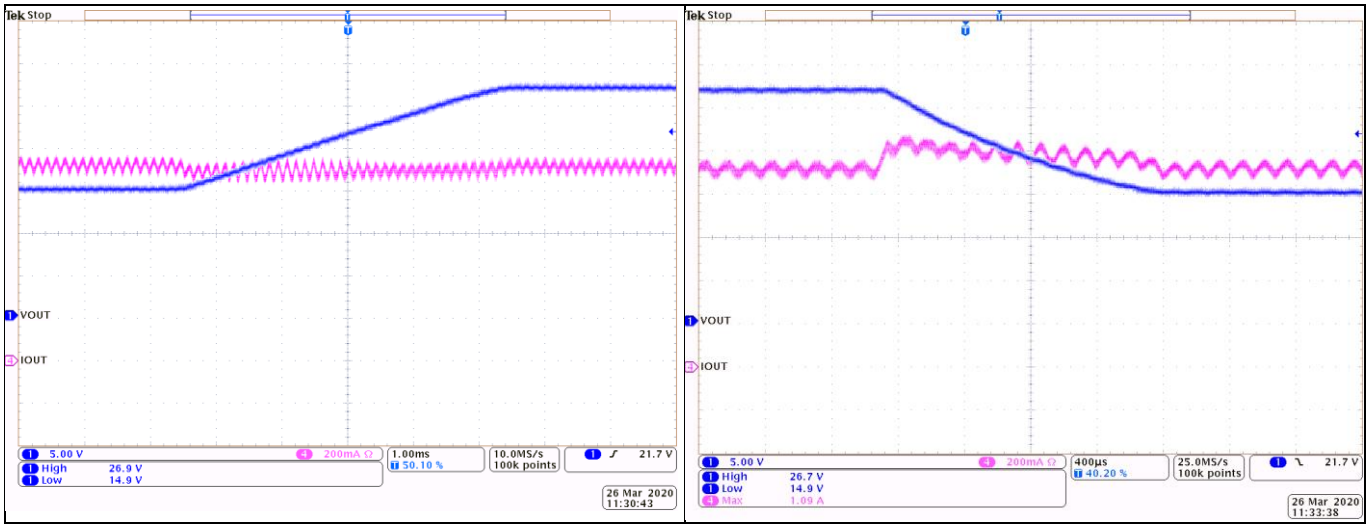


Figure 44 High beam activation and deactivation

3.2 Transient immunity

The following tests will provide a brief understanding of the transient immunity capabilities of the system. As introduced in the design specification, the below tests will be performed:

- Jump start
- Load dump
- Start pulses

During these tests, the PWM dimming function is inactive, while the high-beam is turned on. Whether a test is passed or failed is evaluated based on the “functional state”. In the above given test list, the following requirements are relevant:

- **Functional state A**
  The system fulfills all functions within the specified tolerances
- **Functional state B**
  The system fulfills all functions, tolerances can be violated during the exposure but must return to specified values after the exposure.
- **Functional state C**
  The system does not fulfill all functions during the exposure. Afterwards, the system must immediately return to functional state A automatically. Undefined functions are not permissible at any time

3.2.1 Jump start

This pulse simulates the external supply to a vehicle. The maximum voltage level is related to the electric-system voltages of commercial vehicles. In Table 10, the definition of the test pulse is given.

Table 10 Jump start test pulse parameters

Expected result	**Functional state C**		
Parameters	V_0	0	V
	V_1	3	V
	V_2	10.8	V
	V_3	26	V
	t_1	1	s
	t_2	0.5	s
	t_3	5	s
	t_4	1	s
	t_5	60	s
	t_r	< 2	ms
	t_f	< 100	ms

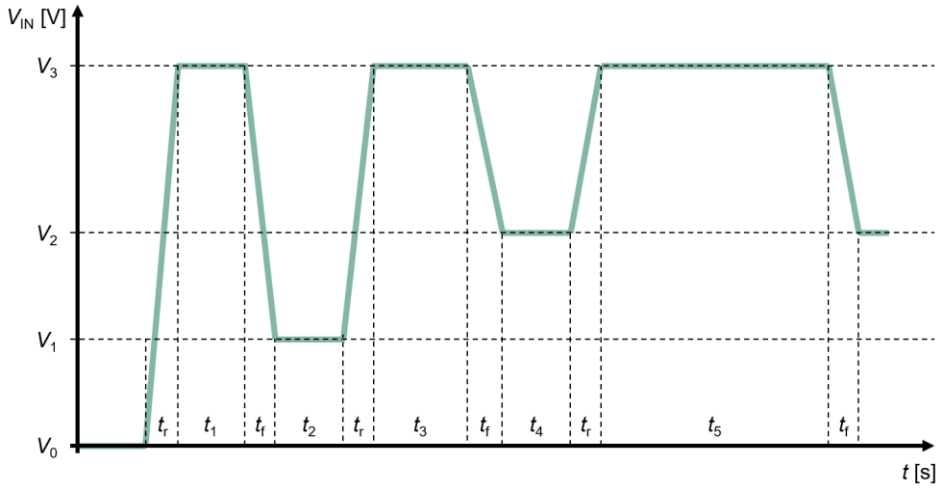
Pulse information	

Figure 45 shows the measurement results of the previously described test scenario. It is seen that the TLD5099EP stops delivering current to the load once the input voltage is lowered to 3 V. Furthermore, the output current ripple increases from 50 mA to 150 mA due to the higher input voltage level. After the exposure, the system returns to its normal operating condition, which fulfills the “Functional state C” requirement.

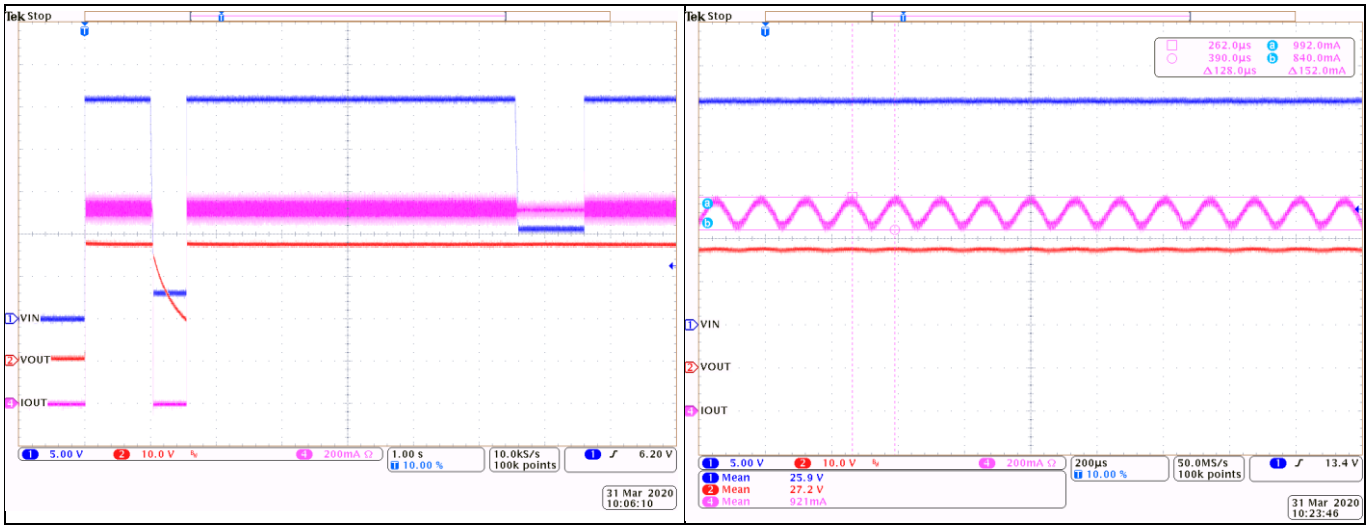


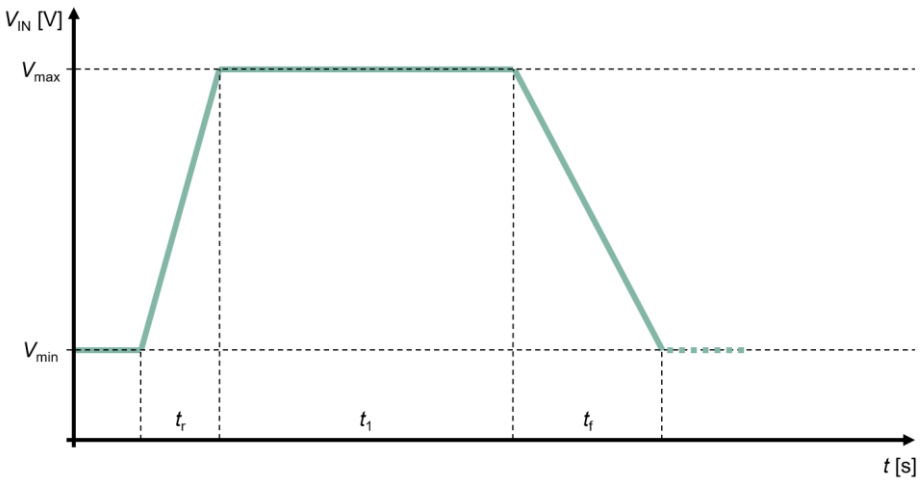
Figure 45 Jump start zoom into the voltage drops (left) and the current ripple at 26 V (right)

3.2.2 Load dump

This pulse simulates the dumping of an electric load, considering a battery with reduced buffering capacity. In Table 11, the definition of the test pulse is given.

Table 11 Load dump test pulse parameters

Expected result	**Functional state A**		
Parameters	V_{min}	13.5	V
	V_{max}	27	V
	t_r	≤ 2	ms
	t_1	300	ms
	t_f	≤ 30	ms

Pulse information	

In Figure 46, the test results are documented. During the rise time of the input voltage, an output current overshoot up to 1.07 A occurs. The system does not show any irregularities during or after the exposure to the pulse, which fulfills the “Functional state A” requirement.

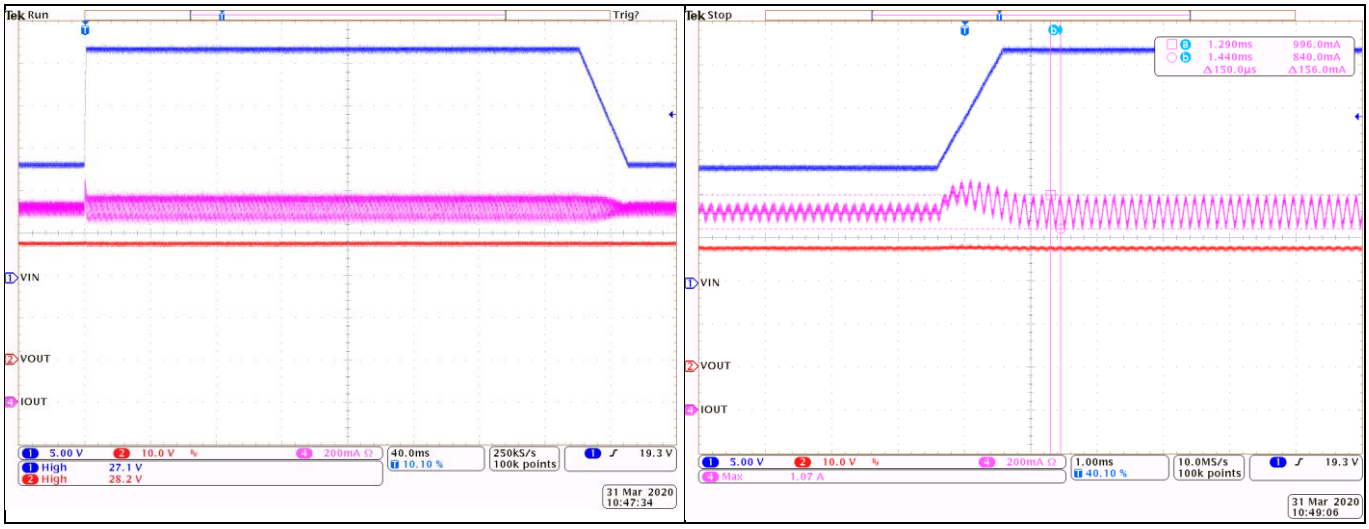


Figure 46 Load dump complete pulse (left) and the current overshoot occurring during the input voltage rise (right)

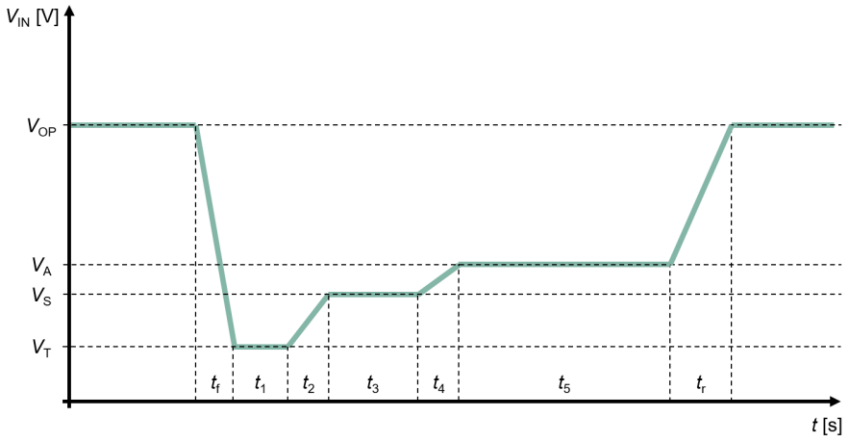
3.2.3 Start pulses

This pulse simulates the battery voltage drop when the engine is started. Due to varying environmental conditions, several test cases are defined.

3.2.3.1 Hot start

The first test is the “hot start”. The following summarizes the voltage levels and timings of the pulse.

Table 12 Start pulses (hot) test pulse parameters

Expected result	Functional state C		
Parameters	V_{OP}	11	V
	V_T	7	V
	V_S	8	V
	V_A	9	V
	t_f	≤ 1	ms
	t_1	15	ms
	t_2	70	ms
	t_3	240	ms
	t_4	70	ms
	t_5	600	ms
	t_r	≤ 1	ms
Pulse information			

The overall performance of the system is given in Figure 47. Here, an output current undershoot at the beginning and a current overshoot at the end of the pulse can be seen. These timeframes are highlighted in Figure 48. Based on these measurements it can be concluded, that the output current drops to a minimum value of 704 mA and reaches a positive peak of 1.04 A.

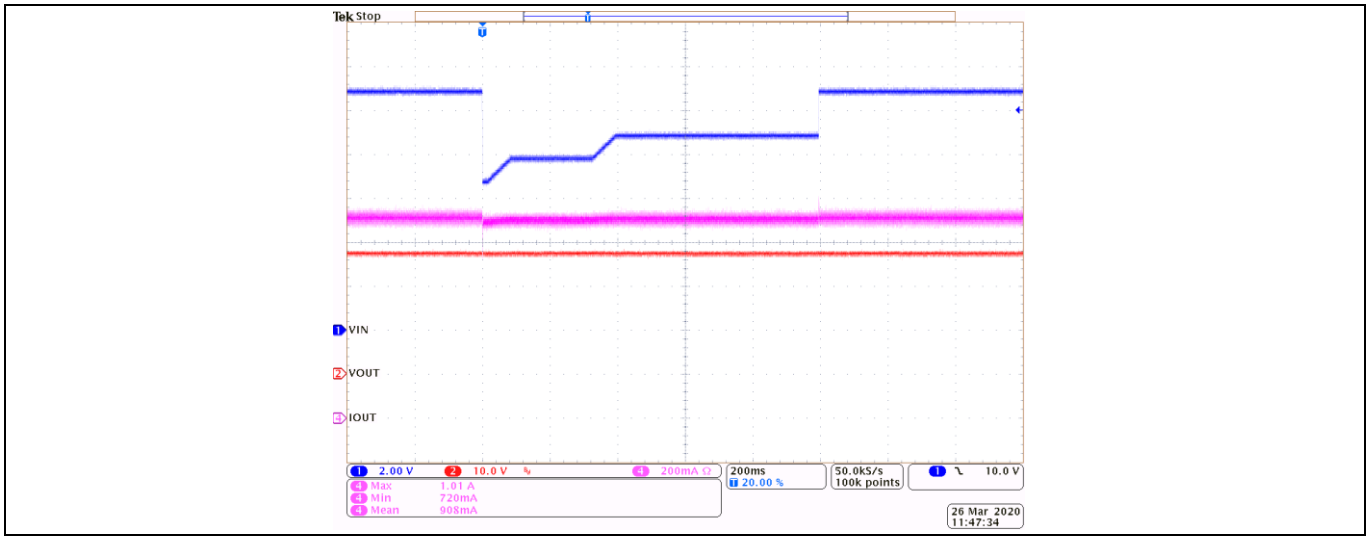


Figure 47 Start pulses (hot) complete pulse

Due to the fact that the system continues to provide current to the load throughout the complete pulse, the required “Functional state B” is fulfilled.

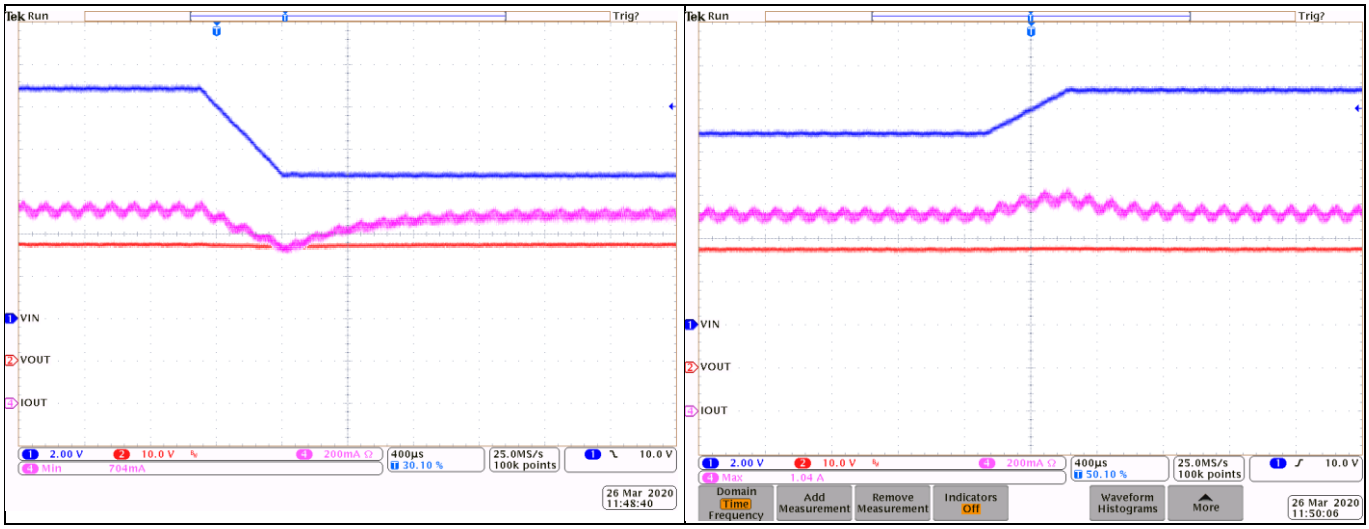


Figure 48 Start pulses (hot) start (left) and end (right) of the pulse

3.2.3.2 Cold start

The second start pulses test is the “cold start”. The two variations “Normal” and “Severe” are described within Table 13.

Table 13 Start pulses (cold) test pulse parameters

Expected result	**Functional state C**			
Parameters		**Normal**	**Severe**	
	V_{OP}	11	11	V
	V_T	4.5	3.2	V
	V_S	4.5	5	V
	V_A	6.5	6	V
	V_R	2	2	V
	t_f	≤ 1	≤ 1	ms
	t_1	0	19	ms
	t_2	0	≤ 1	ms
	t_3	19	329	ms
	t_4	50	50	ms
	t_5	10	10	s
	t_r	100	100	ms
	f	2	2	Hz

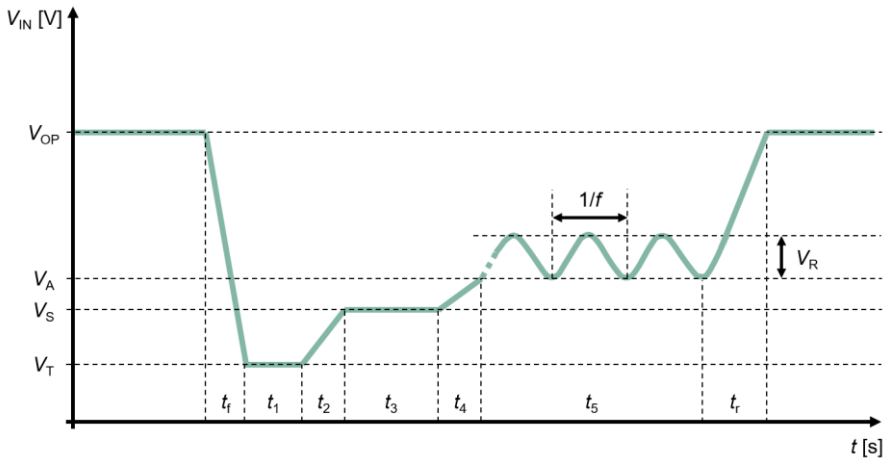
Pulse information	

Figure 49 shows the measurement results of the “normal” cold start case. Once the input voltage drops to 4.5 V, a proper load current supply is not maintained. This leads to a visible flickering effect for a very short timeframe of roughly 55 ms. As this system is not relevant for starting the engine, “Functional state C” is sufficient.

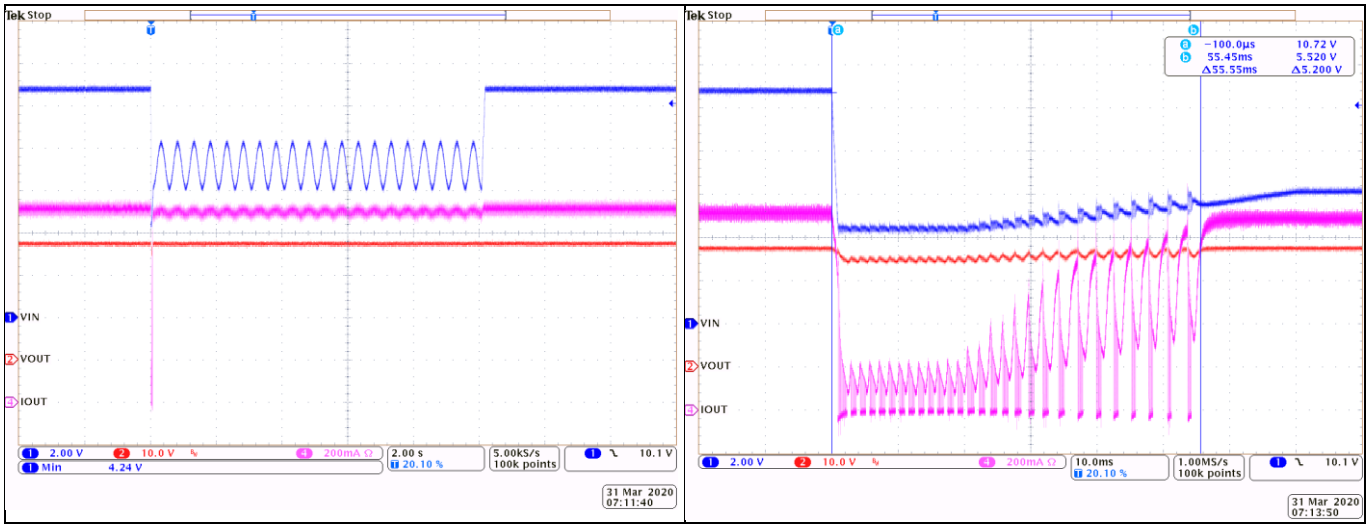


Figure 49 Start pulses (cold “normal”) complete pulse (left) and the first drop (right)

A similar behavior is obtained during the “severe” cold start test given in Figure 50. While the flickering lasts longer in this case (up to 390 ms), the system additionally goes into undervoltage. The desired “Functional state C” requirement is also fulfilled.

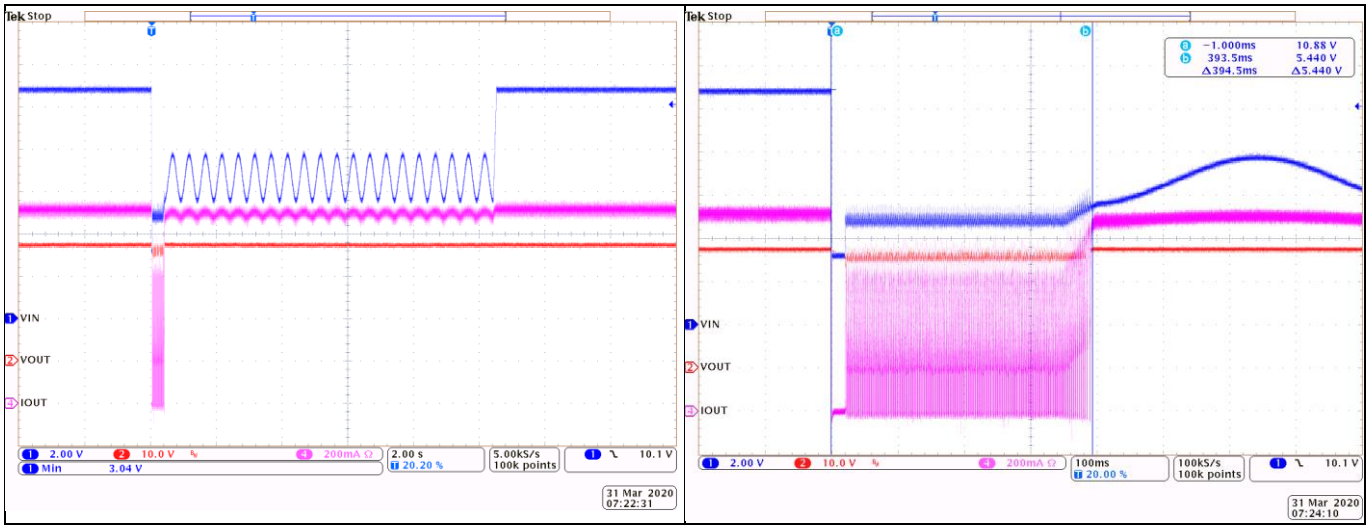
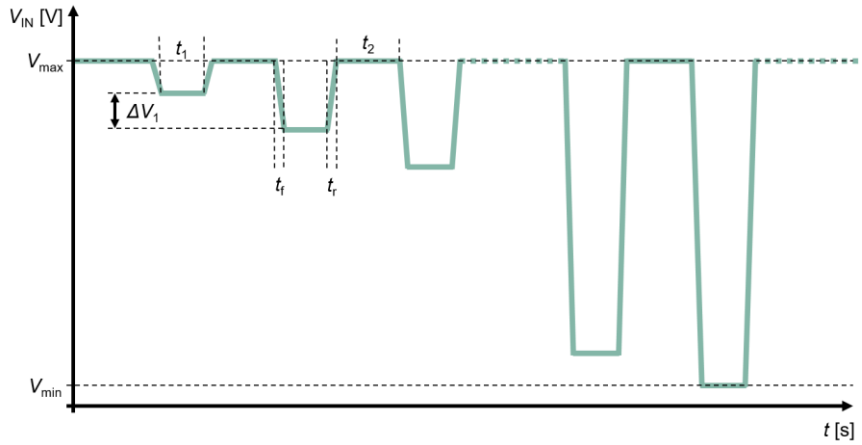


Figure 50 Start pulses (cold “severe”) complete pulse (left) and the first drop (right)

3.2.4 Reverse polarity

Reverse polarity pulse verifies the robustness of the system against reversed battery connection. In Table 14 the test parameters are summarized.

Table 14 Reverse polarity (static) test pulse parameters

Expected result	**Functional state C**		
Parameters	V_{max}	0	V
	V_{min}	-14	V
	ΔV_1	-1	V
	t_1	60	s
	t_2	≥ 60	s
	t_r	≤ 10	ms
	t_f	≤ 10	ms
Pulse information			

As described in Chapter 2.4, a reverse polarity protection based on a p-channel MOSFET is present in the input path of the system. Due to this circuitry, the applied negative voltage does not harm the electronics. Figure 51

shows that the output of the converter remains low during the defined minimum input voltage level. After the exposure, the system performs as specified once a positive input voltage is applied.

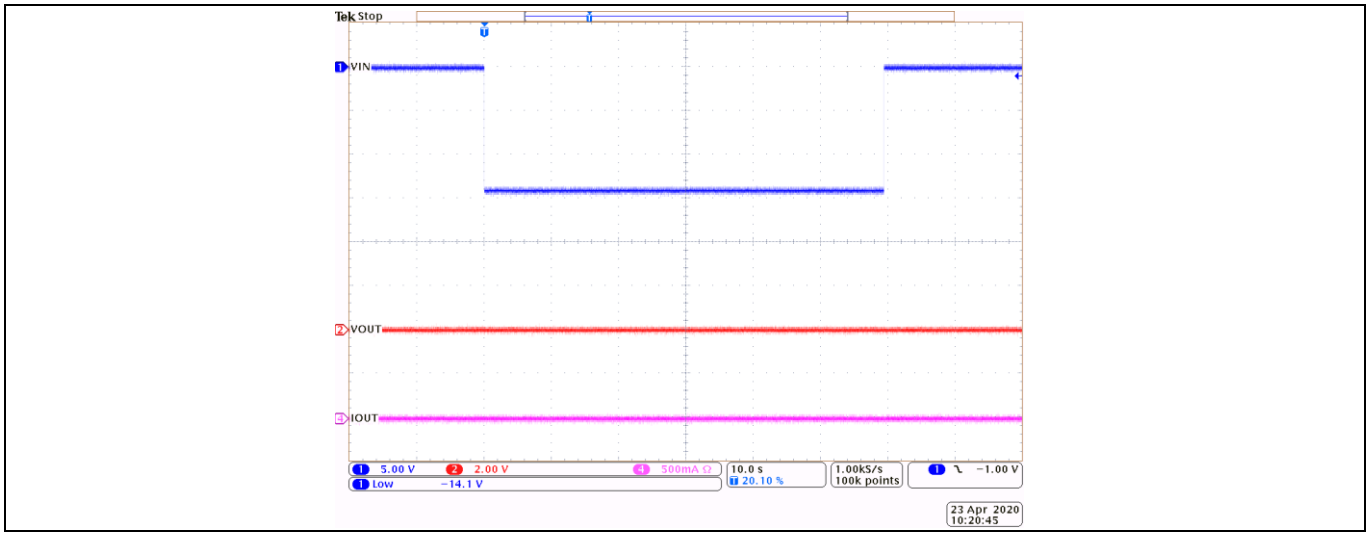


Figure 51 Reverse polarity (static) during an input voltage of -14 V

3.3 Electromagnetic compatibility

Electromagnetic compatibility in road vehicles ensures that a module's electromagnetic emissions and susceptibility stays within a certain level and does not disturb or get disturbed by other modules. The EMC regulations in the automotive industry are very strict, thus designing a compliant system requires know-how about EMC design and knowledge about the regulations in place. It is differentiated between conducted emissions, which propagate along supply lines, and radiated emissions, which propagate as electromagnetic waves.

3.3.1 Conducted emissions

This design is tested according to CISPR25 conducted emissions, more specifically according to conducted emissions from components/modules utilizing the voltage method. The DUT (EUT) is placed in a shielded chamber 50 mm above a reference ground plane. The DUT is supplied via two Line Impedance Stabilization Networks (LISN) which guarantee a specific impedance between the source and the DUT. The impedance simulates the typical wire harness in a car. The LISNs are placed in the positive and negative supply line for this system. An AC voltage is coupled out of the LISN and connected to a spectrum analyzer. Limits for the three detector types (peak, quasipeak, average) of the conducted emissions are separated in five classes, where Class V being the strictest and Class I being the most relaxed. The noise level is measured in dBµV.

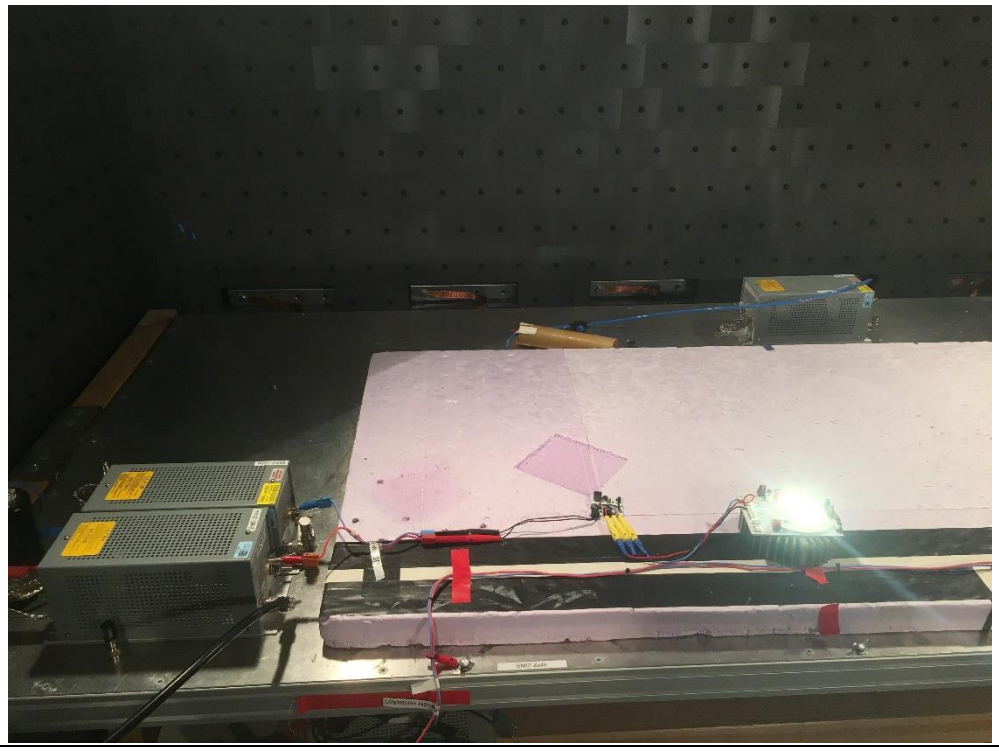


Figure 52 Conducted emissions setup with DUT and LED load according to CISPR25

During a conducted emission test, emissions from both the positive and negative supply line are measured. Since no difference in emissions was detected between the positive and the negative supply line only measurement from the positive supply line is presented. Figure 53 depicts the results for the peak detector and Figure 54 for the average detector. The results are discussed in Chapter 3.3.3.

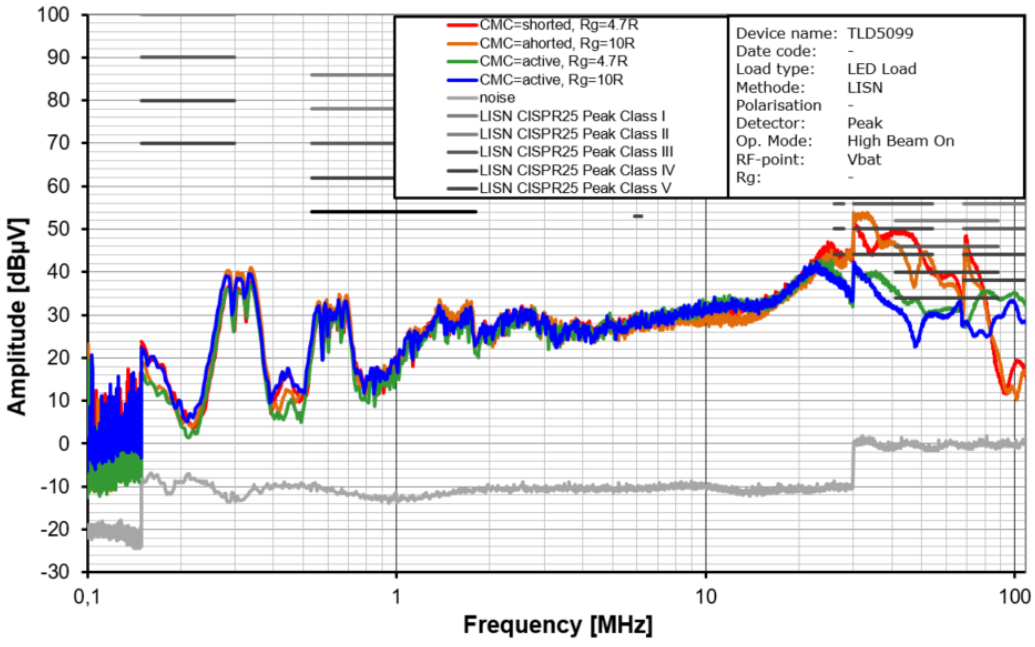


Figure 53 Conducted emissions measured with peak detector in positive supply line with different configurations with HB on and V_{IN} = 13 V

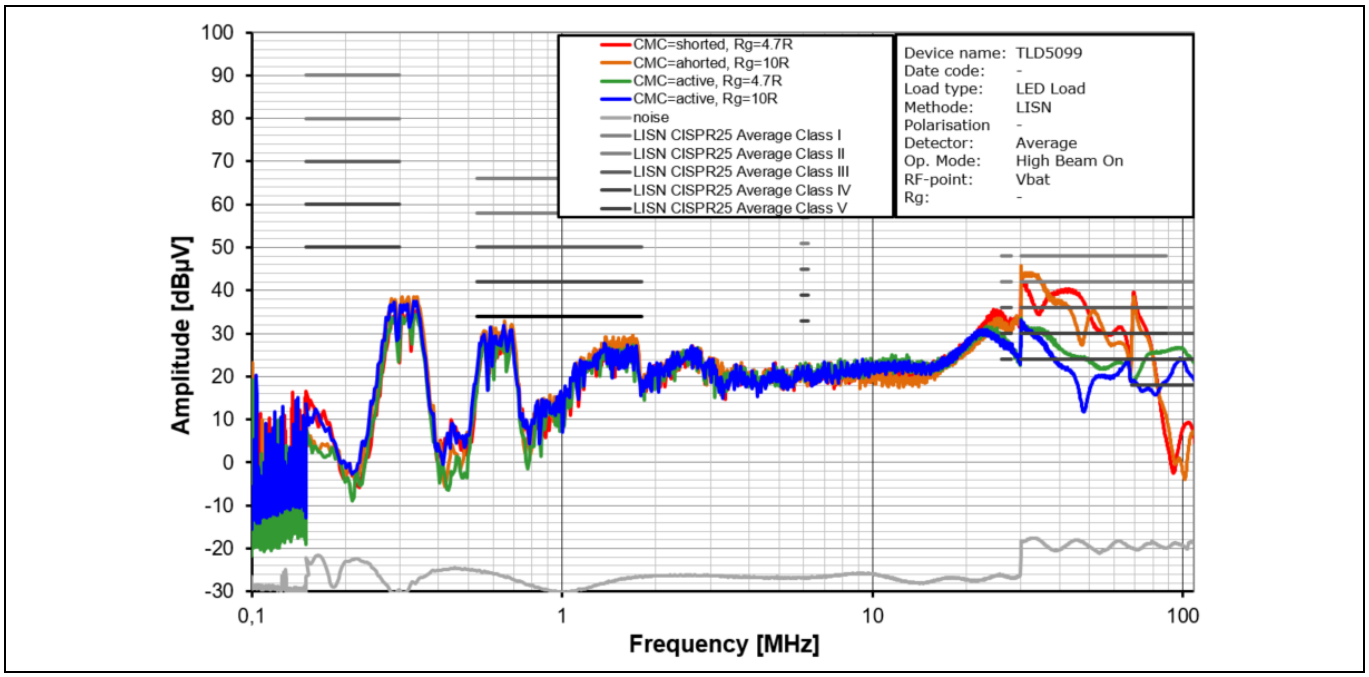


Figure 54 Conducted emissions measured with average detector in positive supply line with different configurations with HB on and V_{IN} = 13 V

3.3.2 Radiated emissions

The setup of the radiated emissions measurement is depicted in Figure 55 with the biconical antenna. The measured frequency range of radiated emissions ranges from 150 kHz up to 2.5 GHz. For different frequency ranges different antennas are recommended:

- 150 kHz to 30 MHz --> 1 m vertical monopole antenna
- 30 MHz to 300 MHz --> biconical antenna
- 200 MHz to 1000 MHz --> log-periodic antenna
- 1000 MHz to 2500 MHz --> horn or log periodic antenna

For these system measurements, from 30 MHz up to 1 GHz are shown and recommended antenna types were used. The results for peak and average detector in vertical and horizontal polarization is shown in Figure 56 to Figure 59.

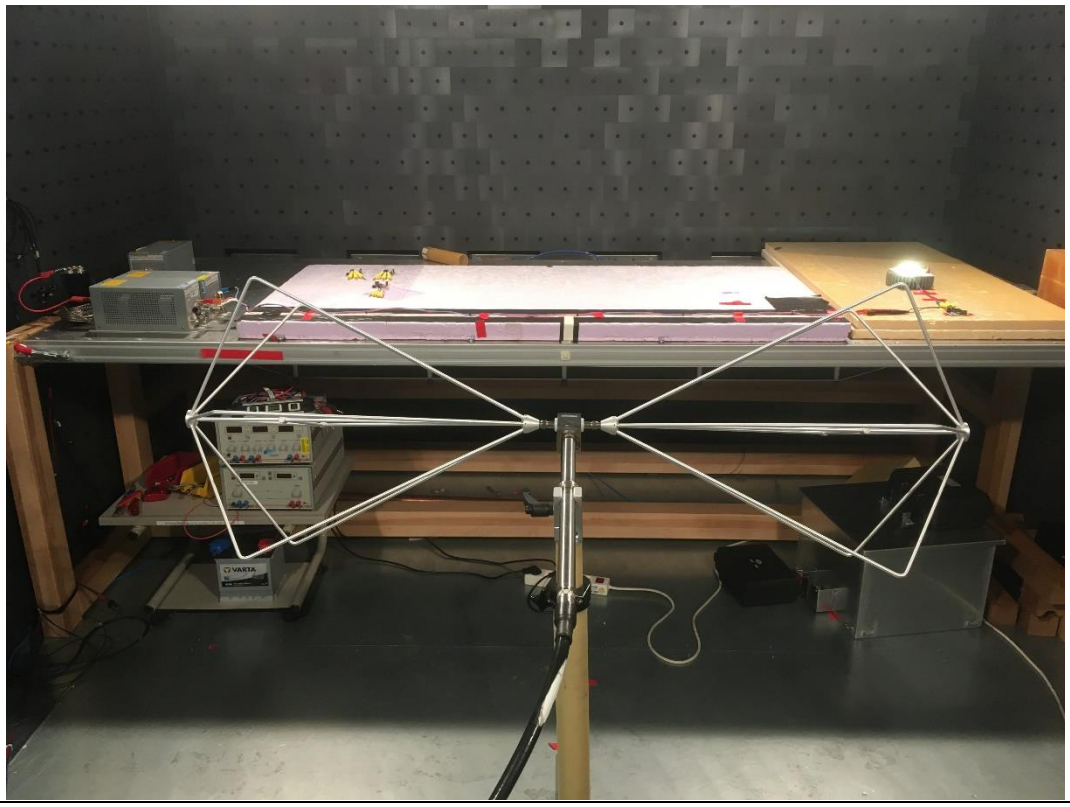


Figure 55 **Radiated emissions setup with DUT and LED load with biconical antenna according to CISPR25**

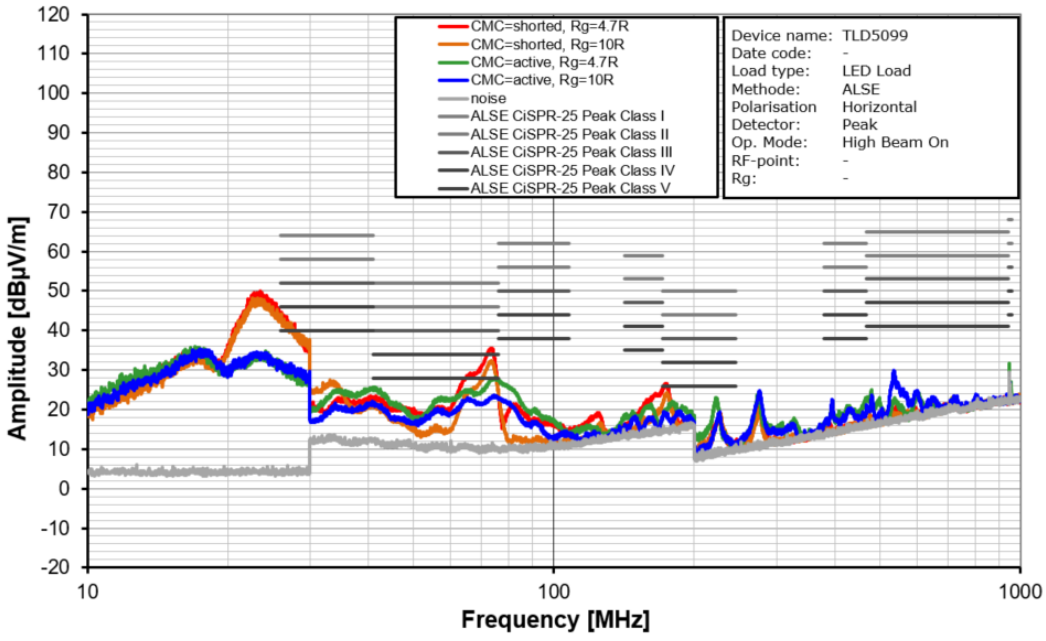


Figure 56 **Radiated emissions measured with peak detector in horizontal polarization for different configurations with HB on and V_{IN} = 13.5 V**

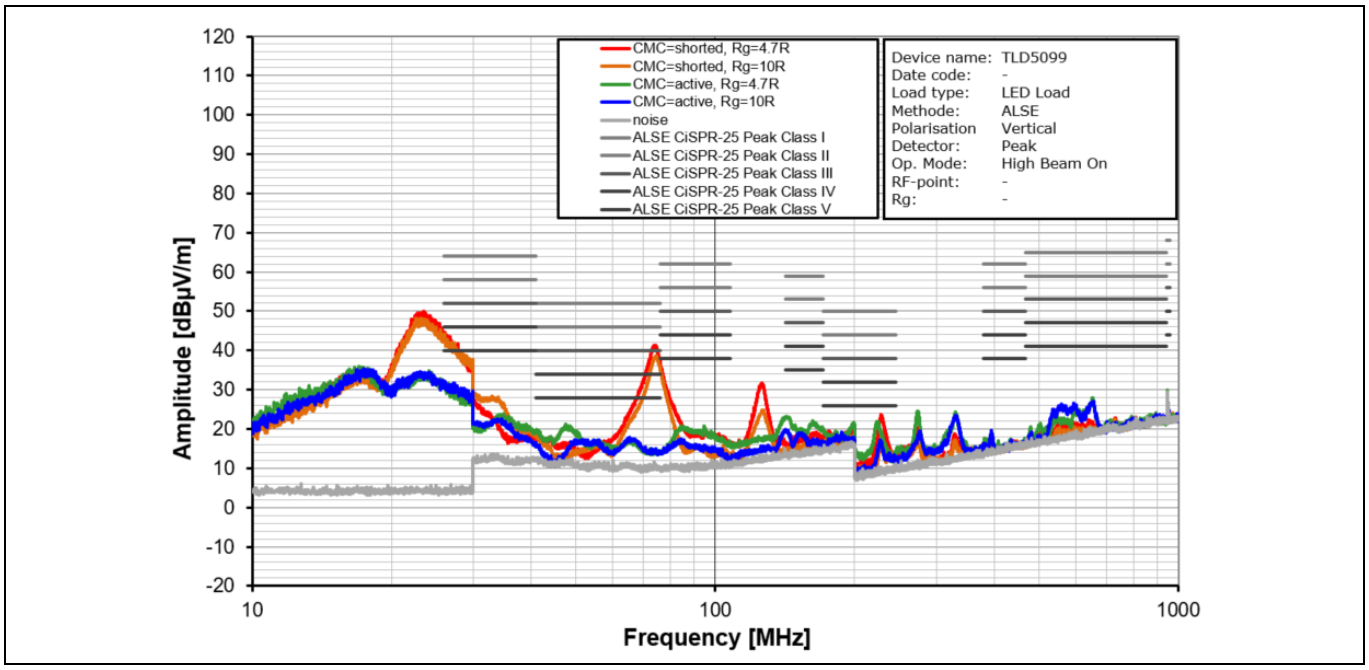


Figure 57 **Radiated emissions measured with peak detector in vertical polarization for different configurations with HB on and V_{IN} = 13.5 V**

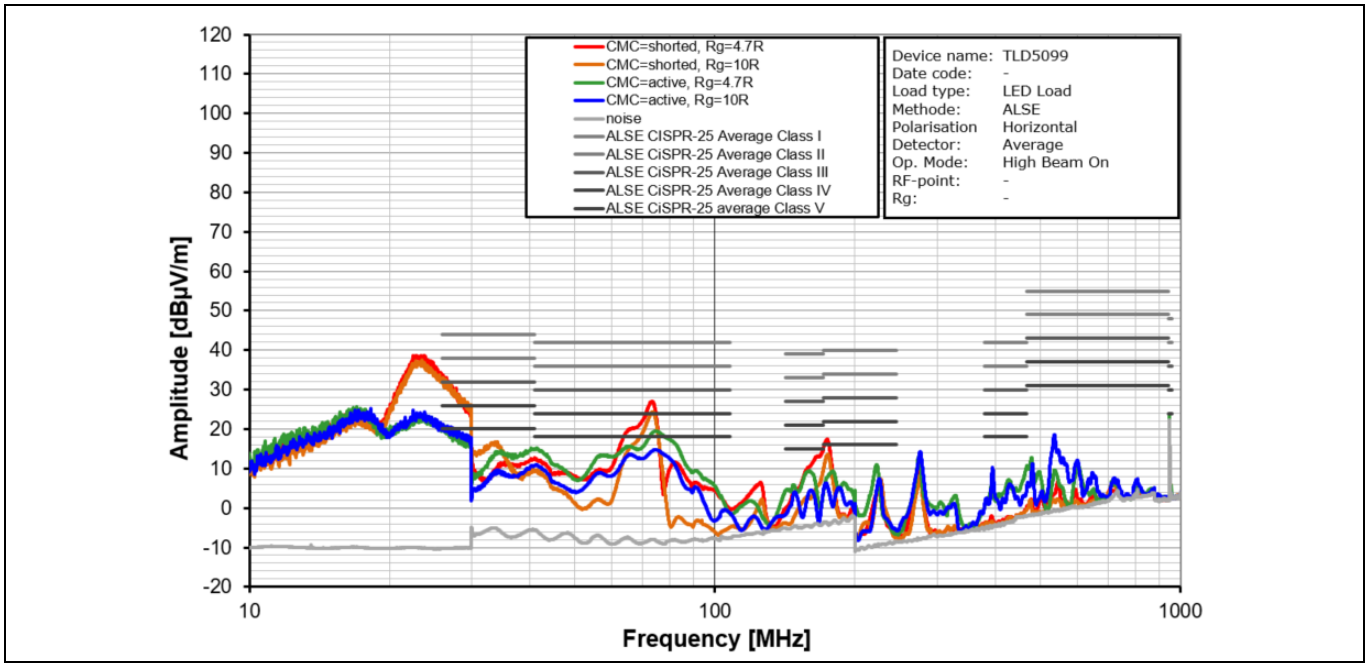


Figure 58 **Radiated emissions measured with average detector in horizontal polarization for different configurations with HB on and V_{IN} = 13.5 V**

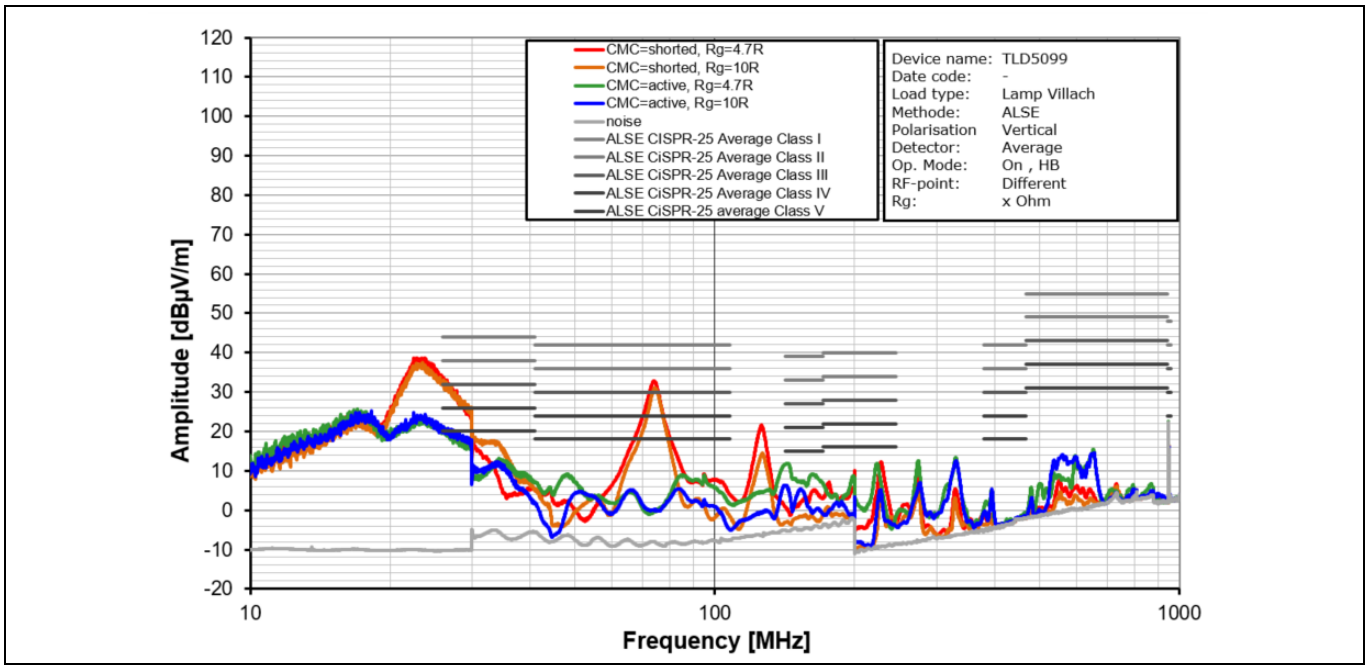


Figure 59 Radiated emissions measured with average detector in vertical polarization for different configurations with HB on and V_{IN} = 13.5 V

3.3.3 Summary and discussion

Table 15 summarizes the results of the conducted and radiated emissions for the configuration with R_G = 10 Ω and CMC active. All radiated emissions from the peak and average detector meet class V requirements. Conducted emissions for the peak detector also meet class V requirements for all services/bands. However, the average detector does not always meet class V requirements:

- VHF (30 – 54 MHz), Class III
- VHF (68 – 87 MHz), Class IV
- FM (76 – 108 MHz), Class IV

Furthermore, it can be also concluded that these results are obtained without any additional shielding from a possible housing, which would further improve these results. It is also considered that no chassis connection is available to place y-capacitors which would greatly limit the common mode noise. From the results one can also conclude that mainly common mode noise dominates from around 20 MHz upwards. This can be identified by comparing the results with and without CMC. The variation in gate resistance shows slightly different results with lower emissions for the higher resistance with R_G = 10 Ω. This can be explained by the slower rise and fall times during the switching activities and therefore lower emissions. For thermal reasons R_G = 4.7 Ω would be the more preferable choice. Here the compromise between EMC performance and thermal performance must be made.

Table 15 Conducted and radiated emission results for different services/bands with R_G = 10 Ω, CMC active, HB on and V_{IN} = 13 V

Conducted emissions			
Service/band	**Frequency range**	**Detector type**	**CISPR25 class**
LW	0.15 – 0.30 MHz	Peak	Class V
		Average	Class V
MW	0.53 – 1.8 MHz	Peak	Class V
		Average	Class V
SW	5.9 – 6.2 MHz	Peak	Class V
		Average	Class V
CB	26 – 28 MHz	Peak	Class V
		Average	Class V
VHF	30 – 54 MHz	Peak	Class V
		Average	Class III
TV Band I	41 – 88 MHz	Peak	Class V
		Average	Class V
VHF	68 – 87 MHz	Peak	Class V
		Average	Class IV
FM	76 – 108 MHz	Peak	Class V
		Average	Class IV
Radiated emissions			
Service/band	**Frequency range**	**Detector type**	**CISPR25 class**
All services/bands	30 MHz – 1 GHz	Peak	Class V
		Average	Class V

3.4 Efficiency

The efficiency of the system for HB off and on with respect to the supply voltage is plotted in Figure 60. A more detailed analysis of the power losses is provided in Chapter 3.4.1.

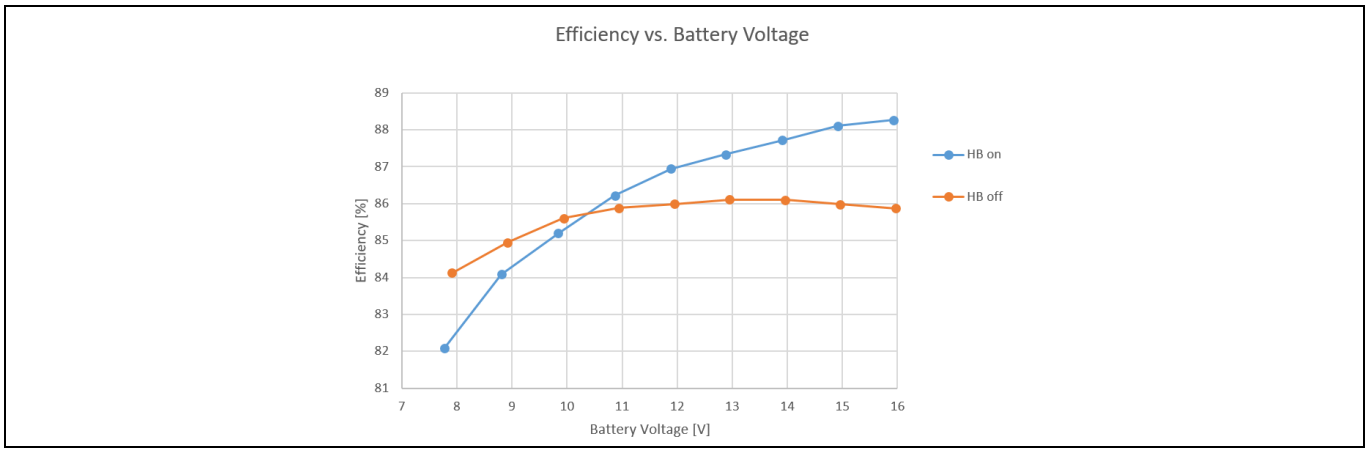


Figure 60 Efficiency vs. supply voltage for HB on and off

Table 16 Efficiency raw data for high beam on

V_{IN} [V]	I_{IN} [A]	V_{OUT} [V]	I_{OUT} [A]	P_{IN} [W]	P_{OUT} [W]	η [%]
7.77	3.886	26.85	0.923	30.19	24.78	82.07
8.81	3.36	26.82	0.928	29.60	24.88	84.07
9.84	2.973	26.77	0.931	29.25	24.92	85.19
10.87	2.663	26.75	0.933	28.94	24.95	86.21
11.89	2.416	26.74	0.934	28.72	24.97	86.94
12.88	2.222	26.73	0.935	28.61	24.99	87.32
13.91	2.046	26.67	0.936	28.45	24.96	87.71
14.92	1.901	26.67	0.937	28.36	24.98	88.10
15.93	1.778	26.68	0.937	28.32	24.99	88.26

Table 17 Efficiency raw data for high beam off

V_{IN} [V]	I_{IN} [A]	V_{OUT} [V]	I_{OUT} [A]	P_{IN} [W]	P_{OUT} [W]	η [%]
7.91	2.124	15.1	0.936	16.80	14.13	84.12
8.92	1.864	15.09	0.936	16.62	14.12	84.94
9.94	1.664	15.11	0.937	16.54	14.15	85.59
10.94	1.506	15.1	0.937	16.47	14.14	85.87
11.95	1.376	15.09	0.937	16.44	14.13	85.98
12.95	1.268	15.09	0.937	16.42	14.13	86.10
13.96	1.178	15.11	0.937	16.44	14.15	86.09
14.96	1.1	15.1	0.937	16.45	14.14	85.97
15.97	1.031	15.09	0.937	16.46507	14.13933	85.8747

3.4.1 Main power loss contributors

Figure 61 provides further information on how the power loss is distributed over the components and how the distribution changes with input voltage. As it can be seen, the Ohmic losses which are scaled with the squared input current are more dominant for a lower input voltage and decrease with higher input voltage. As a good reference point for distribution change, one can use the losses in the switching diode (green) to envisage the scaling since this is fairly constant with respect to the supply voltage.

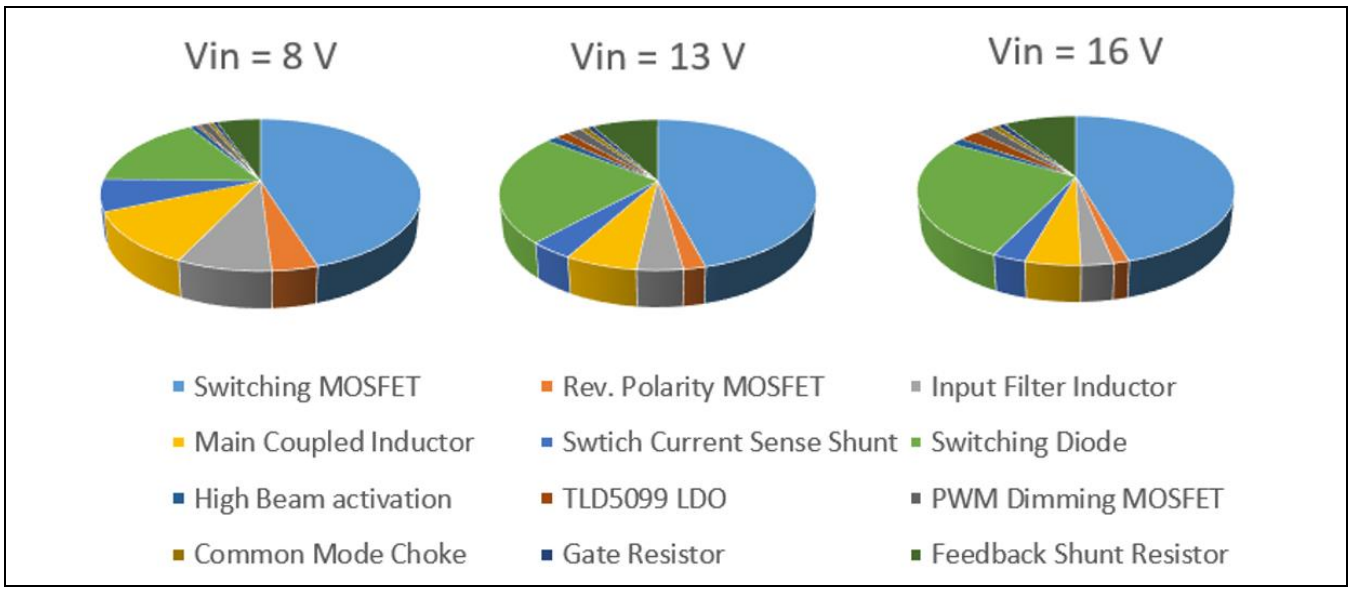


Figure 61 Power loss contribution of different components vs. supply voltage

Total losses:

The total losses from all main contributors are listed in Table 18. A comparison between the measured results and analytic losses is shown and it can be seen that there is a very good correlation. The analytic calculated efficiency, as expected, is slightly higher.

Table 18 Total losses with HB on

	$V_{IN,min}$ = 8 V	$V_{IN,typ}$ = 13 V	$V_{IN,max}$ = 16 V
Power loss	4.87 W	3.26 W	2.97 W
Analytic η	83.57%	88.44%	89.38%
Measured η	82.07%	87.32%	88.26%

Switching MOSFET:

The losses generated in the switching MOSFET are mainly due to conduction, switching and reverse recovery losses. As discussed in Chapter 2.2.2.3 better result accuracy is provided when a simulation is used instead the analytical calculation. The same simulation setup as depicted in Figure 21 is used. Following results can be simulated:

Table 19 Power in switching MOSFET with HB on

	$V_{IN,min}$ = 8 V	$V_{IN,typ}$ = 13 V	$V_{IN,max}$ = 16 V
Power loss	2.2 W	1.5 W	1.35 W

Reverse polarity MOSFET:

The power losses generated in the reverse polarity MOSFET are due to conduction losses. Eq. 44 can be used to calculate the losses.

$$P_{RP} = I_{IN}^2 * R_{DS(ON)} \quad \textit{Eq. 44}$$

Table 20 Power loss in reverse polarity MOSFET with HB on

	$V_{IN,min}$ = 8 V	$V_{IN,typ}$ = 13 V	$V_{IN,max}$ = 16 V
Power loss	189 mW	62 mW	40 mW

Input filter inductor:

The power loss generated in the input filter inductor are mainly due to the DCR of the inductor. Coilcraft offers an online simulator for the losses for a specific operating condition where it can be concluded that core and AC losses are negligible.

$$P_{L,Input} = I_{IN}^2 * DCR \quad \textit{Eq. 45}$$

Table 21 Power loss in input filter inductor with HB on

	$V_{IN,min}$ = 8 V	$V_{IN,typ}$ = 13 V	$V_{IN,max}$ = 16 V
Power loss	392 mW	128 mW	82 mW

Main coupled inductor:

For the power loss in the main coupled inductor only the losses due to the DCR are considered.

$$P_{La} = I_{IN}^2 * DCR$$
$$P_{Lb} = I_{OUT}^2 * DCR \quad \textit{Eq. 46}$$
$$P_L = P_{La} + P_{Lb}$$

Table 22 Power loss in main coupled inductor with HB on

	$V_{IN,min}$ = 8 V	$V_{IN,typ}$ = 13 V	$V_{IN,max}$ = 16 V
Power loss	558 mW	203 mW	141 mW

Switch current sense shunt resistor:

The switch current sense resistor carries the same current as the switching MOSFET.

$$P_{RSWCS} = R_{SWCS} * {I_{Q,RMS}}^2$$
$$I_{Q,RMS} = (I_{IN} + I_{OUT}) * \sqrt{D}$$

Eq. 47

Table 23 Power loss in switch current sense shunt resistor with HB on

	$V_{IN,min}$ = 8 V	$V_{IN,typ}$ = 13 V	$V_{IN,max}$ = 16 V
Power loss	333 mW	124 mW	85 mW

Feedback shunt resistor:

The feedback shunt resistor carries the output current.

$$P_{RFB} = R_{FB} * {I_{OUT}}^2$$

Eq. 48

Table 24 Power loss in feedback shunt resistor with HB on

	$V_{IN,min}$ = 8 V	$V_{IN,typ}$ = 13 V	$V_{IN,max}$ = 16 V
Power loss	254 mW	262 mW	263 mW

Switching diode:

The switching diode is on during the off-time and carries the input current plus the output current.

$$P_D = I_{D,AVG} * V_D$$
$$I_{D,AVG} = (I_{IN} + I_{OUT}) * (1 - D)$$

Eq. 49

Table 25 Power loss in switching diode with HB on

	$V_{IN,min}$ = 8 V	$V_{IN,typ}$ = 13 V	$V_{IN,max}$ = 16 V
Power loss	888 mW	813 mW	800 mW

TLD5099EP LDO:

The LDO of the TLD5099EP generates power loss due to the fact that the gate charge current of the switching MOSFET is provided via the LDO. Depending on the input voltage the power loss changes.

$$I_{IVCC,AVG} = Q_G * f_{SW}$$
$$P_{LDO} = (V_{in} - V_{IVCC}) * I_{IVCC,AVG} \quad \text{Eq. 50}$$

Table 26 Power loss in TLD5099EP LDO with HB on

	$V_{IN,min}$ = 8 V	$V_{IN,typ}$ = 13 V	$V_{IN,max}$ = 16 V
Power loss	19 mW	54 mW	75 mW

High beam activation MOSFET:

When the high beam is active, power loss occurs in the activation MOSFET which are conduction losses.

$$P_{HB,act} = {I_{OUT}}^2 * R_{DS(ON)} \quad \text{Eq. 51}$$

Table 27 Power loss HB activation MOSFET with HB on

	$V_{IN,min}$ = 8 V	$V_{IN,typ}$ = 13 V	$V_{IN,max}$ = 16 V
Power loss	44 mW	45 mW	46 mW

PWM dimming MOSFET:

If no PWM dimming is used the PWM dimming MOSFET is turned on continuously and therefore generates conduction losses.

$$P_{PWMO} = {I_{OUT}}^2 * R_{DS(ON)} \quad \text{Eq. 52}$$

Table 28 Power loss PWM dimming MOSFET with HB on

	$V_{IN,min}$ = 8 V	$V_{IN,typ}$ = 13 V	$V_{IN,max}$ = 16 V
Power loss	56 mW	58 mW	58 mW

Common mode choke:

Power loss in the CMC is generated due to the DCR of the windings.

$$P_{CMC} = {I_{OUT}}^2 * DCR \qquad \text{Eq. 53}$$

Table 29 Power loss common mode choke with HB on

	$V_{IN,min}$ = 8 V	$V_{IN,typ}$ = 13 V	$V_{IN,max}$ = 16 V
Power loss	25 mW	26 mW	26 mW

3.5 Thermal performance

A thermal image is provided to evaluate the thermal performance of the design. Four different spots are monitored. These spots are:

- Spot 1: Main coupled inductor
- Spot 2: Switching MOSFET
- Spot 3: Switching diode
- Spot 3: Current feedback shunt

As already discussed in Chapter 2.2.2.4, derating strategies are applied to the design when input voltage and ambient temperature deviate from the nominal values. Figure 62 shows a thermal image of the design under the load conditions given in the figure title. Predicted by Eq. 35, at an ambient temperature of 75°C a MOSFET temperature of 168°C is estimated. It can be seen that in spot 2, which represents the MOSFET temperature, 103°C is measured. Since this measurement was done at ambient temperature of 25°C, it is necessary to add 50°C to that result to compensate for the missing ambient temperature, which results in 153°C. Compared to the estimated 168°C from Eq. 35 one can conclude that actual performance is better than predicted. These results are without any additional cooling elements and would greatly improve when using such.

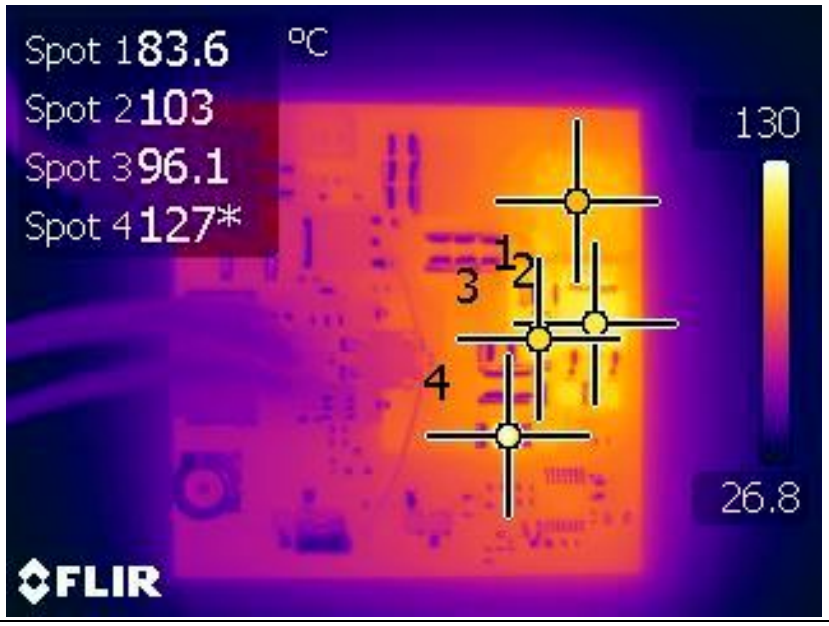


Figure 62 Thermal image at V_{IN} = 13 V, R_G = 10 Ω, CMC active, T_A = 25°C, HB and LB on and no additional cooling elements

4 Abbreviations and definitions

Table 30 Abbreviations

Abbreviation	Definition
SEPIC	Single Ended Primary Inductor
LED	Light Emitting Diode
HB	High Beam
LB	Low Beam
ECU	Electrical Control Unit
PWM	Pulse Width Modulation
PCB	Printed Circuit Board
EMC	Electromagnetic Compatibility
IC	Integrated Circuit
DC	Duty Cycle
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
ESR	Equivalent Series Resistance
CTVS	Ceramic Transient Voltage Suppressor

5 Reference documents

This document should be read in conjunction with the following documents:

[1] TLD5099EP datasheet, Infineon Technologies AG, https://www.infineon.com/dgdl/Infineon-TLD5099EP-DataSheet-v01_00-EN.pdf?fileId=5546d462700c0ae601701fd7e6fc40d4

[2] OSRAM OSLON® Compact PL KW CELNM1.TG datasheet, OSRAM Opto Semiconductors, https://www.osram.com/ecat/OSLON%C2%AE%20Compact%20PL%20KW%20CELNM1.TG/com/en/class_pim_web_catalog_103489/global/prd_pim_device_2190862/

[3] Murata SimSurfing tool, Murata, https://www.murata.com/tool/simsurfing

[4] IPD60N10S4L-12 datasheet, Infineon Technologies AG, https://www.infineon.com/dgdl/Infineon-IPD60N10S4L_12-DS-v01_00-en.pdf?fileId=db3a3043372d5cc801374ffd51cd0505

[5] ACM70V-701-2PL-TL00 datasheet, TDK, https://product.tdk.com/de/search/emc/emc/cmf_cmc/info?part_no=ACM70V-701-2PL-TL00

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