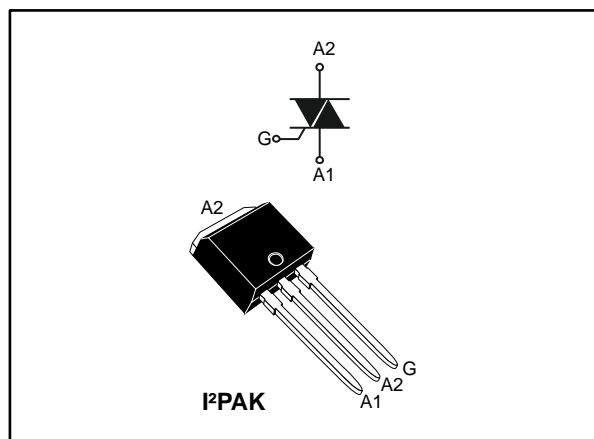


12 A Snubberless™ Triac

Datasheet - production data


Description

Housed in an I²PAK package this device is dedicated to low profile compact applications.

Its fully rated 150 °C junction temperature allows high AC commutation capability for on/off or phase control applications without snubber aid circuit.

Table 1: Device summary

Symbol	Value	Unit
V_{DRM}/V_{RRM}	800	V
I_{GT}	35	mA
T_j	150	°C

Features

- 12 A medium current Triac
- Three triggering quadrants device
- Very high noise immunity and dynamic commutation
- ECOPACK®2 compliant component

Applications

- General purpose AC line load control
- Motor control circuits
- Home, kitchen and tools appliances
- Lighting
- Inrush current limiting circuits

1 Characteristics

Table 2: Absolute ratings (limiting values), $T_j = 25\text{ °C}$, unless otherwise specified

Symbol	Parameter		Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)		$T_C = 128\text{ °C}$ 12	A
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25 °C)		$t_p = 20\text{ ms}$ 90	A
			$t_p = 16.7\text{ ms}$ 95	
I^2t	I^2t value for fusing		$t_p = 10\text{ ms}$ 66	A^2s
di/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, $tr \leq 100\text{ ns}$		$f = 100\text{ Hz}$ 100	$A/\mu s$
V_{DRM} / V_{RRM}	Repetitive peak off-state voltage		$T_j = 125\text{ °C}$ 800	V
			$T_j = 150\text{ °C}$ 600	
V_{DSM} / V_{RSM}	Non repetitive surge peak off-state voltage		$t_p = 10\text{ ms}$ 900	
I_{GM}	Peak forward gate current	$t_p = 20\text{ }\mu s$	$T_j = 150\text{ °C}$ 4	A
$P_{G(AV)}$	Average gate power dissipation		$T_j = 150\text{ °C}$ 1	W
T_{stg}	Storage junction temperature range			-40 to +150 $^{\circ}C$
T_j	Operating junction temperature range			-40 to +150 $^{\circ}C$

Table 3: Electrical characteristics ($T_j = 25\text{ °C}$ unless otherwise specified)

Symbol	Test conditions	Quadrant		Value	Unit
$I_{GT}^{(1)}$	$V_D = 12\text{ V}$, $R_L = 33\text{ }\Omega$	I - II - III	Max.	35	mA
V_{GT}			Max.	1	V
V_{GD}	$V_D = V_{DRM}$, $R_L = 3.3\text{ k}\Omega$, $T_j = 150\text{ °C}$	I - II - III	Min.	0.15	V
$I_H^{(1)}$	$I_T = 500\text{ mA}$, gate open		Max.	35	mA
I_L	$I_G = 1.2 \times I_{GT}$	I - III	Max.	50	mA
		II		80	
$dV/dt^{(2)}$	$V_D = 536\text{ V}$, gate open	$T_j = 125\text{ °C}$	Min.	2000	$V/\mu s$
	$V_D = 402\text{ V}$, gate open	$T_j = 150\text{ °C}$		1000	
$(di/dt)_c^{(2)}$	Without snubber		Min.	$T_j = 125\text{ °C}$ 19.5	A/ms
				$T_j = 150\text{ °C}$ 13	

Notes:

⁽¹⁾minimum I_{GT} is guaranteed at 5% of I_{GT} max.

⁽²⁾for both polarities of A2 referenced to A1.

Table 4: Static electrical characteristics

Symbol	Test conditions			Value	Unit
$V_{TM}^{(1)}$	$I_{TM} = 17 \text{ A}$, $t_p = 380 \text{ } \mu\text{s}$	$T_j = 25 \text{ }^\circ\text{C}$	Max.	1.55	V
$V_{TO}^{(1)}$	Threshold voltage	$T_j = 150 \text{ }^\circ\text{C}$	Max.	0.85	V
$R_D^{(1)}$	Dynamic resistance	$T_j = 150 \text{ }^\circ\text{C}$	Max.	40	m Ω
I_{DRM} / I_{RRM}	$V_D = V_{DRM} = V_R = V_{RRM} = 600 \text{ V}$	$T_j = 25 \text{ }^\circ\text{C}$	Max.	5	μA
		$T_j = 150 \text{ }^\circ\text{C}$	Max.	3.6	mA
	$V_D = V_{DRM} = V_R = V_{RRM} = 800 \text{ V}$	$T_j = 125 \text{ }^\circ\text{C}$	Max.	1.2	mA

Notes:

⁽¹⁾for both polarities of A2 referenced to A1

Table 5: Thermal parameters

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case (AC)	Max.	1.5	$^\circ\text{C/W}$
$R_{th(j-a)}$	Junction to ambient	Typ.	65	

1.1 Characteristics (curves)

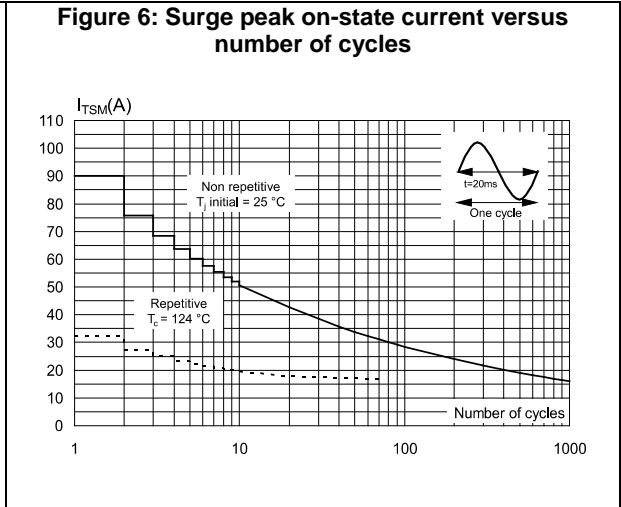
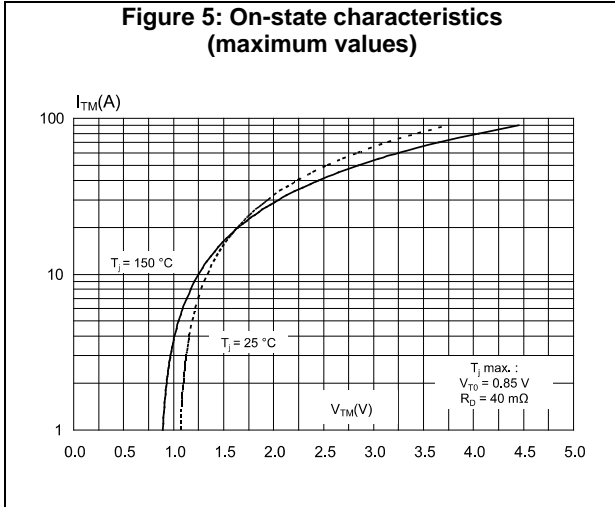
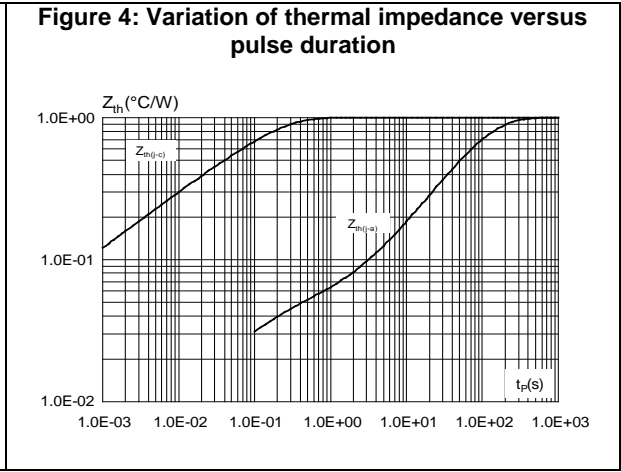
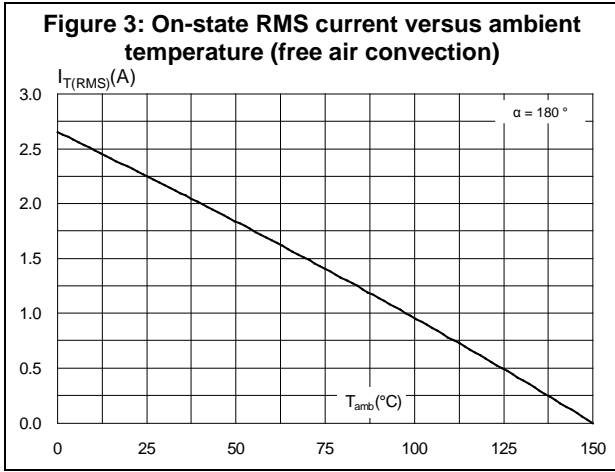
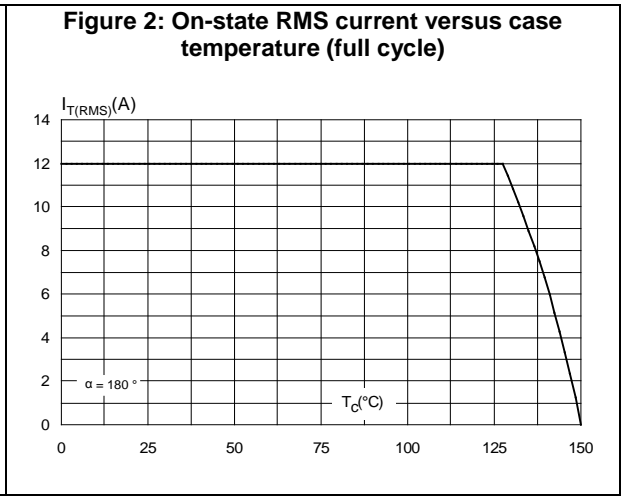
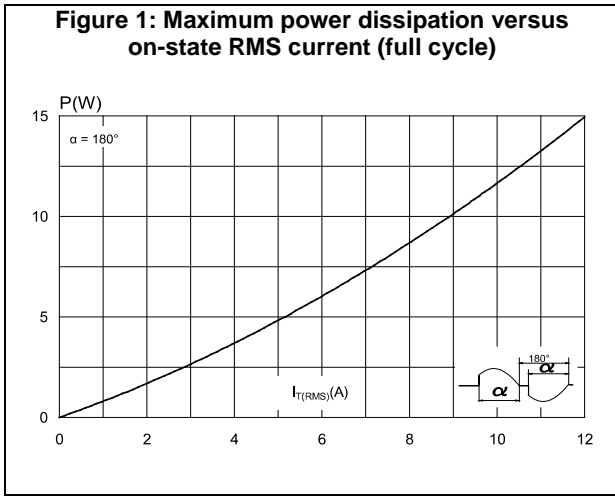


Figure 7: Non repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10$ ms

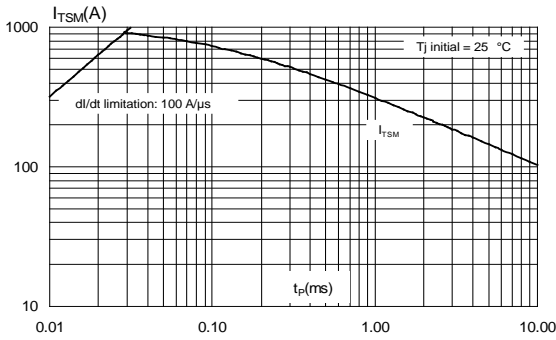


Figure 8: Relative variation of gate current, holding current and latching current versus junction temperature (typical values)

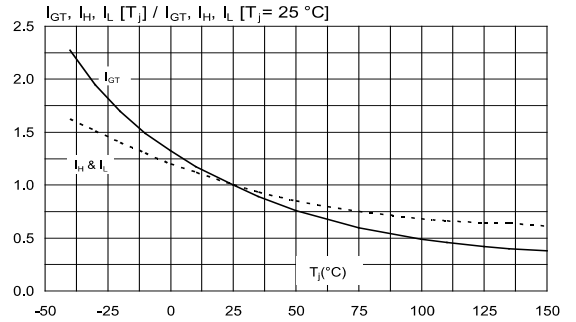


Figure 9: Relative variation of critical rate of decrease of main current versus reapplied dV/dt (typical values)

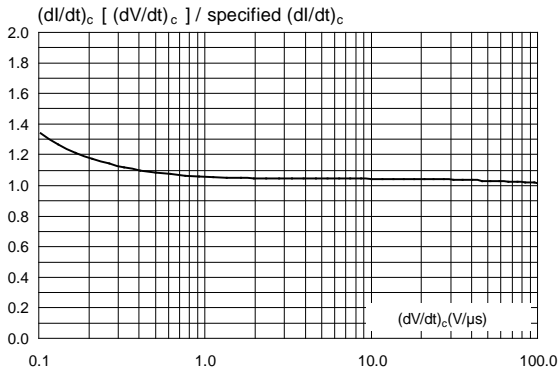


Figure 10: Relative variation of critical rate of decrease of main current versus junction temperature

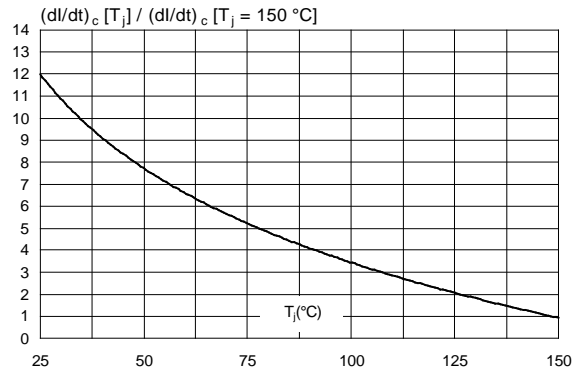


Figure 11: Relative variation of static dV/dt immunity versus junction temperature

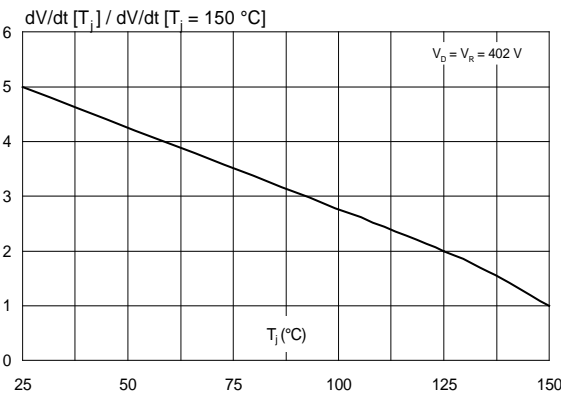
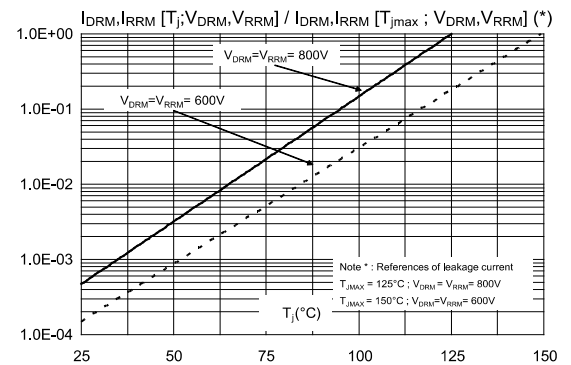


Figure 12: Relative variation of leakage current versus junction temperature for different blocking voltages (typical values)



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

- ECOPACK®2 compliant
- Lead-free package leads finishing
- Molding compound resin is halogen-free and meets UL94 standard level V0

2.1 I²PAK package information

Figure 13: I²PAK package outline

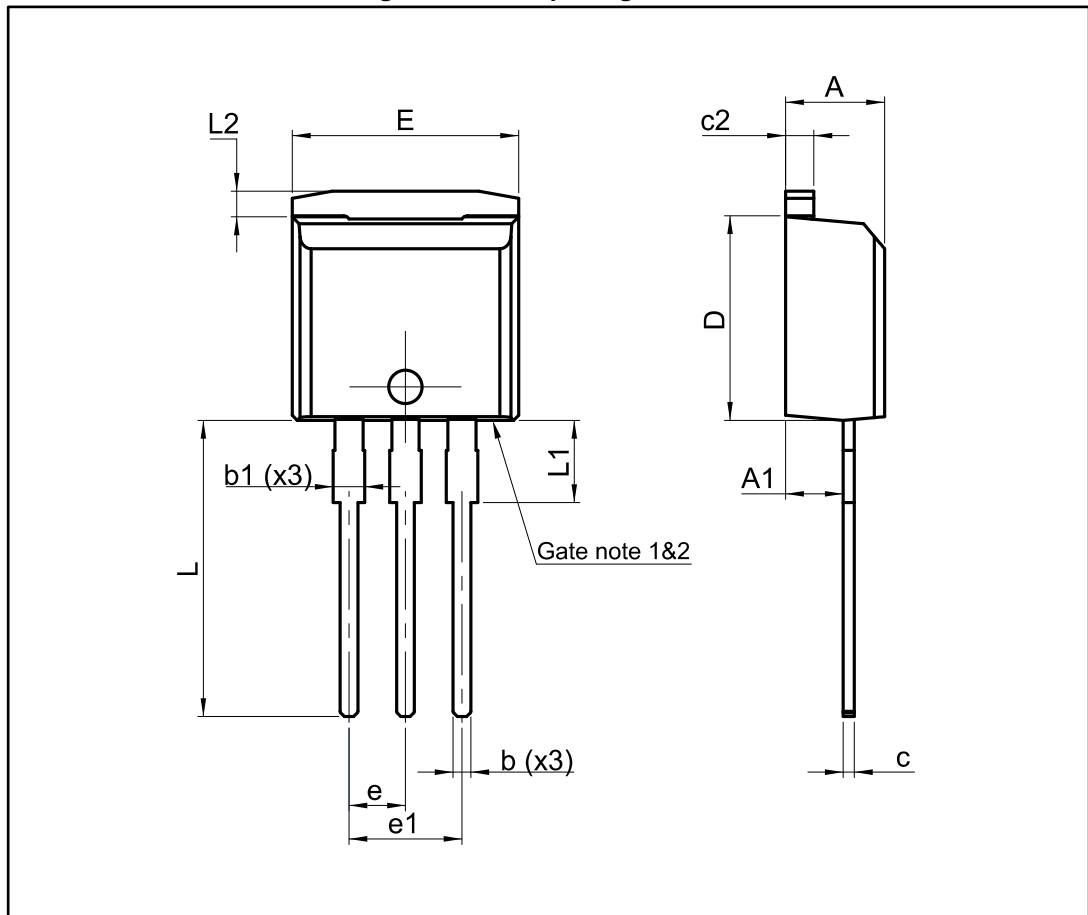


Table 6: PPAK package mechanical data

Ref.	Dimensions			
	Millimeters		Inches ⁽¹⁾	
	Min.	Max.	Min.	Max.
A	4.40	4.60	0.1732	0.1811
A1	2.40	2.72	0.0945	0.1071
b	0.61	0.88	0.0240	0.0346
b1	1.14	1.70	0.0449	0.0669
c	0.49	0.70	0.0193	0.0276
c2	1.23	1.32	0.0484	0.0520
D	8.95	9.35	0.3524	0.3681
e	2.40	2.70	0.0945	0.1063
e1	4.95	5.15	0.1949	0.2028
E	10.00	10.40	0.3937	0.4094
L	13.00	14.00	0.5118	0.5512
L1	3.50	3.93	0.1378	0.1547
L2	1.27	1.40	0.0500	0.0551

Notes:⁽¹⁾Inches dimensions given for reference only

3 Ordering information

Figure 14: Ordering information scheme

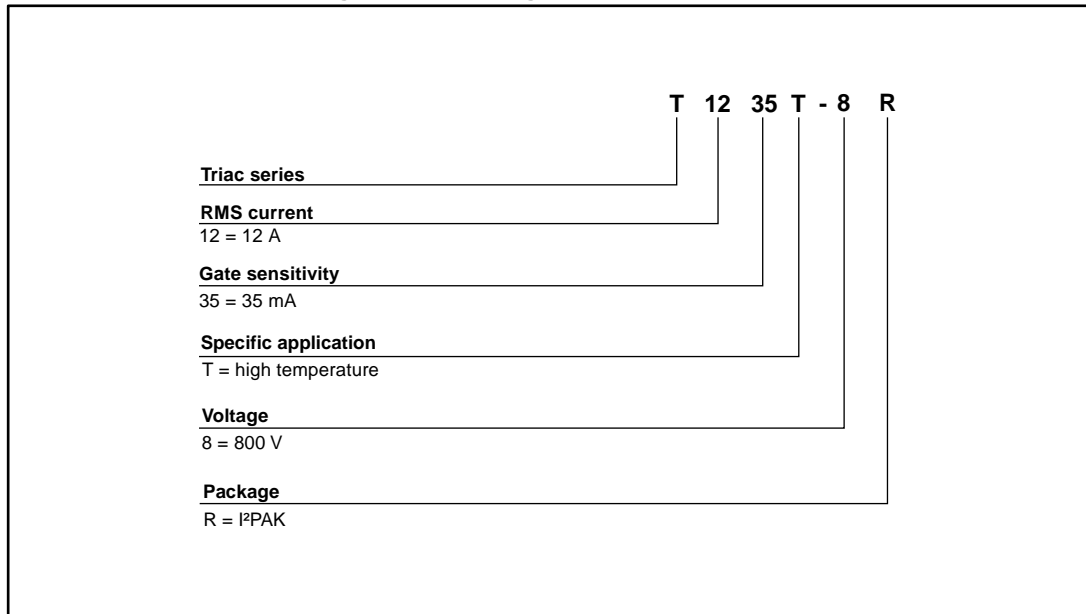


Table 7: Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
T1235T-8R	T1235T-8R	I ² PAK	1.7 g	50	Tube

4 Revision history

Table 8: Document revision history

Date	Revision	Changes
14-Nov-2017	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[STMicroelectronics:](#)

[T1235T-8R](#)