



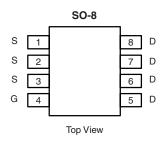
N-Channel 30-V MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)			
30	0.007 at V _{GS} = 10 V	16			
	0.0085 at V _{GS} = 4.5 V	14			

FEATURES

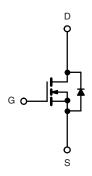
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFETs
- 100 % R_g Tested





Ordering Information: Si4874BDY-T1-E3 (Lead (Pb)-free)

Si4874BDY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T	A = 25 °C, unles	ss otherwise n	oted		
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V _{DS}	30		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Dunin Comment /T 450 90\8	T _A = 25 °C	- I _D	16	12	^
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		13	9	
Pulsed Drain Current		I _{DM}	± 50		Α
Continuous Source Current (Diode Conduction) ^a		I _S	2.7	1.40	
	T _A = 25 °C	P _D	3.0	1.6	W
Maximum Power Dissipation ^a	T _A = 70 °C	T D	2.0	1.0	VV
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 t	o 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Manipular landing to Austriant (MOOFFT)	t ≤ 10 s	R_{thJA}	34	41	
Maximum Junction-to-Ambient (MOSFET) ^a	Steady State	' 'thJA	68	80	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	16	21	

Notes

a. Surface Mounted on 1" x 1" FR4 board.

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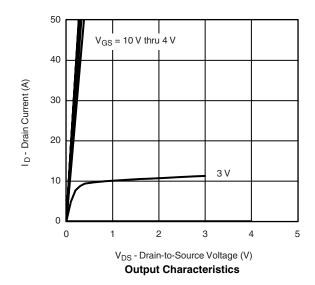
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$ 1.0			3.0	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zara Cata Valtaga Drain Current	1	V _{DS} = 30 V, V _{GS} = 0 V			1		
Zero Gate Voltage Drain Current	DSS	V _{DS} = 30 V, V _{GS} = 0 V, T _J = 70 °C			5	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
	Ъ	$V_{GS} = 10 \text{ V}, I_D = 16 \text{ A}$		0.0057	0.007	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 14 \text{ A}$		0.0068	0.0085		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 16 A		65		S	
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.7 \text{ A}, V_{GS} = 0 \text{ V}$		0.74	1.1	V	
Dynamic ^b				•			
Input Capacitance	C _{iss}			3230			
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		585		pF	
Reverse Transfer Capacitance	C _{rss}			255			
Total Gate Charge	Q_g			21	25		
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 16 \text{ A}$		9.5		nC	
Gate-Drain Charge	Q_{gd}			6.5			
Gate Resistance	R_g		0.4	0.9	1.4	Ω	
Turn-On Delay Time	t _{d(on)}			16	25		
Rise Time	t _r	V_{DD} = 15 V, R_L = 15 Ω		10	20		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 10 V, R_g = 6 Ω		57	90	ns	
Fall Time	t _f			15	25		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.7 A, dl/dt = 100 A/μs		40	60		

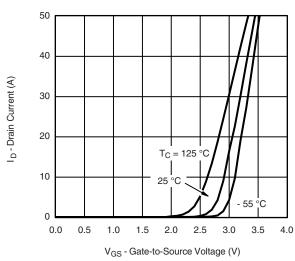
Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

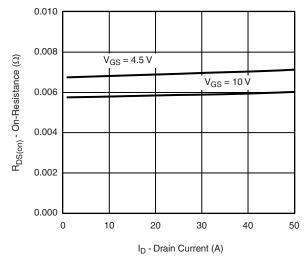
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



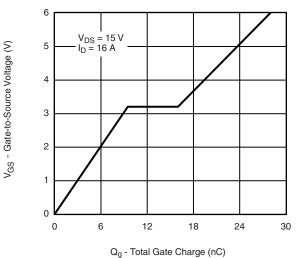




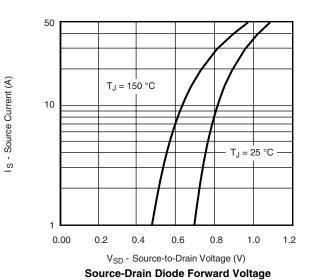
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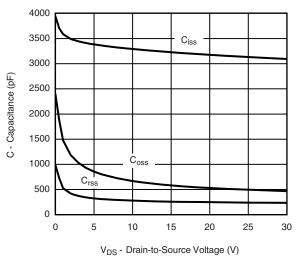


On-Resistance vs. Drain Current

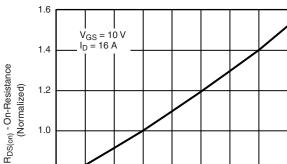


Gate Charge





Capacitance



25

0.8

0.6

- 50 - 25 0

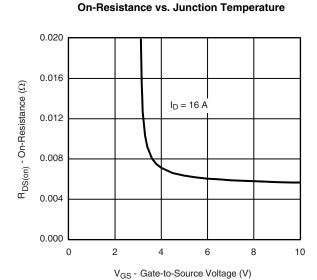
50 T_J - Junction Temperature (°C)

100

125

75

150

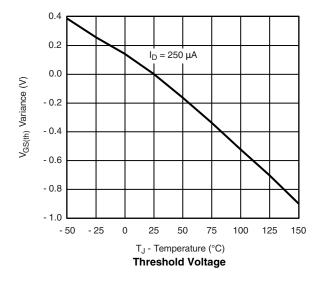


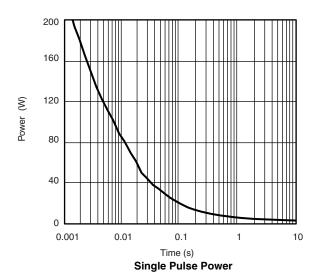
On-Resistance vs. Gate-to-Source Voltage

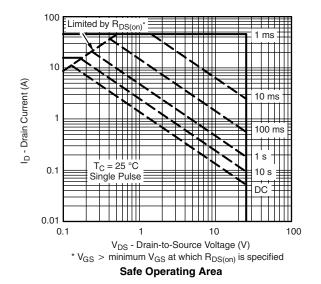
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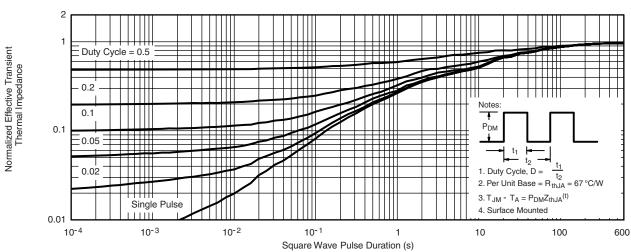
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





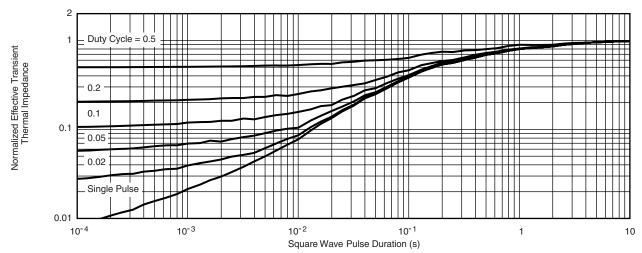




Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg273058.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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