

8 CHANNEL LOW CAPACITANCE TVS DIODE ARRAY
Product Summary

V_{BR} (Min)	I_{PP} (Max)	C_{I/O} (Typ)
5.5V	3	0.45pF

Description

The D3V3X8U9LP3810 is a high-performance device suitable for protecting four high speed I/Os. These devices are assembled in U-DFN3810-9 (Type B) package and have high ESD surge capability, low ESD clamping voltage and ultra-low capacitance.

Applications

Typically used at high-speed ports such as USB 3.0, USB 3.1, Serial ATA, Display port.

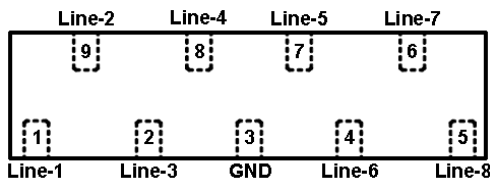
Features

- Clamping Voltage: 7V at 16A TLP
- IEC 61000-4-2 (ESD): Air — ±10kV ,Contact — ±8kV
- IEC 61000-4-5 (Lightning): 3A (8/20µs)
- 8 Channels of ESD Protection
- Ultra-Low Channel Input Capacitance of 0.45pF Typical
- TLP Dynamic Resistance: 0.3Ω
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**

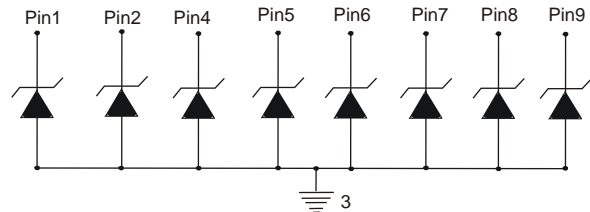
Mechanical Data

- Case: U-DFN3810-9 (Type B)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Schematic
- Terminals: Finish – NiPdAu, Solderable per MIL-STD-202, Method 208 ^(e)
- Weight: 0.005 grams (Approximate)

U-DFN3810-9 (Type B)



Pin Description (Top View)



Device Schematic

Ordering Information (Note 4)

Part Number	Compliance	Marking	Reel Size (inches)	Tape Width (mm)	Quantity
D3V3X8U9LP3810-7	Standard	MW6	7	8	3,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information

U-DFN3810-9 (Type B)



MW6 = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: E = 2017)
 M = Month (ex: 9 = September)

Date Code Key

Year	2016	2017	2018	2019	2020	2021
Code	D	E	F	G	H	I

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Conditions
Peak Pulse Current, per IEC 61000-4-5	I _{PP}	3	A	I/O to V _{SS} , 8/20μs
Peak Pulse Power, per IEC 61000-4-5	P _{PP}	20	W	I/O to V _{SS} , 8/20μs
ESD Protection – Contact Discharge, per IEC 61000-4-2	V _{ESD_CONTACT}	±8	kV	I/O to V _{SS}
ESD Protection – Air Discharge, per IEC 61000-4-2	V _{ESD_AIR}	±10	kV	I/O to V _{SS}
Operating Temperature	T _{OP}	-55 to +85	°C	—
Storage Temperature	T _{STG}	-55 to +150	°C	—

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation Typical (Note 5)	P _D	350	mW
Thermal Resistance, Junction to Ambient Typical (Note 5)	R _{θJA}	360	°C/W

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Reverse Working Voltage	V _{RWM}	—	—	3.3	V	I _R =1mA, I/O to V _{SS}
Reverse Current	I _R	—	—	1.0	μA	V _R = 3.3V, I/O to V _{SS}
Reverse Breakdown Voltage	V _{BR}	5.5	7.0	—	V	I _R = 1mA, I/O to V _{SS}
Forward Clamping Voltage	V _F	-1.0	-0.85	—	V	I _F = -15mA, I/O to V _{SS}
Holding Reverse Voltage	V _{HOLD}	—	1.19	—	V	I/O to V _{SS}
Holding Reverse Current	I _{HOLD}	—	90	—	mA	I/O to V _{SS}
Clamping Voltage (Note 6)	V _C	—	7	—	V	TLP, 16A, tp = 100ns, I/O to V _{SS}
Clamping Voltage (Note 6)	V _C	—	7	—	V	TLP, -16A, tp = 100ns, I/O to V _{SS}
Dynamic Reverse Resistance	R _{DIF-R}	—	0.3	—	Ω	TLP, 10A, tp = 100ns, I/O to V _{SS}
Dynamic Forward Resistance	R _{DIF-F}	—	0.25	—	Ω	TLP, 10A, tp = 100ns, V _{SS} to I/O
Channel Input Capacitance	C _{I/O}	—	0.45	—	pF	V _{I/O} = 0V, V _{SS} = 0V, f = 1MHz

- Notes:
- Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes Incorporated's suggested pad layout, which can be found on our website at <http://www.diodes.com/package-outlines.html>.
 - Clamping voltage value is based on a TLP model. TLP conditions: Z₀=50Ω, tp = 100ns, averaging window; t₁=70ns to t₂=90ns.

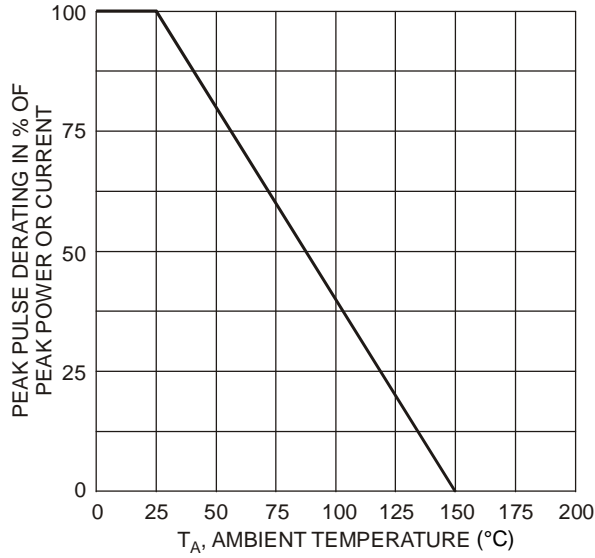


Figure 1 Pulse Derating Curve

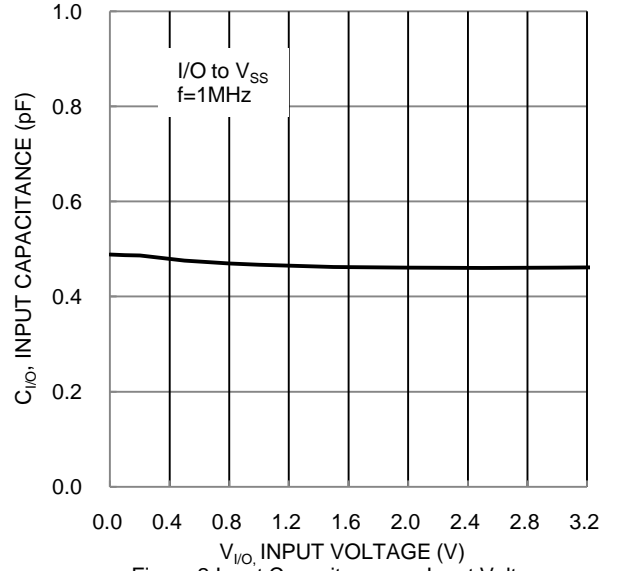


Figure 2 Input Capacitance vs. Input Voltage

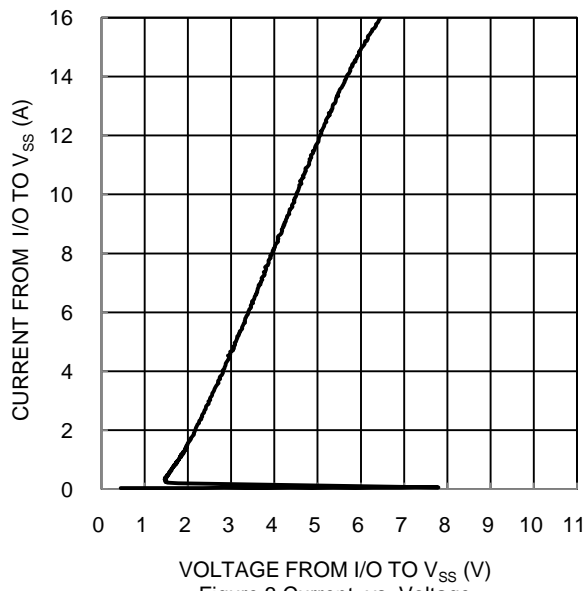


Figure 3 Current vs. Voltage

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