PESD36VS1UJ

Unidirectional ESD protection diode

16 September 2015 **Product data sheet**

1. General description

Unidirectional ElectroStatic Discharge (ESD) protection diode in a flat lead very small SOD323F Surface-Mounted Device (SMD) plastic package designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- ESD protection of one line
- ESD protection up to 30 kV
- IEC 61000-4-5; (surge); I_{PPM} = 2.5 A
- Rated peak pulse power: P_{PPM} = 150 W
- Ultra low leakage current: I_{RM} < 1 nA
- AEC-Q101 qualified

3. Applications

- computers and peripherals
- audio and video equipment
- cellular handsets and accessories
- portable electronics
- communication systems

4. Quick reference data

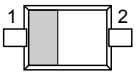
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	36	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	18	30	pF

nexperia

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode[1]	 SOD323F	 sym035
2	A	anode		

[1] The marking bar indicates the cathode.

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD36VS1UJ	SOD323F	plastic surface-mounted package; 2 leads	SOD323F

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD36VS1UJ	BG

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{PPM}	peak pulse power	t_p = 8/20 µs	[1][2]	-	150	W
I_{PPM}	peak pulse current		[1][2]	-	2.5	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2][3]	-	30	kV
		IEC 61000-4-2; air discharge	[2]	-	30	kV

[1] Device stressed with ten non-repetitive ESD pulses (8/20 µs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321).
[2] Measured from pin 1 to pin 2.
[3] Device stressed with ten non-repetitive ESD pulses.

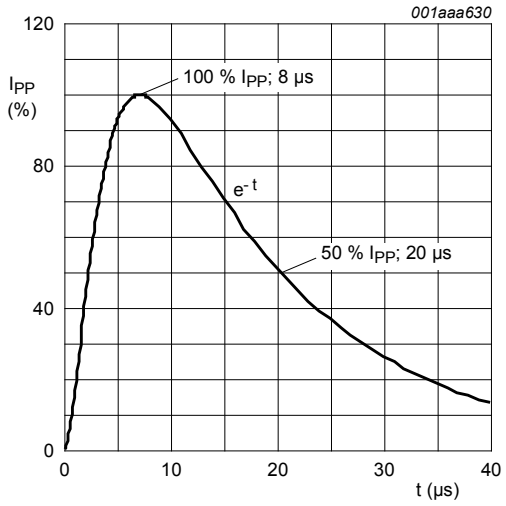


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

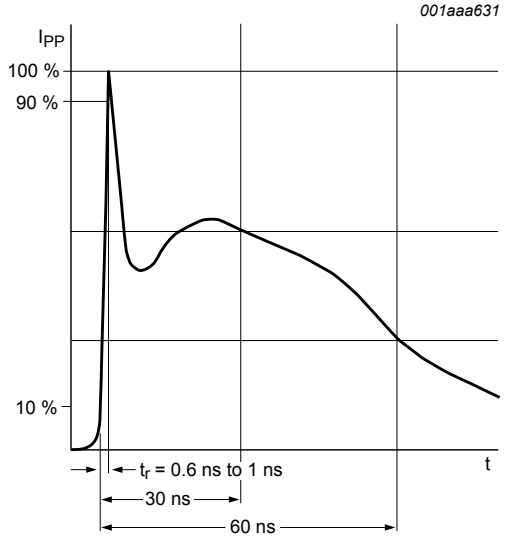


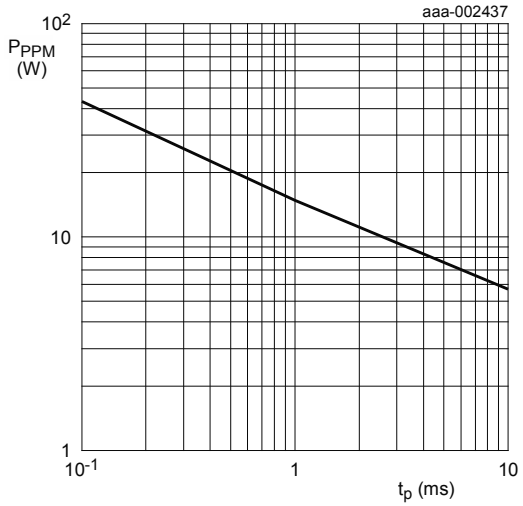
Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	36	V
I_{RM}	reverse leakage current	V_{RWM} = 36 V; T_{amb} = 25 °C		-	1	10	nA
V_{BR}	breakdown voltage	I_R = 2 mA; T_{amb} = 25 °C		38.2	39	39.8	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C		-	18	30	pF
V_{CL}	clamping voltage	I_{PP} = 1 A; T_{amb} = 25 °C	[1][2]	-	-	58	V
		I_{PPM} = 2.5 A; T_{amb} = 25 °C	[1][2]	-	-	80	V
R_{dyn}	dynamic resistance	T_{amb} = 25 °C	[3]	-	9.5	-	Ω

[1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321.
[2] Measured from pin 1 to pin 2.
[3] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.



T_{amb} = 25 °C

Fig. 3. Rated peak pulse power as a function of square pulse duration; maximum values

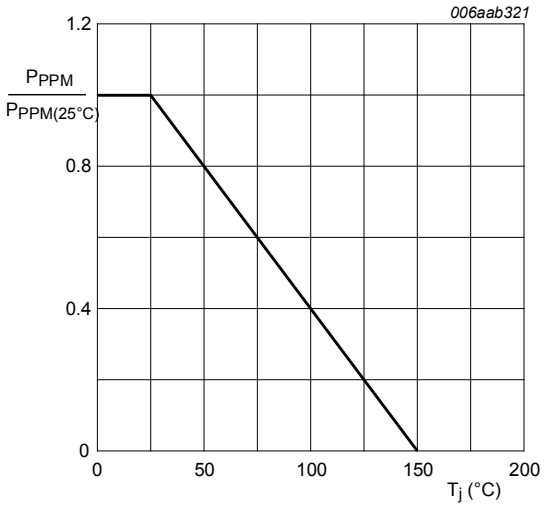
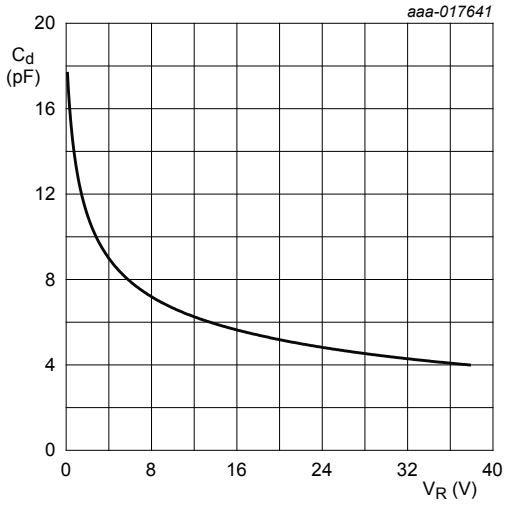


Fig. 4. Relative variation of rated peak pulse power as a function of junction temperature; typical values



f = 1 MHz; T_{amb} = 25 °C

Fig. 5. Diode capacitance as a function of reverse voltage; typical values

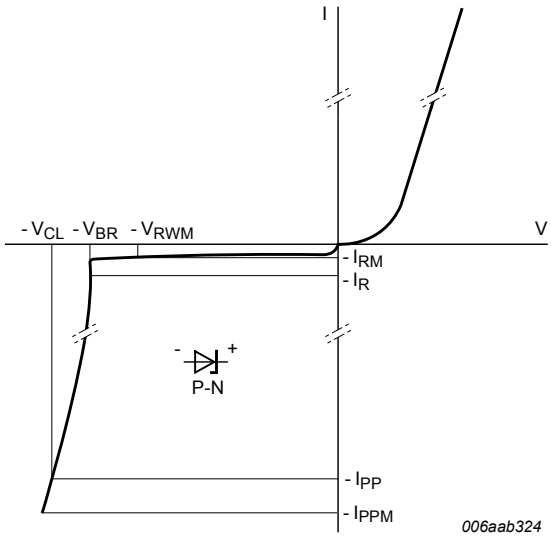


Fig. 6. V-I characteristics for a unidirectional ESD protection diode

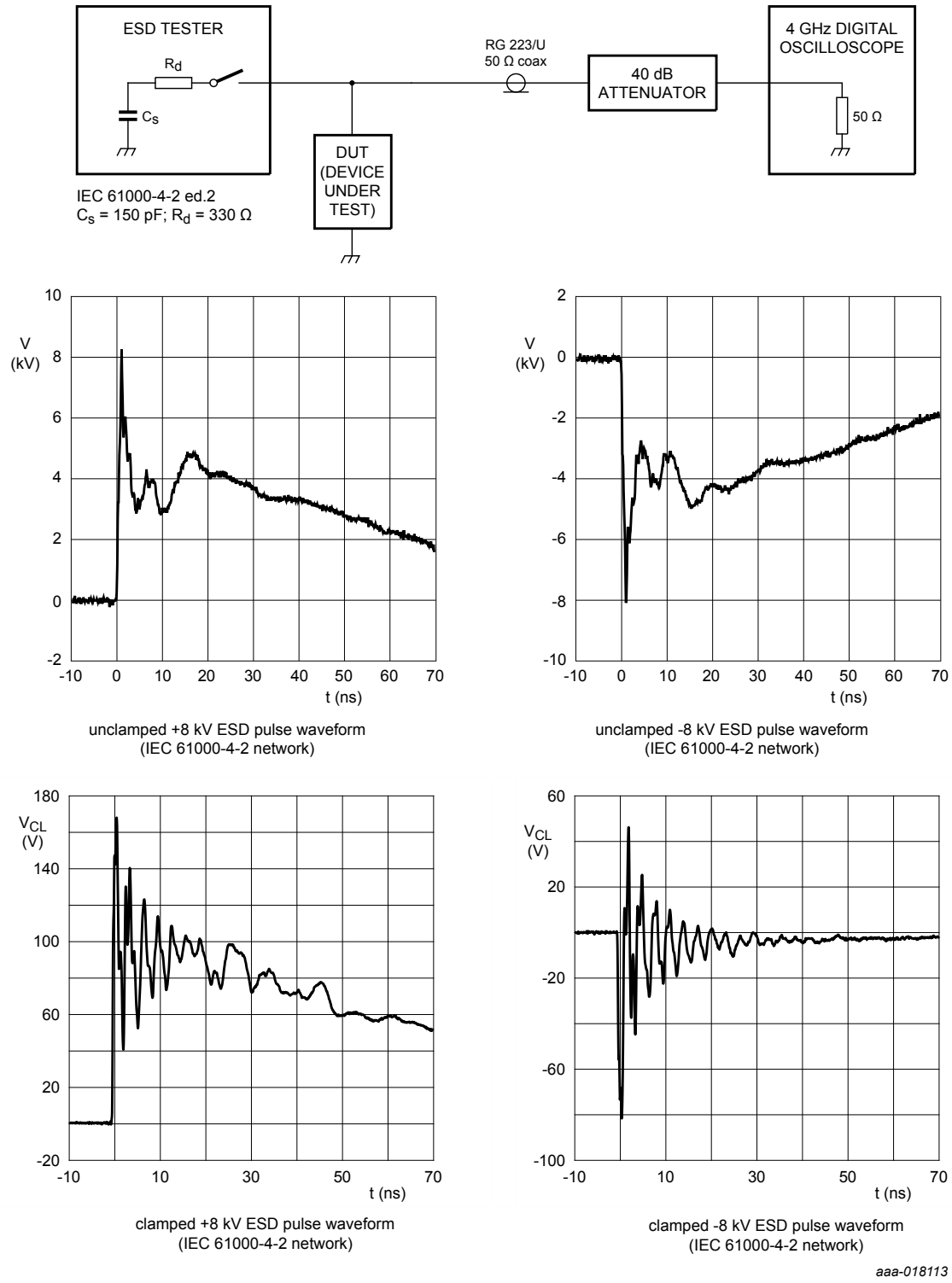


Fig. 7. ESD clamping test setup and waveforms

10. Application information

The device is designed for the protection of one unidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are either positive or negative with respect to ground. The device provides a surge capability of 150 W for an 8/20 µs waveform.

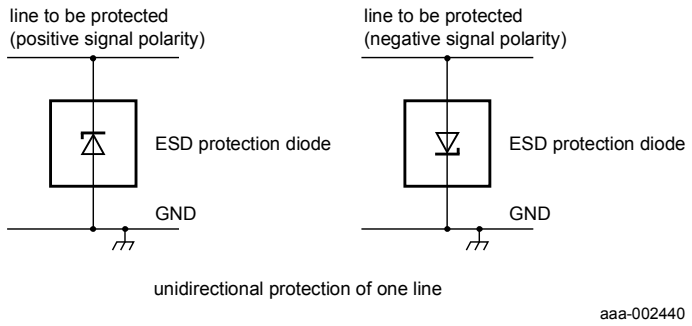


Fig. 8. Application diagram

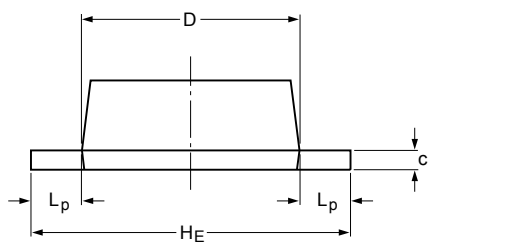
Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

Plastic surface-mounted package; 2 leads **SOD323F**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	H_E	L_p	w
mm	0.80 0.65	0.40 0.25	0.25 0.10	1.8 1.6	1.35 1.15	2.7 2.3	0.5 0.3	0.1

Note
1. The marking bar indicates the cathode

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOD323F			SC-90			~~04-09-13~~ 06-03-16

Fig. 9. Package outline SOD323F

12. Soldering

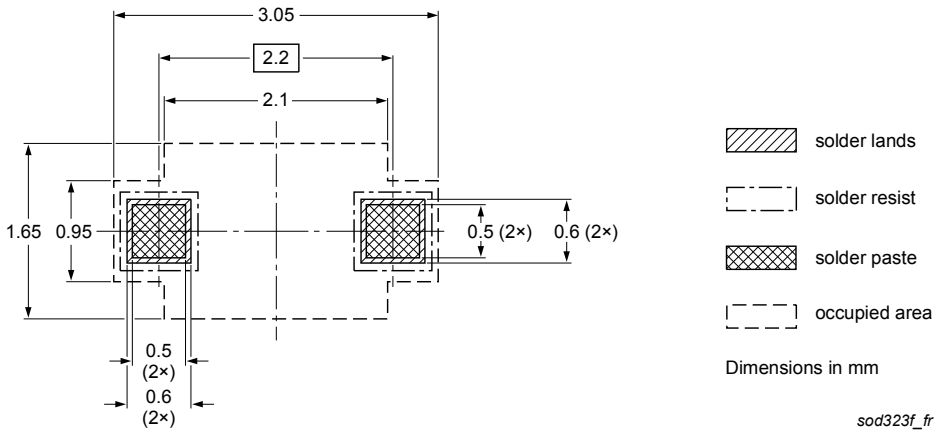


Fig. 10. Reflow soldering footprint for SOD323F

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD36VS1UJ v.1	20150916	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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15. Contents

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