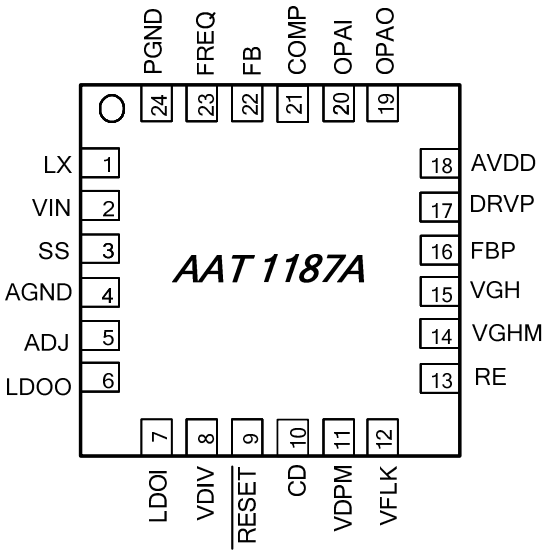
BOOST CONVERTER FOR WLED DRIVER

FEATURES

- **Built in 2A (Max.), 0.2Ω Switching NMOS**
- **Positive Charge Pump for Gate-High Supply**
- **V_{COM} Operational Amplifier**
- **Up to 350mA LDO**
- **Reset Signal Output for T-CON**
- **28V High Voltage Switch for VGHM**
- **Adjustable Soft-Start Function**
- **640kHz / 1.2MHz Selectable Switching Frequency**
- **Fault and Thermal Protection**
- **Low Dissipation Current : Typical 2.3mA in Operation**
- **QFN-24 Package Available**

PIN CONFIGURATION



GENERAL DESCRIPTION

The AAT1187A provides a boost PWM controller, positive charge pump, low dropout linear regulator, V_{COM} operational amplifier and one high voltage switch (up to 28V) for TFT LCD display. $\overline{\text{RESET}}$ pin will issue a reset signal to T-CON when V_{IN} voltage is too low.

The PWM controller consists of an on-chip voltage reference, oscillator, error amplifier, current sense circuit, comparator, under-voltage lockout protection and soft-start control circuit. The thermal and power fault protection prevents excessive power from damaging internal circuit.

The positive charge pump generates VGH voltage (gate high voltage) setting by external resistor divider. For the flicker compensation, VGHM will be connected to VGH when VFLK is high and connected to RE when VFLK goes low.

The AAT1187A contains one operational amplifier capable of supplying 200mA to V_{COM}.

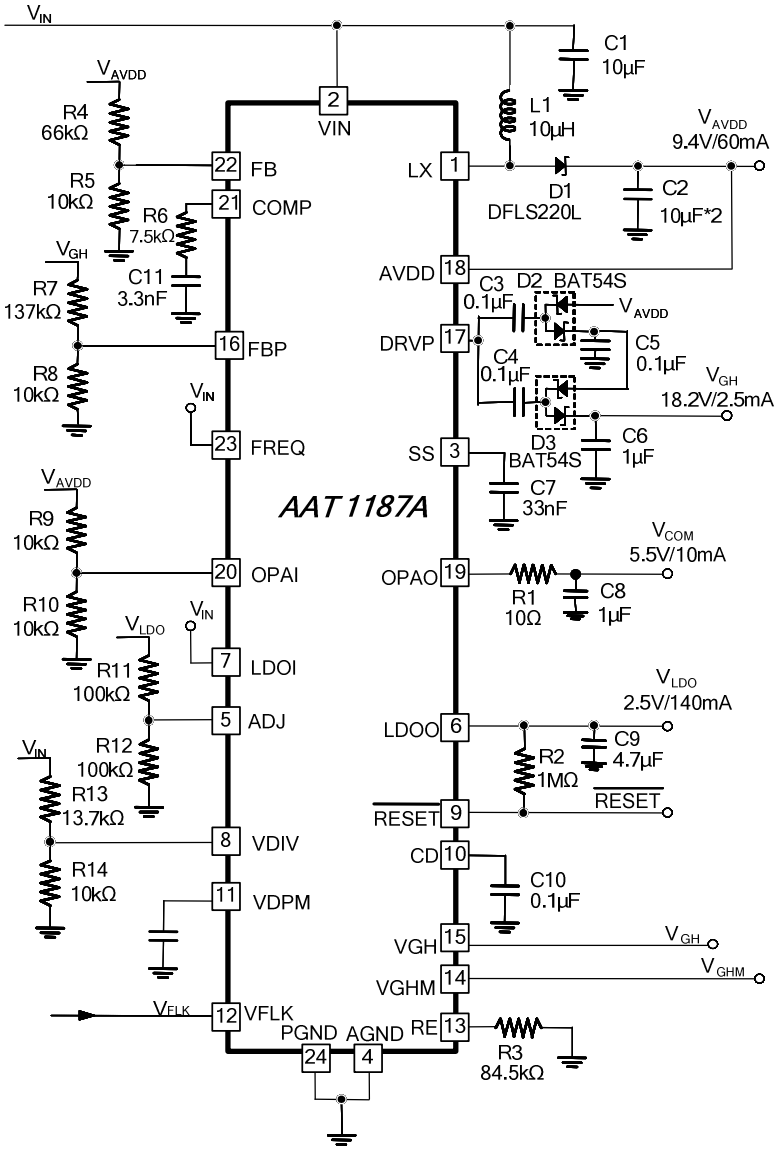
With the minimal external components, the AAT1187A offers a simple and economical solution for TFT LCD power.

ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT1187A	AAT1187A-Q7-T	Q7:VQFN 24-4*4	T: Tape and Reel	–40°C to +85°C	TBA	TBA

Note: All AAT products are lead free and halogen free.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
VIN, VFLK, LDOI to AGND	V_{IN}	7	V
AVDD, LX to AGND	V_{H1}	16	V
VGH to AGND	V_{H2}	30	V
DRVP to AGND	V_{H3}	16	V
Input Voltage 1 (FB, FBP, ADJ , VDIV, CD, VDPM, SS, FREQ)	V_{I1}	V_{IN} +0.3	V
Input Voltage 2 (OPAI)	V_{I2}	V_{H1} +0.3	V
Output Voltage 1 (COMP, $\overline{\text{RESET}}$, LDOO, VREF)	V_{O1}	V_{H1} +0.3	V
Output Voltage 2 (OPAO, DRVP)	V_{O2}	V_{H1} +0.3	V
Output Voltage 3 (RE, VGHM)	V_{O3}	V_{H2} +0.3	V
Operating Ambient Temperature Range	T_C	–40 to +85	°C
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
Package Thermal Resistance	θ_{JA}	36	°C /W
Power Dissipation, @ T_C = +25°C , T_J = +125 °C	P_d	2.78	W

Note:
1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.
2. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, V_{AVDD} = 10V, unless otherwise specified.)

Operating Power

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VIN Input Voltage Range	V_{IN}		2.5	-	5.5	V
AVDD Input Voltage Range	V_{AVDD}		6	-	15	V
VIN Under Voltage Lockout	V_{UVLO}	Rising	2.11	2.21	2.31	V
		Falling	2.01	2.11	2.2	
VIN Operating Current	I_{VIN}	V_{FB} = 1.5V, Not Switching	-	0.4	0.8	mA
		V_{FB} = 1.2V, Switching	-	2.3	5.0	mA
AVDD Operating Current	I_{AVDD}	V_{OPAI} = 4V	-	1.2	3.0	mA
LDOI Operating Current	I_{LDOI}	V_{LDOI} = 5V, I_{LDOO} = 0mA	-	0.2	0.4	mA
Thermal Shutdown	T_{SHDN}		-	160	-	°C

Oscillator

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Oscillation Frequency	f_{OSC}	FREQ = Low	540	640	740	kHz
		FREQ = High	1.0	1.2	1.4	MHz
Maximum Duty Cycle	D_{MAX}		86	90	94	%

Soft Start & Fault Detect

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Channel 1 Soft Start Current	I_{SS}	V_{SS} = 1V	2	4	6	µA
During Fault Protect Trigger Time	t_{FP}		150	164	180	ms
FB Fault Protection Voltage	V_{F1}		1.00	1.05	1.10	V
FBP Fault Protection Voltage	V_{F3}		1.00	1.05	1.10	V

EIECTRICAL CHERACTERISTICS

(V_{IN} = 3.3V, V_{AVDD} = 10V, unless otherwise specified.)

Error Amplifier (Channel 1)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Feedback Voltage	V_{FB}		1.228	1.240	1.252	V
Input Bias Current	I_{B1}	V_{FB} = 1V to 1.5V	–40	0	+40	nA
Feedback-Voltage Line Regulation		Level to Produce V_{COMP} = 1.24V 2.3V < V_{IN} < 5.5V	-	0.05	0.15	%/V
Transconductance	G_m	ΔI = 5μA	70	105	240	μS
Voltage Gain	A_V		-	700	-	V/V

N-MOS Switch (Channel 1)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Current Limit	I_{LIM}		1.5	2.0	2.5	A
On-Resistance	R_{ON}	I_{LX} = 1.0A	-	0.2	0.5	Ω
Leakage Current	I_{LXOFF}	V_{LX} = 12V	-	0.01	20.0	μA

Positive Charge Pump (Channel 3)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
FBP Threshold Voltage	V_{FBP}		1.216	1.240	1.264	V
FBP Input Bias Current	I_{B3}	V_{FBP} = 1.5V	–50	-	+50	nA
DRVP Switch R-on	R_{ONP3}		-	20	40	Ω
	R_{ONN3}		-	20	40	Ω
Continuous Output Current	I_{DRVP}		20	-	-	mA

EIECTRICAL CHERACTERISTICS

(V_{IN} = 3.3V, V_{AVDD} = 10V, unless otherwise specified.)

Low Voltage LDO

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{LDOI}		2.5	-	5.5	V
ADJ Threshold Voltage	V_{ADJ}	I_{LDOO} = 100mA	1.224	1.240	1.256	V
ADJ Input Bias Current	I_{B4}	V_{ADJ} = 0V to 1.5V	–40	0	+40	nA
Dropout Voltage	V_{DROP}	I_{LDOO} = 250mA	-	350	500	mV
LDO Output Current	I_{LDOO}		350	-	-	mA
LDO Output Current Limit	I_{LIMO}		450	600	750	mA
Line Regulation		Measure V_{ADJ}, V_{LDOI} = 2.5V ~ 5V	-	-	5	%/V
Load Regulation		Measure V_{ADJ}, I_{LDOO} = 20mA ~ 300mA	-	-	0.1	%/mA

High Voltage Switch Controller

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VFLK Input Low Voltage	V_{IL}		-	-	0.5	V
VFLK Input High Voltage	V_{IH}		2	-	-	V
VFLK Input Bias Current	I_{B5}	V_{FLK} = 0 to V_{IN}	–40	0	+40	nA
VDPM Charge Current	I_{DPM}	V_{DPM} = 1V	18	20	22	µA
Propagation Delay VFLK to VGHM (form Low to High)	t_{PPLH}	V_{GH} = 25V	-	170	500	ns
Propagation Delay VFLK to VGHM (form High to Low)	t_{PPHL}	V_{GH} = 25V	-	110	500	ns
VGH to VGHM Switch R-on	R_{ONSC}	V_{DPM} = 1.5V, V_{FLK} = V_{IN}	-	30	60	Ω
RE to VGHM Switch R-on	R_{ONDC}	V_{DPM} = 1.5V, V_{FLK} = V_{AGND}	-	50	100	Ω

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, V_{AVDD} = 10V, unless otherwise specified.)

Reset Output

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Operating Voltage	V_{OP}		1.6	-	-	V
$\overline{RESET}$ Output Voltage	$V_{\overline{RESET}}$	$I_{\overline{RESET}}$ = 1.2mA	-	-	0.2	V
VDIV Threshold Voltage	V_{DIV}		1.0	1.1	1.2	V
CD Source Current	I_{CD}	V_{CD} = 1V	5	10	15	µA
CD Threshold Voltage	V_{CD}		1.20	1.24	1.28	V

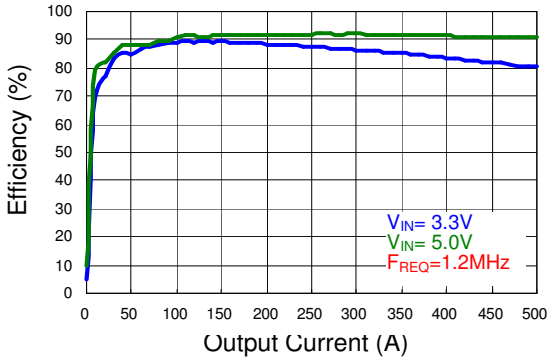
V_{COM} Buffer

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Offset Voltage	V_{OS}	V_{OPAI} = 4V	-	2	12	mV
Input Bias Current	I_{B6}	V_{OPAI} = 4V	–40	0	+40	nA
Output Swing	V_{OH}	I_{OPAO} = –50mA, V_{OPAI} = 4V	-	4.03	4.05	V
	V_{OL}	I_{OPAO} = 50mA, V_{OPAI} = 4V	3.95	3.97	-	
Short Circuit Current	I_{SHORT}	Measure I_{OPAO}	±150	±250	±350	mA
Slew Rate	SR	V_{OPAI} = 2V to 8V, V_{OPAI} = 8V to 2V, 20% to 80%	–1	+12	-	µs
Settling Time	t_S	V_{OPAI} = 3.5V to 4.5V, 90%	-	5	20	µs

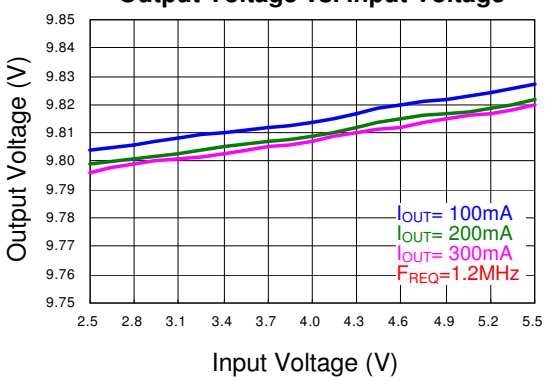
TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 3.3 V, V_{AVDD} = 9.8 V, V_{LDO} = 2.5 V, V_{GL} = –6.8 V, V_{GH} = 18 V, T_C = +25°C , unless otherwise noted.)

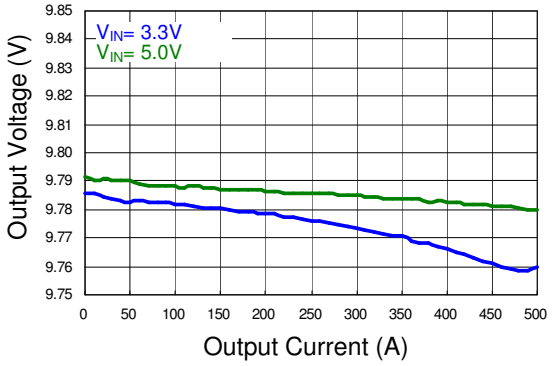
Boost Converter
Efficiency vs. Output Current



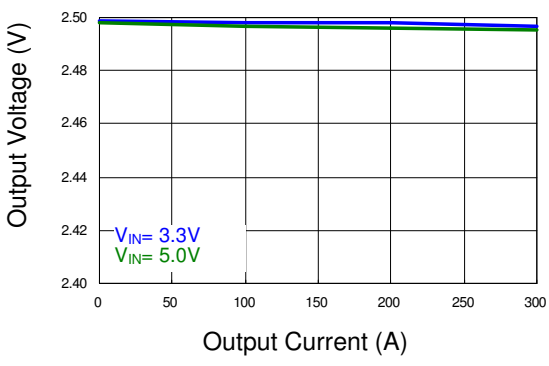
Boost Converter
Output Voltage vs. Input Voltage



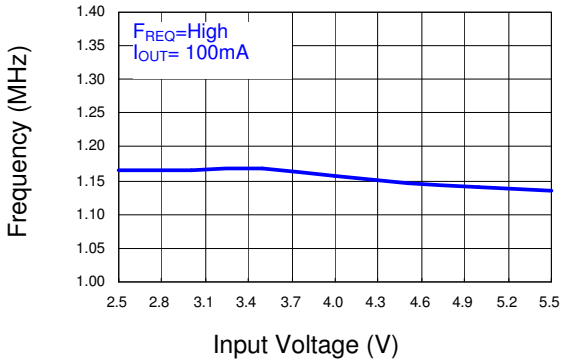
Boost Converter
Output Voltage vs. Output Current



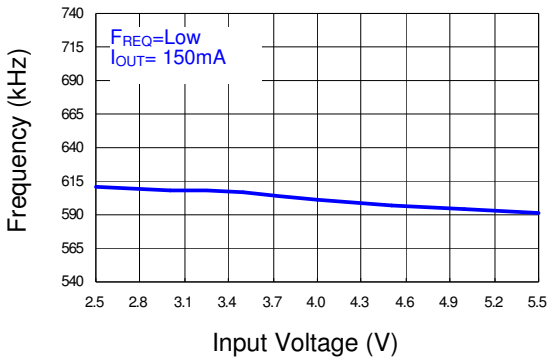
Low Voltage LDO
Output Voltage vs. Output Current



Boost Converter
Frequency vs. Input Voltage



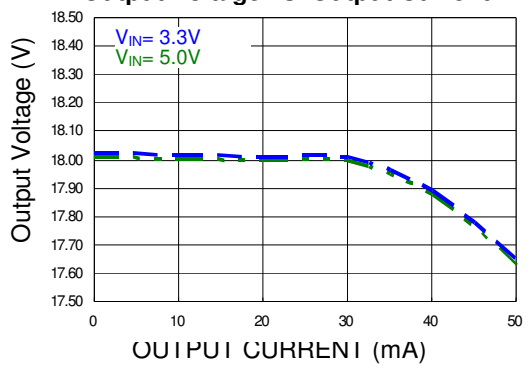
Boost Converter
Frequency vs. Input Voltage



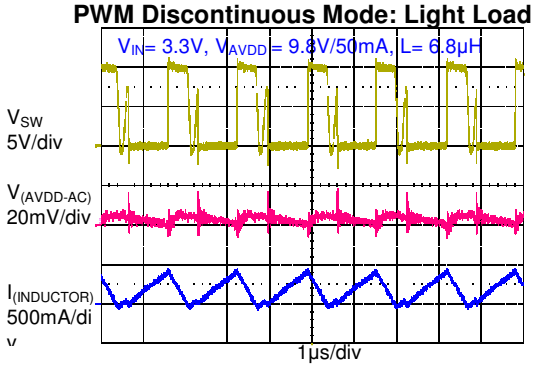
TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 3.3 V, V_{AVDD} = 9.8 V, V_{LDO} = 2.5 V, V_{GL} = –6.8 V, V_{GH} = 18 V, T_C = +25°C , unless otherwise noted.)

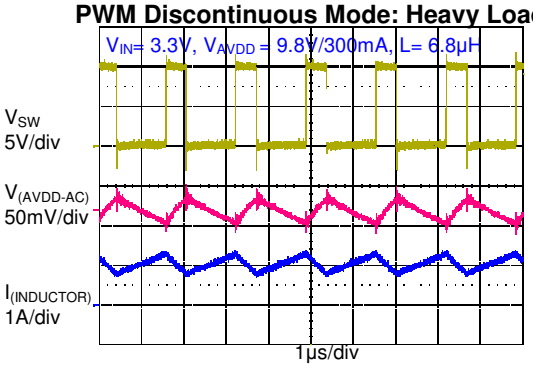
Positive Charge Pump
Output Voltage vs. Output Current



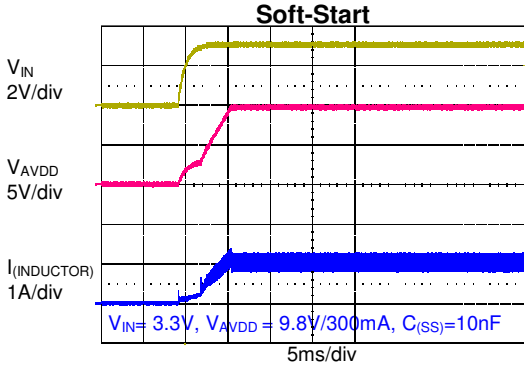
Boost Converter
PWM Discontinuous Mode: Light Load



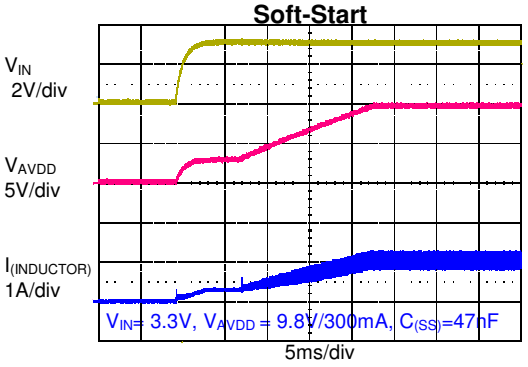
Boost Converter
PWM Discontinuous Mode: Heavy Load



Boost Converter
Soft-Start



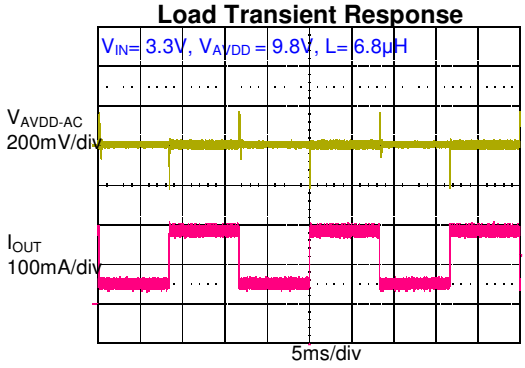
Boost Converter
Soft-Start



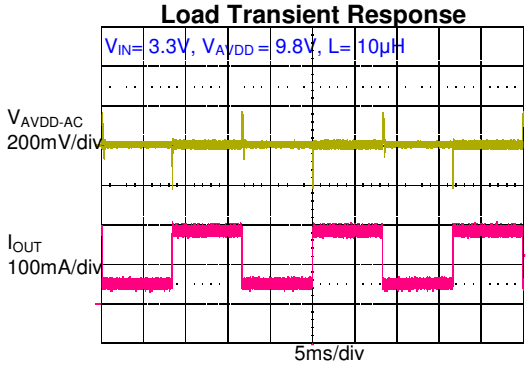
TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 3.3 V, V_{AVDD} = 9.8 V, V_{LDO} = 2.5 V, V_{GL} = –6.8 V, V_{GH} = 18 V, T_C = +25°C , unless otherwise noted.)

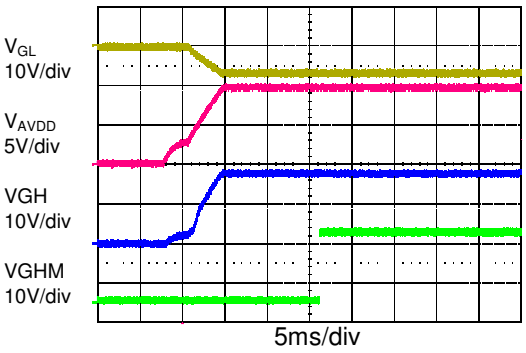
Boost Converter Load Transient Response



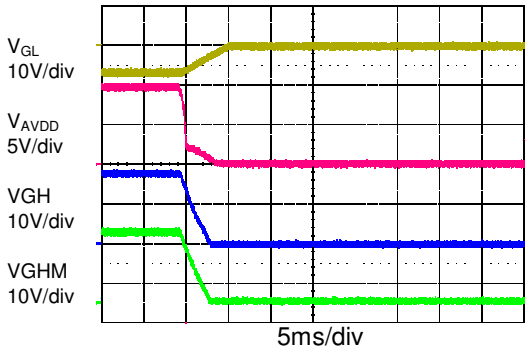
Boost Converter Load Transient Response



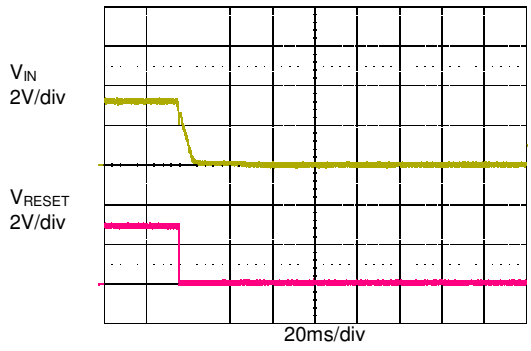
Power-On Sequence



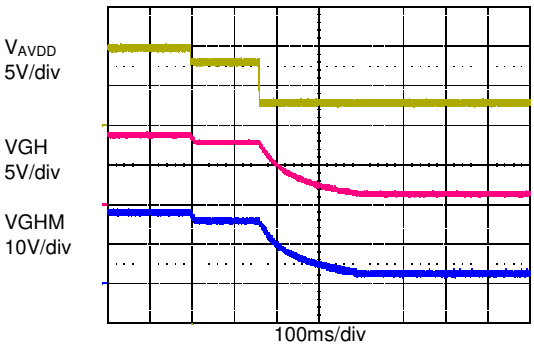
Power-Off Sequence



Reset Output Waveform



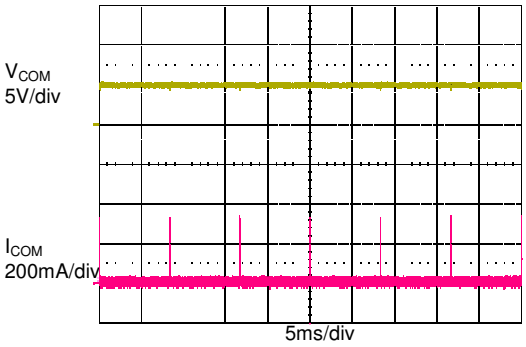
Fault Protection Waveform



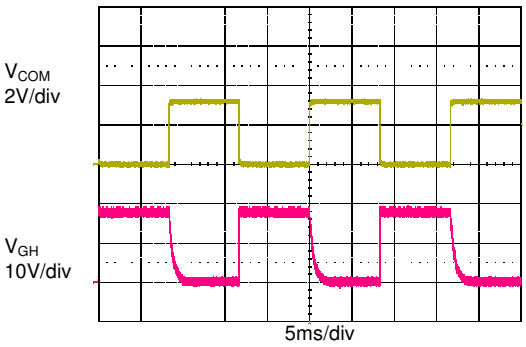
TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 3.3 V, V_{AVDD} = 9.8 V, V_{LDO} = 2.5 V, V_{GL} = –6.8 V, V_{GH} = 18 V, T_C = +25°C , unless otherwise noted.)

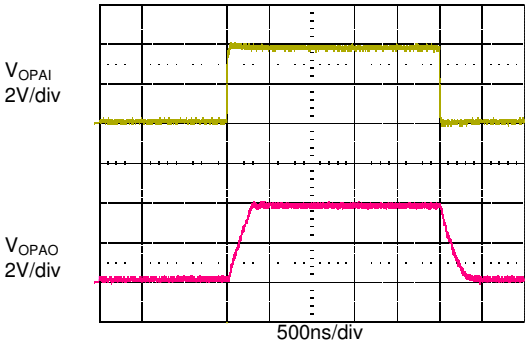
V_{COM} Buffer Waveform



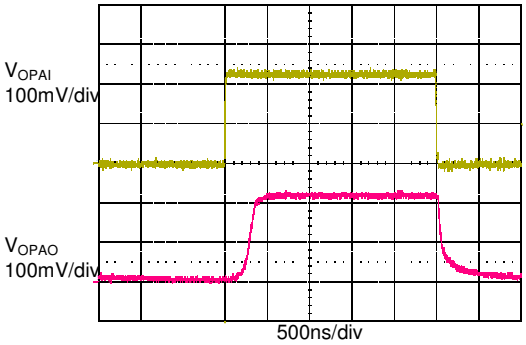
High Voltage Switch Control Waveform



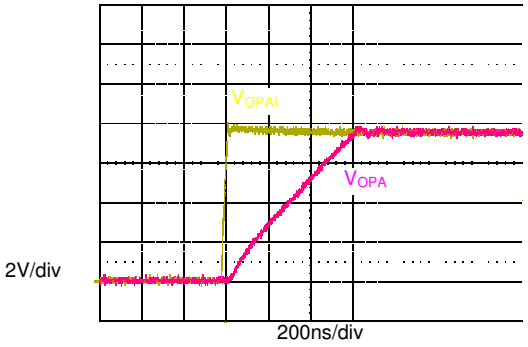
V_{COM} Large Signal Waveform



V_{COM} Small Signal Waveform



V_{COM} Slew Rate Waveform

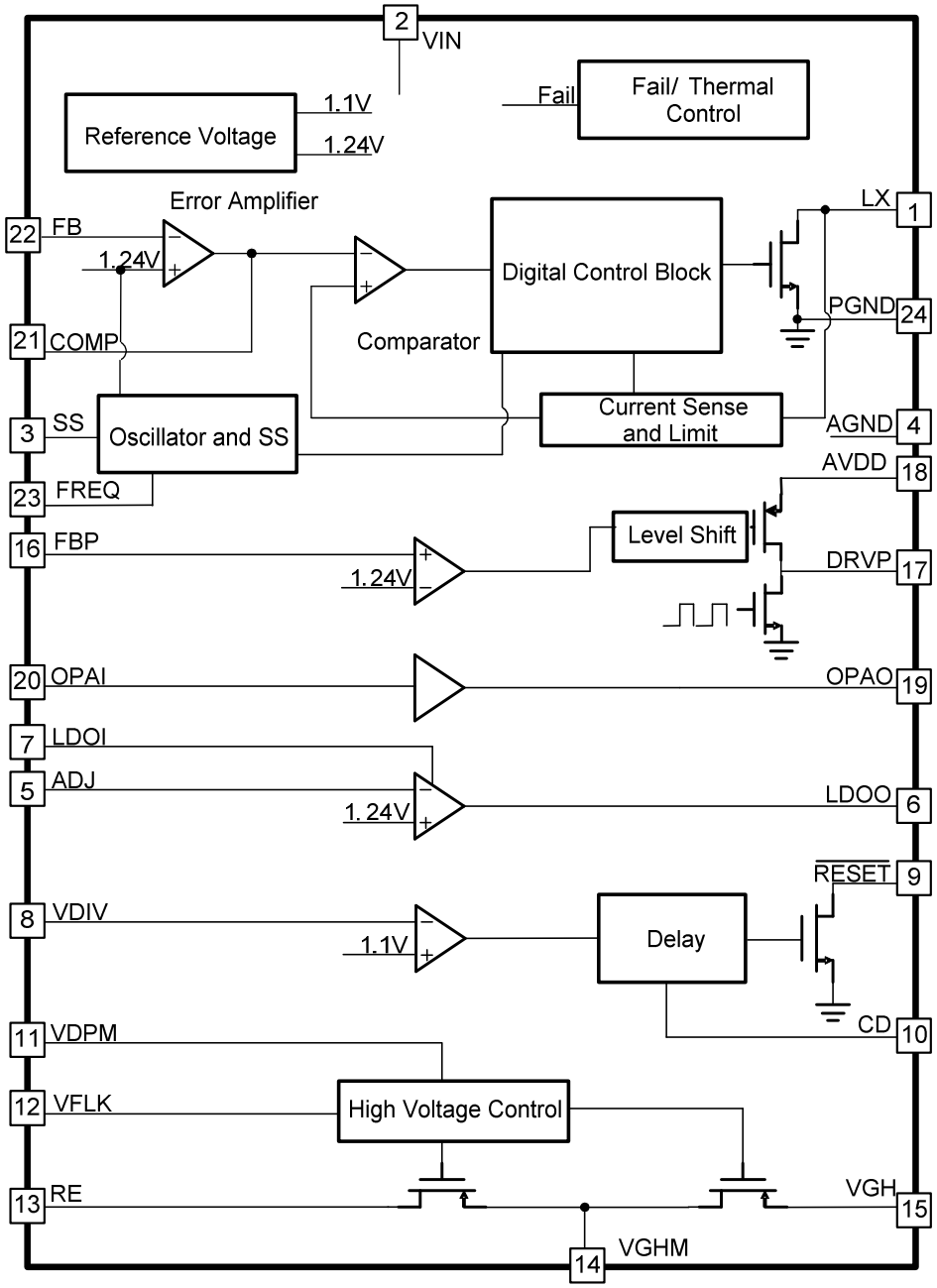


PIN DESCRIPTION

PIN No. QFN-24	NAME	I/O	DESCRIPTION
1	LX	-	Main PWM Switching Pin
2	VIN	-	Power Supply Input
3	SS	I	Main PWM Soft Start Control Pin
4	AGND	-	Ground
5	ADJ	I	Low Voltage LDO Feedback Pin
6	LDOO	O	Low Voltage LDO Output Pin
7	LDOI	-	Low Voltage LDO Power Pin
8	VDIV	I	Reset Signal Detection Input
9	$\overline{\text{RESET}}$	O	Reset Signal Output
10	CD	I	Reset Signal Delay Control
11	VDPM	I	High Voltage Switch Enable Pin
12	VFLK	I	High Voltage Switch Control Pin
13	RE	O	Gate High Voltage Fall Time Setting Pin
14	VGHM	O	Switching Gate High Voltage for TFT
15	VGH	-	Gate High Voltage Input (Channel 3 Output Voltage)
16	FBP	I	Positive Charge Pump Regulated Voltage Feedback Pin
17	DRVP	O	Positive Charge Pump Output
18	AVDD	-	High Voltage Power Supply Input
19	OPAO	O	Operational Amplifier Output
20	OPAI	I	Operational Amplifier Positive Input
21	COMP	O	Main PWM Error Amplifier Output
22	FB	I	Main PWM Feedback Pin
23	FREQ	I	Frequency Select Pin
24	PGND	-	LX MOS Ground

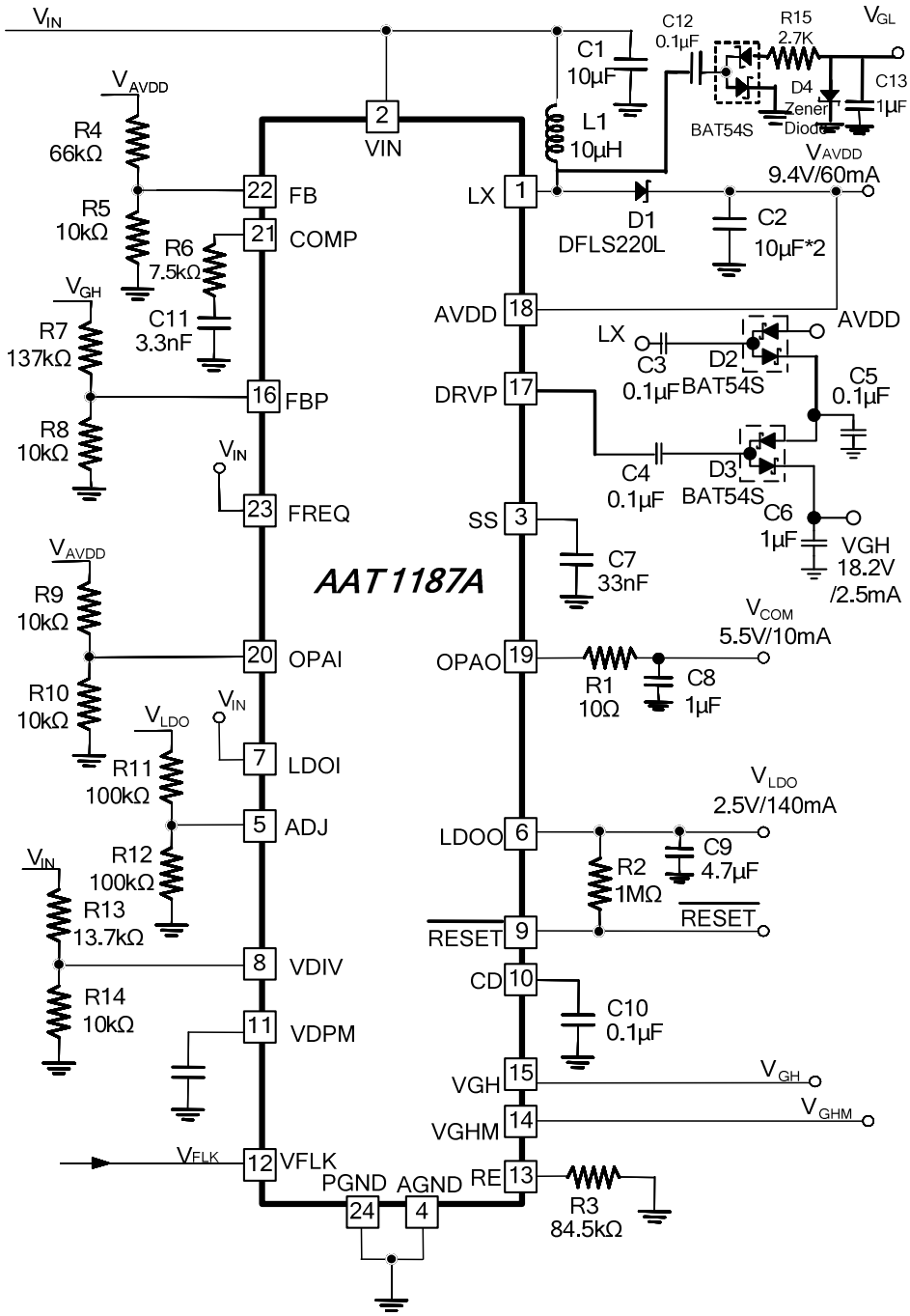
FUNCTION BLOCK DIAGRAM

AAT1187A



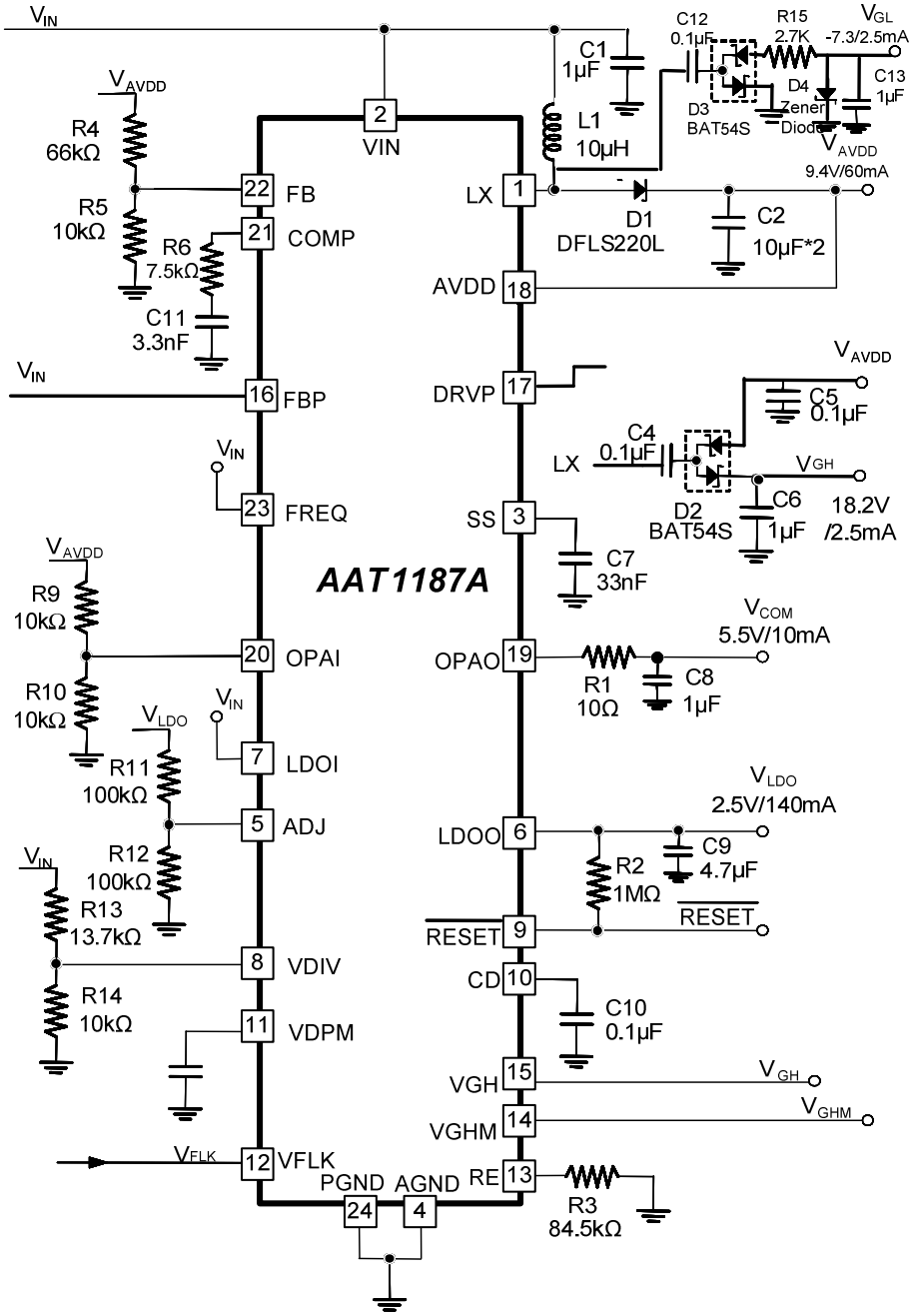
TYPICAL APPLICATION CIRCUIT

AAT1187A Normal Circuit



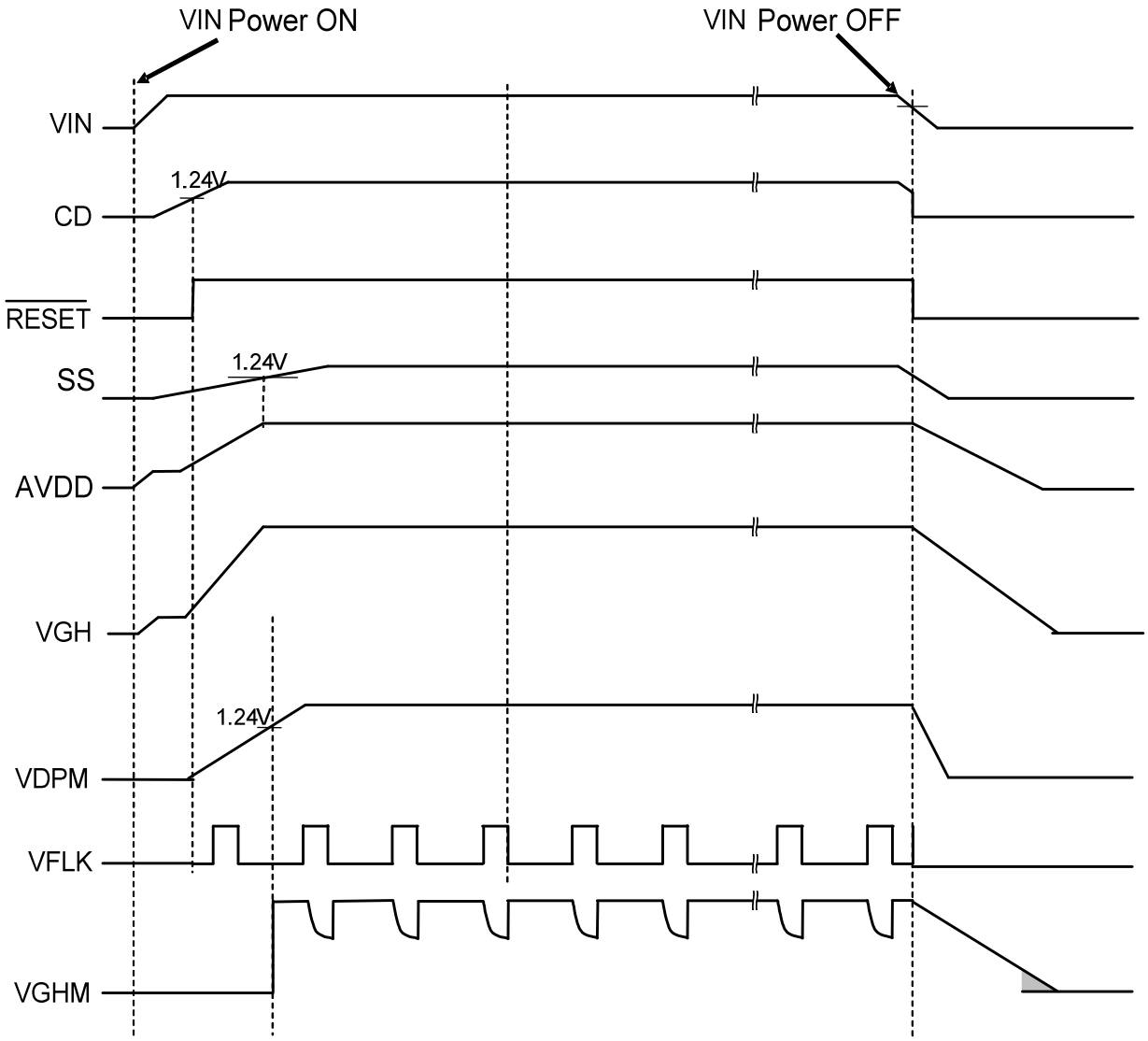
TYPICAL APPLICATION CIRCUIT

AAT1187A Circuit for DRVP Floating



POWER ON AND POWER OFF TIMING CHART

AAT1187A



DETAILED DESCRIPTION

The AAT1187A is a compact power solution designed for TFT LCD panels. It consists of a current mode boost pulse-width modulation, positive charge pump regulator, rail-to-rail buffer, low voltage high driving LDO, GPM function, and reset function.

Boost DC-DC Converter

The inductor undergoes current rise during on time. When the inductor current reaches a current tri-point predetermined by internal error amplifier, power MOS turns off, and energy stored in inductor is released to boost regulated output voltage. The internal error amplifier output (EO) determines the necessary current amount to support the load.

Frequency Selection

The AAT1187A has a frequency selection pin, which allows users to set operational frequency to 640kHz or 1.2MHz. Connecting FREQ pin to VDD, users may operate the device at 1.2MHz switching frequency. In addition, the boost regulated output voltage also has a lower output ripple voltage. When working with a 640kHz switching frequency, simply connect FREQ pin to ground or leave it floating as FREQ pin is equipped with internal 5µA pull down current.

Under Voltage Lockout

To avoid abnormal operation at lower VDD voltage, the under voltage lockout function (UVLO voltage 2.1V) monitors the controller. When VDD falls bellow UVLO voltage, AAT1187A disables functions including boost pulse-width modulation function, positive charge pump regulator, GPM, and buffer function. LDO, bandgap reference, and reset function remain enabled.

Fault Protection

Fault protection in AAT1187A includes the following:

OVC :

OVC is a cycle-by-cycle current limit in boost controller, which limits peak inductor current UVP. When boost feedback voltage and positive charge pump feedback voltage falls under 85% of the default setting, AAT1187A activates timer. If UV condition remains at 160ms, AAT1187A launches fault latch.

OTP (Over Temperature Detection):

When junction temperature exceeds 160 °C , AAT1187A activates timer. If OTP condition remains for 160ms, AAT1187A launches fault latch.

Setting the Boost Soft-Start

The AAT1187A has an adjustable soft-start function to prevent high inrush current during start up. The soft-start function can be implemented with an external capacitor with a 4µA constant current.

When V_{IN} voltage is higher than UVLO value, a 4µA constant current charges an external capacitor $C_{SS.}$ When SS voltage is higher than the V_{FB} voltage, the boost controller starts and rises to V_{AVDD} voltage. The Soft-start function would be completed when SS reaches 1.24V.

$$SS = \frac{I_{SS}}{C_{SS}} \times T_{SS}$$

The typical soft-start capacitance ranges from 22nF to 220nF. A 100nF capacitor is usually sufficient for most of the applications.

DESIGN PROCEDURE

Boost Converter Design

Inductor Selection

The minimum inductance value, resistance of the resistors in series connection, and peak current rating are important factors that influence converter efficiency.

The minimum value of inductor is selected to ensure that the system operates in continuous conduction mode (CCM) for high efficiency and EMI-free performance. The equation of inductor selection uses a parameter κ, which is the ratio of peak to peak ripple current of the inductor to the input DC current. The best trade-off between voltage ripple of transient output current and permanent output current has a κ between 0.2 and 0.4.

$$L \geq \frac{\eta V_O}{\kappa I_O f_S} D(1-D)^2, \quad D = 1 - \frac{V_{IN}}{V_O}, \quad \kappa = \frac{\Delta I_{Lpeak\text{-}peak}}{I_{IN}}$$

η: Boost Converter Efficiency

κ: Ratio of the Inductor Peak-to-Peak Ripple Current and the Input DC Current

V_{IN}: Input Voltage

V_O: Output Voltage

I_O: Output Load Current

f_S: Switching Frequency

D: Duty Cycle

$\Delta I_{Lpeak\text{-}peak}$: Inductor Peak-to-Peak Ripple Current

I_{IN}: Input DC Current

The AAT1187A SW current limit (I_{LIM}) and inductor's saturation current rating (I_{LSAT}) should exceed $I_{L(peak)}$, and the inductor's DC current rating should exceed I_{IN}. For optimal efficiency, choose an inductor with less DC resistance (r_L). ESR DSR DCR

I_{LIM} and $I_{LSAT} > I_{L(peak)}$

$I_{LDC} > I_{IN}$

$$I_{L(peak)} = I_{IN} + \frac{V_{IN} D}{2Lf_S},$$

$$I_{IN} = \frac{I_O}{\eta(1-D)}, \quad P_{DCR} \approx \left(\frac{I_O}{\eta(1-D)}\right)^2 r_L$$

I_{LDC}: DC Current Rating of Inductor

P_{DCR}: Power Loss of Inductor Resistance

Table 1. Inductor Data List

C6-K1.8L	r_L	DC CURRENT RATING
3.9µH	41mΩ	2.5A
6.8µH	68mΩ	2.2A
10.0µH	81mΩ	1.8A
MITSUMI Product-Max Height: 1.9mm		

Example: In the typical application circuit, output load current is 200mA with 8.6V output voltage and input voltage of 3.3V. Choose a κ of 0.3 and efficiency of 90%.

$$L \geq \frac{0.9 \times 8.6}{0.3 \times 0.2 \times (1.2)^6} \times 0.6163 \times (0.3837)^2 \approx 10\mu H$$

$$I_{IN} = \frac{I_O}{\eta(1-D)} = 0.579A$$

$$I_{L(peak)} = I_{IN} + \frac{V_{IN} D}{2Lf_s} = 0.664A$$

P_{DCR} = 0.0272W or 1.58% power loss

Rectifier Diode Selection

The Schottky diode is a recommended component for the switching converter. To achieve optimal efficiency, choose a Schottky diode with less recovery capacitor (C_T) for shorter recovery time and lower forward voltage (V_F).

For boost converter, reverse voltage rating (V_R) should be higher than maximum output voltage, and the current rating should exceed the maximum inductor current.

$P_{DIODE} = P_{DSW} + P_{DCOM}$
$P_{DSW} = (1–D)\ V_F Q_R f_S$
$Q_R = V_R C_T$
$P_{DCOM} = V_F I_O\ (1–D)$
P_{DIODE}: Total Power Loss of Diode for Boost Converter
P_{DSW}: Switching Loss of Diode for Boost Converter
P_{DCOM}: Conduction Loss of Diode for Boost Converter

Table 2. Schottky Data List

SMA	V_F	V_R	C_T
B220A	0.24V	14V	150pF
B240A	0.24V	28V	150pF
DIODES Product-MAX Height: 2.3mm			

For example,
$P_{DIODE} = P_{DSW} + P_{DCOM} = 0.203W$ or 5.1% power loss.

Input Capacitor Selection

The input capacitors have two important functions in a PWM controller. First, an input capacitor provides power for soft-start procedure, and supply current for the gate-driving circuit. A 10µF ceramic capacitor is sufficient for most of the applications. Second, an input bypass capacitor reduces the current peaks when the input voltage drops and noise interferences with the IC. A low ESR ceramics capacitor with 0.1µF capacitance is used in a typical circuit. The bypass capacitor should be placed as close as possible from V_{IN} (Pin2) to PGND (Pin24). V_{IN} is decoupled from input capacitor with an RC low pass filter to ensure noise-free power.

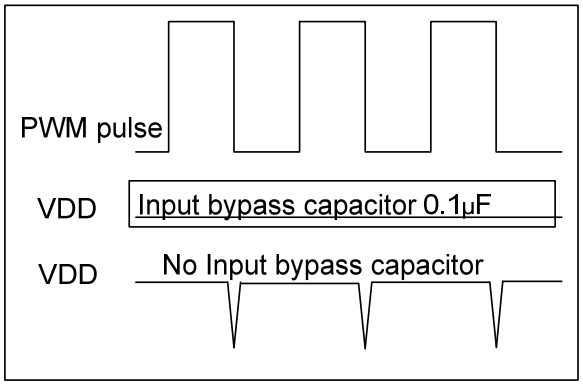


Figure 1. Input Bypass Capacitor Results in V_{DD} Drop

V_{AVDD} Output Capacitor Selection

The output capacitor maintains the DC output voltage at a certain level. A Low ESR (r_C) ceramic capacitor is recommended to allow smaller output ripple and lower power loss.

There are two parameters, which can affect the output voltage ripple:

1. Voltage drops when the inductor current flows through the ESR of output capacitor
2. Charging and discharging of the output capacitor

$$V_{RIPPLE} = V_{RIPPLE}(C_{OUT}) + V_{RIPPLE}(ESR)$$

$$V_{RIPPLE}(C_{OUT}) \approx \frac{I_O D}{f_S C_{OUT}}$$

$$V_{RIPPLE}(ESR) \approx I_{L(peak)} r_C$$

$$P_{ESR} = (I_{Lpeak})^2 . r_C$$

ESR: Equivalent Series Resistance

Example2: C_{OUT} = 38µF, r_C = 20mΩ

V_{RIPPLE} (C_{OUT}) = 4mV

V_{RIPPLE} (ESR) = 22mV

V_{RIPPLE} = 26mV

P_{ESR} = 0.023W or 0.6% power loss

Setting the V_{AVDD} Output Voltage

The V_{AVDD} output voltage of main PWM converter is set by the resistor divider between the output (V_{AVDD}) and GND with a center tap connected to FB. V_{FB} is the main PWM feedback with a typical voltage value of 1.24V.

Choose R_2 (Figure 2) between 5.1kΩ and 51kΩ and calculate R_1 to satisfy the following equation.

$$R_1 = R_2\left(\frac{V_{AVDD}}{V_{FB}} - 1\right), \quad V_{AVDD} = V_{FB}\left(1 + \frac{R_1}{R_2}\right)$$

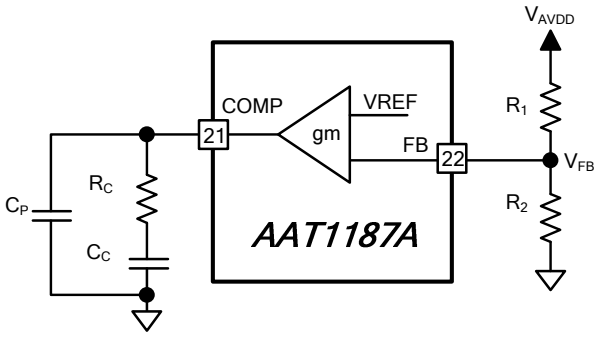


Figure 2. Feedback Circuit

Loop Compensation Design

The voltage-loop gain with current loop closed sets the stability of a steady state response and dynamic performance of transient response. The loop compensation design is as follows:

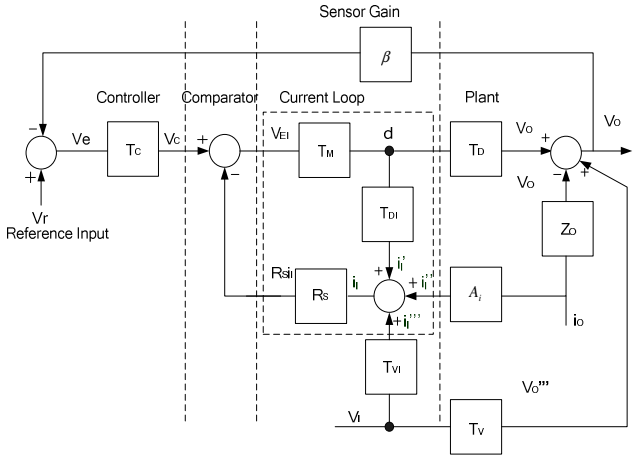


Figure 3. Closed-Current Loop for Boost with PCM

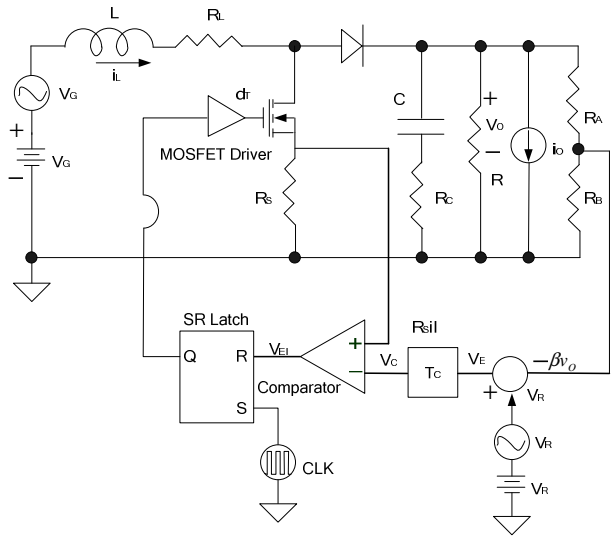


Figure 4. Block Diagram of Boost Converter with Peak Current Mode (PCM)

Power Stage Transfer Functions

The duty to output voltage transfer function T_p is:

$$T_p(s) = \frac{V_o}{d} = T_{p0}\frac{(s + w_{esr})(s - w_{z2})}{s^2 + 2\xi w_n s + w_n^2}$$

$$\text{Where } T_{p0} = V_O\frac{-r_c}{(1-D)(R_L + r_c)}, w_{esr} = \frac{1}{Cr_c}$$

And

$$w_{z2} = \frac{R_L(1-D)^2 - r}{L}, w_n = \sqrt{\frac{(1-D)^2 R_L + r}{LC(R_L + r_c)}}$$

$$\xi = \frac{C[r(R_L + r_c) + R_L r_c(1-D)^2] + L}{2\sqrt{LC(R_L + r_c)[r + (1-D)^2 R_L]}},$$

$$r = r_L + Dr_{DS} + (1-D)R_F$$

r_L is the inductor DC resistance, r_C is capacitor ESR, R_L is the converter load resistance, C is output filter capacitor, r_{DS} is the transistor turn on resistance, and R_F is the diode forward resistance.

The duty to inductor current transfer function T_{pi} is:

$$T_{pi}(s) = \frac{i_l}{d} = T_{pi0}\frac{s + w_{zi}}{s^2 + 2\xi w_n s + w_n^2}$$

$$\text{Where } T_{pi0} = \frac{V_O(R_L + 2r_c)}{L(R_L + r_c)}, w_{zi} = \frac{1}{C(R_L/2 + r_c)}$$

Current Sampling Transfer Function

Error voltage to duty transfer function F_m is:

$$F_m(s) = \frac{d}{v_{ei}} = \frac{2f_s^2\left(s^2 + 2\xi w_n s + w_n^2\right)}{T_{pi0}R_{cs}s(s + w_{zi})(s + w_{sh})}$$

$$\text{Where } w_{sh} = \frac{3w_s}{\pi}\left(\frac{1-\alpha}{1+\alpha}\right), \alpha = \frac{M_2 - M_a}{M_1 + M_a},$$

$$w_s = 2\pi f_s$$

Therefore, F_m depends on inductor current transfer function, T_{pi}, clock switching frequency, f_S, and current-sense amplifier transresistance, R_{CS}.

For the boost converter $M_1 = V_{IN}/L$ and $M_2 = (V_O - V_{IN})/L$.

For AAT1187A, R_{CS} = 0.24 V/A, M_a is slope compensation, $M_a = 0.8\times10^6$.

The closed-current loop transfer function T_{icl} is:

$$T_{icl}(s) = \frac{12f_s^2}{R_{cs}T_{pi0}} \times \frac{\left(s^2 + 2\xi w_n s + w_n^2\right)}{(s + w_{zi})\left(s^2 + w_{sh}s + 12f_s^2\right)}$$

The Voltage-Loop Gain with Current Loop Closed

The control to output voltage transfer function T_d is:

$$T_d(s) = \frac{V_O(s)}{V_C(s)} = T_{icl}(s)T_p(s)$$

The voltage-loop gain with current loop closed is:

$$L_{vi}(s) = \beta T_c(s)T_d(s)$$

$$= \beta g_m R_c \frac{s + w_c}{s} \frac{12 f_s{}^2 T_{p0}}{R_{cs} T_{pi0}} \times$$

$$\frac{(s + w_{z1})(s - w_{z2})}{(s + w_{zi})(s^2 + s w_{sh} + 12 f_s{}^2)}$$

$$\text{Where } \beta = \frac{V_{FB}}{Vo}$$

The compensator transfer function

$$T_c(s) = \frac{V_C}{V_{fb}} = g_m R_c \frac{s + w_c}{s},$$

$$\text{Where } w_c = \frac{1}{R_c C_c}$$

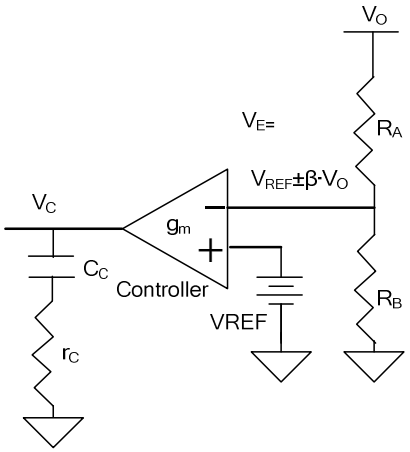


Figure 5. Voltage Loop Compensator

Compensator design guide:

1. Crossover frequency $f_{ci} < \frac{1}{2} f_s$

2. Gain margin>10dB

3. Phase margin>45°

4. The $|L_{vi}(s)| = 1$ at crossover frequency, Therefore, the compensator resistance, R_C is determined by:

$$R_c = \frac{V_O}{V_{FB}} \frac{2\pi f_{ci} C R_{cs}}{g_m k} \frac{(R_L + 2r_c)}{\left[(1-D)R_L - \frac{r}{(1-D)}\right]}$$

Table 3. K Factor Table

C	Best Corner Frequency	K Factor
21.533µF	23.740kHz	4.692
25.079µF	21.842kHz	5.083
32.587µF	20.095kHz	6.042
36.312µF	15.649kHz	5.230
38.469µF	13.247kHz	4.703

5. The output filter capacitor is chosen so C R_L pole cancels R_C C_C zero

$$\varepsilon R_c C_c = C\left(\frac{R_L}{2} + r_c\right), \text{ and } C_c = \frac{C}{\varepsilon R_c}\left(\frac{R_L}{2} + r_c\right)$$

$\varepsilon = (1 \sim 3)$

Example 3:

V_{IN} = 5V, V_O = 13.3V, I_O = 300mA, f_s = 1,190kHz,
V_{FB} = 1.233V, L = 6.65µH, g_m = 85µS, R_l = 76.689mΩ
r_C = 9.13mΩ, R_F = 0.7667Ω, C_C = 1.95nF,
R_C = 7.6kΩ, C = 38.5cF, ε = 3, R_{CS} = 0.23V/A.

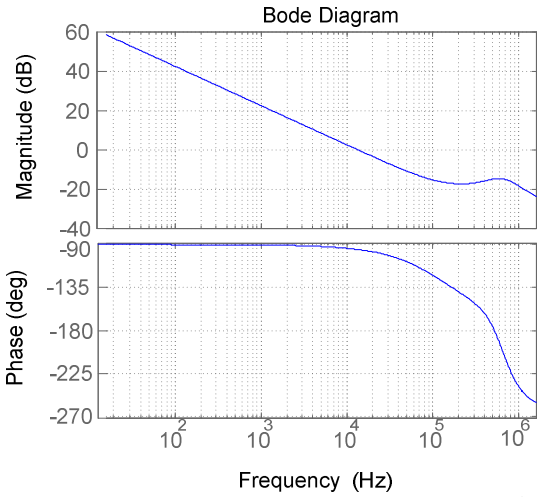


Figure 6. Bode Plot of Loop Gain Using Matlab® Simulation

However, it is found that the measured gain increased because of the extra small signal path provided by the 10Ω resistor in the spectrum analyzer. A modified formula is presented in this thesis to improve the gain observed in bode plot. Theoretically calculated result is confirmed by measurement data.

Loss(dB) = 20dB+20log10(10/r)
R = VADD/I_O
Loss(dB) = 7dB

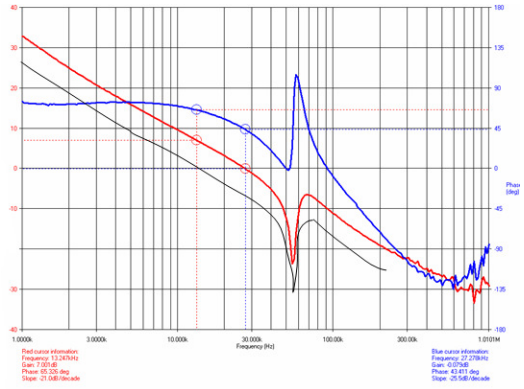


Figure 7. Bode Diagram of Loop Gain Using Frequency Response Analyzer Measurement

(Red line: gain of measurement, Blue line: phase of measurement, Black line: correct gain).

Setting the V_{GH} Output Voltage

The positive charge pump driver provides a regulated output voltage set by a resistor divider from the V_{GH} to GND with a center tap connected to the FBP.

V_{FBP} is the positive LDO driver feedback regulation and voltage feedback voltage is typically 1.24V.

Set R_8 (Figure8) between 5.1kΩ and 51kΩ, and calculate R_7 with the following equation.

$$R_7 = R_8\left(\frac{V_{GH}}{V_{FBP}} - 1\right)$$

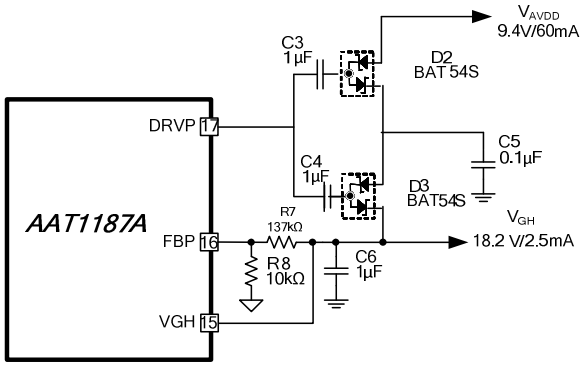


Figure 8. The Positive LDO Driver

Setting the V_{GL} Output Voltage

Choose a Zener diode to be in parallel connection with the V_{GL} output node. Because it's essential for the Zener to have a break down current around 1mA, the charge pump circuit requires resistor, R_{15}, in series connection.

$V_{GL} = -V_Z$

V_Z = Zener diode voltage

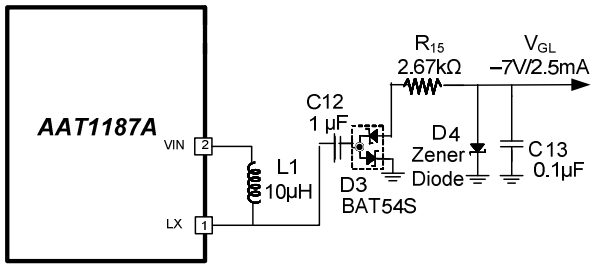


Figure 9. The Negative Charge Pump Circuit

Setting the LDO Voltage

The LDO can supply up to 600mA current and it is suitable to supply voltage for $T_{CON.}$

LDO voltage is set by the resistor divider from the V_{LDO} to GND with a center tap connected to the ADJ.

V_{LDO} feedback voltage is typically 1.24V. Assume R_{14} (Figure 10) has a value between 5.1kΩ and 51kΩ and calculate R_{13} to satisfy the following equation.

$$R_{13} = R_{14}\left(\frac{V_{LDO}}{V_{ADJ}} - 1\right)$$

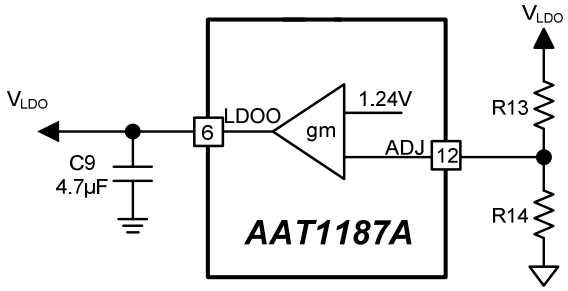


Figure 10. LDO Circuit

Setting the Reset Voltage

The AAT1187A series has an integrated reset voltage detector with an open drain output. (Figure 11)

Once V_{VDIV} is under VDIV threshold voltage, 1.1V, the RESET pin would be pulled low by internal NMOS. V_{IN} can be calculated as below :

$$V_{DETECT} = 1.1V \times \left(1 + \frac{R_{13}}{R_{14}}\right)$$

$$R_{13} = \left(\frac{V_{DETECT}}{1.1V} - 1\right) \times R_{14}$$

Recommended $R_{14\ value}$ is between 5.1kΩ and 30kΩ.

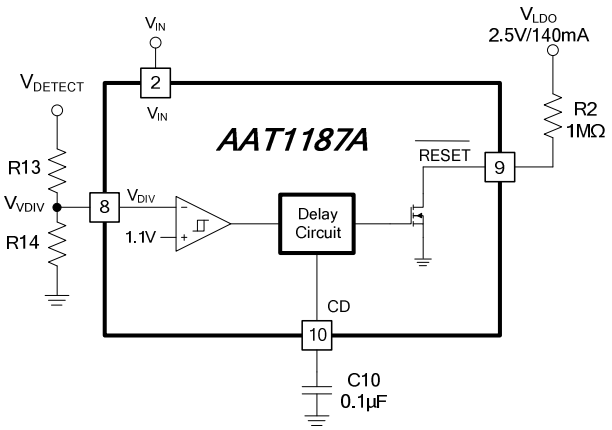


Figure 11. Reset Function Block

The delay time (t_D) is programmable by an external capacitor C_{10}. Pleaser refers to Figure 12. For a reference timing chart of reset function.
The delay time (t_D) can be calculated as below:

$$t_D = 1.24V \times \left(\frac{C_{10}}{I_{CD}}\right) = \frac{1.24V}{I_{CD}} \times C_{10} = 124k \times C_{10}$$

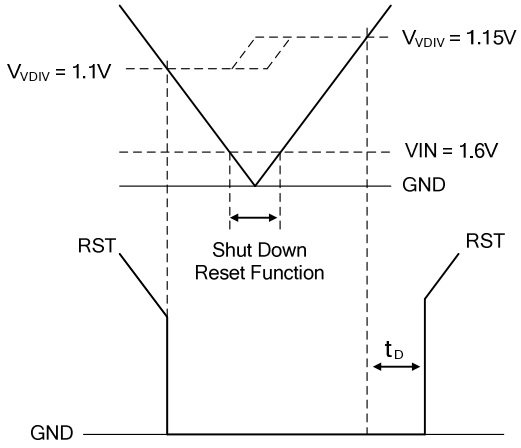


Figure 12. Timing Chart of Reset Function

Referring to Figure 12., reset output voltage is not able to remain low when V_{IN} is under 1.6V. Therefore, it's recommended to set the pulled high resistor, R_2 to greater than 500kΩ.

GPM Function

At power on, high voltage switch controlled by V_{FLK} latches until V_{DPM} reaches 1.24V (Figure 13.).

If VFLK = "Low", VGHM = VGH VDPM >1.24V)

If VFLK = "High", VGHM = RE (VDPM >1.24V)
The formula of V_{GHM} discharge.

$$V_{GHM}\,(\text{discharge}) = VGH \times e^{\frac{-t}{R_E C_L}}$$

C_L = The parasitic capacitor of panel
t = Discharge time

V_{DPM} pin connects a capacitor, C_{DPM}, to analog ground to set delay time.
V_{GHM} delay time,
$t_{DPM} = (V_{DPM} \times C_{DPM})/I_{DPM}$

$$= \frac{1.24V}{20\mu A} C_{DPM} = 62k \times C_{DPM}$$

When UVLO condition occurs or reset function activates, $V_{GHM} = V_{GH}$. Even VIN fast below 0.5V, GPM function keeps $V_{GHM} = V_{GH}$ status.

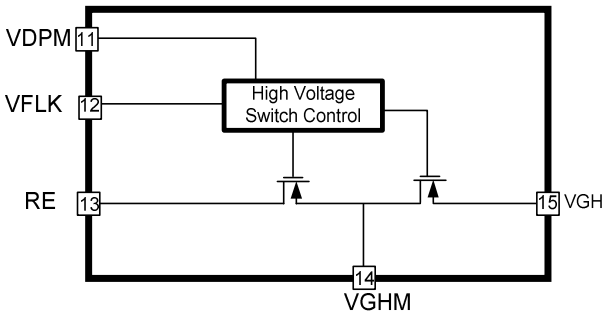


Figure 13. GPM Circuit

V_{COM} Buffer

The operational amplifiers are usually used to drive V_{COM} for TFT-LCD. The 10Ω output resistor and 1μF capacitor act as low pass filter and compensator for unity GAIN stable.

LAYOUT CONSIDERATION

The system's performances including switching noise, transient response, and PWM feedback loop stability are greatly affected by the PC board layout and grounding. There are some general guidelines for layout:

Inductor

Always try to use a low EMI inductor with a ferrite core.

Filter Capacitors

Place low ESR ceramics filter capacitors (between 0.1µF and 0.22µF) close to V_{DD} and V_{REF} pins. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. The ground connection of the V_{DD} and V_{REF} bypass capacitor should be connected to the analog ground pin (GND) with a wide trace.

Output Capacitors

Place output capacitors as close as possible to the IC. Minimize the length and maximize the width of traces to get the best transient response and reduce the ripple noise. We choose 10µF ceramics capacitor to reduce the ripple voltage, and use 0.1µF ceramics capacitor to reduce the ripple noise.

Feedback

If external compensation components are needed for stability, they should also be placed close to the IC. Take care to avoid the feedback voltage-divider resistors' trace near the SW. Minimize feedback track lengths to avoid the digital signal noise of TFT control board.

Ground Plane

The grounds of the IC input capacitors and output capacitors should be connected close to a ground plane. It would be a good design rule to have a ground plane on the PCB. This will reduce noise and ground loop errors as well as absorb more of the EMI radiated by the inductor. For boards with more than two layers, a ground plane can be used to separate the power plane and the signal plane for improved performance.

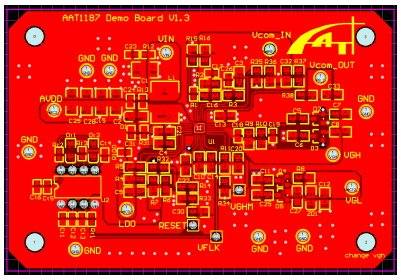


Figure 14. Top Layer

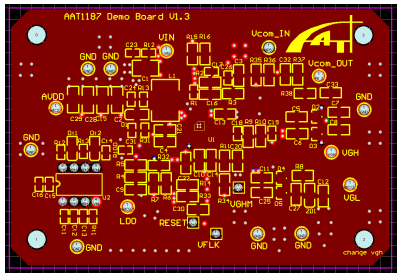


Figure 15. Power Layer

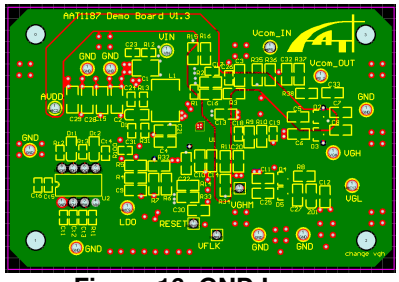


Figure 16. GND Layer

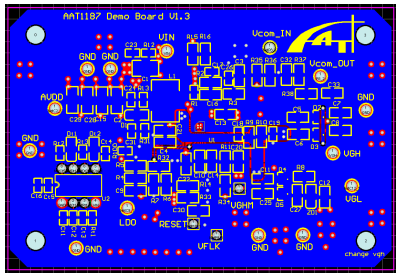
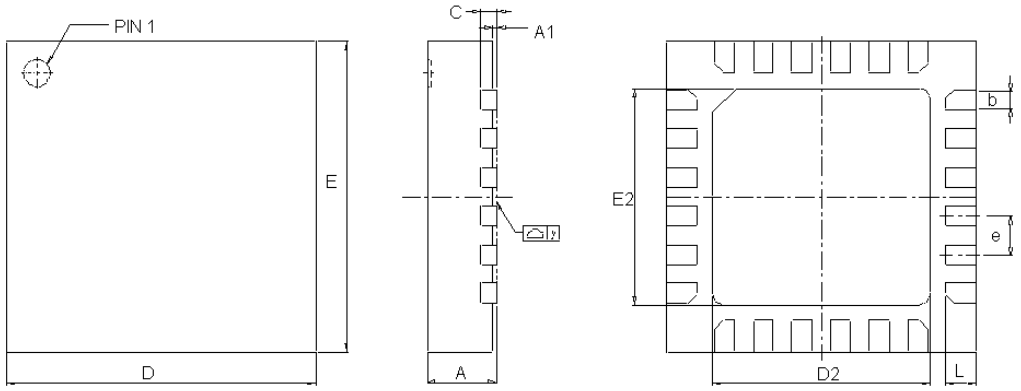


Figure 17. Bottom Layer

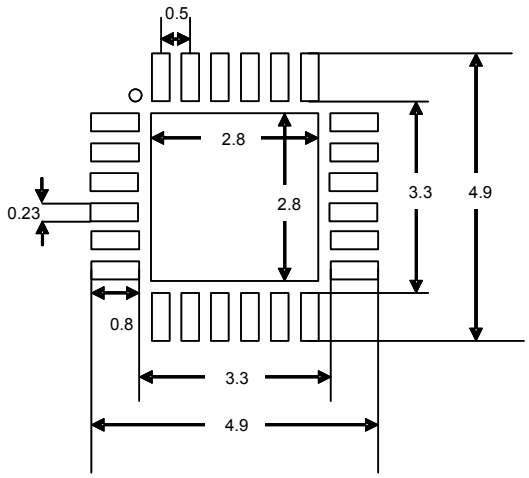
PACKAGE DIMENSION

VQFN-24



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.75	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.23	0.30
C	0.19	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
e	------	0.50	------
L	0.30	0.40	0.50
y	0.00	-----	0.076

AAT1187A Footprint of PCB



VERSION AND HISTORY

Version	Date	Description	Note
V0.01	2008/3/25	Original	AAT1187
V0.02	2008/5/23	Modify 'order information'	
V0.03/4	2008/9/16	Adding 'typical application characteristics'	
V0.05/6	2009/8/10	Adding 'application note and description'	
V1.00	2009/9/22	AAT1187A modify application note	AAT1187A
		Adding GPM description	