Precision, Miniature MEMs IMU

FEATURES

- Triaxial, digital gyroscope
  - ±125°/sec, ±500°/sec, ±2000°/sec range models
  - 2°/hr in-run bias stability (ADIS16477-1)
  - 0.15°/√hr angle random walk (ADIS16477-1 and ADIS16477-2)
  - ±0.1° axis-to-axis misalignment error
- Triaxial, digital accelerometer, ±40 *g*
  - 13 µ*g* in-run bias stability
- Triaxial, delta angle and delta velocity outputs
- Factory calibrated sensitivity, bias, and axial alignment
  - Calibration temperature range: −40°C to +85°C
- SPI compatible data communications
- Programmable operation and control
  - Automatic and manual bias correction controls
  - Data ready indicator for synchronous data acquisition
  - External sync modes: direct, pulse, scaled, and output
  - On demand self test of inertial sensors
  - On demand self test of flash memory
- Single-supply operation (VDD): 3.0 V to 3.6 V
- 2000 *g* mechanical shock survivability
- Operating temperature range: −40°C to +105°C

APPLICATIONS

- Navigation, stabilization, and instrumentation
- Unmanned and autonomous vehicles
- Smart agriculture/construction machinery
- Factory/industrial automation, robotics
- Virtual/augmented reality
- Internet of Moving Things

GENERAL DESCRIPTION

The ADIS16477 is a precision, miniature MEMS inertial measurement unit (IMU) that includes a triaxial gyroscope and a triaxial accelerometer. Each inertial sensor in the ADIS16477 combines with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, linear acceleration (gyroscope bias), and point of percussion (accelerometer location). As a result, each sensor has dynamic compensation formulas that provide accurate sensor measurements over a broad set of conditions.

The ADIS16477 provides a simple, cost effective method for integrating accurate, multiaxis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The serial peripheral interface (SPI) and register structure provide a simple interface for data collection and configuration control.

The ADIS16477 is available in a 44-ball, ball grid array (BGA) package that is approximately 11 mm × 15 mm × 11 mm.

FUNCTIONAL BLOCK DIAGRAM

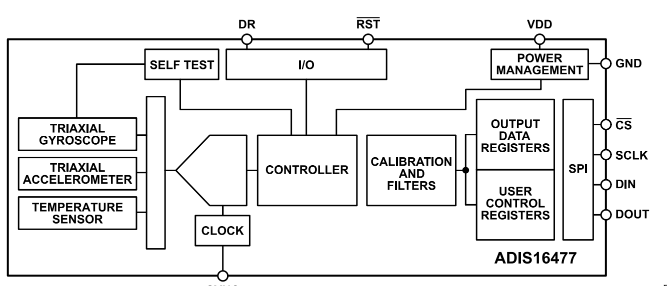


Figure 1.

Rev. E

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

TABLE OF CONTENTS

TABLE OF CONTENTS

REVISION HISTORY

7/2022—Rev. D to Rev. E

SPECIFICATIONS

Case temperature (T_C) = 25°C, VDD = 3.3 V, angular rate = 0°/sec, dynamic range = ±2000°/sec ± 1 *g*, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range	ADIS16477-1	±125			°/sec
	ADIS16477-2	±500			°/sec
	ADIS16477-3	±2000			°/sec
Sensitivity	ADIS16477-1, 16-bit		160		LSB/°/sec
	ADIS16477-2, 16-bit		40		LSB/°/sec
	ADIS16477-3, 16-bit		10		LSB/°/sec
	ADIS16477-1, 32-bit		10,485,760		LSB/°/sec
	ADIS16477-2, 32-bit		2,621,440		LSB/°/sec
	ADIS16477-3, 32-bit		655,360		LSB/°/sec
Error over Temperature	$-40°C \leq T_C \leq +85°C$, 1 σ		±0.3		%
Repeatability[1]	$-40°C \leq T_C \leq +85°C$, 1 σ		±0.3		%
Misalignment Error	Axis to axis, $-40°C \leq T_C \leq +85°C$, 1 σ		±0.1		Degrees
Nonlinearity[2]	ADIS16477-1, full scale (FS) = 125°/sec		0.2		% FS
	ADIS16477-2, FS = 500°/sec		0.2		% FS
	ADIS16477-3, FS = 2000°/sec		0.25		% FS
Bias					
Repeatability[1]	$-40°C \leq T_C \leq +85°C$, 1 σ		0.7		°/sec
In-Run Bias Stability	ADIS16477-1, 1 σ		2		°/hr
	ADIS16477-2, 1 σ		2.5		°/hr
	ADIS16477-3, 1 σ		7		°/hr
Angular Random Walk	ADIS16477-1, 1 σ		0.15		°/√hr
	ADIS16477-2, 1 σ		0.15		°/√hr
	ADIS16477-3, 1 σ		0.3		°/√hr
Error over Temperature	$-40°C \leq T_C \leq +85°C$, 1 σ		±0.2		°/sec
Linear Acceleration Effect	Any direction, 1 σ		0.01		°/sec/*g*
Vibration Rectified Error (VRE)	Random vibration, 2 g_{rms}, 50 Hz to 2 kHz		0.0005		°/sec/g^2
Output Noise	ADIS16477-1, 1 σ, no filtering		0.07		°/sec rms
	ADIS16477-2, 1 σ, no filtering		0.08		°/sec rms
	ADIS16477-3, 1 σ, no filtering		0.17		°/sec rms
Rate Noise Density	ADIS16477-1, f = 10 Hz to 40 Hz		0.003		°/sec/√Hz rms
	ADIS16477-2, f = 10 Hz to 40 Hz		0.003		°/sec/√Hz rms
	ADIS16477-3, f = 10 Hz to 40 Hz		0.007		°/sec/√Hz rms
3 dB Bandwidth			550		Hz
Sensor Resonant Frequency			66		kHz
ACCELEROMETERS[3]	Each axis				
Dynamic Range		±40			*g*
Sensitivity	32-bit data format		52,428,800		LSB/*g*
Error over temperature	$-40°C \leq T_C \leq +85°C$, 1 σ		±0.1		%
Repeatability[1]	$-40°C \leq T_C \leq +85°C$, 1 σ		±0.1		%
Misalignment Error	Axis to axis, $-40°C \leq T_C \leq +85°C$, 1 σ		±0.05		Degrees
Nonlinearity	Best fit straight line, ±10 *g*		0.02		% FS
	Best fit straight line, ±20 *g*		0.4		% FS
	Best fit straight line, ±40 *g*		1.5		% FS
Bias					
Repeatability[1]	$-40°C \leq T_C \leq +85°C$, 1 σ		6		m*g*
In-Run Bias Stability	1 σ		13		μ*g*

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Velocity Random Walk	1 σ		0.037		m/sec/√hr
Error over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		±3		m*g*
Output Noise	No filtering		2.3		m*g* rms
Noise Density	f = 10 Hz to 40 Hz, no filtering		100		μ*g*/√Hz rms
3 dB Bandwidth			600		Hz
Sensor Resonant Frequency	Y-axis and z-axis		5.65		kHz
	X-axis		5.25		kHz
TEMPERATURE SENSOR					
Scale Factor	Output = 0x0000 at 0°C (±5°C)		0.1		°C/LSB
LOGIC INPUTS[4]					
Input Voltage					
High, V_{IH}		2.0			V
Low, V_{IL}				0.8	V
$\overline{RST}$ Pulse Width		1			μs
Input Current					
Logic 1, I_{IH}	V_{IH} = 3.3 V			10	μA
Logic 0, I_{IL}	V_{IL} = 0 V				
All Pins Except $\overline{RST}$				10	μA
$\overline{RST}$ Pin			0.33		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output Voltage					
High, V_{OH}	I_{SOURCE} = 0.5 mA	2.4			V
Low, V_{OL}	I_{SINK} = 2.0 mA			0.4	V
FLASH MEMORY	Endurance[5]	10000			Cycles
Data Retention[6]	T_J = 85°C	20			Years
FUNCTIONAL TIMES[7]	Time until data is available				
Power-On Start-Up Time			252		ms
Reset Recovery Time[8]	GLOB_CMD, Bit 7 = 1 (see Table 113)		193		ms
Factory Calibration Restore	GLOB_CMD, Bit 1 = 1 (see Table 113)		142		ms
Flash Memory Backup	GLOB_CMD, Bit 3 = 1 (see Table 113)		72		ms
Flash Memory Test Time	GLOB_CMD, Bit 4 = 1 (see Table 113)		32		ms
Self Test Time[9]	GLOB_CMD, Bit 2 = 1 (see Table 113)		14		ms
CONVERSION RATE			2000		SPS
Initial Clock Accuracy			3		%
Sync Input Clock		1.9		2.1	kHz
POWER SUPPLY, VDD	Operating voltage range	3.0		3.6	V
Power Supply Current[10]	Normal mode, VDD = 3.3 V		44	55	mA

1 Bias repeatability provides an estimate for long-term drift in the bias, as observed during 500 hours of high temperature operating life (HTOL) at 105°C.

2 This measurement is based on the deviation from a best fit linear model.

3 All specifications associated with the accelerometers relate to the full-scale range of ±8 *g*, unless otherwise noted.

4 The digital input/output signals use a 3.3 V system.

5 Endurance is qualified as per JEDEC Standard 22, Method A117, measured at −40°C, +25°C, +85°C, and +125°C.

6 The data retention specification assumes a junction temperature (T_J) of 85°C per JEDEC Standard 22, Method A117. Data retention lifetime decreases with T_J.

7 These times do not include thermal settling and internal filter response times, which may affect overall accuracy.

8 The $\overline{RST}$ line must be in a low state for at least 10 μs to ensure a proper reset initiation and recovery.

9 The self test time can extend when using external clock rates lower than 2000 Hz.

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit

[10] Power supply current transients can reach 100 mA during initial startup or reset recovery.

TIMING SPECIFICATIONS

T_A = 25°C, VDD = 3.3 V, unless otherwise noted.

Table 2.

		Normal Mode			Burst Read Mode			
Parameter	Description	Min	Typ	Max	Min[1]	Typ	Max	Unit
f_{SCLK}	Serial clock	0.1		2	0.1		1	MHz
t_{STALL}	Stall period between data	16			N/A			µs
$t_{READRATE}$	Read rate	24						µs
$t_{\overline{CS}}$	Chip select to SCLK edge	200			200			ns
t_{DAV}	DOUT valid after SCLK edge			25			25	ns
t_{DSU}	DIN setup time before SCLK rising edge	25			25			ns
t_{DHD}	DIN hold time after SCLK rising edge	50			50			ns
t_{SCLKR}, t_{SCLKF}	SCLK rise/fall times		5	12.5		5	12.5	ns
t_{DR}, t_{DF}	DOUT rise/fall times		5	12.5		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			0			ns
t_1	Input sync positive pulse width; pulse sync mode, MSC_CTRL = 101 (binary, see Table 105)	5			5			µs
t_{STDR}	Input sync to data ready valid transition							
	Direct sync mode, MSC_CTRL = 001 (binary, see Table 105)		256			256		µs
	Pulse sync mode, MSC_CTRL = 101 (binary, see Table 105)		256			256		µs
t_{NV}	Data invalid time		20			20		µs
t_2	Input sync period[2]	477			477			µs

[1] N/A means not applicable.

[2] This specification is rounded up from the cycle time that comes from the maximum input clock frequency (2100 Hz).

Timing Diagrams

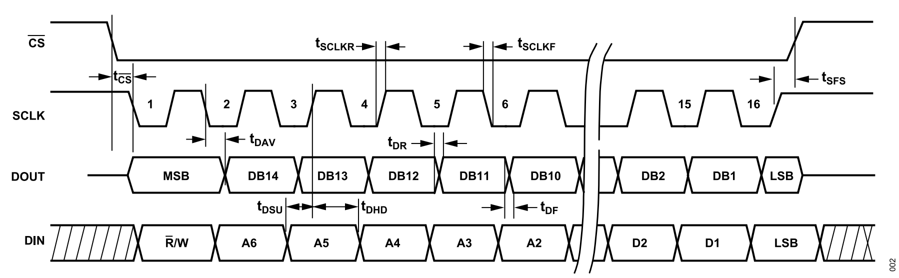


Figure 2. SPI Timing and Sequence Diagram

SPECIFICATIONS

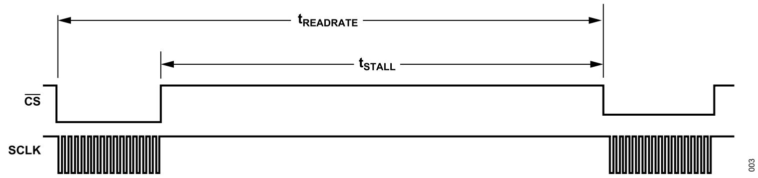


Figure 3. Stall Time and Data Rate Timing Diagram

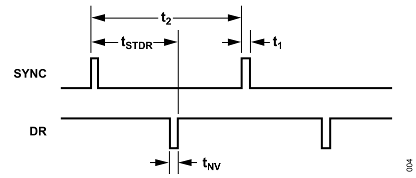


Figure 4. Input Clock Timing Diagram, Pulse Sync Mode, Register MSC_CTRL, Bits[4:2] = 101 (Binary)

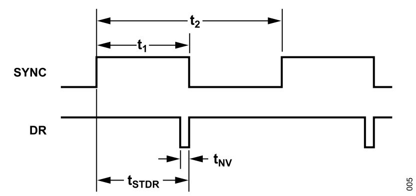


Figure 5. Input Clock Timing Diagram, Direct Sync Mode, Register MSC_CTRL, Bits[4:2] = 001 (Binary)

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Mechanical Shock Survivability	
Any Axis, Unpowered	2000 *g*
Any Axis, Powered	2000 *g*
VDD to GND	−0.3 V to +3.6 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.2 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.2 V
Calibration Temperature Range	−40°C to +85°C
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range[1]	−65°C to +150°C
Barometric Pressure	2 bar

[1] Extended exposure to temperatures that are lower than −40°C or higher than +105°C may adversely affect the accuracy of the factory calibration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

The ADIS16477 is a multichip module that includes many active components. The values in Table 4 identify the thermal response of the hottest component inside of the ADIS16477, with respect to the overall power dissipation of the module. This approach enables a simple method for predicting the temperature of the hottest junction, based on either ambient or case temperature.

For example, when the ambient temperature is 70°C, the hottest junction temperature (T_J) inside of the ADIS16477 is 76.7°C.

$$T_J = \theta_{JA} \times VDD \times I_{DD} + 70°C$$

$$T_J = 158.2°C/W \times 3.3\ V \times 0.044\ A + 70°C$$

$$T_J = 93°C$$

Table 4. Package Characteristics

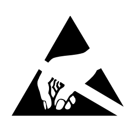
Package Type	θ_{JA}[1]	θ_{JC}[2]	Device Weight
ML-44-1[3]	158.2°C/W	106.1°C/W	1.3 g

[1] θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

[2] θ_{JC} is the junction to case thermal resistance.

[3] Thermal impedance values come from direct observation of the hottest temperature inside of the ADIS16477, when it is attached to an FR4-08 PCB that has two metal layers and has a thickness of 0.063 inches.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

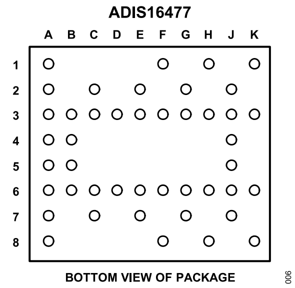


Figure 6. Pin Assignments, Bottom View

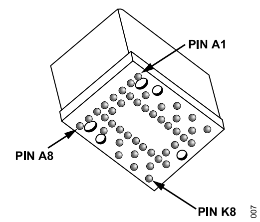


Figure 7. Pin Assignments, Package Level View

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
A1	GND	Supply	Power Ground
A2	GND	Supply	Power Ground
A3	GND	Supply	Power Ground
A4	GND	Supply	Power Ground
A5	GND	Supply	Power Ground
A6	GND	Supply	Power Ground
A7	GND	Supply	Power Ground
A8	GND	Supply	Power Ground
B3	GND	Supply	Power Ground
B4	GND	Supply	Power Ground
B5	GND	Supply	Power Ground
B6	GND	Supply	Power Ground
C2	GND	Supply	Power Ground
C3	DNC	Not applicable	Do Not Connect
C6	GND	Supply	Power Ground
C7	VDD	Supply	Power Supply
D3	GND	Supply	Power Ground
D6	VDD	Supply	Power Supply
E2	GND	Supply	Power Ground
E3	VDD	Supply	Power Supply
E6	GND	Supply	Power Ground
E7	GND	Supply	Power Ground
F1	GND	Supply	Power Ground
F3	$\overline{RST}$	Input	Reset
F6	GND	Supply	Power Ground
F8	GND	Supply	Power Ground
G2	GND	Supply	Power Ground
G3	$\overline{CS}$	Input	SPI, Chip Select
G6	DIN	Input	SPI, Data Input
G7	GND	Supply	Power Supply
H1	VDD	Supply	Power Supply
H3	DOUT	Output	SPI, Data Output
H6	SCLK	Input	SPI, Serial Clock
H8	GND	Supply	Power Ground
J2	GND	Supply	Power Ground
J3	SYNC	Input	Sync (External Clock)
J4	VDD	Supply	Power Supply
J5	VDD	Supply	Power Supply

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
J6	DR	Output	Data Ready
J7	GND	Supply	Power Ground
K1	GND	Supply	Power Ground
K3	GND	Supply	Power Ground
K6	VDD	Supply	Power Supply
K8	GND	Supply	Power Ground

TYPICAL PERFORMANCE CHARACTERISTICS

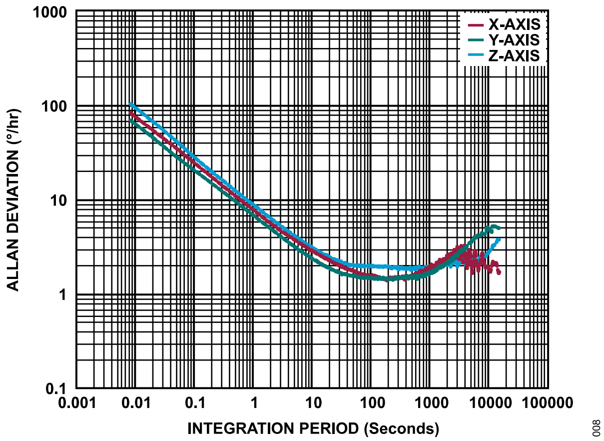


Figure 8. Gyroscope Allan Deviation, T_C = 25°C, ADIS16477-1

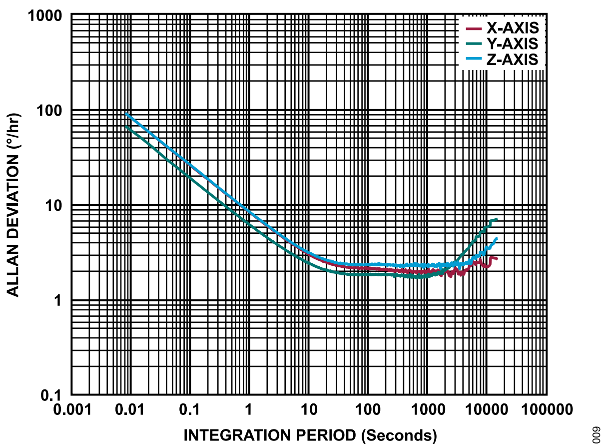


Figure 9. Gyroscope Allan Deviation, T_C = 25°C, ADIS16477-2

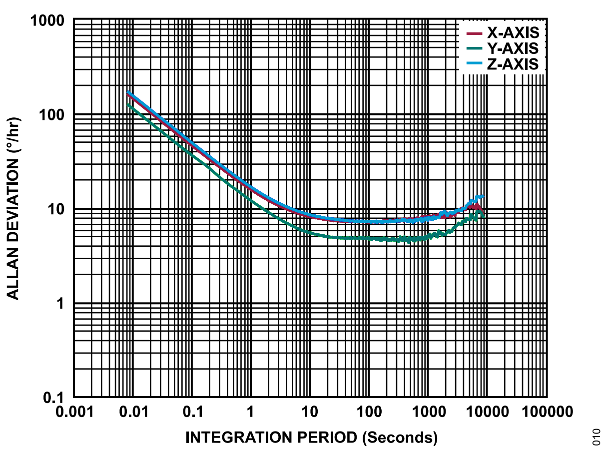


Figure 10. Gyroscope Allan Deviation, T_C = 25°C, ADIS16477-3

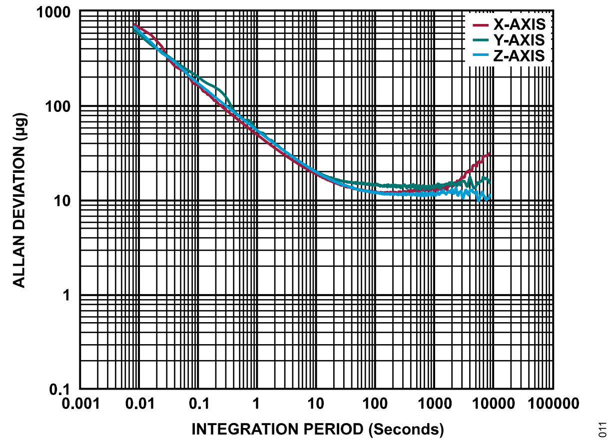


Figure 11. Accelerometer Allan Deviation, T_C = 25°C

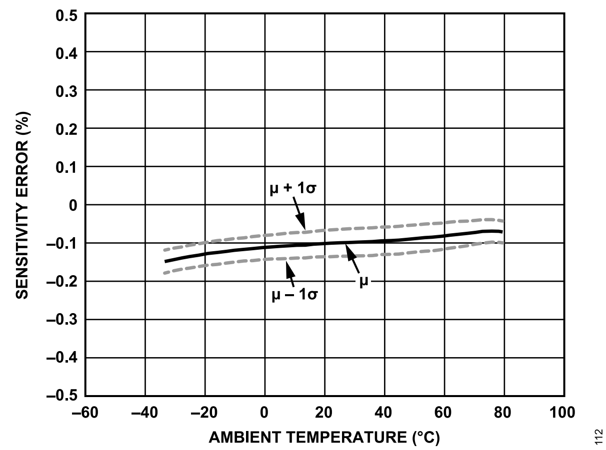


Figure 12. ADIS16477-1 Gyroscope Sensitivity Error vs. Ambient Temperature

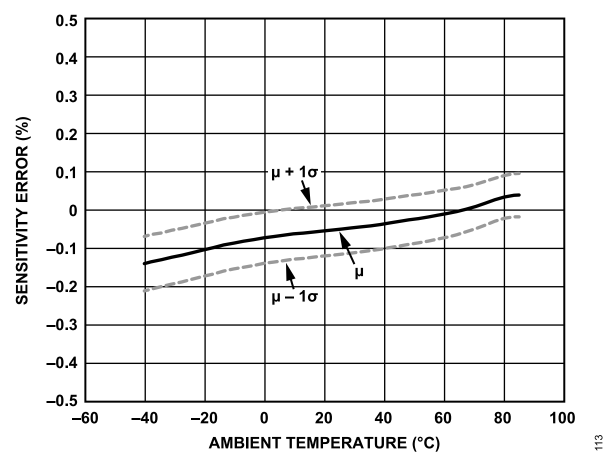


Figure 13. ADIS16477-2 Gyroscope Sensitivity Error vs. Ambient Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

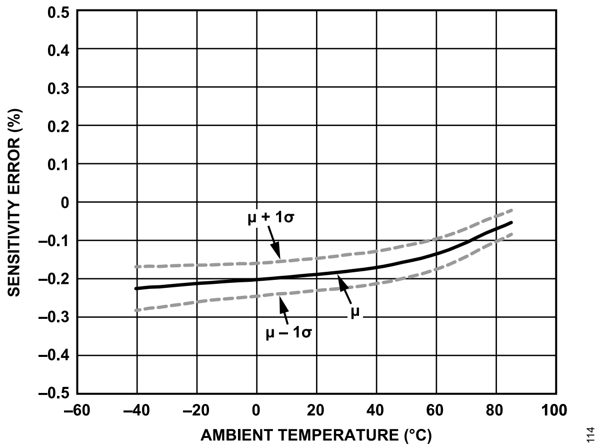


Figure 14. ADIS16477-3 Gyroscope Sensitivity Error vs. Ambient Temperature

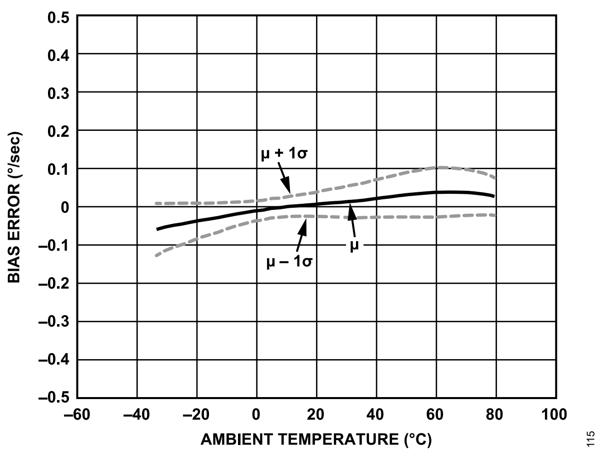


Figure 15. ADIS16477-1 Gyroscope Bias Error vs. Ambient Temperature

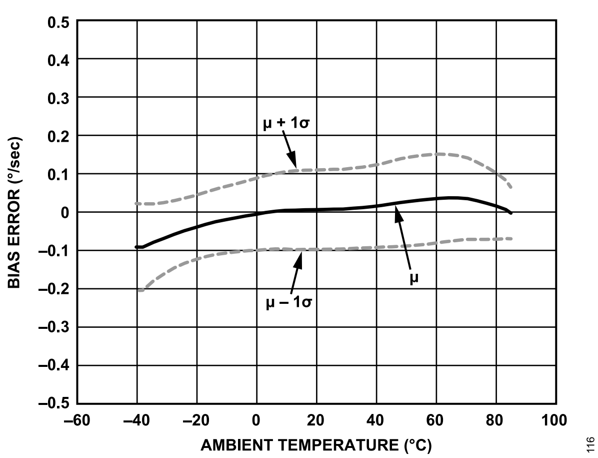


Figure 16. ADIS16477-2 Gyroscope Bias Error vs. Ambient Temperature

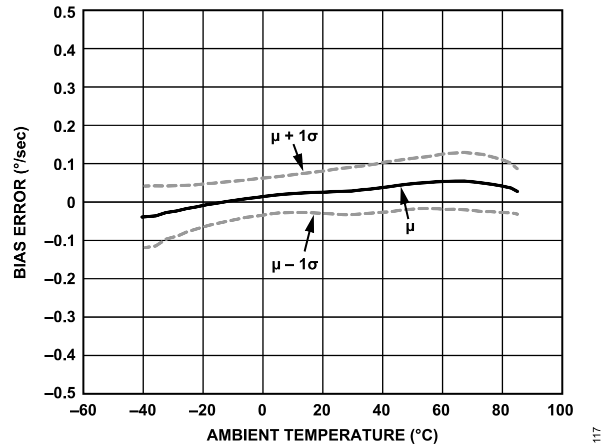


Figure 17. ADIS16477-3 Gyroscope Bias Error vs. Ambient Temperature

THEORY OF OPERATION

INTRODUCTION

When using the factory default configuration for all user configurable control registers, the ADIS16477 initializes itself and automatically starts a continuous process of sampling, processing, and loading calibrated sensor data into its output registers at a rate of 2000 SPS.

INERTIAL SENSOR SIGNAL CHAIN

Figure 18 provides the basic signal chain for the inertial sensors in the ADIS16477. This signal chain produces an update rate of 2000 SPS in the output data registers when it operates in internal clock mode (default, see Register MSC_CTRL, Bits[4:2] in Table 105).

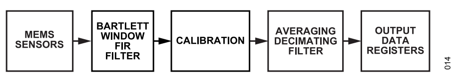


Figure 18. Signal Processing Diagram, Inertial Sensors

Gyroscope Data Sampling

The three gyroscopes produce angular rate measurements around three orthogonal axes (x, y, and z). Figure 19 shows the data sampling plan for each gyroscope when the ADIS16477 operates in internal clock mode (default, see Register MSC_CTRL, Bits[4:2] in Table 105). Each gyroscope has an analog-to-digital converter (ADC) and sample clock (f_{SG}) that drives data sampling at a rate of 4100 Hz (±5%). The internal processor reads and processes this data from each gyroscope at a rate of 2000 Hz (f_{SM}).

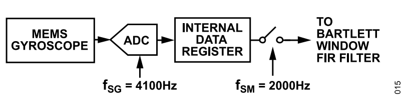


Figure 19. Gyroscope Data Sampling

Accelerometer Data Sampling

The three accelerometers produce linear acceleration measurements along the same orthogonal axes (x, y, and z) as the gyroscopes. Figure 20 shows the data sampling plan for each accelerometer when the ADIS16477 operates in internal clock mode (default, see Register MSC_CTRL, Bits[4:2] in Table 105).

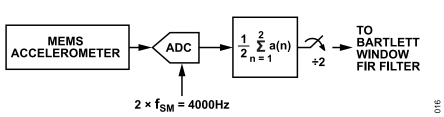


Figure 20. Accelerometer Data Sampling

External Clock Options

The ADIS16477 provides three different modes of operation that support the device using an external clock to control the internal processing rate (f_{SM} in Figure 19 and Figure 20) through the SYNC pin. The MSC_CTRL register (see Table 105) provides the configuration options for these external clock modes in Bits[4:2].

Inertial Sensor Calibration

The inertial sensor calibration function for the gyroscopes and the accelerometers has two components: factory calibration and user calibration (see Figure 21).

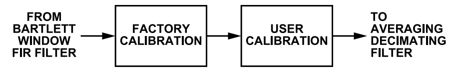


Figure 21. Inertial Sensor Calibration Processing

The factory calibration of the gyroscope applies the following correction formulas to the data of each gyroscope:

$$\begin{bmatrix}\omega_{XC}\\ \omega_{YC}\\ \omega_{ZC}\end{bmatrix}=\begin{bmatrix}m_{11}&m_{12}&m_{13}\\ m_{21}&m_{22}&m_{23}\\ m_{31}&m_{32}&m_{33}\end{bmatrix}\times\left[\begin{bmatrix}\omega_X\\ \omega_Y\\ \omega_Z\end{bmatrix}+\begin{bmatrix}b_X\\ b_Y\\ b_Z\end{bmatrix}\right]+\begin{bmatrix}l_{11}&l_{12}&l_{13}\\ l_{21}&l_{22}&l_{23}\\ l_{31}&l_{32}&l_{33}\end{bmatrix}\times\begin{bmatrix}a_{XC}\\ a_{YC}\\ a_{ZC}\end{bmatrix}$$

where:
ω_{XC}, ω_{YC}, and ω_{ZC} are the gyroscope outputs (post calibration).
m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} provide scale and alignment correction.
ω_X, ω_Y, and ω_Z are the gyroscope outputs (precalibration).
b_X, b_Y, and b_Z provide bias correction.
l_{11}, l_{12}, l_{13}, l_{21}, l_{22}, l_{23}, l_{31}, l_{32}, and l_{33} provide linear *g* correction.
a_{XC}, a_{YC}, and a_{ZC} are the accelerometer outputs (post calibration).

All of the correction factors in this relationship come from direct observation of the response of each gyroscope at multiple temperatures over the calibration temperature range (−40°C ≤ T_C ≤ +85°C). These correction factors are stored in the flash memory bank, but they are not available for observation or configuration. Register MSC_CTRL, Bit 7 (see Table 105) provides the only user configuration option for the factory calibration of the gyroscopes: an on/off control for the linear *g* compensation. See Figure 44 for more details on the user calibration options available for the gyroscopes.

The factory calibration of the accelerometer applies the following correction formulas to the data of each accelerometer:

$$\begin{bmatrix}a_{XC}\\ a_{YC}\\ a_{ZC}\end{bmatrix}=\begin{bmatrix}m_{11}&m_{12}&m_{13}\\ m_{21}&m_{22}&m_{23}\\ m_{31}&m_{32}&m_{33}\end{bmatrix}\times\left[\begin{bmatrix}a_X\\ a_Y\\ a_Z\end{bmatrix}+\begin{bmatrix}b_X\\ b_Y\\ b_Z\end{bmatrix}\right]+\begin{bmatrix}0&p_{12}&p_{13}\\ p_{21}&0&p_{23}\\ p_{31}&p_{32}&0\end{bmatrix}\times\begin{bmatrix}\omega_{XC}^2\\ \omega_{YC}^2\\ \omega_{ZC}^2\end{bmatrix}$$

where:
a_{XC}, a_{YC}, and a_{ZC} are the accelerometer outputs (post calibration).

THEORY OF OPERATION

m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} provide scale and alignment correction.
a_X, a_Y, and a_Z are the accelerometer outputs (precalibration).
b_X, b_Y, and b_Z provide bias correction.
p_{12}, p_{13}, p_{21}, p_{23}, p_{31} and p_{32} provide a point of percussion alignment correction (see Figure 47).
ω^2_{XC}, ω^2_{YC}, and ω^2_{ZC} are the square of the gyroscope outputs (post calibration).

All of the correction factors in this relationship come from direct observation of the response of each accelerometer at multiple temperatures, over the calibration temperature range ($-40°C \leq T_C \leq +85°C$). These correction factors are stored in the flash memory bank, but they are not available for observation or configuration. MSC_CTRL, Bit 6 (see Table 105) provides the only user configuration option for the factory calibration of the accelerometers: an on/off control for the point of percussion, alignment function. See Figure 45 for more details on the user calibration options available for the accelerometers.

Bartlett Window FIR Filter

The Bartlett window finite impulse response (FIR) filter (see Figure 22) contains two averaging filter stages, in a cascade configuration. The FILT_CTRL register (see Table 101) provides the configuration controls for this filter.

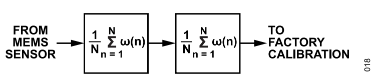


Figure 22. Bartlett Window FIR Filter Signal Path

Averaging/Decimating Filter

The second digital filter averages multiple samples together to produce each register update. In this type of filter structure, the number of samples in the average is equal to the reduction in the update rate for the output data registers. The DEC_RATE register (see Table 109) provides the configuration controls for this filter.

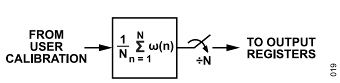


Figure 23. Averaging/Decimating Filter Diagram

REGISTER STRUCTURE

All communication between the ADIS16477 and an external processor involves either reading the contents of an output register or writing configuration/command information to a control register. The output data registers include the latest sensor data, error flags, and identification information. The control registers include sample rate, filtering, calibration, and diagnostic options. Each user accessible register has two bytes (upper and lower), each of which has its own unique address. See Table 8 for a detailed list of all user registers, along with their addresses.

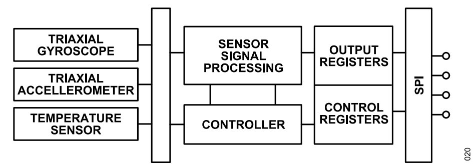


Figure 24. Basic Operation of the ADIS16477

SERIAL PERIPHERAL INTERFACE (SPI)

The SPI provides access to the user registers (see Table 8). Figure 25 shows the most common connections between the ADIS16477 and a SPI host device which is often an embedded processor that has a SPI-compatible interface. In this example, the SPI host uses an interrupt service routine to collect data every time the data ready (DR) signal pulses.

Additional information on the ADIS16477 SPI can be found in the Serial Port Operation section of this data sheet.

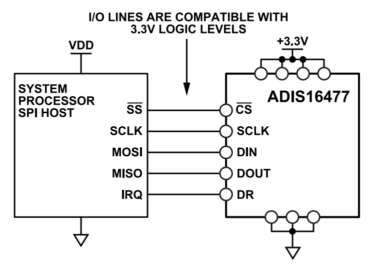


Figure 25. Electrical Connection Diagram

Table 6. Generic SPI Host Pin Names and Functions

Mnemonic	Function
SS	Peripheral select
SCLK	Serial clock
MOSI	Host output, peripheral input
MISO	Host input, peripheral output
IRQ	Interrupt request

Embedded processors typically use control registers to configure their serial ports for communicating with SPI peripheral devices such as the ADIS16477. Table 7 provides a list of settings that describe the SPI protocol of the ADIS16477. The initialization routine of the host processor typically establishes these settings using firmware commands to write them into the control registers.

Table 7. Generic Host Processor SPI Settings

Processor Setting	Description
Host	ADIS16477 operates as peripheral
Maximum SCLK Frequency[1]	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), CPHA = 1 (phase)
MSB First Mode	Bit sequence, see Figure 30 for coding
16-Bit Mode	Shift register and data length

[1] See Table 2 for the maximum SCLK frequency.

THEORY OF OPERATION

DATA READY (DR)

The factory default configuration provides users with a DR signal on the DR pin (see Table 5), which pulses when the output data registers are updating. Connect the DR pin to a pin on the embedded processor, which triggers data collection, on the second edge of this pulse. The MSC_CTRL register, Bit 0 (see Table 105), controls the polarity of this signal. In Figure 26, Register MSC_CTRL, Bit 0 = 1, which means that data collection must start on the rising edges of the DR pulses.

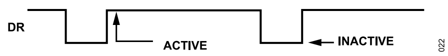


Figure 26. Data Ready When Register MSC_CTRL, Bit 0 = 1 (Default)

During the start-up and reset recovery processes, the DR signal may exhibit some transient behavior before data production begins. Figure 27 shows an example of the DR behavior during startup, and Figure 28 and Figure 29 provide examples of the DR behavior during recovery from reset commands.

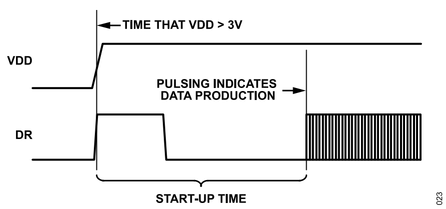


Figure 27. Data Ready Response During Startup

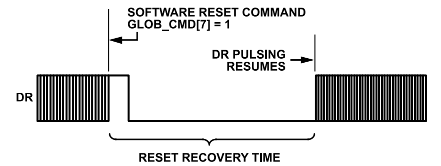


Figure 28. Data Ready Response During Reset (Register GLOB_CMD, Bit 7 = 1) Recovery

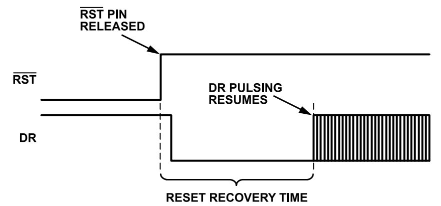


Figure 29. Data Ready Response During Reset (RST = 0) Recovery

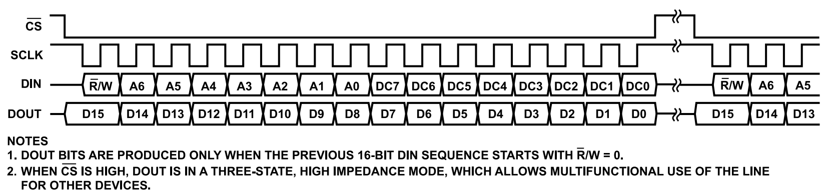


Figure 30. SPI Communication Bit Sequence

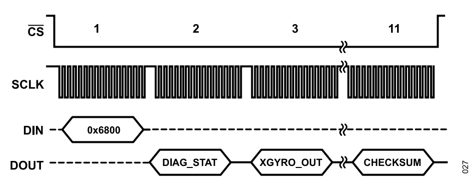


Figure 31. Burst Read Sequence

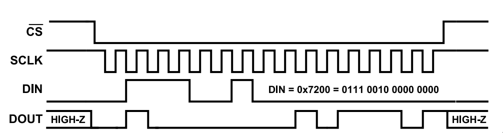


Figure 32. SPI Signal Pattern Showing a Read of the PROD_ID Register

THEORY OF OPERATION

READING SENSOR DATA

Reading a single register requires two 16-bit cycles on the SPI: one to request the contents of a register and another to receive those contents. The 16-bit command code (see Figure 30) for a read request on the SPI has three parts: the read bit ($\overline{R}$/W = 0), either address of the register, [A6:A0], and eight don't care bits, [DC7:DC0]. Figure 33 shows an example that includes two register reads in succession. This example starts with DIN = 0x0C00, to request the contents of the Z_GYRO_LOW register, and follows with 0x0E00, to request the contents of the Z_GYRO_OUT register. The sequence in Figure 33 also shows full duplex mode of operation, which means that the ADIS16477 can receive requests on DIN while also transmitting data out on DOUT within the same 16-bit SPI cycle.

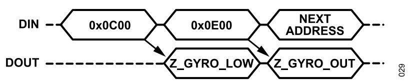


Figure 33. SPI Read Example

Figure 32 provides an example of the four SPI signals when reading the PROD_ID register (see Table 121) in a repeating pattern. This pattern can be helpful when troubleshooting the SPI interface setup and communications because the signals are the same for each 16-bit sequence, except during the first cycle.

Burst Read Function

The burst read function provides a way to read a batch of output data registers, using a continuous stream of bits, at a rate of up to 1 MHz (SCLK). This method does not require a stall time between each 16-bit segment (see Figure 3). As shown in Figure 31, start this mode by setting DIN = 0x6800, and then read each of the registers in the sequence out of DOUT while keeping $\overline{CS}$ low for the entire sequence.

The sequence of registers (and checksum value) in the burst read response depends on which sample clock mode that the ADIS16477 is operating in Register MSC_CTRL, Bits[4:2] (see Table 105). In all clock modes, except when operating in scaled sync mode (Register MSC_CTRL, Bits[4:2] = 010), the burst read response ends with the DATA_CNTR, Bits[7:0] register contents, followed by the checksum value. Checksum value computations for the various burst modes are described in the following sections.

Scaled sync mode (Register MSC_CTRL, Bits[4:2] = 010) uses an identical format to that described in the previous paragraph, except that the DATA_CNTR, Bits[7:0] register is replaced by the TIME_STAMP, Bits[7:0] register. In scaled sync mode, the TIME_STAMP, Bits[7:0] register always replaces the DATA_CNTR, Bits[7:0] register for all combinations of the BURST_SEL and BURST32 settings. Refer to the Miscellaneous Control Register (MSC_CTRL) section for more details.

Note that the 32-bit burst modes and BURST_SEL function are only available in Firmware Version 1.34 and newer. Older firmware versions only have 16-bit burst transfer with BURST_SEL = 0. See the FIRM_REV, Bits[7:0] for the firmware revision.

16-Bit Burst Mode with BURST_SEL = 0

In 16-bit burst mode with BURST_SEL = 0, a burst contains calibrated gyroscope and accelerometer data in 16-bit format. This mode is particularly appropriate for cases where there is no decimation nor filtering. Not only is the sample rate high (~2 kSPS), the lower 16 bits are not used unless the user is averaging or filtering. Note that when using this mode, the linear *g* compensation must be disabled because the linear *g* compensation relies on 32-bit data to perform optimally.

The sequence of registers (and checksum value) in the burst read includes the following registers and value: DIAG_STAT, X_GYRO_OUT, Y_GYRO_OUT, Z_GYRO_OUT, X_ACCL_ OUT, Y_ACCL_OUT, Z_ACCL_OUT, TEMP_OUT, DATA_ CNTR, and the checksum value.

In these cases, use the following formula to verify the 16-bit checksum value, treating each byte in the formula as an independent, unsigned, 8-bit number:

Checksum = DIAG_STAT, Bits[15:8] + DIAG_STAT, Bits[7:0] + X_GYRO_OUT, Bits[15:8] + X_GYRO_OUT, Bits[7:0] + Y_GYRO_OUT, Bits[15:8] + Y_GYRO_OUT, Bits[7:0] + Z_GYRO_OUT, Bits[15:8] + Z_GYRO_OUT, Bits[7:0] + X_ACCL_OUT, Bits[15:8] + X_ACCL_OUT, Bits[7:0] + Y_ACCL_OUT, Bits[15:8] + Y_ACCL_OUT, Bits[7:0] + Z_ACCL_OUT, Bits[15:8] + Z_ACCL_OUT, Bits[7:0] + TEMP_OUT, Bits[15:8] + TEMP_OUT, Bits[7:0] + DATA_CNTR, Bits[15:8] + DATA_CNTR, Bits[7:0]

16-Bit Burst Mode with BURST_SEL = 1

In 16-bit burst mode with BURST_SEL = 1, a burst contains calibrated delta angle and delta velocity data in 16-bit format. This mode is particularly appropriate for cases where there is no decimation nor filtering. Not only is the sample rate high (~2 kSPS), the lower 16 bits are not used.

The sequence of registers (and checksum value) in the burst read includes the following registers and value: DIAG_STAT, X_DELTANG_OUT, Y_DELTANG_OUT, Z_DELTANG_OUT, X_DELTVEL_OUT, Y_DELTVEL_OUT, Z_DELTVEL_OUT, TEMP_OUT, DATA_CNTR, and the checksum value.

In these cases, use the following formula to verify the 16-bit checksum value, treating each byte in the formula as an independent, unsigned, 8-bit number:

Checksum = DIAG_STAT, Bits[15:8] + DIAG_STAT, Bits[7:0] + X_DELTANG_OUT, Bits[15:8] + X_DELTANG_OUT, Bits[7:0] + Y_DELTANG_OUT, Bits[15:8] + Y_DELTANG_OUT, Bits[7:0] + Z_DELTANG_OUT, Bits[15:8] + Z_DELTANG_OUT, Bits[7:0] + X_DELTVEL_OUT, Bits[15:8] + X_DELTVEL_OUT, Bits[7:0] + Y_DELTVEL_OUT, Bits[15:8] + Y_DELTVEL_OUT, Bits[7:0] + Z_DELTVEL_OUT, Bits[15:8] + Z_DELTVEL_OUT, Bits[7:0] +

THEORY OF OPERATION

TEMP_OUT, Bits[15:8] + TEMP_OUT, Bits[7:0] + DATA_CNTR, Bits[15:8] + DATA_CNTR, Bits[7:0]

32-Bit Burst Mode with BURST_SEL = 0

In 32-bit burst mode with BURST_SEL = 0, a burst contains calibrated gyroscope and accelerometer data in 32-bit format. This mode is appropriate for cases where there is averaging (decimation) and/or low-pass filtering of the data. This mode is also the recommended burst mode if the application depends on optimal performance of the linear *g* compensation feature.

The sequence of registers (and checksum value) in the burst read includes the following registers and value: DIAG_STAT, X_GYRO_LOW, X_GYRO_OUT, Y_GYRO_LOW, Y_GYRO_OUT, Z_GYRO_LOW, Z_GYRO_OUT, X_ACCL_LOW, X_ACCL_OUT, Y_ACCL_LOW, Y_ACCL_OUT, Z_ACCL_LOW, Z_ACCL_OUT, TEMP_OUT, DATA_ CNTR, and the checksum value. In these cases, use the following formula to verify the 16-bit checksum value, treating each byte in the formula as an independent, unsigned, 8-bit number:

Checksum = DIAG_STAT, Bits[15:8] + DIAG_STAT, Bits[7:0] + X_GYRO_LOW, Bits[15:8] + X_GYRO_LOW, Bits[7:0] + X_GYRO_OUT, Bits[15:8] + X_GYRO_OUT, Bits[7:0] + Y_GYRO_LOW, Bits[15:8] + Y_GYRO_LOW, Bits[7:0] + Y_GYRO_OUT, Bits[15:8] + Y_GYRO_OUT, Bits[7:0] + Z_GYRO_LOW, Bits[15:8] + Z_GYRO_LOW, Bits[7:0] + Z_GYRO_OUT, Bits[15:8] + Z_GYRO_OUT, Bits[7:0] + X_ACCL_LOW, Bits[15:8] + X_ACCL_LOW, Bits[7:0] + X_ACCL_OUT, Bits[15:8] + X_ACCL_OUT, Bits[7:0] + Y_ACCL_LOW, Bits[15:8] + Y_ACCL_LOW, Bits[7:0] + Y_ACCL_OUT, Bits[15:8] + Y_ACCL_OUT, Bits[7:0] + Z_ACCL_LOW, Bits[15:8] + Z_ACCL_LOW, Bits[7:0] + Z_ACCL_OUT, Bits[15:8] + Z_ACCL_OUT, Bits[7:0] + TEMP_OUT, Bits[15:8] + TEMP_OUT, Bits[7:0] + DATA_CNTR, Bits[15:8] + DATA_CNTR, Bits[7:0]

32-Bit Burst Mode with BURST_SEL = 1

In 32-bit burst mode with BURST_SEL = 1, a burst contains calibrated delta angle and delta velocity data in 32-bit format. This mode is appropriate for cases where there is averaging (decimation) and/or low-pass filtering of the data.

The sequence of registers (and checksum value) in the burst read includes the following registers and value: DIAG_STAT, X_DELTANG_LOW, X_DELTANG_OUT, Y_DELTANG_LOW, Y_DELTANG_OUT, Z_DELTANG_LOW, Z_DELTANG_OUT, X_DELTVEL_LOW, X_DELTVEL_OUT, Y_DELTVEL_LOW, Y_DELTVEL_OUT, Z_DELTVEL_LOW, Z_DELTVEL_OUT, TEMP_OUT, DATA_ CNTR, and the checksum value. In these cases, use the following formula to verify the 16-bit checksum value, treating each byte in the formula as an independent, unsigned, 8-bit number:

Checksum = DIAG_STAT, Bits[15:8] + DIAG_STAT, Bits[7:0] + X_DELTANG_LOW, Bits[15:8] + X_DELTANG_LOW, Bits[7:0] + X_DELTANG_OUT, Bits[15:8] + X_DELTANG_OUT, Bits[7:0] + Y_DELTANG_LOW, Bits[15:8] + Y_DELTANG_LOW, Bits[7:0] + Y_DELTANG_OUT, Bits[15:8] + Y_DELTANG_OUT, Bits[7:0] + Z_DELTANG_LOW, Bits[15:8] + Z_DELTANG_LOW, Bits[7:0] + Z_DELTANG_OUT, Bits[15:8] + Z_DELTANG_OUT, Bits[7:0] + X_DELTVEL_LOW, Bits[15:8] + X_DELTVEL_LOW, Bits[7:0] + X_DELTVEL_OUT, Bits[15:8] + X_DELTVEL_OUT, Bits[7:0] + Y_DELTVEL_LOW, Bits[15:8] + Y_DELTVEL_LOW, Bits[7:0] + Y_DELTVEL_OUT, Bits[15:8] + Y_DELTVEL_OUT, Bits[7:0] + Z_DELTVEL_LOW, Bits[15:8] + Z_DELTVEL_LOW, Bits[7:0] + Z_DELTVEL_OUT, Bits[15:8] + Z_DELTVEL_OUT, Bits[7:0] + TEMP_OUT, Bits[15:8] + TEMP_OUT, Bits[7:0] + DATA_CNTR, Bits[15:8] + DATA_CNTR, Bits[7:0]

DEVICE CONFIGURATION

Each configuration register contains 16 bits (two bytes). Bits[7:0] contain the low byte, and Bits[15:8] contain the high byte of each register. Each byte has its own unique address in the user register map (see Table 8). Updating the contents of a register requires writing to both of its bytes in the following sequence: low byte first, high byte second. There are three parts to coding a SPI command (see Figure 30) that write a new byte of data to a register: the write bit ($\overline{R}$/W = 1), the address of the byte, [A6:A0], and the new data for that location, [DC7:DC0]. Figure 34 shows a coding example for writing 0x0004 to the FILT_CTRL register (see Table 101). In Figure 34, the 0xDC04 command writes 0x04 to Address 0x5C (lower byte) and the 0xDD00 command writes 0x00 to Address 0x5D (upper byte).

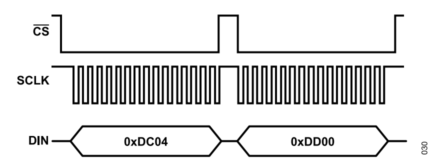


Figure 34. SPI Sequence for Writing 0x0004 to FILT_CTRL

Memory Structure

Figure 35 provides a functional diagram for the memory structure of the ADIS16477. The flash memory bank contains the operational code, unit specific calibration coefficients and user configuration settings. During initialization (power application or reset recover), this information loads from the flash memory into the static random access memory (SRAM), which supports all normal operation, including register access through the SPI port. Writing to a configuration register using the SPI updates the SRAM location of the register but does not automatically update its settings in the flash memory bank. The manual flash memory update command (Register GLOB_CMD, Bit 3, see Table 113) provides a convenient method for saving all of these settings to the flash memory bank at one time. A yes in the flash backup column of Table 8 identifies the registers that have storage support in the flash memory bank.

THEORY OF OPERATION

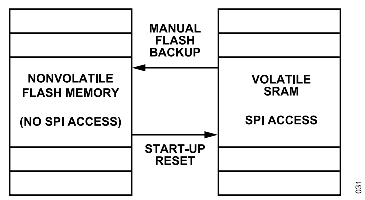


Figure 35. SRAM and Flash Memory Diagram

USER REGISTER MEMORY MAP

Table 8. User Register Memory Map (N/A Means Not Applicable)

Name	R/W	Flash Backup	Address	Default	Register Description
Reserved	N/A	N/A	0x00, 0x01	N/A	Reserved
DIAG_STAT	R	No	0x02, 0x03	0x0000	Output, system error flags
X_GYRO_LOW	R	No	0x04, 0x05	N/A	Output, x-axis gyroscope, low word
X_GYRO_OUT	R	No	0x06, 0x07	N/A	Output, x-axis gyroscope, high word
Y_GYRO_LOW	R	No	0x08, 0x09	N/A	Output, y-axis gyroscope, low word
Y_GYRO_OUT	R	No	0x0A, 0x0B	N/A	Output, y-axis gyroscope, high word
Z_GYRO_LOW	R	No	0x0C, 0x0D	N/A	Output, z-axis gyroscope, low word
Z_GYRO_OUT	R	No	0x0E, 0x0F	N/A	Output, z-axis gyroscope, high word
X_ACCL_LOW	R	No	0x10, 0x11	N/A	Output, x-axis accelerometer, low word
X_ACCL_OUT	R	No	0x12, 0x13	N/A	Output, x-axis accelerometer, high word
Y_ACCL_LOW	R	No	0x14, 0x15	N/A	Output, y-axis accelerometer, low word
Y_ACCL_OUT	R	No	0x16, 0x17	N/A	Output, y-axis accelerometer, high word
Z_ACCL_LOW	R	No	0x18, 0x19	N/A	Output, z-axis accelerometer, low word
Z_ACCL_OUT	R	No	0x1A, 0x1B	N/A	Output, z-axis accelerometer, high word
TEMP_OUT	R	No	0x1C, 0x1D	N/A	Output, temperature
TIME_STAMP	R	No	0x1E, 0x1F	N/A	Output, time stamp
Reserved	N/A	N/A	0x20, 0x21	N/A	Reserved
DATA_CNTR	R	No	0x22, 0x23	N/A	New data counter
X_DELTANG_LOW	R	No	0x24, 0x25	N/A	Output, x-axis delta angle, low word
X_DELTANG_OUT	R	No	0x26, 0x27	N/A	Output, x-axis delta angle, high word
Y_DELTANG_LOW	R	No	0x28, 0x29	N/A	Output, y-axis delta angle, low word
Y_DELTANG_OUT	R	No	0x2A, 0x2B	N/A	Output, y-axis delta angle, high word
Z_DELTANG_LOW	R	No	0x2C, 0x2D	N/A	Output, z-axis delta angle, low word
Z_DELTANG_OUT	R	No	0x2E, 0x2F	N/A	Output, z-axis delta angle, high word
X_DELTVEL_LOW	R	No	0x30, 0x31	N/A	Output, x-axis delta velocity, low word
X_DELTVEL_OUT	R	No	0x32, 0x33	N/A	Output, x-axis delta velocity, high word
Y_DELTVEL_LOW	R	No	0x34, 0x35	N/A	Output, y-axis delta velocity, low word
Y_DELTVEL_OUT	R	No	0x36, 0x37	N/A	Output, y-axis delta velocity, high word
Z_DELTVEL_LOW	R	No	0x38, 0x39	N/A	Output, z-axis delta velocity, low word
Z_DELTVEL_OUT	R	No	0x3A, 0x3B	N/A	Output, z-axis delta velocity, high word
Reserved	N/A	N/A	0x3C to 0x3F	N/A	Reserved
XG_BIAS_LOW	R/W	Yes	0x40, 0x41	0x0000	Calibration, offset, gyroscope, x-axis, low word
XG_BIAS_HIGH	R/W	Yes	0x42, 0x43	0x0000	Calibration, offset, gyroscope, x-axis, high word
YG_BIAS_LOW	R/W	Yes	0x44, 0x45	0x0000	Calibration, offset, gyroscope, y-axis, low word
YG_BIAS_HIGH	R/W	Yes	0x46, 0x47	0x0000	Calibration, offset, gyroscope, y-axis, high word
ZG_BIAS_LOW	R/W	Yes	0x48, 0x49	0x0000	Calibration, offset, gyroscope, z-axis, low word
ZG_BIAS_HIGH	R/W	Yes	0x4A, 0x4B	0x0000	Calibration, offset, gyroscope, z-axis, high word
XA_BIAS_LOW	R/W	Yes	0x4C, 0x4D	0x0000	Calibration, offset, accelerometer, x-axis, low word
XA_BIAS_HIGH	R/W	Yes	0x4E, 0x4F	0x0000	Calibration, offset, accelerometer, x-axis, high word
YA_BIAS_LOW	R/W	Yes	0x50, 0x51	0x0000	Calibration, offset, accelerometer, y-axis, low word
YA_BIAS_HIGH	R/W	Yes	0x52, 0x53	0x0000	Calibration, offset, accelerometer, y-axis, high word
ZA_BIAS_LOW	R/W	Yes	0x54, 0x55	0x0000	Calibration, offset, accelerometer, z-axis, low word
ZA_BIAS_HIGH	R/W	Yes	0x56, 0x57	0x0000	Calibration, offset, accelerometer, z-axis, high word
Reserved	N/A	N/A	0x58 to 0x5B	N/A	Reserved
FILT_CTRL	R/W	Yes	0x5C, 0x5D	0x0000	Control, Bartlett window FIR filter
RANG_MDL	R	No	0x5E, 0x5F	N/A[1]	Measurement range (model specific) identifier
MSC_CTRL	R/W	Yes	0x60, 0x61	0x00C1	Control, input/output and other miscellaneous options
UP_SCALE	R/W	Yes	0x62, 0x63	0x07D0	Control, scale factor for input clock, pulse per second (PPS) mode
DEC_RATE	R/W	Yes	0x64, 0x65	0x0000	Control, decimation filter (output data rate)

USER REGISTER MEMORY MAP

Table 8. User Register Memory Map (N/A Means Not Applicable)

Name	R/W	Flash Backup	Address	Default	Register Description
NULL_CNFG	R/W	Yes	0x66, 0x67	0x070A	Control, bias estimation period
GLOB_CMD	W	No	0x68, 0x69	N/A	Control, global commands
Reserved	N/A	N/A	0x6A to 0x6B	N/A	Reserved
FIRM_REV	R	No	0x6C, 0x6D	N/A	Identification, firmware revision
FIRM_DM	R	No	0x6E, 0x6F	N/A	Identification, date code, day and month
FIRM_Y	R	No	0x70, 0x71	N/A	Identification, date code, year
PROD_ID	R	No	0x72, 0x73	0x405D	Identification, device number
SERIAL_NUM	R	No	0x74, 0x75	N/A	Identification, serial number
USER_SCR_1	R/W	Yes	0x76, 0x77	N/A	User Scratch Register 1
USER_SCR_2	R/W	Yes	0x78, 0x79	N/A	User Scratch Register 2
USER_SCR_3	R/W	Yes	0x7A, 0x7B	N/A	User Scratch Register 3
FLSHCNT_LOW	R	No	0x7C, 0x7D	N/A	Output, flash memory write cycle counter, lower word
FLSHCNT_HIGH	R	No	0x7E, 0x7E	N/A	Output, flash memory write cycle counter, upper word

[1] See Table 102 for the default value in this register, which is model specific.

USER REGISTER DEFINITIONS

STATUS/ERROR FLAG INDICATORS (DIAG_STAT)

Table 9. DIAG_STAT Register Definition

Addresses	Default	Access	Flash Backup
0x02, 0x03	0x0000	R	No

Table 10. DIAG_STAT Bit Assignments

Bits	Description
[15:8]	Reserved.
7	Clock error. A 1 indicates that the internal data sampling clock (f_{SM}, see Figure 19 and Figure 20) does not synchronize with the external clock, which only applies when using scaled sync mode (Register MSC_CTRL, Bits[4:2] = 010, see Table 105). When this error occurs, adjust the frequency of the clock signal on the SYNC pin to operate within the appropriate range.
6	Memory failure. A 1 indicates a failure in the flash memory test (Register GLOB_CMD, Bit 4, see Table 113), which involves a comparison between a cyclic redundancy check (CRC) calculation of the present flash memory and a CRC calculation from the same memory locations at the time of initial programming (during the production process). If this error occurs, repeat the same test. If this error persists, replace the ADIS16477 device.
5	Sensor failure. A 1 indicates failure of at least one sensor, at the conclusion of the self test (Register GLOB_CMD, Bit 2, see Table 113). If this error occurs, repeat the same test. If this error persists, replace the ADIS16477. Motion, during the execution of this test, can cause a false failure.
4	Standby mode. A 1 indicates that the voltage across VDD and GND is <2.8 V, which causes data processing to stop. When VDD ≥ 2.8 V for 250 ms, the ADIS16477 reinitializes itself and starts producing data again.
3	SPI communication error. A 1 indicates that the total number of SCLK cycles is not equal to an integer multiple of 16. When this error occurs, repeat the previous communication sequence. Persistence in this error may indicate a weakness in the SPI service that the ADIS16477 is receiving from the system it is supporting.
2	Flash memory update failure. A 1 indicates that the most recent flash memory update (Register GLOB_CMD, Bit 3, see Table 113) failed. If this error occurs, ensure that VDD ≥ 3 V and repeat the update attempt. If this error persists, replace the ADIS16477.
1	Data path overrun. A 1 indicates that one of the data paths experienced an overrun condition. If this error occurs, initiate a reset using the $\overline{\text{RST}}$ pin (see Table 5, Pin F3) or Register GLOB_CMD, Bit 7 (see Table 113). See the Serial Port Operation section for more details on conditions that may cause this bit to be set to 1.
0	Reserved

The DIAG_STAT register (see Table 9 and Table 10) provides error flags for monitoring the integrity and operation of the ADIS16477. Reading this register causes all of its bits to return to 0. The error flags in DIAG_STAT are sticky, meaning that, when they raise to a 1, they remain there until a read request clears them. If an error condition persists, the flag (bit) automatically returns to an alarm value of 1.

GYROSCOPE DATA

The gyroscopes in the ADIS16477 measure the angular rate of rotation around three orthogonal axes (x, y, and z). Figure 36 shows the orientation of each gyroscope axis, along with the direction of rotation that produces a positive response in each of their measurements.

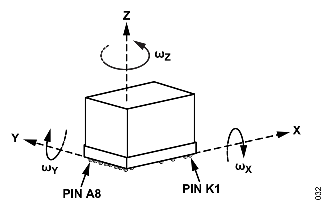


Figure 36. Gyroscope Axis and Polarity Assignments

Each gyroscope has two output data registers. Figure 37 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis gyroscope measurements. This format also applies to the y- and z-axes.

Additional information on the precision and resolution of the accelerometers can be found in the Digital Resolution of Gyroscopes and Accelerometers section of this data sheet.

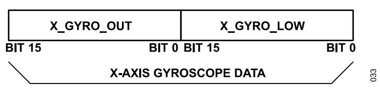


Figure 37. Gyroscope Output Data Structure

GYROSCOPE MEASUREMENT RANGE/SCALE FACTOR

Table 11 provides the measurement range ($\pm\omega_{MAX}$) and scale factor (K_G) for the gyroscope in each ADIS16477 model.

Table 11. Gyroscope Measurement Range and Scale Factors

Model	Range, $\pm\omega_{MAX}$ (°/sec)	Scale Factor, K_G (LSB/°/sec)
ADIS16477-1	±125	160
ADIS16477-2	±500	40
ADIS16477-3	±2000	10

GYROSCOPE DATA FORMATTING

Table 12 and Table 13 offer various numerical examples that demonstrate the format of the rotation rate data in both 16-bit and 32-bit formats.

Table 12. 16-Bit Gyroscope Data Format Examples

Rotation Rate	Decimal	Hex	Binary
$+\omega_{MAX}$	+20,000	0x4E20	0100 1110 0010 0000
$+2/K_G$	+2	0x0002	0000 0000 0000 0010
$+1/K_G$	+1	0x0001	0000 0000 0000 0001
0°/sec	0	0x0000	0000 0000 0000 0000
$-1/K_G$	−1	0xFFFF	1111 1111 1111 1111
$-2/K_G$	−2	0xFFFE	1111 1111 1111 1110
$-\omega_{MAX}$	−20,000	0xB1E0	1011 0001 1110 0000

Table 13. 32-Bit Gyroscope Data Format Examples

Rotation Rate (°/sec)	Decimal	Hex
$+\omega_{MAX}$	+1,310,720,000	0x4E200000
$+2/(K_G \times 2^{16})$	+2	0x00000002
$+1/(K_G \times 2^{16})$	+1	0x00000001
0	0	0x0000000
$-1/(K_G \times 2^{16})$	−1	0xFFFFFFFF
$-2/(K_G \times 2^{16})$	−2	0xFFFFFFFE
$-\omega_{MAX}$	−1,310,720,000	0xB1E00000

X-AXIS GYROSCOPE (X_GYRO_LOW AND X_GYRO_OUT)

Table 14. X_GYRO_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x04, 0x05	Not applicable	R	No

Table 15. X_GYRO_LOW Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope data; additional resolution bits

Table 16. X_GYRO_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x06, 0x07	Not applicable	R	No

Table 17. X_GYRO_OUT Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope data; high word; twos complement, 0°/sec = 0x0000, 1 LSB = $1/K_G$ (See Table 11 for K_G)

The X_GYRO_LOW (see Table 14 and Table 15) and X_GYRO_OUT (see Table 16 and Table 17) registers contain the gyroscope data for the x-axis.

Y-AXIS GYROSCOPE (Y_GYRO_LOW AND Y_GYRO_OUT)

Table 18. Y_GYRO_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x08, 0x09	Not applicable	R	No

Table 19. Y_GYRO_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope data; additional resolution bits

Table 20. Y_GYRO_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x0A, 0x0B	Not applicable	R	No

Table 21. Y_GYRO_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope data; high word; twos complement, 0°/sec = 0x0000, 1 LSB = $1/K_G$ (see Table 11 for K_G)

The Y_GYRO_LOW (see Table 18 and Table 19) and Y_GYRO_OUT (see Table 20 and Table 21) registers contain the gyroscope data for the y-axis.

GYROSCOPE DATA

Z-AXIS GYROSCOPE (Z_GYRO_LOW AND Z_GYRO_OUT)

Table 22. Z_GYRO_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x0C, 0x0D	Not applicable	R	No

Table 23. Z_GYRO_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope data; additional resolution bits

Table 24. Z_GYRO_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x0E, 0x0F	Not applicable	R	No

Table 25. Z_GYRO_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope data; high word; twos complement, 0°/sec = 0x0000, 1 LSB = $1/K_G$ (see Table 11 for K_G)

The Z_GYRO_LOW (see Table 22 and Table 23) and Z_GYRO_OUT (see Table 24 and Table 25) registers contain the gyroscope data for the z-axis.

ACCELERATION DATA

The accelerometers in the ADIS16477 measure both dynamic and static (response to gravity) acceleration along the same three orthogonal axes that define the axes of rotation for the gyroscopes (x, y, and z). Figure 38 shows the orientation of each accelerometer axis, along with the direction of acceleration that produces a positive response in each of their measurements.

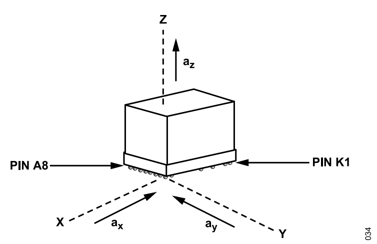


Figure 38. Accelerometer Axis and Polarity Assignments

Each accelerometer has two output data registers. Figure 39 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis accelerometer measurements. This format also applies to the y- and z-axes.

Additional information on the precision and resolution of the accelerometers can be found in the Digital Resolution of Gyroscopes and Accelerometers section of this data sheet.

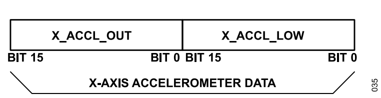


Figure 39. Accelerometer Output Data Structure

ACCELEROMETER DATA FORMATTING

Table 26 and Table 27 offer various numerical examples that demonstrate the format of the linear acceleration data in both 16-bit and 32-bit formats.

Table 26. 16-Bit Accelerometer Data Format Examples

Acceleration	Decimal	Hex	Binary
+40 *g*	+32,000	0x7D00	0111 1101 0000 0000
+2.5 m*g*	+2	0x0002	0000 0000 0000 0010
+1.25 m*g*	+1	0x0001	0000 0000 0000 0001
0 m*g*	0	0x0000	0000 0000 0000 0000
−1.25 m*g*	−1	0xFFFF	1111 1111 1111 1111
−2.5 m*g*	−2	0xFFFE	1111 1111 1111 1110
−40 *g*	−32,000	0x8300	1000 0011 0000 0000

Table 27. 32-Bit Accelerometer Data Format Examples

Acceleration	Decimal	Hex
+40 *g*	+2,097,152,000	0x7D000000
$+1.25/2^{15}$ m*g*	+2	0x00000002
$+1.25/2^{16}$ m*g*	+1	0x00000001
0	0	0x00000000
$−1.25/2^{16}$ m*g*	−1	0xFFFFFFFF
$−1.25/2^{15}$ m*g*	−2	0xFFFFFFFE
−40 *g*	−2,097,152,000	0x83000000

X-AXIS ACCELEROMETER (X_ACCL_LOW AND X_ACCL_OUT)

Table 28. X_ACCL_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x10, 0x11	Not applicable	R	No

Table 29. X_ACCL_LOW Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer data; additional resolution bits

Table 30. X_ACCL_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x12, 0x13	Not applicable	R	No

Table 31. X_ACCL_OUT Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer data, high word; twos complement, ±40 *g* range; 0 *g* = 0x0000, 1 LSB = 1.25 m*g*

The X_ACCL_LOW (see Table 28 and Table 29) and X_ACCL_OUT (see Table 30 and Table 31) registers contain the accelerometer data for the x-axis.

Y-AXIS ACCELEROMETER (Y_ACCL_LOW AND Y_ACCL_OUT)

Table 32. Y_ACCL_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x14, 0x15	Not applicable	R	No

GYROSCOPE DATA

Table 33. Y_ACCL_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer data; additional resolution bits

Table 34. Y_ACCL_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x16, 0x17	Not applicable	R	No

Table 35. Y_ACCL_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer data, high word; twos complement, ±40 *g* range; 0 *g* = 0x0000, 1 LSB = 1.25 m*g*

The Y_ACCL_LOW (see Table 32 and Table 33) and Y_ACCL_OUT (see Table 34 and Table 35) registers contain the accelerometer data for the y-axis.

Z-AXIS ACCELEROMETER (Z_ACCL_LOW AND Z_ACCL_OUT)

Table 36. Z_ACCL_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x18, 0x19	Not applicable	R	No

Table 37. Z_ACCL_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer data; additional resolution bits

Table 38. Z_ACCL_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x1A, 0x1B	Not applicable	R	No

Table 39. Z_ACCL_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer data, high word; twos complement, ±40 *g* range; 0 *g* = 0x0000, 1 LSB = 1.25 m*g*

The Z_ACCL_LOW (see Table 36 and Table 37) and Z_ACCL_OUT (see Table 38 and Table 39) registers contain the accelerometer data for the z-axis.

INTERNAL TEMPERATURE (TEMP_OUT)

Table 40. TEMP_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x1C, 0x1D	Not applicable	R	No

Table 41. TEMP_OUT Bit Definitions

Bits	Description
[15:0]	Temperature data; twos complement, 1 LSB = 0.1°C, 0°C = 0x0000

The TEMP_OUT register (see Table 40 and Table 41) provides a coarse measurement of the temperature inside of the ADIS16477. This data is most useful for monitoring relative changes in the thermal environment.

Table 42. TEMP_OUT Data Format Examples

Temperature (°C)	Decimal	Hex	Binary
+105	+1050	0x041A	0000 0100 0001 1010
+25	+250	0x00FA	0000 0000 1111 1010
+0.2	+2	0x0002	0000 0000 0000 0010
+0.1	+1	0x0001	0000 0000 0000 0001
+0	0	0x0000	0000 0000 0000 0000
+0.1	−1	0xFFFF	1111 1111 1111 1111
+0.2	−2	0xFFFE	1111 1111 1111 1110
−40	−400	0xFE70	1111 1110 0111 0000

TIME STAMP (TIME_STAMP)

Table 43. TIME_STAMP Register Definition

Addresses	Default	Access	Flash Backup
0x1E, 0x1F	Not applicable	R	No

Table 44. TIME_STAMP Bit Definitions

Bits	Description
[15:0]	Time from the last pulse on the SYNC pin; offset binary format, 1 LSB = 49.02 μs

The TIME_STAMP register (see Table 43 and Table 44) works in conjunction with scaled sync mode (Register MSC_CTRL, Bits[4:2] = 010, see Table 105). The 16-bit number in TIME_ STAMP contains the time associated with the last sample in each data update relative to the most recent edge of the clock signal in the SYNC pin. For example, when the value in the UP_SCALE register (see Table 107) represents a scale factor of 20, DEC_RATE = 0, and the external SYNC rate = 100 Hz, the following time stamp sequence results: 0 LSB, 10 LSB, 21 LSB, 31 LSB, 41 LSB, 51 LSB, 61 LSB, 72 LSB, …, 194 LSB for the 20th sample, which translates to 0 μs, 490 μs, …, 9510 μs, the time from the first SYNC edge.

DATA UPDATE COUNTER (DATA_CNTR)

Table 45. DATA_CNTR Register Definition

Addresses	Default	Access	Flash Backup
0x22, 0x23	Not applicable	R	No

Table 46. DATA_CNTR Bit Definitions

Bits	Description
[15:0]	Data update counter, offset binary format

When the ADIS16477 goes through its power-on sequence or when it recovers from a reset command, DATA_CNTR (see Table 45 and Table 46) starts with a value of 0x0000 and increments every time new data loads into the output registers. When the DATA_CNTR value reaches 0xFFFF, the next data update causes it to wrap back around to 0x0000, where it continues to increment every time new data loads into the output registers.

DELTA ANGLES

In addition to the angular rate of rotation (gyroscope) measurements around each axis (x, y, and z), the ADIS16477 also provides delta angle measurements that represent a calculation of angular displacement between each sample update.

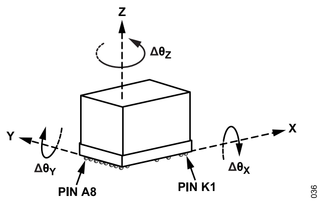


Figure 40. Delta Angle Axis and Polarity Assignments

The delta angle outputs represent an integration of the gyroscope measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta\theta_{x,\,nD} = \frac{1}{2 \times f_S} \times \sum_{d=0}^{D-1} \left(\omega_{x,\,nD+d} + \omega_{x,\,nD+d-1}\right)$$

where:
D is the decimation rate (DEC_RATE + 1, see Table 109).
f_S is the sample rate. d is the incremental variable in the summation formula.
ω_X is the x-axis rate of rotation (gyroscope).
n is the sample time, prior to the decimation filter.

When using the internal sample clock, f_S is equal to a nominal rate of 2000 SPS. For better precision in this measurement, measure the internal sample rate (f_S) using the data ready signal on the DR pin (DEC_RATE = 0x0000, see Table 108), divide each delta angle result (from the delta angle output registers) by the data ready frequency and multiply it by 2000. Each axis of the delta angle measurements has two output data registers. Figure 41 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis delta angle measurements. This format also applies to the y- and z-axes.

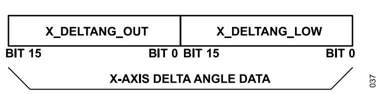


Figure 41. Delta Angle Output Data Structure

DELTA ANGLE MEASUREMENT RANGE

Table 47 shows the measurement range and scale factor for each ADIS16477 model.

Table 47. Delta Angle Measurement Range and Scale Factor

Model	Measurement Range, $\pm\Delta\theta_{MAX}$ (°)
ADIS16477-1BMLZ	±360
ADIS16477-2BMLZ	±720
ADIS16477-3BMLZ	±2160

X-AXIS DELTA ANGLE (X_DELTANG_LOW AND X_DELTANG_OUT)

Table 48. X_DELTANG_LOW Register Definitions

Addresses	Default	Access	Flash Backup
0x24, 0x25	Not applicable	R	No

Table 49. X_DELTANG_LOW Bit Definitions

Bits	Description
[15:0]	X-axis delta angle data; low word

Table 50. X_DELTANG_OUT Register Definitions

Addresses	Default	Access	Flash Backup
0x26, 0x27	Not applicable	R	No

Table 51. Table 51. X_DELTANG_OUT Bit Definitions

Bits	Description
[15:0]	X-axis delta angle data; twos complement, 0° = 0x0000, 1 LSB = $\Delta\theta_{MAX}/2^{15}$ (see Table 47 for $\Delta\theta_{MAX}$)

The X_DELTANG_LOW (see Table 48 and Table 49) and X_DELTANG_OUT (see Table 50 and Table 51) registers contain the delta angle data for the x-axis.

Y-AXIS DELTA ANGLE (Y_DELTANG_LOW AND Y_DELTANG_OUT)

Table 52. Y_DELTANG_LOW Register Definitions

Addresses	Default	Access	Flash Backup
0x28, 0x29	Not applicable	R	No

Table 53. Y_DELTANG_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis delta angle data; low word

Table 54. Y_DELTANG_OUT Register Definitions

Addresses	Default	Access	Flash Backup
0x2A, 0x2B	Not applicable	R	No

Table 55. Y_DELTANG_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis delta angle data; twos complement, 0° = 0x0000, 1 LSB = $\Delta\theta_{MAX}/2^{15}$ (see Table 47 for $\Delta\theta_{MAX}$)

The Y_DELTANG_LOW (see Table 52 and Table 53) and Y_DELTANG_OUT (see Table 54 and Table 55) registers contain the delta angle data for the y-axis.

Z-AXIS DELTA ANGLE (Z_DELTANG_LOW AND Z_DELTANG_OUT)

Table 56. Z_DELTANG_LOW Register Definitions

Addresses	Default	Access	Flash Backup
0x2C, 0x2D	Not applicable	R	No

Table 57. Z_DELTANG_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis delta angle data; low word

DELTA ANGLES

Table 58. Z_DELTANG_OUT Register Definitions

Addresses	Default	Access	Flash Backup
0x2E, 0x2F	Not applicable	R	No

Table 59. Z_DELTANG_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis delta angle data; twos complement, 0° = 0x0000, 1 LSB = $\Delta\theta_{MAX}/2^{15}$ (see Table 47 for $\Delta\theta_{MAX}$)

The Z_DELTANG_LOW (see Table 56 and Table 57) and Z_DELTANG_OUT (see Table 58 and Table 59) registers contain the delta angle data for the z-axis.

DELTA ANGLE RESOLUTION

Table 60 and Table 61 show various numerical examples that demonstrate the format of the delta angle data in both 16-bit and 32-bit formats.

Table 60. 16-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hex	Binary
$\Delta\theta_{MAX} \times (2^{15}-1)/2^{15}$	+32,767	0x7FFF	0111 1111 1110 1111
$+\Delta\theta_{MAX}/2^{14}$	+2	0x0002	0000 0000 0000 0010
$+\Delta\theta_{MAX}/2^{15}$	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
$-\Delta\theta_{MAX}/2^{15}$	−1	0xFFFF	1111 1111 1111 1111
$-\Delta\theta_{MAX}/2^{14}$	−2	0xFFFE	1111 1111 1111 1110
$-\Delta\theta_{MAX}$	−32,768	0x8000	1000 0000 0000 0000

Table 61. 32-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hex
$+\Delta\theta_{MAX} \times (2^{31} - 1)/2^{31}$	+2,147,483,647	0x7FFFFFFF
$+\Delta\theta_{MAX}/2^{30}$	+2	0x00000002
$+\Delta\theta_{MAX}/2^{31}$	+1	0x00000001
0	0	0x00000000
$-\Delta\theta_{MAX}/2^{31}$	−1	0xFFFFFFFF
$-\Delta\theta_{MAX}/2^{30}$	−2	0xFFFFFFFE
$-\Delta\theta_{MAX}$	−2,147,483,648	0x80000000

DELTA VELOCITY

In addition to the linear acceleration measurements along each axis (x, y, and z), the ADIS16477 also provides delta velocity measurements that represent a calculation of linear velocity change between each sample update.

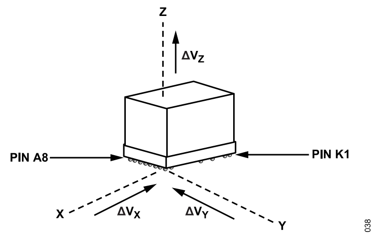


Figure 42. Delta Velocity Axis and Polarity Assignments

The delta velocity outputs represent an integration of the acceleration measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta V_{x,\ nD} = \frac{1}{2 \times f_S} \times \sum_{d=0}^{D-1} \left(a_{x,\ nD+d} + a_{x,\ nD+d-1}\right)$$

where:
x is the x-axis. n is the sample time, prior to the decimation filter.
D is the decimation rate (DEC_RATE + 1, see Table 109).
f_S is the sample rate.
d is the incremental variable in the summation formula.
a_X is the x-axis acceleration.

When using the internal sample clock, f_S is equal to a nominal rate of 2000 SPS. For better precision in this measurement, measure the internal sample rate (f_S) using the data ready signal on the DR pin (DEC_RATE = 0x0000, see Table 108), divide each delta angle result (from the delta angle output registers) by the data ready frequency and multiply it by 2000. Each axis of the delta velocity measurements has two output data registers. Figure 43 shows how these two registers combine to support 32-bit, twos complement data format for the delta velocity measurements along the x-axis. This format also applies to the y- and z-axes.

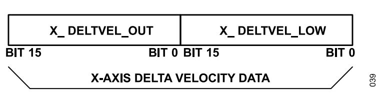


Figure 43. Delta Angle Output Data Structure

X-AXIS DELTA VELOCITY (X_DELTVEL_LOW AND X_DELTVEL_OUT)

Table 62. X_DELTVEL_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x30, 0x31	Not applicable	R	No

Table 63. X_DELTVEL_LOW Bit Definitions

Bits	Description
[15:0]	X-axis delta velocity data; additional resolution bits

Table 64. X_DELTVEL_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x32, 0x33	Not applicable	R	No

Table 65. X_DELTVEL_OUT Bit Definitions

Bits	Description
[15:0]	X-axis delta velocity data; twos complement, ±400 m/sec range, 0 m/sec = 0x0000; 1 LSB = 400 m/sec ÷ 2^{15} = ~0.01221 m/sec

The X_DELTVEL_LOW (see Table 62 and Table 63) and X_DELTVEL_OUT (see Table 64 and Table 65) registers contain the delta velocity data for the x-axis.

Y-AXIS DELTA VELOCITY (Y_DELTVEL_LOW AND Y_DELTVEL_OUT)

Table 66. Y_DELTVEL_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x34, 0x35	Not applicable	R	No

Table 67. Y_DELTVEL_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis delta velocity data; additional resolution bits

Table 68. Y_DELTVEL_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x36, 0x37	Not applicable	R	No

Table 69. Y_DELTVEL_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis delta velocity data; twos complement, ±400 m/sec range, 0 m/sec = 0x0000; 1 LSB = 400 m/sec ÷ 2^{15} = ~0.01221 m/sec

The Y_DELTVEL_LOW (see Table 66 and Table 67) and Y_DELTVEL_OUT (see Table 68 and Table 69) registers contain the delta velocity data for the y-axis.

Z-AXIS DELTA VELOCITY (Z_DELTVEL_LOW AND Z_DELTVEL_OUT)

Table 70. Z_DELTVEL_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x38, 0x39	Not applicable	R	No

Table 71. Z_DELTVEL_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis delta velocity data; additional resolution bits

Table 72. Z_DELTVEL_OUT Register Definition

Addresses	Default	Access	Flash Backup
0x3A, 0x3B	Not applicable	R	No

Table 73. Z_DELTVEL_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis delta velocity data; twos complement,

DELTA VELOCITY

Table 73. Z_DELTVEL_OUT Bit Definitions

Bits	Description
	±400 m/sec range, 0 m/sec = 0x0000; 1 LSB = 400 m/sec ÷ 2^{15} = ~0.01221 m/sec

The Z_DELTVEL_LOW (see Table 70 and Table 71) and Z_DELTVEL_OUT (see Table 72 and Table 73) registers contain the delta velocity data for the z-axis.

DELTA VELOCITY RESOLUTION

Table 74 and Table 75 offer various numerical examples that demonstrate the format of the delta velocity data in both 16-bit and 32-bit formats.

Table 74. 16-Bit Delta Velocity Data Format Examples

Velocity (m/sec)	Decimal	Hex	Binary
$+400 \times (2^{15} - 1)/2^{15}$	+32,767	0x7FFF	0111 1111 1111 1111
$+400/2^{14}$	+2	0x0002	0000 0000 0000 0010
$+400/2^{15}$	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
$-400/2^{15}$	−1	0xFFFF	1111 1111 1111 1111
$-400/2^{14}$	−2	0xFFFE	1111 1111 1111 1110
−400	−32,768	0x8000	1000 0000 0000 0000

Table 75. 32-Bit Delta Velocity Data Format Examples

Velocity (m/sec)	Decimal	Hex
$+400 \times (2^{31} - 1)/2^{31}$	+2,147,483,647	0x7FFFFFFF
$+400/2^{30}$	+2	0x00000002
$+400/2^{31}$	+1	0x00000001
0	0	0x00000000
$-400/2^{31}$	−1	0xFFFFFFFF
$-400/2^{30}$	−2	0xFFFFFFFE
−400	+2,147,483,648	0x80000000

CALIBRATION

The signal chain of each inertial sensor (accelerometers and gyroscopes) includes the application of unique correction formulas, which are derived from extensive characterization of bias, sensitivity, alignment, response to linear acceleration (gyroscopes), and point of percussion (accelerometer location) over a temperature range of −40°C to +85°C, for each ADIS16477. These correction formulas are not accessible, but users do have the opportunity to adjust the bias for each sensor individually through user accessible registers. These correction factors follow immediately after the factory derived correction formulas in the signal chain, which processes at a rate of 2000 Hz when using the internal sample clock.

CALIBRATION, GYROSCOPE BIAS (XG_BIAS_LOW AND XG_BIAS_HIGH)

Table 76. XG_BIAS_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x40, 0x41	0x0000	R/W	Yes

Table 77. XG_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope offset correction; lower word

Table 78. XG_BIAS_HIGH Register Definition

Addresses	Default	Access	Flash Backup
0x42, 0x43	0x0000	R/W	Yes

Table 79. XG_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope offset correction factor, upper word

The XG_BIAS_LOW (see Table 76 and Table 77) and XG_BIAS_HIGH (see Table 78 and Table 79) registers combine to allow users to adjust the bias of the x-axis gyroscopes. The data format examples in Table 12 also apply to the XG_BIAS_HIGH register, and the data format examples in Table 13 apply to the 32-bit combination of the XG_BIAS_LOW and XG_BIAS_HIGH registers. See Figure 44 for an illustration of how these two registers combine and influence the x-axis gyroscope measurements.

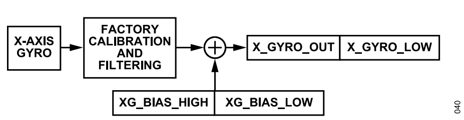


Figure 44. User Calibration Signal Path, Gyroscopes

CALIBRATION, GYROSCOPE BIAS (YG_BIAS_LOW AND YG_BIAS_HIGH)

Table 80. YG_BIAS_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x44, 0x45	0x0000	R/W	Yes

Table 81. YG_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope offset correction; lower word

Table 82. YG_BIAS_HIGH Register Definition

Addresses	Default	Access	Flash Backup
0x46, 0x47	0x0000	R/W	Yes

Table 83. YG_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Y-axis gyroscope offset correction factor, upper word

The YG_BIAS_LOW (see Table 80 and Table 81) and YG_BIAS_HIGH (see Table 82 and Table 83) registers combine to allow users to adjust the bias of the y-axis gyroscopes. The data format examples in Table 12 also apply to the YG_BIAS_HIGH register, and the data format examples in Table 13 apply to the 32-bit combination of the YG_BIAS_LOW and YG_BIAS_HIGH registers. These registers influence the y-axis gyroscope measurements in the same manner that the XG_BIAS_LOW and XG_BIAS_HIGH registers influence the x-axis gyroscope measurements (see Figure 44).

CALIBRATION, GYROSCOPE BIAS (ZG_BIAS_LOW AND ZG_BIAS_HIGH)

Table 84. ZG_BIAS_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x48, 0x49	0x0000	R/W	Yes

Table 85. ZG_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope offset correction; lower word

Table 86. ZG_BIAS_HIGH Register Definition

Addresses	Default	Access	Flash Backup
0x4A, 0x4B	0x0000	R/W	Yes

Table 87. ZG_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Z-axis gyroscope offset correction factor, upper word

The ZG_BIAS_LOW (see Table 84 and Table 85) and ZG_BIAS_HIGH (see Table 86 and Table 87) registers combine to allow users to adjust the bias of the z-axis gyroscopes. The data format examples in Table 12 also apply to the ZG_BIAS_HIGH register, and the data format examples in Table 13 apply to the 32-bit combination of the ZG_BIAS_LOW and ZG_BIAS_HIGH registers. These registers influence the z-axis gyroscope measurements in the same manner that the XG_BIAS_LOW and XG_BIAS_HIGH registers influence the x-axis gyroscope measurements (see Figure 44).

CALIBRATION, ACCELEROMETER BIAS (XA_BIAS_LOW AND XA_BIAS_HIGH)

Table 88. XA_BIAS_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x4C, 0x4D	0x0000	R/W	Yes

CALIBRATION

Table 89. XA_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer offset correction; lower word

Table 90. XA_BIAS_HIGH Register Definition

Addresses	Default	Access	Flash Backup
0x4E, 0x4F	0x0000	R/W	Yes

Table 91. XA_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	X-axis accelerometer offset correction, upper word

The XA_BIAS_LOW (see Table 88 and Table 89) and XA_BIAS_HIGH (see Table 90 and Table 91) registers combine to allow users to adjust the bias of the x-axis accelerometers. The data format examples in Table 26 also apply to the XA_BIAS_HIGH register, and the data format examples in Table 27 apply to the 32-bit combination of the XA_BIAS_LOW and XA_BIAS_HIGH registers. See Figure 45 for an illustration of how these two registers combine and influence the x-axis accelerometer measurements.

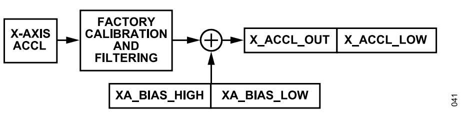


Figure 45. User Calibration Signal Path, Accelerometers

CALIBRATION, ACCELEROMETER BIAS (YA_BIAS_LOW AND YA_BIAS_HIGH)

Table 92. YA_BIAS_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x50, 0x51	0x0000	R/W	Yes

Table 93. YA_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer offset correction; lower word

Table 94. YA_BIAS_HIGH Register Definition

Addresses	Default	Access	Flash Backup
0x52, 0x53	0x0000	R/W	Yes

Table 95. YA_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Y-axis accelerometer offset correction, upper word

The YA_BIAS_LOW (see Table 92 and Table 93) and YA_BIAS_HIGH (see Table 94 and Table 95) registers combine to allow users to adjust the bias of the y-axis accelerometers. The data format examples in Table 26 also apply to the YA_BIAS_HIGH register, and the data format examples in Table 27 apply to the 32-bit combination of the YA_BIAS_LOW and YA_BIAS_HIGH registers. These registers influence the y-axis accelerometer measurements in the same manner that the XA_BIAS_LOW and XA_BIAS_HIGH registers influence the x-axis accelerometer measurements (see Figure 45).

CALIBRATION, ACCELEROMETER BIAS (ZA_BIAS_LOW AND ZA_BIAS_HIGH)

Table 96. ZA_BIAS_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x54, 0x55	0x0000	R/W	Yes

Table 97. ZA_BIAS_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer offset correction; lower word

Table 98. ZA_BIAS_HIGH Register Definition

Addresses	Default	Access	Flash Backup
0x56, 0x57	0x0000	R/W	Yes

Table 99. ZA_BIAS_HIGH Bit Definitions

Bits	Description
[15:0]	Z-axis accelerometer offset correction, upper word

The ZA_BIAS_LOW (see Table 96 and Table 97) and ZA_BIAS_HIGH (see Table 98 and Table 99) registers combine to allow users to adjust the bias of the z-axis accelerometers. The data format examples in Table 26 also apply to the ZA_BIAS_HIGH register, and the data format examples in Table 27 apply to the 32-bit combination of the ZA_BIAS_LOW and ZA_BIAS_HIGH registers. These registers influence the z-axis accelerometer measurements in the same manner that the XA_BIAS_LOW and XA_BIAS_HIGH registers influence the x-axis accelerometer measurements (see Figure 45).

FILTER CONTROL REGISTER (FILT_CTRL)

Table 100. FILT_CTRL Register Definition

Addresses	Default	Access	Flash Backup
0x5C, 0x5D	0x0000	R/W	Yes

Table 101. FILT_CTRL Bit Definitions

Bits	Description
[15:3]	Not used
[2:0]	Filter Size Variable B, number of taps in each stage; $N = 2^B$

The FILT_CTRL register (see Table 100 and Table 101) provides user controls for the Bartlett window FIR filter (see Figure 22), which contains two cascaded averaging filters. For example, use the following sequence to set Register FILT_CTRL, Bits[2:0] = 100, which sets each stage to have 16 taps: 0xCC04 and 0xCD00. Figure 46 provides the frequency response for several settings in the FILT_CTRL register.

CALIBRATION

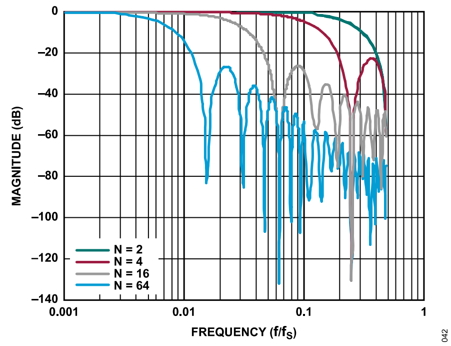


Figure 46. Bartlett Window, FIR Filter Frequency Response (Phase Delay = N Samples)

RANGE IDENTIFIER (RANG_MDL)

Table 102. RANG_MDL Register Definition

Addresses	Default	Access	Flash Backup
0x5E, 0x5F	Not applicable	R	No

Table 103. RANG_MDL Bit Definitions

Bits	Description
[15:3]	Not used
[3:2]	Gyroscope measurement range 00 = ±125°/sec (ADIS16477-1BMLZ) 01 = ±500°/sec (ADIS16477-2BMLZ) 10 = reserved 11 = ±2000°/sec (ADIS16477-3BMLZ)
[1:0]	Reserved, binary value = 11

MISCELLANEOUS CONTROL REGISTER (MSC_CTRL)

Table 104. MSC_CTRL Register Definition

Addresses	Default	Access	Flash Backup
0x60, 0x61	0x00C1	R/W	Yes

Table 105. MSC_CTRL Bit Definitions

Bits	Description
[15:10]	Not used.
9	BURST32. 32-bit burst enable bit. The user must wait until a full data ready cycle until the burst array updates with the desired data type. Changes to this bit may take up to 200 µs after writing to indicate the new value during readback. Note that this bit exists only in Firmware Revision 1.34 and newer. 1 = 32-bit burst data. 0 = 16-bit burst data (default).
8	BURST_SEL. Burst read output array selection. This bit controls what calibrated data is in a burst read. Changes to this bit may take up to 200 µs after writing to indicate the new value during readback. Note that this bit exists only in Firmware Revision 1.34 and newer. 1 = burst data has delta angle and delta velocity data. 0 = burst data has gyroscope and accelerometer data (default).
7	Linear *g* compensation for gyroscopes. When enabled, factory calibrated linear acceleration compensation data is applied to the gyroscope outputs. Changes to this bit may take up to 200 µs after writing to indicate the new value during readback. 1 = enabled (default). 0 = disabled.
6	Point of percussion alignment. When set, this bit allows relocation of the acceleration sensors to a common point of percussion on the package corner by considering angular rotations. Changes to this bit may take up to 200 µs after writing to indicate the new value during readback. 1 = enabled (default). 0 = disabled.
5	Not used, always set to zero.
[4:2]	SYNC function setting. 111 = reserved (do not use). 110 = reserved (do not use). 101 = pulse sync mode. 100 = reserved (do not use). 011 = output sync mode. 010 = scaled sync mode. 001 = direct sync mode. 000 = internal clock mode (default).
1	SYNC polarity (input or output). 1 = rising edge triggers sampling. 0 = falling edge triggers sampling (default).
0	DR polarity. 1 = active high when data is valid (default). 0 = active low when data is valid.

POINT OF PERCUSSION

Register MSC_CTRL, Bit 6 (see Table 105) offers an on/off control for the point of percussion alignment function, which maps the accelerometer sensors to the corner of the package that is closest to Pin A1 (see Figure 47). The factory default setting in the MSC_CTRL register activates this function. To turn this function off while retaining the rest of the factory default settings in the MSC_CTRL register, set Register MSC_CTRL, Bit 6 = 0, using the following command sequence on the DIN pin: 0xE081, then 0xE100.

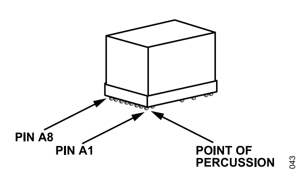


Figure 47. Point of Percussion Reference Point

LINEAR ACCELERATION EFFECT ON GYROSCOPE BIAS

Register MSC_CTRL, Bit 7 (see Table 105) provides an on/off control for the linear *g* compensation in the signal calibration routines

CALIBRATION

of the gyroscope. The factory default contents in the MSC_CTRL register enable this compensation. To turn the compensation off, set Register MSC_CTRL, Bit 7 = 0, using the following sequence on the DIN pin: 0xE04, then 0xEF00.

INTERNAL CLOCK MODE

Register MSC_CTRL, Bits[4:2] (see Table 105), provides five different configuration options for controlling the clock (f_{SM}; see Figure 19 and Figure 20), which controls data acquisition and processing for the inertial sensors. The default setting for Register MSC_CTRL, Bits[4:2] is 000 (binary), which places the ADIS16477 in the internal clock mode. In this mode, an internal clock controls inertial sensor data acquisition and processing at a nominal rate of 2000 Hz. In this mode, each accelerometer data update comes from an average of two data samples (sample rate = 4000 Hz).

OUTPUT SYNC MODE

When Register MSC_CTRL, Bits[4:2] = 011, the ADIS16477 operates in output sync mode, which is the same as internal clock mode with one exception, the SYNC pin pulses when the internal processor collects data from the inertial sensors. Figure 48 provides an example of this signal.

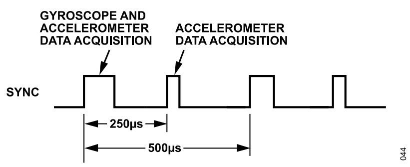


Figure 48. Sync Output Signal, Register MSC_CTRL, Bits[4:2] = 011

DIRECT SYNC MODE

When Register MSC_CTRL, Bits[4:2] = 001, the ADIS16477 operates in direct sync mode. The signal on the SYNC pin directly controls the sample clock. In this mode, the internal processor collects gyroscope data samples on the rising edge of the clock signal (SYNC pin) and collects accelerometer data samples on both rising and falling edges of the clock signal. The internal processor averages both accelerometer samples (from rising and falling edges of the clock signal) together to produce a single data sample. Therefore, when operating the ADIS16477 in this mode, the clock signal (SYNC pin) must have a duty cycle of 50% and a frequency that is within the range of 1900 Hz to 2100 Hz. The ADIS16477 is capable of operating when the clock frequency (SYNC pin) is less than 1900 Hz, but with risk of performance degradation, especially when tracking dynamic inertial conditions (including vibration).

PULSE SYNC MODE

When operating in pulse sync mode (Register MSC_CTRL, Bits[4:2] = 101), the internal processor only collects accelerometer samples on the leading edge of the clock signal, which enables the use of a narrow pulse width (see Table 2) in the clock signal on the SYNC pin. Using pulse sync mode also lowers the bandwidth on the inertial sensors to 370 Hz. When operating in pulse sync mode, the ADIS16477 provides the best performance when the frequency of the clock signal (SYNC pin) is within the range of 1000 Hz to 2100 Hz. The ADIS16477 is capable of operating when the clock frequency (SYNC pin) is less than 1000 Hz, but with risk of performance degradation, especially when tracking dynamic inertial conditions (including vibration).

SCALED SYNC MODE

When Register MSC_CTRL, Bits[4:2] = 010, the ADIS16477 operates in scaled sync mode that supports a frequency range of 1 Hz to 128 Hz for the clock signal on the SYNC pin. This mode of operation is particularly useful when synchronizing the data processing with a PPS signal from a global positioning system (GPS) receiver or with a synchronization signal from a video processing system. When operating in scaled sync mode, the frequency of the sample clock is equal to the product of the external clock scale factor, K_{ECSF}, (from the UP_SCALE register, see Table 106 and Table 107) and the frequency of the clock signal on the SYNC pin.

For example, when using a 1 Hz input signal, set UP_SCALE = 0x07D0 (K_{ECSF} = 2000 (decimal)) to establish a sample rate of 2000 SPS for the inertial sensors and their signal processing. Use the following sequence on the DIN pin to configure UP_SCALE for this scenario: 0xE2D0, then 0xE307.

Table 106. UP_SCALE Register Definition

Addresses	Default	Access	Flash Backup
0x62, 0x63	0x07D0	R/W	Yes

Table 107. UP_SCALE Bit Definitions

Bits	Description
[15:0]	K_{ECSF}; binary format

DECIMATION FILTER (DEC_RATE)

Table 108. DEC_RATE Register Definition

Addresses	Default	Access	Flash Backup
0x64, 0x65	0x0000	R/W	Yes

Table 109. DEC_RATE Bit Definitions

Bits	Description
[15:11]	Don't care
[10:0]	Decimation rate, binary format, maximum = 1999

The DEC_RATE register (see Table 108 and Table 109) provides user control for the averaging decimating filter, which averages and decimates the gyroscope and accelerometer data; it also extends the time that the delta angle and the delta velocity track between each update. When the ADIS16477 operates in internal clock mode (see Register MSC_CTRL, Bits [4:2], in Table 105), the nominal output data rate is equal to 2000/(DEC_RATE + 1). For example, set DEC_RATE = 0x0013 to reduce the output sample rate to 100 SPS (2000 ÷ 20), using the following DIN pin sequence: 0xE413, then 0xE500.

CALIBRATION

DATA UPDATE RATE IN EXTERNAL SYNC MODES

When using the input sync option, in scaled sync mode (Register MSC_CTRL, Bits[4:2] = 010, see Table 105), the output data rate is equal to

$(f_{SYNC} \times K_{ECSF})/(DEC\_RATE + 1)$

where:
f_{SYNC} is the frequency of the clock signal on the SYNC pin.
K_{ESCF} is the value from the UP_SCALE register (see Table 107).

When using direct sync mode and pulse sync mode, K_{ESCF} = 1.

CONTINUOUS BIAS ESTIMATION (NULL_CNFG)

Table 110. NULL_CNFG Register Definition

Addresses	Default	Access	Flash Backup
0x66, 0x67	0x070A	R/W	Yes

Table 111. NULL_CNFG Bit Definitions

Bits	Description
[15:14]	Not used
13	Z-axis accelerometer bias correction enable (1 = enabled)
12	Y-axis accelerometer bias correction enable (1 = enabled)
11	X-axis accelerometer bias correction enable (1 = enabled)
10	Z-axis gyroscope bias correction enable (1 = enabled)
9	Y-axis gyroscope bias correction enable (1 = enabled)
8	X-axis gyroscope bias correction enable (1 = enabled)
[7:4]	Not used
[3:0]	Time base control (TBC), range: 0 to 12 (default = 10); $t_B = 2^{TBC}/2000$, time base; $t_A = 64 \times t_B$, average time

The NULL_CNFG register (see Table 110 and Table 111) provides the configuration controls for the continuous bias estimator (CBE), which associates with the bias correction update command in Register GLOB_CMD, Bit 0 (see Table 113). Register NULL_CNFG, Bits[3:0], establishes the total average time (t_A) for the bias estimates and Register NULL_CNFG, Bits[13:8], provides the on/off controls for each sensor. The factory default configuration for the NULL_CNFG register enables the bias null command for the gyroscopes, disables the bias null command for the accelerometers, and sets the average time to ~32 sec.

GLOBAL COMMANDS (GLOB_CMD)

Table 112. GLOB_CMD Register Definition

Addresses	Default	Access	Flash Backup
0x68, 0x69	Not applicable	W	No

Table 113. GLOB_CMD Bit Definitions

Bits	Description
[15:8]	Not used
7	Software reset
[6:5]	Not used
4	Flash memory test
3	Flash memory update
2	Sensor self test
1	Factory calibration restore
0	Bias correction update

The GLOB_CMD register (see Table 112 and Table 113) provides trigger bits for several operations. Write a 1 to the appropriate bit in GLOB_CMD to start a particular function. During the execution of these commands, data production stops, pulsing stops on the DR pin, and the SPI interface does not respond to requests. Table 1 provides the execution time for each GLOB_CMD command.

SOFTWARE RESET

Use the following DIN sequence to set Register GLOB_CMD, Bit 7 = 1, which triggers a reset: 0xE880, then 0xE900. This reset clears all data, and then restarts data sampling and processing. This function provides a firmware alternative to toggling the $\overline{RST}$ pin (see Table 5, Pin F3).

FLASH MEMORY TEST

Use the following DIN sequence to set Register GLOB_CMD, Bit 4 = 1, which tests the flash memory: 0xE810, then 0xE900. The command performs a CRC computation on the flash memory (excluding user register locations) and compares it to the original CRC value, which comes from the factory configuration process. If the current CRC value does not match the original CRC value, Register DIAG_STAT, Bit 6 (see Table 10), rises to 1, indicating a failing result.

FLASH MEMORY UPDATE

Use the following DIN sequence to set Register GLOB_CMD, Bit 3 = 1, which triggers a backup of all user configurable registers in the flash memory: 0xE808, then 0xE900. Register DIAG_STAT, Bit 2 (see Table 10) identifies success (0) or failure (1) in completing this process.

SENSOR SELF TEST

Use the following DIN sequence to set Register GLOB_CMD, Bit 2 = 1, which triggers the self test routine for the inertial sensors: 0xE804 and 0xE900. The self test routine uses the following steps to validate the integrity of each inertial sensor:

1. Measure the output on each sensor.
2. Activate an internal stimulus on the mechanical elements of each sensor to move them in a predictable manner and create an observable response in the sensors.
3. Measure the output response on each sensor.
4. Deactivate the internal stimulus on each sensor.
5. Calculate the difference between the sensor measurements from Step 1 (stimulus is off) and from Step 3 (stimulus is on).

CALIBRATION

6. Compare the difference with internal pass and fail criteria.
7. Report the pass and fail result to Register DIAG_STAT, Bit 5 (see Table 10).

Motion, during the execution of this test, can indicate a false failure.

FACTORY CALIBRATION RESTORE

Use the following DIN sequence to set Register GLOB_CMD, Bit 1 = 1 to restore the factory default settings for the MSC_ CTRL, DEC_RATE, and FILT_CTRL registers and to clear all user configurable bias correction settings: 0xE802, then 0xE900. Executing this command results in writing 0x0000 to the following registers: XG_BIAS_LOW, XG_BIAS_HIGH, YG_BIAS_LOW, YG_BIAS_HIGH, ZG_BIAS_LOW, ZG_BIAS_ HIGH, XA_BIAS_LOW, XA_BIAS_HIGH, YA_BIAS_LOW, YA_BIAS_HIGH, ZA_BIAS_LOW, and ZA_BIAS_HIGH.

BIAS CORRECTION UPDATE

Use the following DIN pin sequence to set Register GLOB_CMD, Bit 0 = 1 to trigger a bias correction, using the correction factors from the CBE (see Table 111): 0xE801, then 0xE900.

FIRMWARE REVISION (FIRM_REV)

Table 114. FIRM_REV Register Definition

Addresses	Default	Access	Flash Backup
0x6C, 0x6D	Not applicable	R	No

Table 115. FIRM_REV Bit Definitions

Bits	Description
[15:0]	Firmware revision, binary coded decimal (BCD) format

The FIRM_REV register (see Table 114 and Table 115) provides the firmware revision for the internal firmware. This register uses a BCD format, where each nibble represents a digit. For example, if FIRM_REV = 0x0104, the firmware revision is 1.04.

FIRMWARE REVISION DAY AND MONTH (FIRM_DM)

Table 116. FIRM_DM Register Definition

Addresses	Default	Access	Flash Backup
0x6E, 0x6F	Not applicable	R	No

Table 117. FIRM_DM Bit Definitions

Bits	Description
[15:8]	Factory configuration month, BCD format
[7:0]	Factory configuration day, BCD format

The FIRM_DM register (see Table 116 and Table 117) contains the month and day of the factory configuration date. Register FIRM_DM, Bits[15:8], contains digits that represent the month of the factory configuration. For example, November is the 11th month in a year and is represented by Register FIRM_DM, Bits[15:8] = 0x11. Register FIRM_DM, Bits[7:0], contain the day of factory configuration. For example, the 27th day of the month is represented by Register FIRM_DM, Bits[7:0] = 0x27.

FIRMWARE REVISION YEAR (FIRM_Y)

Table 118. FIRM_Y Register Definition

Addresses	Default	Access	Flash Backup
0x70, 0x71	Not applicable	R	No

Table 119. FIRM_Y Bit Definitions

Bits	Description
[15:0]	Factory configuration year, BCD format

The FIRM_Y register (see Table 118 and Table 119) contains the year of the factory configuration date. For example, the year, 2017, is represented by FIRM_Y = 0x2017.

PRODUCT IDENTIFICATION (PROD_ID)

Table 120. PROD_ID Register Definition

Addresses	Default	Access	Flash Backup
0x72, 0x73	0x405D	R	No

Table 121. PROD_ID Bit Definitions

Bits	Description
[15:0]	Product identification = 0x405D

The PROD_ID register (see Table 120 and Table 121) contains the numerical portion of the device number (16,477). See Figure 32 for an example of how to use a looping read of this register to validate the integrity of the communication.

SERIAL NUMBER (SERIAL_NUM)

Table 122. SERIAL_NUM Register Definition

Addresses	Default	Access	Flash Backup
0x74, 0x75	Not applicable	R	No

Table 123. SERIAL_NUM Bit Definitions

Bits	Description
[15:0]	Lot specific serial number

SCRATCH REGISTERS (USER_SCR_1 TO USER_SCR_3)

Table 124. USER_SCR_1 Register Definition

Addresses	Default	Access	Flash Backup
0x76, 0x77	Not applicable	R/W	Yes

Table 125. USER_SCR_1 Bit Definitions

Bits	Description
[15:0]	User defined

Table 126. USER_SCR_2 Register Definition

Addresses	Default	Access	Flash Backup
0x78, 0x79	Not applicable	R/W	Yes

CALIBRATION

Table 127. USER_SCR_2 Bit Definitions

Bits	Description
[15:0]	User defined

Table 128. USER_SCR_3 Register Definition

Addresses	Default	Access	Flash Backup
0x7A, 0x7B	Not applicable	R/W	Yes

Table 129. USER_SCR_3 Bit Definitions

Bits	Description
[15:0]	User defined

The USER_SCR_1 (see Table 124 and Table 125), USER_SCR_2 (see Table 126 and Table 127), and USER_SCR_3 (see Table 128 and Table 129) registers provide three locations for the user to store information. For nonvolatile storage, use the manual flash memory update command (Register GLOB_CMD, Bit 3, see Table 113), after writing information to these registers.

FLASH MEMORY ENDURANCE COUNTER (FLSHCNT_LOW AND FLSHCNT_HIGH)

Table 130. FLSHCNT_LOW Register Definition

Addresses	Default	Access	Flash Backup
0x7C, 0x7D	Not applicable	R	No

Table 131. FLSHCNT_LOW Bit Definitions

Bits	Description
[15:0]	Flash memory write counter, low word

Table 132. FLSHCNT_HIGH Register Definition

Addresses	Default	Access	Flash Backup
0x7E, 0x7F	Not applicable	R	No

Table 133. FLSHCNT_HIGH Bit Definitions

Bits	Description
[15:0]	Flash memory write counter, high word

The FLSHCNT_LOW (see Table 130 and Table 131) and FLSHCNT_HIGH (see Table 132 and Table 133) registers combine to provide a 32-bit, binary counter that tracks the number of flash memory write cycles. In addition to the number of write cycles, the flash memory has a finite service lifetime, which depends on the junction temperature. Figure 49 provides guidance for estimating the retention life for the flash memory at specific junction temperatures. The junction temperature is approximately 7°C above the case temperature.

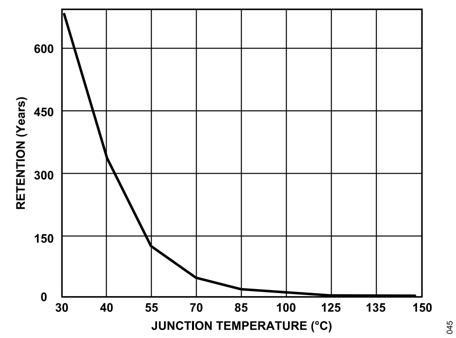


Figure 49. Flash Memory Retention

APPLICATIONS INFORMATION

ASSEMBLY AND HANDLING TIPS

Package Attributes

The ADIS16477 is a multichip module package that has a 44-ball BGA interface. This package has three basic attributes that influence its handling and assembly to the PCB of the system: the lid, the substrate, and the BGA pattern. The material of the lid is a liquid crystal polymer (LCP), and its nominal thickness is 0.5 mm. The substrate is a laminate composition that has a nominal thickness of 1.57 mm. The solder ball material is SAC305, and each ball has a nominal diameter of 0.75 mm (±0.15 mm). The BGA pattern follows an 8 × 10 array, with 36 unpopulated positions, which simplifies the escape pattern for the power, ground, and signal traces on the system PCB.

Assembly Tips

When developing a process to attach the ADIS16477 to a PCB, consider the following guidelines and insights:

- The ADIS16477 is capable of supporting solder reflow attachment processes, which are in accordance with J-STD-020E.
- Limit device exposure to one pass through the solder reflow process (no rework).
- The hole in the top of the lid (see Figure 50) provides venting and pressure relief during the assembly process of the ADIS16477. Keep this hole clear of obstruction while attaching the ADIS16477 to a PCB.

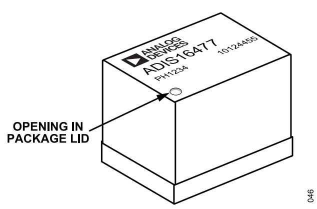


Figure 50. Pressure Relief Hole

- Use no clean flux to avoid exposing the device to water or cleaning solvents, which can penetrate the inside of the ADIS16477 through the hole in the lid and be difficult to remove. When the assembly process requires the use of liquids that can reach the hole in the lid, use a temporary seal to prevent entrapment of those liquids inside the cavity. The user must also avoid having liquid near the base of the white cover because the cover is not hermetically attached to the base of the IMU. However, the use of any liquids for post solder cleaning is not endorsed by Analog Devices, Inc.
- Manage moisture exposure prior to the solder reflow processing, in accordance with J-STD-033, Moisture Sensitivity Level 5.
- Avoid exposing the ADIS16477 to mechanical shock survivability that exceeds the maximum rating of 2000 *g* (see Table 3). In standard PCB processing, high speed handling equipment and panel separation processes often present the most risk of introducing harmful levels of mechanical shock survivability.

PCB Layout Suggestions

Figure 51 shows an example of the pad design and layout for the ADIS16477 on a PCB. This example uses a solder mask opening, with a diameter of 0.73 mm, around a metal pad that has a diameter of 0.56 mm. When using a material for the system PCB, which has similar thermal expansion properties as the substrate material of the ADIS16477, the system PCB can also use the solder mask to define the pads that support attachment to the balls of the ADIS16477. The coefficient of thermal expansion (CTE) in the substrate of the ADIS16477 is approximately 14 ppm/°C.

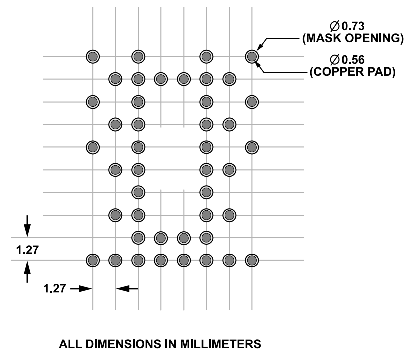


Figure 51. Recommend PCB Pattern, Solder Mask Defined Pads

Underfill

Underfill can be a useful technique in managing certain threats to the integrity of the solder joints of the ADIS16477, including peeling stress and extended exposure to vibration. When selecting underfill material and developing an application and curing process, ensure that the material fills the gap between each surface (the ADIS16477 substrate and system PCB) and adheres to both surfaces. The ADIS16477 does not require the use of underfill materials in applications that do not anticipate exposure to these types of mechanical stresses and when the CTE of the system PCB is close to the same value as the CTE of the substrate of the ADIS16477 (~14 ppm/°C).

Process Validation and Control

These guidelines provide a starting point for developing a process for attaching the ADIS16477 to a system PCB. Because each system and situation may present unique requirements for this attachment process, ensure that the process supports optimal solder joint integrity, verify that the final system meets all environmental test requirements, and establish observation and control strategies for all key process attributes (for example, peak temperatures, dwell times, and ramp rates).

POWER SUPPLY CONSIDERATIONS

The ADIS16477 contains 6 µF of decoupling capacitance across the VDD and GND pins. When the VDD voltage rises from 0 V to 3.3 V, the charging current for this capacitor bank imposes the following current profile (in amperes):

APPLICATIONS INFORMATION

$$I_{DD}(t) = C\frac{dVDD}{dt} = 6 \times 10^{-6} \times \frac{dVDD(t)}{dt}$$

where:
$I_{DD}(t)$ is the current demand on the VDD pin during the initial power supply ramp, with respect to time.
C is the internal capacitance across the VDD and GND pins (6 µF).
VDD(t) is the voltage on the VDD pin, with respect to time.

For example, if VDD follows a linear ramp from 0 V to 3.3 V, in 66 µs, the charging current is 300 mA for that timeframe. The ADIS16477 also contains embedded processing functions that present transient current demands during initialization or reset recovery operations. During these processes, the peak current demand reaches 250 mA and occurs at a time that is approximately 40 ms after VDD reaches 3.0 V (or ~40 ms after initiating a reset sequence).

SERIAL PORT OPERATION

Maximum Throughput

When operating with the maximum output data (DEC_RATE = 0x0000, as described in Table 109), the maximum SCLK rate (defined in Table 2) and minimum stall time, the SPI port can support up to 12, 16-bit register reads in between each pulse of the data ready signal. Attempting to read more than 12 registers can result in a datapath overrun error in the DIAG_STAT register (see Table 10). The serial port stall time (t_{STALL}) to meet these requirements must be no more than 10% greater than the minimum specification for t_{STALL} in Table 2.

The number of allowable registers reads between each pulse on the data ready line increases proportionally with the decimation rate (set by the DEC_RATE register, see Table 109). For example, when the decimation rate equals 3 (DEC_RATE = 0x0002), the SPI is able to support up to 36 register reads, assuming maximum SCLK rate and minimum stall times in the protocol. Decreasing the SCLK rate and increasing the stall time lowers the total number of register reads supported by the ADIS16477 before a datapath overrun error occurs.

This limitation of reading 12, 16-bit registers does not impact the ability of the user to access the full precision of the gyroscopes and accelerometers if the factory default settings of DEC_RATE = 0x0000 and FILT_CTRL = 0x0000 are used. In this case, the data width for the gyroscope and accelerometer data is 16 bits, and application processors can acquire all relevant information through the X_GYRO_OUT, Y_GYRO_ OUT, Z_GYRO_OUT, X_ACCEL_OUT, Y_ACCEL_OUT, and Z_ACCEL_OUT registers. Thirty-two bit reads of the sensor data do not provide additional precision in this case. See the Gyroscope Data Width (Digital Resolution) section and the Accelerometer Data Width (Digital Resolution) section for more information.

Serial Port SCLK Underrun/Overrun Conditions

The serial port operates in 16-bit segments, and it is critical that the number of SCLK cycles be equal to an integer multiple of 16 when the $\overline{CS}$ pin is low. Failure to meet this condition causes the serial port controller inside of the ADIS16477 to be unable to correctly receive and respond to new requests.

If too many SCLK cycles are received before the $\overline{CS}$ pin is deasserted, the user can recover serial port operation by asserting $\overline{CS}$, providing 17 rising edges on the SCLK line, deasserting $\overline{CS}$, and then attempting to correctly read the PROD_ID (or other read-only) register on the ADIS16477. The user should repeat these steps up to a maximum of 15 times until the correct data is read.

If $\overline{CS}$ is deasserted before enough SCLK cycles are received, the user must either power cycle or issue a hard reset (using the $\overline{RST}$ pin) to regain SPI port access.

DIGITAL RESOLUTION OF GYROSCOPES AND ACCELEROMETERS

Gyroscope Data Width (Digital Resolution)

The decimation filter (DEC_RATE register, see Table 109) and Bartlett window filter (FILT_CTRL register, see Table 101) have direct influence over the total number of bits in the output data registers, which contain relevant information. When using the factory default settings (DEC_RATE = 0x0000, FILT_CTRL = 0x0000) for these filters, the gyroscope data width is 16 bits, which means that application processors can acquire all relevant information through the X_GYRO_OUT, Y_GYRO_OUT, and Z_GYRO_OUT registers. However, for optimal performance in demanding applications, use 32-bit transfers to preserve the accuracy of the linear *g* compensation.

The X_GYRO_LOW, Y_GYRO_LOW, and Z_GYRO_LOW registers capture the bit growth that comes from each accumulation operation in the decimation and Bartlett window filters. When using these filters (DEC_RATE ≠ 0x0000 and/or FILT_CTRL ≠ 0x0000), the data width increases by one bit every time the number of summations (in a filter stage) increases by a factor of two. For example, when DEC_RATE = 0x0007, the decimation filter adds eight (7 + 1 = 8, see Table 109) successive samples together, which causes the data width to increase by 3 bits ($\log_2 8 = 3$). When FILT_CTRL = 0x0002, both stages in the Bartlett window filter use four ($2^2 = 4$, see Table 101) summation operations, which increases the data width by 2 bits ($\log_2 4 = 2$). When using both DEC_RATE = 0x0007 and FILT_CTRL = 0x0002, the total bit growth is 7 bits, which increases the overall data width to 23 bits.

Accelerometer Data Width (Digital Resolution)

The decimation filter (DEC_RATE register, see Table 109) and Bartlett window filter (FILT_CTRL register, see Table 101) have direct influence over the total number of bits in the output data registers, which contain relevant information. When using the factory default

APPLICATIONS INFORMATION

settings (DEC_RATE = 0x0000, FILT_CTRL = 0x0000) for these filters, the accelerometer data width is 20 bits. The X_ACCL_OUT, Y_ACCL_OUT, and Z_ACCL_OUT registers contain the most significant 16 bits of this data, while the remaining (least significant) bits are in the upper 4 bits of the X_ACCL_LOW, Y_ACCL_LOW, and Z_ACCL_LOW registers. Since the total noise (0.6 m*g* rms, see Table 1) in the accelerometer data (DEC_RATE = 0x0000, FILT_CTRL = 0x0000) is greater than the 16-bit quantization noise (0.25 m*g* ÷ $12^{0.5}$ = 0.072 m*g*), application processors can acquire all relevant information through the X_ACCL_OUT, Y_ACCL_OUT, and Z_ACCL_OUT registers. This enables applications to preserve optimal performance, while using the burst read (see Figure 31), which only provides 16-bit data for the accelerometers.

The X_ACCL_LOW, Y_ACCL_LOW, and Z_ACCL_LOW registers also capture the bit growth that comes from each accumulation operation in the decimation and Bartlett window filters. When using these filters (DEC_RATE ≠ 0x0000 and/or FILT_CTRL ≠ 0x0000), the data width increases by one bit every time the number of summations (in a filter stage) increases by a factor of two. For example, when DEC_RATE = 0x0001, the decimation filter adds two (1 + 1 = 2, see Table 109) successive samples together, which causes the data width to increase by 1 bit ($\log_2 2 = 1$). When FILT_CTRL = 0x0001, both stages in the Bartlett window filter add two ($2^1 = 2$, see Table 101) successive samples together, which increases the data width by 1 bit ($\log_2 2 = 1$) as well. When using both DEC_RATE = 0x0001 and FILT_CTRL = 0x0001, the total bit growth is 3 bits, which increases the overall data width to 23 bits.

EVALUATION TOOLS

Breakout Boards

The ADIS16477 has three difference breakout boards, which provide a simple way to connect an ADIS16477 model and an existing embedded processor platform. Table 134 provides a list of the model numbers for each breakout board, along with the ADIS16477 model that is on each breakout board.

Table 134. Breakout Board Models

Breakout Board Model	ADIS16477 Model
ADIS16477-1/PCBZ	ADIS16477-1BMLZ
ADIS16477-2/PCBZ	ADIS16477-2BMLZ
ADIS16477-3/PCBZ	ADIS16477-3BMLZ

The electrical interface (J1) on each breakout board comes from a dual row, 2 mm pitch, 16-pin interface, which supports standard ribbon cabling (1 mm pitch). Table 135 provides the J1 pin assignments, which support direct connection with an embedded processor board, using standard ribbon cables. Although each case may present its own set of sensitivities (such as electromagnetic interference (EMI)), these boards can typically support reliable communication over ribbon cables up to 20 cm in length.

Table 135. J1 Pin Assignments, Breakout Board

J1 Pin Number	Signal	Function
1	$\overline{\text{RST}}$	Reset
2	SCLK	SPI
3	$\overline{\text{CS}}$	SPI
4	DOUT	SPI
5	NC	No connect
6	DIN	SPI
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	VDD	Power, 3.3 V
11	VDD	Power, 3.3 V
12	VDD	Power, 3.3 V
13	DR	Data ready
14	SYNC	Input clock
15	NC	No connect
16	NC	No connect

Figure 52 provides a top level view of the breakout board, including dimensional locations for all the key mechanical features, such as the mounting holes and the 16-pin header. Breakout Boards provides an electrical schematic for this breakout board. For additional information, refer to the ADIS1647x/PCB Wiki Guide.

APPLICATIONS INFORMATION

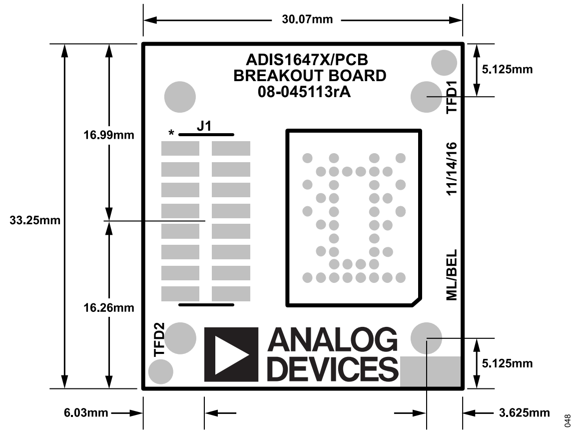


Figure 52. Top Level View of the Breakout Board

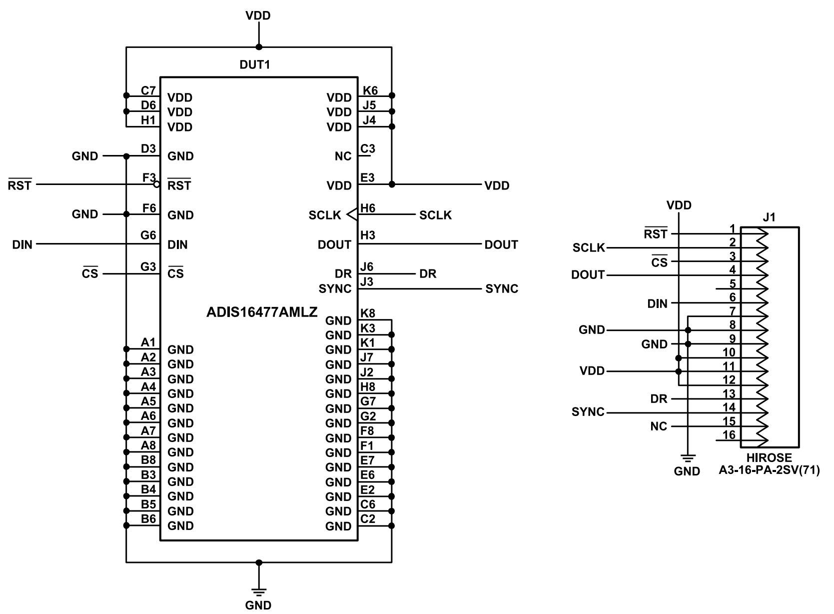


Figure 53. Breakout Board Schematic

PC-Based Evaluation, EVAL-ADIS-FX3

In addition to supporting quick prototype connections between the ADIS16477 and an embedded processing system, J1 on the breakout board also connects directly to P3 on the EVAL-ADIS-FX3 evaluation system.

EVAL-ADIS-FX3 is a completely open-source evaluation platform for Windows-based systems. The FX3 application programming interface (API) manages all the complex USB transactions and implements all the necessary tools to begin capturing high speed, high performance data in custom applications. This .NET-compatible API, written in VB.NET and C#, includes data streaming features tailored to reliably capturing inertial sensor data at the maximum data rate. The API is also fully documented, open-source, and is licensed under the MIT license. The API also includes a wrapper library, allowing users to use the same API in any development environment with support for .NET (for example, MATLAB®, LabVIEW®, and Python).

TRAY DRAWING

The ADIS16477 parts are shipped in the tray shown in Figure 54.

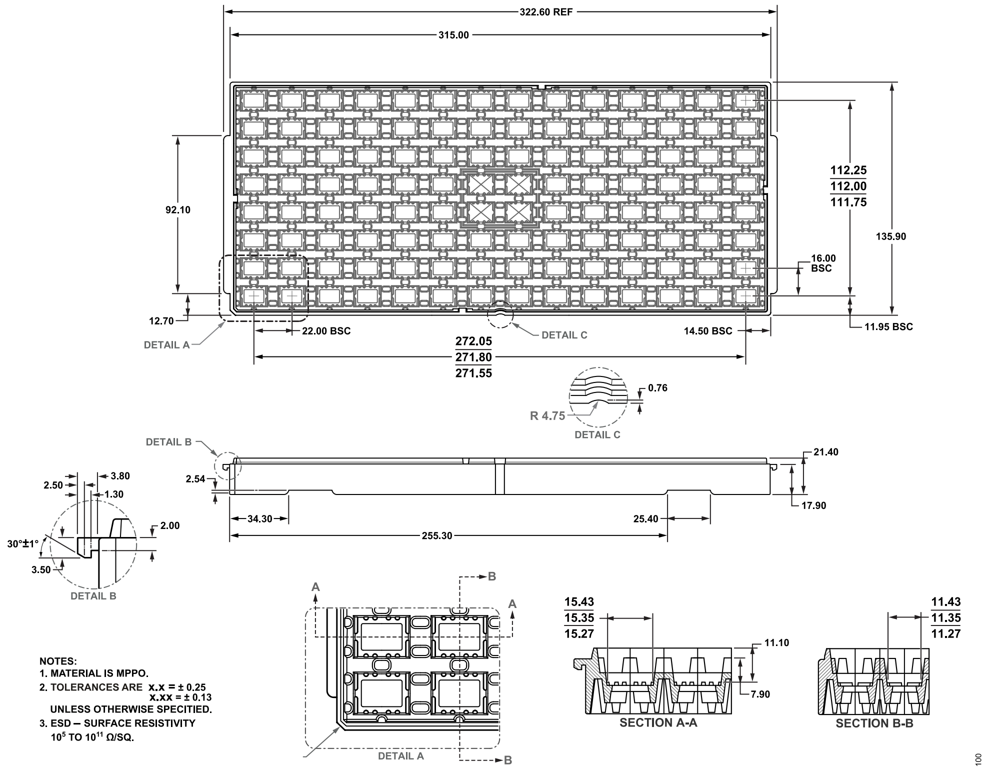


Figure 54. Drawing of Shipping Tray

OUTLINE DIMENSIONS

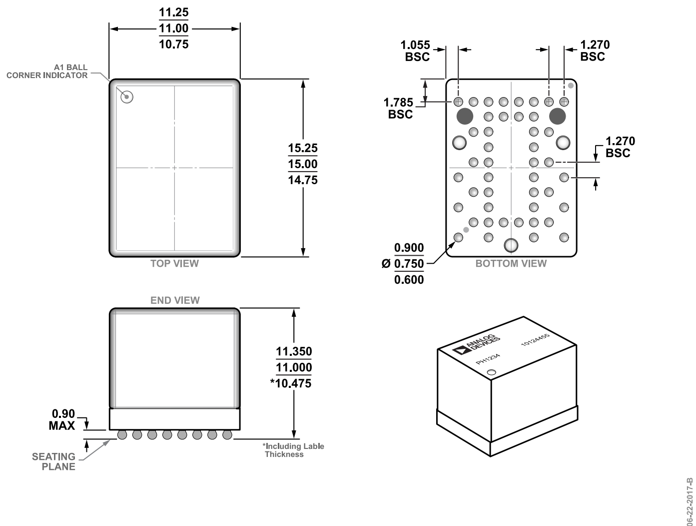


Figure 55. 44-Ball Ball Grid Array Module (ML-44-1) Dimensions shown in millimeters

Updated: June 18, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16477-1BMLZ	-40°C to +105°C	44-Ball BGA Module	ML-44-1
ADIS16477-2BMLZ	-40°C to +105°C	44-Ball BGA Module	ML-44-1
ADIS16477-3BMLZ	-40°C to +105°C	44-Ball BGA Module	ML-44-1

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADIS16477-1/PCBZ	ADIS16477-1 Breakout Board
ADIS16477-2/PCBZ	ADIS16477-2 Breakout Board
ADIS16477-3/PCBZ	ADIS16477-3 Breakout Board
EVAL-ADIS-FX3Z	Evaluation Board

[1] Z = RoHS Compliant Part.