

74VHC4051AFT, 74VHC4052AFT, 74VHC4053AFT

1. Functional Description

74VHC4051AFT: 8-Channel Analog Multiplexer/Demultiplexer
 74VHC4052AFT: Dual 4-Channel Analog Multiplexer/Demultiplexer
 74VHC4053AFT: Triple 2-Channel Analog Multiplexer/Demultiplexer

2. General

The 74VHC4051AFT, 74VHC4052AFT and 74VHC4053AFT are high-speed, low-voltage drive analog multiplexer/demultiplexers using silicon gate CMOS technology. In 3 V and 5 V systems these can achieve high-speed operation with the low power dissipation that is a feature of CMOS.

The 74VHC4051AFT, 74VHC4052AFT and 74VHC4053AFT offer analog/digital signal selection as well as mixed signals. The 74VHC4051AFT has an 8-channel configuration, the 74VHC4052AFT has an 4-channel $\times 2$ configuration, and the 74VHC4053AFT has a 2-channel $\times 3$ configuration.

The switches for each channel are turned ON by the control pin digital signals.

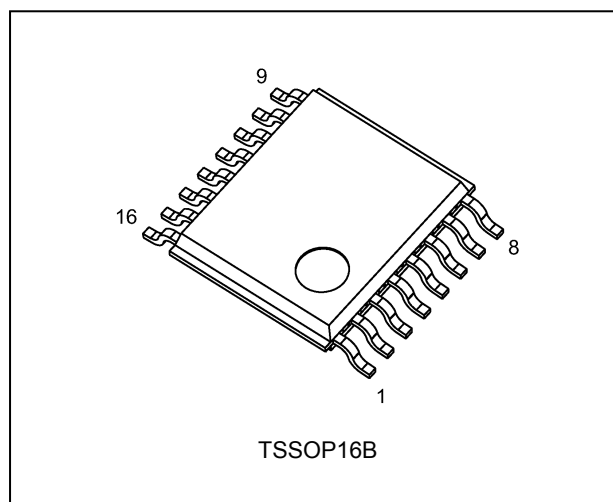
All control inputs are equipped with a newly developed input protection circuit that avoids the need for a diode on the plus side (forward side from the input to the V_{CC}). As a result, for example, 5.5 V signals can be permitted on the inputs even when the power supply voltage to the circuits is off. As a result of this input power protection, the 74VHC4051AFT, 74VHC4052AFT and 74VHC4053AFT can be used in a variety of applications, including in the system which has two power supplies, and in battery backup circuits.

3. Features

- (1) AEC-Q100 (Rev. H) (Note 1)
- (2) Wide operating temperature range: $T_{opr} = -40$ to 125 °C
- (3) Low ON-resistance: $R_{ON} = 45$ Ω (typ.) ($V_{CC} = 3.0$ V)
 $R_{ON} = 24$ Ω (typ.) ($V_{CC} = 4.5$ V)
- (4) Low power dissipation: $I_{CC} = 2.0$ μ A (max) ($T_a = 25$ °C)
- (5) High noise immunity: $V_{IL} = 0.8$ V (max) $V_{CC} = 3.0$ V
 $V_{IH} = 2.0$ V (min) $V_{CC} = 3.0$ V
- (6) Power down protection is provided on all control inputs.

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

4. Packaging

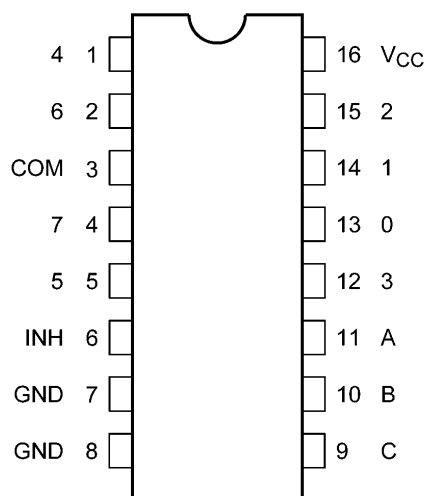


Start of commercial production

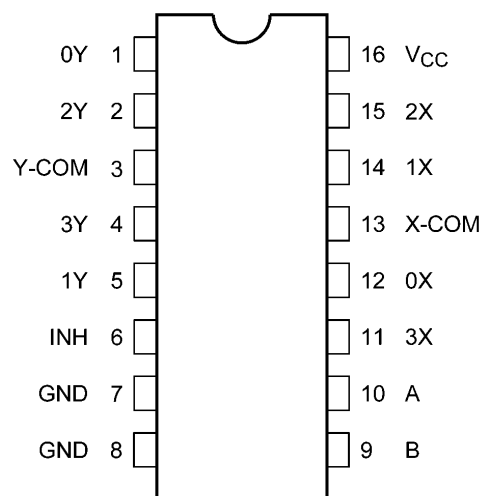
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5. Pin Assignment

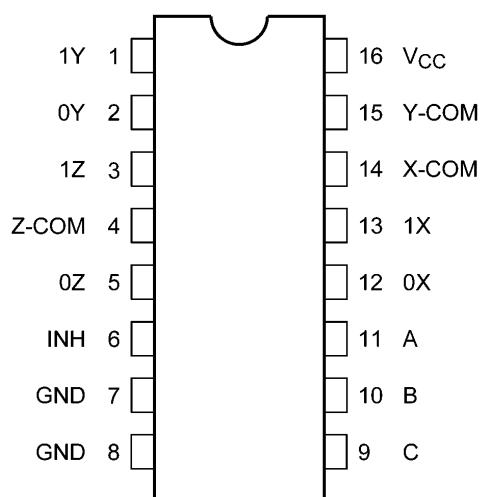
74VHC4051AFT



74VHC4052AFT

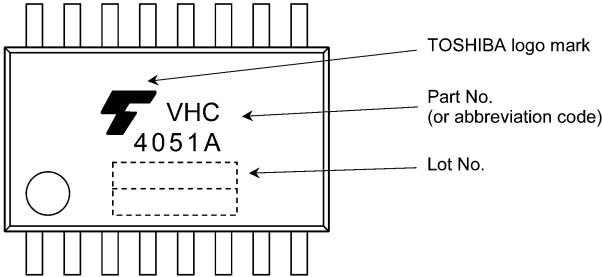


74VHC4053AFT

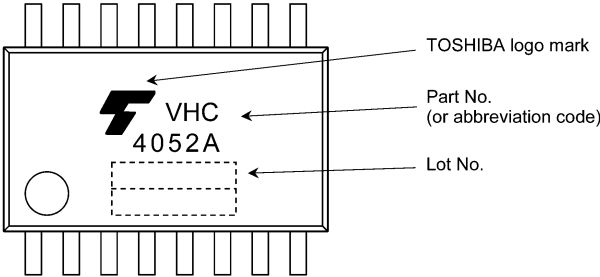


6. Marking

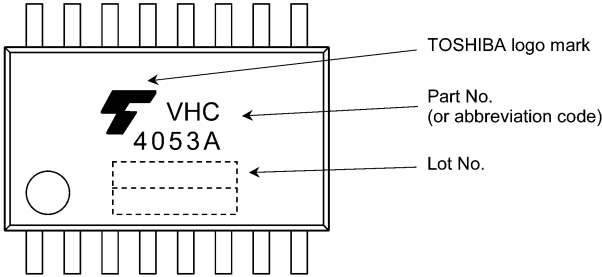
74VHC4051AFT



74VHC4052AFT

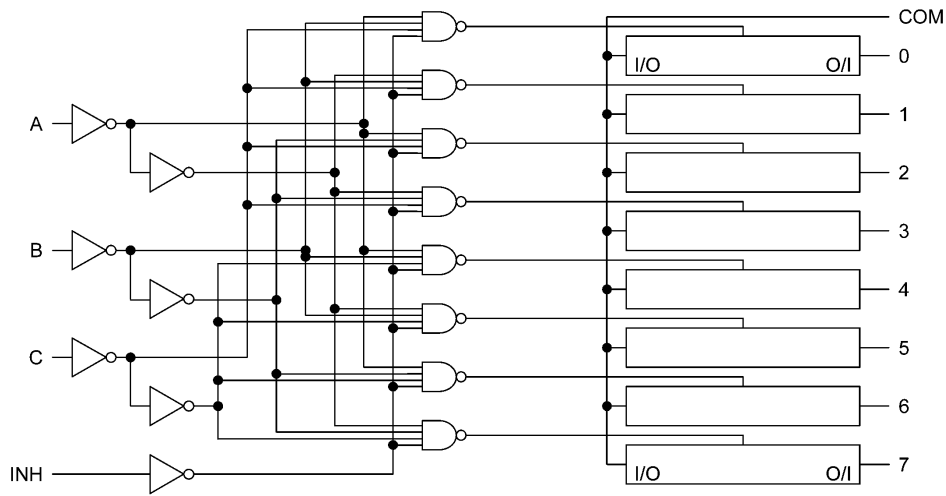


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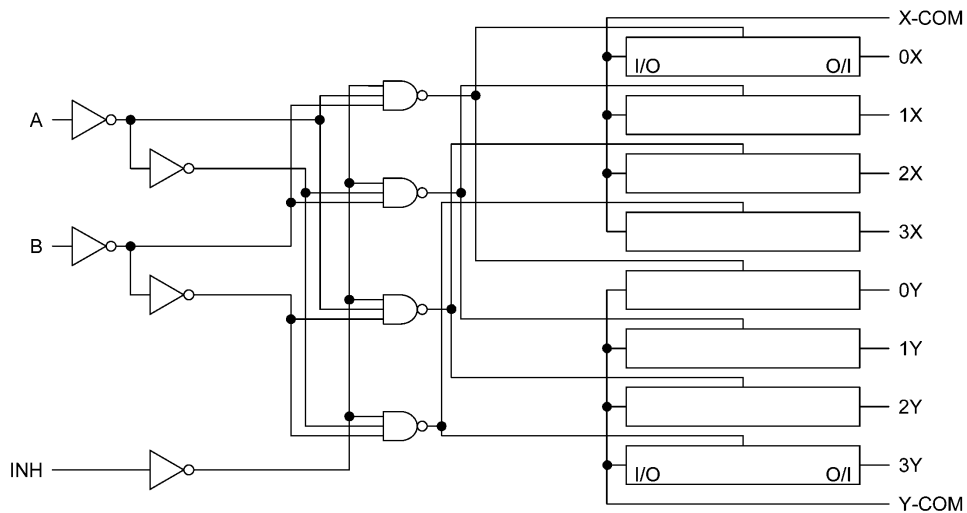


7. System Diagram

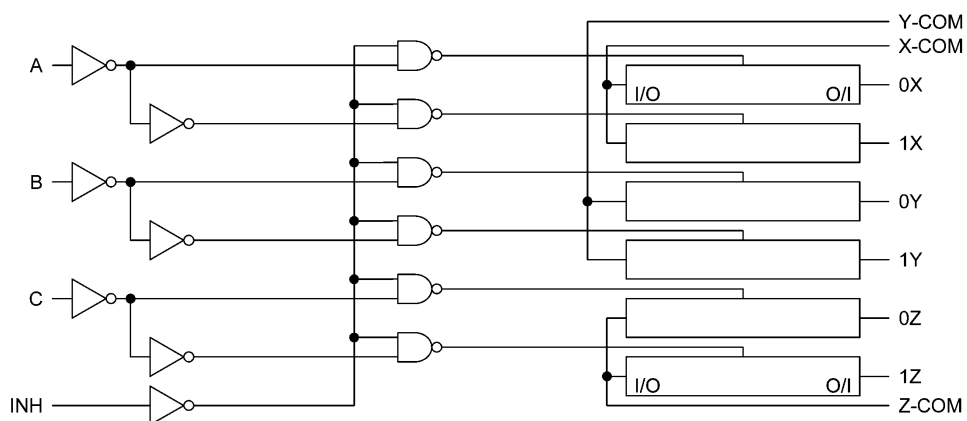
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74VHC4052AFT



74VHC4053AFT



8. Truth Table

| Input Inhibit | Input C* | Input B | Input A | ON Channel 74VHC4051AFT | ON Channel 74VHC4052AFT | ON Channel 74VHC4053AFT |
|---------------|----------|---------|---------|----------------------------|----------------------------|----------------------------|
| L | L | L | L | 0 | 0X, 0Y | 0X, 0Y, 0Z |
| L | L | L | H | 1 | 1X, 1Y | 1X, 0Y, 0Z |
| L | L | H | L | 2 | 2X, 2Y | 0X, 1Y, 0Z |
| L | L | H | H | 3 | 3X, 3Y | 1X, 1Y, 0Z |
| L | H | L | L | 4 | — | 0X, 0Y, 1Z |
| L | H | L | H | 5 | — | 1X, 0Y, 1Z |
| L | H | H | L | 6 | — | 0X, 1Y, 1Z |
| L | H | H | H | 7 | — | 1X, 1Y, 1Z |
| H | X | X | X | None | None | None |

X: Don't care

*: Except 74VHC4052AFT

9. Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Note | Rating | Unit |
|--------------------------|------------|----------|------------------------|------|
| Supply voltage | V_{CC} | | -0.5 to 7.0 | V |
| Input voltage | V_{IN} | | -0.5 to 7.0 | V |
| Switch I/O voltage | $V_{I/O}$ | | -0.5 to $V_{CC} + 0.5$ | V |
| Input diode current | I_{IK} | | -20 | mA |
| I/O diode current | $I_{I/OK}$ | | ± 25 | mA |
| Switch through current | I_T | | ± 25 | mA |
| V_{CC} /ground current | I_{CC} | | ± 50 | mA |
| Power dissipation | P_D | (Note 1) | 180 | mW |
| Storage temperature | T_{stg} | | -65 to 150 | °C |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 180 mW in the range of $T_a = -40$ to 85 °C. From $T_a = 85$ to 125 °C a derating factor of -3.25 mW/°C shall be applied until 50 mW.

10. Operating Ranges (Note)

| Characteristics | Symbol | Test Condition | Rating | Unit |
|---------------------------|-----------|--------------------------|---------------|------|
| Supply voltage | V_{CC} | | 2.0 to 5.5 | V |
| Input voltage | V_{IN} | | 0 to 5.5 | V |
| Switch I/O voltage | V_S | | 0 to V_{CC} | V |
| Operating temperature | T_{opr} | | -40 to 125 | °C |
| Input rise and fall times | dt/dv | $V_{CC} = 2.5 \pm 0.2$ V | 0 to 200 | ns/V |
| | | $V_{CC} = 3.3 \pm 0.3$ V | 0 to 100 | |
| | | $V_{CC} = 5 \pm 0.5$ V | 0 to 20 | |

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either V_{CC} or GND.

11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

| Characteristics | Symbol | Test Condition | V_{CC} (V) | Min | Typ. | Max | Unit |
|---|-----------------|--|--------------|------|------|-----------|---------------|
| High-level input voltage | V_{IH} | — | 2.0 | 1.5 | — | — | V |
| | | | 3.0 | 2.0 | — | — | |
| | | | 4.5 | 3.15 | — | — | |
| | | | 5.5 | 3.85 | — | — | |
| Low-level input voltage | V_{IL} | — | 2.0 | — | — | 0.5 | V |
| | | | 3.0 | — | — | 0.8 | |
| | | | 4.5 | — | — | 1.35 | |
| | | | 5.5 | — | — | 1.65 | |
| ON-resistance | R_{ON} | $V_{IN} = V_{IH}$ or V_{IL} $V_{I/O} = V_{CC}$ to GND $I_{I/O} = 2\text{ mA}$ | 2.3 | — | 200 | — | Ω |
| | | | 3.0 | — | 45 | 86 | |
| | | | 4.5 | — | 24 | 37 | |
| | | $V_{IN} = V_{IH}$ or V_{IL} $V_{I/O} = V_{CC}$ or GND $I_{I/O} = 2\text{ mA}$ | 2.3 | — | 28 | 73 | |
| | | | 3.0 | — | 22 | 38 | |
| | | | 4.5 | — | 17 | 27 | |
| Difference of ON-resistance between switches | ΔR_{ON} | $V_{IN} = V_{IH}$ or V_{IL} $V_{I/O} = V_{CC}$ to GND $I_{I/O} = 2\text{ mA}$ | 2.3 | — | 10 | 25 | Ω |
| | | | 3.0 | — | 5 | 15 | |
| | | | 4.5 | — | 5 | 13 | |
| Input/Output leakage current (Switch OFF) | I_{OFF} | $V_{OS} = V_{CC}$ or GND $V_{IS} = \text{GND}$ to V_{CC} $V_{IN} = V_{IH}$ or V_{IL} | 5.5 | — | — | ± 0.1 | μA |
| Input/Output leakage current (Switch ON, Output OPEN) | $I_{I/O}$ | $V_{OS} = V_{CC}$ or GND $V_{IN} = V_{IH}$ or V_{IL} | 5.5 | — | — | ± 0.1 | μA |
| Control input leakage current | I_{IN} | $V_{IN} = V_{CC}$ or GND | 5.5 | — | — | ± 0.1 | μA |
| Quiescent supply current | I_{CC} | $V_{IN} = V_{CC}$ or GND | 5.5 | — | — | 2.0 | μA |

11.2. DC Characteristics (Unless otherwise specified, $T_a = -40$ to 85 °C)

| Characteristics | Symbol | Test Condition | V_{CC} (V) | Min | Max | Unit |
|---|-----------------|---|--------------|------|-----------|----------|
| High-level input voltage | V_{IH} | — | 2.0 | 1.5 | — | V |
| | | | 3.0 | 2.0 | — | |
| | | | 4.5 | 3.15 | — | |
| | | | 5.5 | 3.85 | — | |
| Low-level input voltage | V_{IL} | — | 2.0 | — | 0.50 | V |
| | | | 3.0 | — | 0.8 | |
| | | | 4.5 | — | 1.35 | |
| | | | 5.5 | — | 1.65 | |
| ON-resistance | R_{ON} | $V_{IN} = V_{IH}$ or V_{IL} $V_{I/O} = V_{CC}$ to GND $I_{I/O} = 2$ mA | 2.3 | — | — | Ω |
| | | | 3.0 | — | 108 | |
| | | | 4.5 | — | 46 | |
| | | $V_{IN} = V_{IH}$ or V_{IL} $V_{I/O} = V_{CC}$ or GND $I_{I/O} = 2$ mA | 2.3 | — | 84 | |
| | | | 3.0 | — | 44 | |
| | | | 4.5 | — | 31 | |
| Difference of ON-resistance between switches | ΔR_{ON} | $V_{IN} = V_{IH}$ or V_{IL} $V_{I/O} = V_{CC}$ to GND $I_{I/O} = 2$ mA | 2.3 | — | 35 | Ω |
| | | | 3.0 | — | 20 | |
| | | | 4.5 | — | 18 | |
| Input/Output leakage current (Switch OFF) | I_{OFF} | $V_{OS} = V_{CC}$ or GND $V_{IS} =$ GND to V_{CC} $V_{IN} = V_{IH}$ or V_{IL} | 5.5 | — | ± 1.0 | μA |
| Input/Output leakage current (Switch ON, Output OPEN) | $I_{I/O}$ | $V_{OS} = V_{CC}$ or GND $V_{IN} = V_{IH}$ or V_{IL} | 5.5 | — | ± 1.0 | μA |
| Control input leakage current | I_{IN} | $V_{IN} = V_{CC}$ or GND | 5.5 | — | ± 1.0 | μA |
| Quiescent supply current | I_{CC} | $V_{IN} = V_{CC}$ or GND | 5.5 | — | 20.0 | μA |

11.3. DC Characteristics (Unless otherwise specified, $T_a = -40$ to 125 °C)

| Characteristics | Symbol | Test Condition | V_{CC} (V) | Min | Max | Unit |
|---|-----------------|---|--------------|------|-----------|----------|
| High-level input voltage | V_{IH} | — | 2.0 | 1.5 | — | V |
| | | | 3.0 | 2.0 | — | |
| | | | 4.5 | 3.15 | — | |
| | | | 5.5 | 3.85 | — | |
| Low-level input voltage | V_{IL} | — | 2.0 | — | 0.5 | V |
| | | | 3.0 | — | 0.8 | |
| | | | 4.5 | — | 1.35 | |
| | | | 5.5 | — | 1.65 | |
| ON-resistance | R_{ON} | $V_{IN} = V_{IH}$ or V_{IL} $V_{I/O} = V_{CC}$ to GND $I_{I/O} = 2$ mA | 2.3 | — | — | Ω |
| | | | 3.0 | — | 125 | |
| | | | 4.5 | — | 54 | |
| | | $V_{IN} = V_{IH}$ or V_{IL} $V_{I/O} = V_{CC}$ or GND $I_{I/O} = 2$ mA | 2.3 | — | 105 | |
| | | | 3.0 | — | 55 | |
| | | | 4.5 | — | 39 | |
| Difference of ON-resistance between switches | ΔR_{ON} | $V_{IN} = V_{IH}$ or V_{IL} $V_{I/O} = V_{CC}$ to GND $I_{I/O} = 2$ mA | 2.3 | — | 45 | Ω |
| | | | 3.0 | — | 25 | |
| | | | 4.5 | — | 23 | |
| Input/Output leakage current (Switch OFF) | I_{OFF} | $V_{OS} = V_{CC}$ or GND $V_{IS} = GND$ to V_{CC} $V_{IN} = V_{IH}$ or V_{IL} | 5.5 | — | ± 4.0 | μA |
| Input/Output leakage current (Switch ON, Output OPEN) | $I_{I/O}$ | $V_{OS} = V_{CC}$ or GND $V_{IN} = V_{IH}$ or V_{IL} | 5.5 | — | ± 4.0 | μA |
| Control input leakage current | I_{IN} | $V_{IN} = V_{CC}$ or GND | 5.5 | — | ± 2.0 | μA |
| Quiescent supply current | I_{CC} | $V_{IN} = V_{CC}$ or GND | 5.5 | — | 40.0 | μA |

11.4. AC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

| Characteristics | Part Number | Symbol | Test Condition | V_{CC} (V) | C_L (pF) | Min | Typ. | Max | Unit | |
|--|--------------|--------------------|--------------------------------------|---------------|------------|-----|------|------|------|---|
| Phase difference between input to output | | $\phi_{I/O}$ | | 2.5 ± 0.2 | 15 | — | 1.2 | 10 | ns | |
| | | | | | 50 | — | 2.6 | 12 | | |
| | | | | 3.3 ± 0.3 | 15 | — | 0.8 | 6 | | |
| | | | | | 50 | — | 1.5 | 9 | | |
| | | | | 5.0 ± 0.5 | 15 | — | 0.3 | 4 | | |
| | | | | | 50 | — | 0.6 | 6 | | |
| Output enable time | | t_{PZL}, t_{PZH} | $R_L = 1\text{ k}\Omega$ Figure 1 | 2.5 ± 0.2 | 15 | — | 3.3 | 15 | ns | |
| | | | | | 50 | — | 4.2 | 25 | | |
| | | | | 3.3 ± 0.3 | 15 | — | 2.3 | 11 | | |
| | | | | | 50 | — | 3.0 | 18 | | |
| | | | | 5.0 ± 0.5 | 15 | — | 1.6 | 7 | | |
| | | | | | 50 | — | 2.1 | 12 | | |
| Output disable time | | t_{PLZ}, t_{PHZ} | $R_L = 1\text{ k}\Omega$ Figure 1 | 2.5 ± 0.2 | 15 | — | 6 | 15 | ns | |
| | | | | | 50 | — | 9.6 | 25 | | |
| | | | | 3.3 ± 0.3 | 15 | — | 4.5 | 11 | | |
| | | | | | 50 | — | 7.2 | 18 | | |
| | | | | 5.0 ± 0.5 | 15 | — | 3.2 | 7 | | |
| | | | | | 50 | — | 5.1 | 12 | | |
| Control input capacitance | | C_{IN} | All types | — | — | — | 2 | — | pF | |
| Common terminal capacitance | 74VHC4051AFT | C_{IS} | Figure 2 | — | — | — | 23.4 | — | pF | |
| | 74VHC4052AFT | | | | | | — | 13.1 | | — |
| | 74VHC4053AFT | | | | | | — | 8.2 | | — |
| Switch terminal capacitance | 74VHC4051AFT | C_{OS} | Figure 2 | — | — | — | 5.7 | — | pF | |
| | 74VHC4052AFT | | | | | | — | 5.6 | | — |
| | 74VHC4053AFT | | | | | | — | 5.6 | | — |
| Feedthrough capacitance | 74VHC4051AFT | C_{IOS} | Figure 2 | — | — | — | 0.5 | — | pF | |
| | 74VHC4052AFT | | | | | | — | 0.5 | | — |
| | 74VHC4053AFT | | | | | | — | 0.5 | | — |
| Power dissipation capacitance | 74VHC4051AFT | C_{PD} | Figure 2 (Note 1) | — | — | — | 15 | — | pF | |
| | 74VHC4052AFT | | | | | | — | 24 | | — |
| | 74VHC4053AFT | | | | | | — | 12 | | — |

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$$

11.5. AC Characteristics

(Unless otherwise specified, $T_a = -40$ to 85 °C, Input: $t_r = t_f = 3$ ns)

| Characteristics | Symbol | Test Condition | V_{CC} (V) | C_L (pF) | Min | Max | Unit | | | | |
|--|--------------------|----------------------------------|---------------------------|--------------------|----------------------------------|---------------|------|----|----|----|----|
| Phase difference between input to output | $\phi_{I/O}$ | | 2.5 ± 0.2 | 15 | — | 16 | ns | | | | |
| | | | | 50 | — | 18 | | | | | |
| | | | 3.3 ± 0.3 | 15 | — | 10 | | | | | |
| | | | | 50 | — | 12 | | | | | |
| | | | 5.0 ± 0.5 | 15 | — | 7 | | | | | |
| | | | | 50 | — | 8 | | | | | |
| | | | Output enable time | t_{PZL}, t_{PZH} | $R_L = 1$ k Ω Figure 1 | 2.5 ± 0.2 | | 15 | — | 20 | ns |
| | | | | | | | | 50 | — | 32 | |
| 3.3 ± 0.3 | 15 | — | | | | 15 | | | | | |
| | 50 | — | | | | 22 | | | | | |
| 5.0 ± 0.5 | 15 | — | | | | 10 | | | | | |
| | 50 | — | | | | 16 | | | | | |
| Output disable time | t_{PLZ}, t_{PHZ} | $R_L = 1$ k Ω Figure 1 | | | | 2.5 ± 0.2 | 15 | — | 23 | ns | |
| | | | | | | | 50 | — | 32 | | |
| | | | 3.3 ± 0.3 | 15 | — | 15 | | | | | |
| | | | | 50 | — | 22 | | | | | |
| | | | 5.0 ± 0.5 | 15 | — | 10 | | | | | |
| | | | | 50 | — | 16 | | | | | |
| | | | Control input capacitance | C_{IN} | — | — | — | — | 10 | | pF |

11.6. AC Characteristics

(Unless otherwise specified, $T_a = -40$ to 125 °C, Input: $t_r = t_f = 3$ ns)

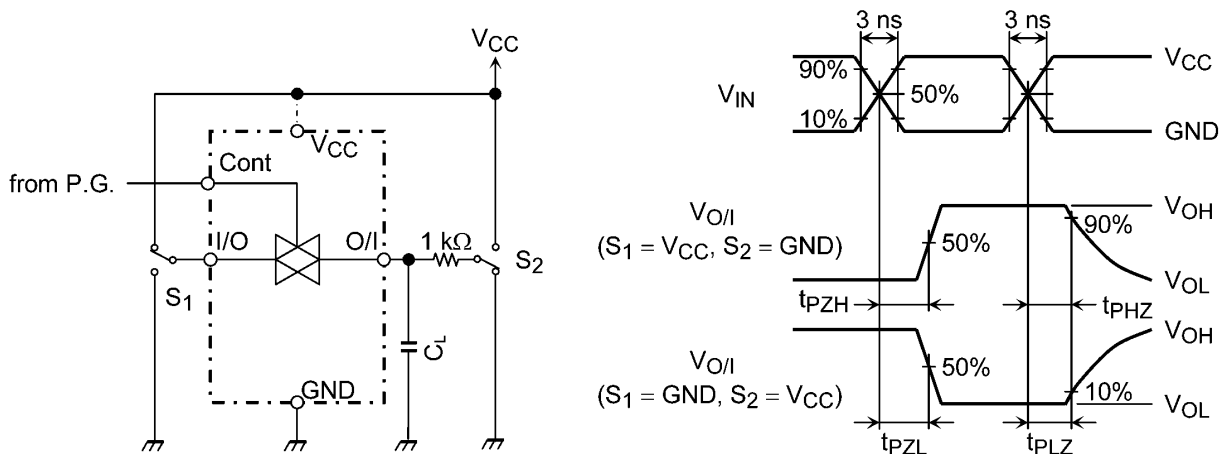
| Characteristics | Symbol | Test Condition | V_{CC} (V) | C_L (pF) | Min | Max | Unit | | | | |
|--|--------------------|----------------------------------|---------------------------|--------------------|----------------------------------|---------------|------|----|------|------|----|
| Phase difference between input to output | $\phi_{I/O}$ | | 2.5 ± 0.2 | 15 | — | 20 | ns | | | | |
| | | | | 50 | — | 22 | | | | | |
| | | | 3.3 ± 0.3 | 15 | — | 13 | | | | | |
| | | | | 50 | — | 14 | | | | | |
| | | | 5.0 ± 0.5 | 15 | — | 9 | | | | | |
| | | | | 50 | — | 9.5 | | | | | |
| | | | Output enable time | t_{PZL}, t_{PZH} | $R_L = 1$ k Ω Figure 1 | 2.5 ± 0.2 | | 15 | — | 23.5 | ns |
| | | | | | | | | 50 | — | 37 | |
| 3.3 ± 0.3 | 15 | — | | | | 18 | | | | | |
| | 50 | — | | | | 25 | | | | | |
| 5.0 ± 0.5 | 15 | — | | | | 12 | | | | | |
| | 50 | — | | | | 19 | | | | | |
| Output disable time | t_{PLZ}, t_{PHZ} | $R_L = 1$ k Ω Figure 1 | | | | 2.5 ± 0.2 | 15 | — | 28.5 | ns | |
| | | | | | | | 50 | — | 37 | | |
| | | | 3.3 ± 0.3 | 15 | — | 18 | | | | | |
| | | | | 50 | — | 25 | | | | | |
| | | | 5.0 ± 0.5 | 15 | — | 12 | | | | | |
| | | | | 50 | — | 19 | | | | | |
| | | | Control input capacitance | C_{IN} | — | — | — | — | 10 | | pF |

11.7. Analog Switch Characteristics ($T_a = 25\text{ }^\circ\text{C}$) (Note)

| Characteristics | Part Number | Symbol | Test Condition | V_{CC} (V) | Typ. | Unit | |
|--|--------------|----------------|---|-------------------------------|------|------|---|
| Sine Wave Distortion | | THD | $R_L = 10\text{ k}\Omega$, $C_L = 50\text{ pF}$ $f_{IN} = 1\text{ kHz}$ | $V_{IN} = 2.0\text{ V}_{p-p}$ | 3.0 | 0.1 | % |
| | | | | $V_{IN} = 4.0\text{ V}_{p-p}$ | 4.5 | 0.03 | |
| Maximum frequency response | 74VHC4051AFT | $f_{MAX(I/O)}$ | V_{IN} is centered at $(V_{CC}/2)$. Adjust input for 0 dBm. Increase f_{IN} frequency until dB meter reads -3 dB. $R_L = 50\text{ }\Omega$, $C_L = 10\text{ pF}$, sine wave Figure 3 | 3.0 | 150 | MHz | |
| | 74VHC4052AFT | | | | 200 | | |
| | 74VHC4053AFT | | | 240 | | | |
| | 74VHC4051AFT | | | 4.5 | 180 | | |
| | 74VHC4052AFT | | | | 230 | | |
| | 74VHC4053AFT | | | | 280 | | |
| Feed through attenuation (switch OFF) | | FTH | V_{IN} is centered at $(V_{CC}/2)$. Adjust input for 0 dBm. $R_L = 600\text{ }\Omega$, $C_L = 50\text{ pF}$, $f_{IN} = 1\text{ MHz}$, sine wave Figure 4 | 3.0 | -45 | dB | |
| | | | | 4.5 | -45 | | |
| | | | | 3.0 | -65 | | |
| | | | | 4.5 | -65 | | |
| Crosstalk (control input to signal output) | | X_{talk} | $R_L = 600\text{ }\Omega$, $C_L = 50\text{ pF}$, $f_{IN} = 1\text{ MHz}$, square wave ($t_r = t_f = 6\text{ ns}$) Figure 5 | 3.0 | 60 | mV | |
| | | | | 4.5 | 100 | | |
| Crosstalk (between any switches) | | X_{talk} | V_{IN} is centered at $(V_{CC}/2)$. Adjust input for 0 dBm. $R_L = 600\text{ }\Omega$, $C_L = 50\text{ pF}$, $f_{IN} = 1\text{ MHz}$, sine wave Figure 6 | 3.0 | -45 | dB | |
| | | | | 4.5 | -45 | | |

Note: These characteristics are determined by design of devices.

12. AC Test Circuit



Cont : Control Inputs A or B or C or INH (C: Except VHC4052A)

P.G. : Pulse generator

Figure 1 t_{PLZ} , t_{PHZ} , t_{PLH} , t_{PHL}

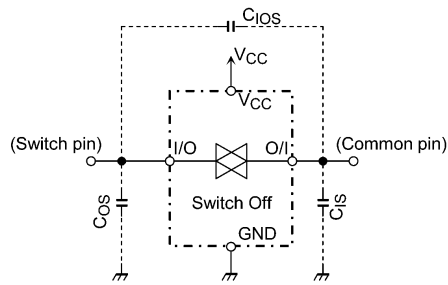


Figure 2 C_{IOS} , C_{IS} , C_{OS}

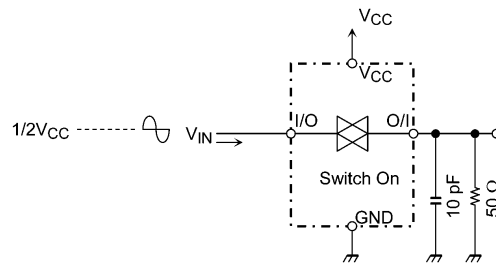


Figure 3 Frequency Response

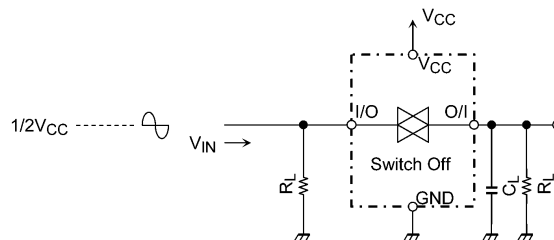
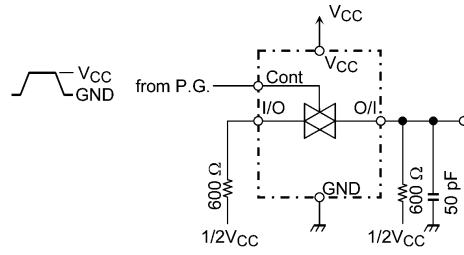


Figure 4 Feedthrough Attenuation



Cont : Control Inputs A or B or C or INH (C:Except VHC4052A)

P.G. : Pulse generator

Figure 5 Cross Talk (control input to output signal)

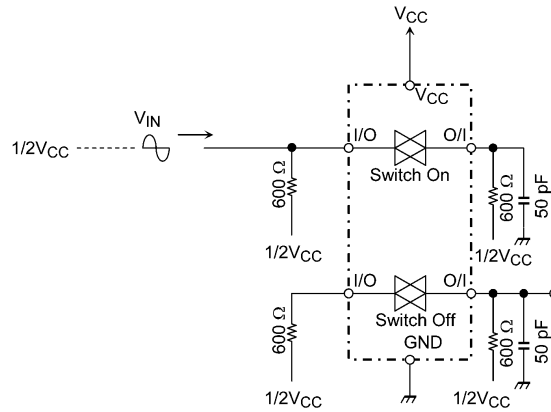
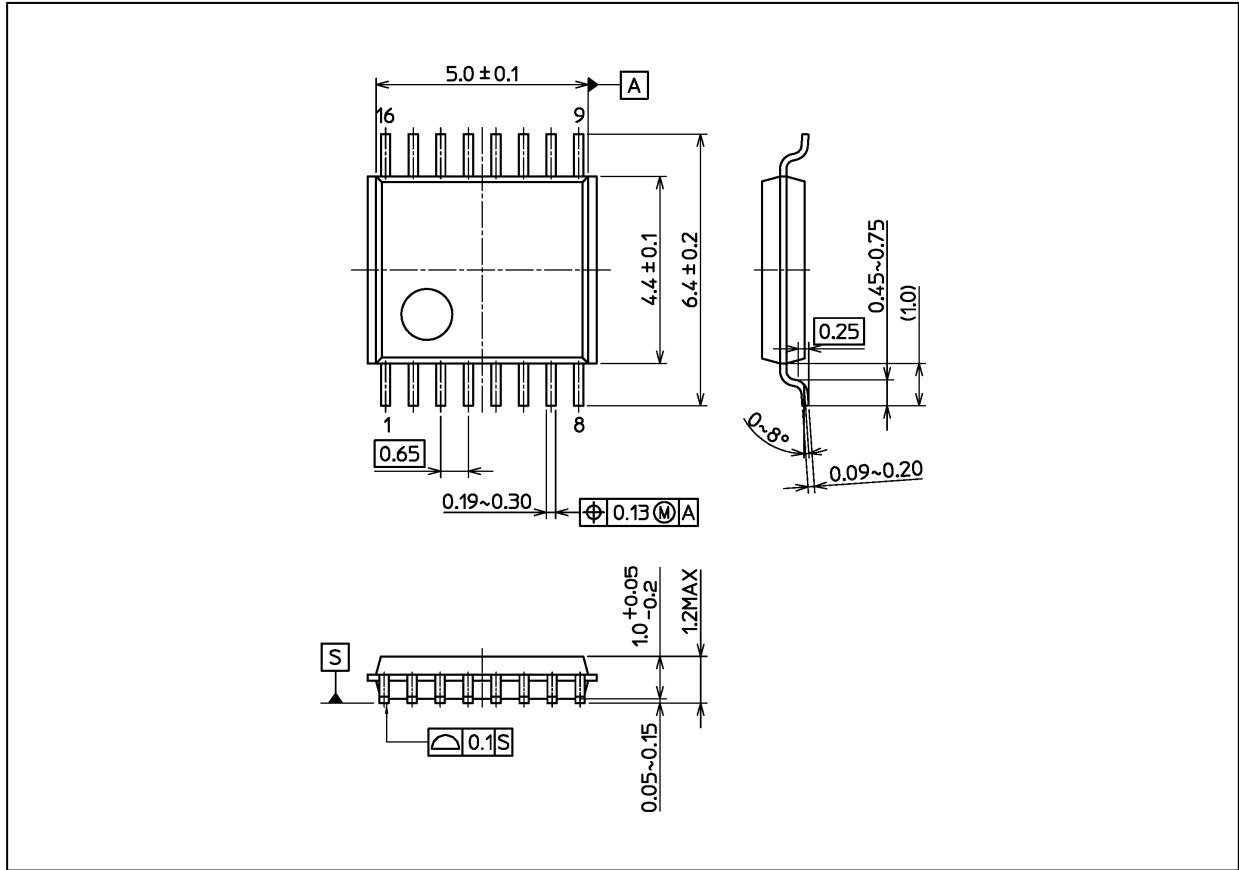


Figure 6 Cross Talk (between any two switches)

Package Dimensions

Unit: mm



Weight: 0.055 g (typ.)

| |
|--------------------|
| Package Name(s) |
| Nickname: TSSOP16B |

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