

FEATURES

Ultrawideband frequency range: 9 kHz to 44 GHz

Reflective design

Low insertion loss

1.5 dB to 18 GHz

2.4 dB to 40 GHz

2.7 dB to 44 GHz

High isolation

47 dB to 18 GHz

33 dB to 40 GHz

31 dB to 44 GHz

High input linearity

P0.1 dB: 26.5 dBm typical

IP3: 50 dBm typical

High RF input power handling

Through path: 26 dBm

Hot switching: 26 dBm

No low frequency spurious

0.1 dB RF settling time: 5.2 μ s

20-terminal, 3 mm \times 3 mm, RoHS-compliant, LGA package

Pin compatible with [ADRF5046](#), fast switching version

APPLICATIONS

Industrial scanner

Test instrumentation

Cellular infrastructure—mmWave 5G

Military radios, radars, and electronic counter measures (ECMs)

Microwave radios and very small aperture terminals (VSATs)

GENERAL DESCRIPTION

The ADRF5047 is a reflective, single-pole, four-throw (SP4T) switch manufactured in the silicon process.

The ADRF5047 operates from 9 kHz to 44 GHz with an insertion loss of lower than 2.7 dB and an isolation of higher than 31 dB. The device has a radio frequency (RF) input power handling capability of 26.5 dBm for both through path and hot switching.

The ADRF5047 draws a low current of 3 μ A on the positive supply of +3.3 V, and -110μ A on the negative supply of -3.3 V. The device provides complementary metal-oxide semiconductor (CMOS)/low voltage transistor-transistor logic (LVTTL)-compatible controls.

FUNCTIONAL BLOCK DIAGRAM

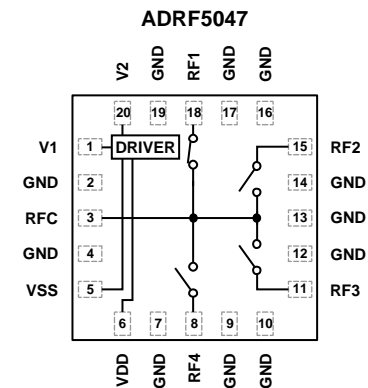


Figure 1.

The ADRF5047 is pin-compatible with the [ADRF5046](#) fast switching version, which operates from 100 MHz to 44 GHz.

The ADRF5047 comes in a 20-terminal, 3 mm \times 3 mm, RoHS-compliant, land grid array (LGA) package and operates from -40°C to $+105^{\circ}\text{C}$.

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REVISION HISTORY

11/2019—Revision 0: Initial Version

SPECIFICATIONS

Positive supply voltage (V_{DD}) = +3.3 V, negative supply voltage (V_{SS}) = -3.3 V, digital control input voltage (V_{CTL}) = 0 V or +3.3 V, and case temperature (T_{CASE}) = 25°C on a 50 Ω system, unless otherwise noted.

Table 1.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|----------------------------------|----------------------|---|-------|------|--------|---------|
| FREQUENCY RANGE | f | | 0.009 | | 44,000 | MHz |
| INSERTION LOSS | | | | | | |
| Between RFC and RF1 to RF4 (On) | | 9 kHz to 18 GHz | | 1.5 | | dB |
| | | 18 GHz to 26 GHz | | 1.6 | | dB |
| | | 26 GHz to 35 GHz | | 2.2 | | dB |
| | | 35 GHz to 40 GHz | | 2.4 | | dB |
| | | 40 GHz to 44 GHz | | 2.7 | | dB |
| ISOLATION | | | | | | |
| Between RFC and RF1 to RF4 (Off) | | 9 kHz to 18 GHz | | 47 | | dB |
| | | 18 GHz to 26 GHz | | 41 | | dB |
| | | 26 GHz to 35 GHz | | 35 | | dB |
| | | 35 GHz to 40 GHz | | 33 | | dB |
| | | 40 GHz to 44 GHz | | 31 | | dB |
| RETURN LOSS | | | | | | |
| RFC and RF1 to RF4 (On) | | 9 kHz to 18 GHz | | 15 | | dB |
| | | 18 GHz to 26 GHz | | 16 | | dB |
| | | 26 GHz to 35 GHz | | 15 | | dB |
| | | 35 GHz to 40 GHz | | 15 | | dB |
| | | 40 GHz to 44 GHz | | 14 | | dB |
| SWITCHING CHARACTERISTICS | | | | | | |
| Rise Time and Fall Time | t_{RISE}, t_{FALL} | 10% to 90% of RF output | | 1.4 | | μs |
| On Time and Off Time | t_{ON}, t_{OFF} | 50% V_{CTL} to 90% of RF output | | 3.4 | | μs |
| RF Settling Time | | | | | | |
| 0.1 dB | | 50% V_{CTL} to 0.1 dB of final RF output | | 5.2 | | μs |
| 0.05 dB | | 50% V_{CTL} to 0.05 dB of final RF output | | 7.2 | | μs |
| INPUT LINEARITY ¹ | | | | | | |
| 0.1 dB Power Compression | P0.1dB | f = 200 kHz to 40 GHz | | 26.5 | | dBm |
| Third-Order Intercept | IP3 | Two-tone input power = 14 dBm each tone, f = 200 kHz to 40 GHz, $\Delta f = 1$ MHz | | 50 | | dBm |
| Second-Order Intercept | IP2 | Two-tone input power = 14 dBm each tone, f = 10 GHz, $\Delta f = 1$ MHz | | 100 | | dBm |
| VIDEO FEEDTHROUGH ² | | | | 2 | | mV p-p |
| SUPPLY CURRENT | | VDD, VSS pins | | | | |
| Positive | I_{DD} | | | 3 | | μA |
| Negative | I_{SS} | | | -110 | | μA |
| DIGITAL CONTROL INPUTS | | V1, V2 pins | | | | |
| Voltage | | | | | | |
| Low | V_{INL} | | 0 | | 0.8 | V |
| High | V_{INH} | | 1.2 | | 3.3 | V |
| Current | | | | | | |
| Low | I_{INL} | | | <1 | | μA |
| High | I_{INH} | | | 35 | | μA |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---------------------------------|------------|---|-------|-----|----------|------|
| RECOMMENDED OPERATING CONDITONS | | | | | | |
| Supply Voltage | | | | | | |
| Positive | V_{DD} | | 3.15 | | 3.45 | V |
| Negative | V_{SS} | | -3.45 | | -3.15 | V |
| Digital Control Inputs Voltage | V_{CTL} | | 0 | | V_{DD} | V |
| RFx Input Power ³ | P_{IN} | $f = 200 \text{ kHz to } 40 \text{ GHz}, T_{CASE} = 85^\circ\text{C}^4$ | | | | |
| Through Path | | RF signal is applied to RFC or through connected RF throw port | | | 26 | dBm |
| Hot Switching | | RF signal is present at RFC while switching between RF throw port | | | 26 | dBm |
| Case Temperature | T_{CASE} | | -40 | | +105 | °C |

¹ For input linearity performance over frequency, see Figure 19 to Figure 22.

² Video feedthrough is the spurious dc transient measured at the RF ports in a 50 Ω test setup, without an RF signal present while switching the control voltage.

³ For power derating over frequency, see Figure 2 and Figure 3.

⁴ For 105°C operation, the power handling degrades from the $T_{CASE} = 85^\circ\text{C}$ specification by 3 dB.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2.

| Parameter | Rating |
|---|----------------------------|
| Supply Voltage | |
| Positive | -0.3 V to +3.6 V |
| Negative | -3.6 V to +0.3 V |
| Digital Control Inputs Voltage | -0.3 V to $V_{DD} + 0.3$ V |
| RFx Input Power ($f^1 = 5$ MHz to 40 GHz, $T_{CASE} = 85^\circ\text{C}^2$) | |
| Through Path | 26.5 dBm |
| Hot Switching | 26.5 dBm |
| Temperature | |
| Junction, T_J | 135°C |
| Storage | -65°C to +150°C |
| Electrostatic Discharge (ESD) Sensitivity | |
| Human Body Model (HBM) | |
| RFx Pins | 2000 V |
| Supply and Digital Control Pins | 2000 V |

¹ For power derating over frequency, see Figure 2 and Figure 3.

² For 105°C operation, the power handling degrades from the $T_{CASE} = 85^\circ\text{C}$ specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

| Package Type | θ_{JC} | Unit |
|-----------------------|---------------|------|
| CC-20-6, Through Path | 240 | °C/W |

POWER DERATING CURVES

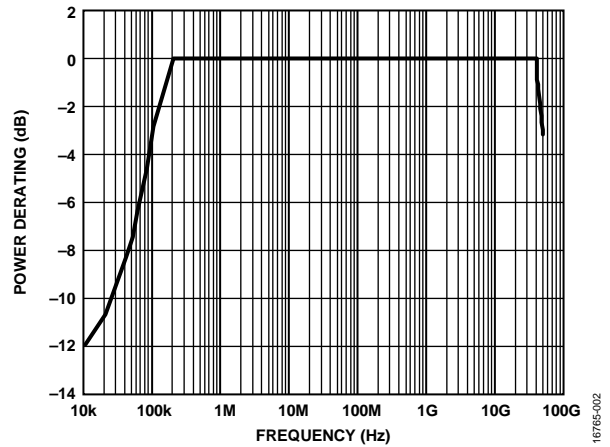


Figure 2. Power Derating vs. Frequency, Low Frequency Detail, $T_{CASE} = 85^\circ\text{C}$

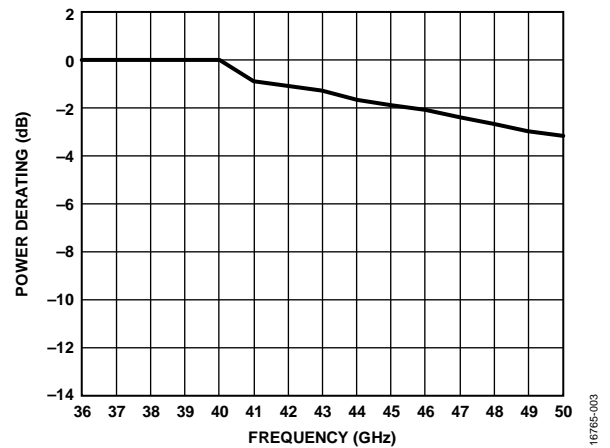


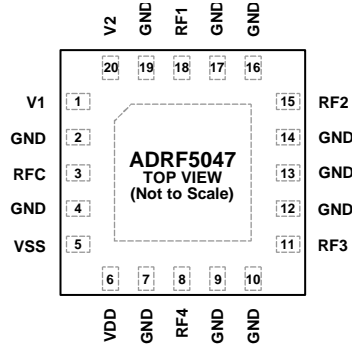
Figure 3. Power Derating vs. Frequency, High Frequency Detail, $T_{CASE} = 85^\circ\text{C}$

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO RF AND DC GROUND OF THE PCB.

16765-004

Figure 4. Pin Configuration (Top View)

Table 4. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|--------------------------------------|----------|--|
| 1 | V1 | Control Input 1. See Table 5 for the control voltage truth table, and see Figure 6 for the interface schematic. |
| 2, 4, 7, 9, 10, 12 to 14, 16, 17, 19 | GND | Ground. These pins must be connected to the RF and dc ground of the PCB. |
| 3 | RFC | RF Common Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic. |
| 5 | VSS | Negative Supply Voltage. |
| 6 | VDD | Positive Supply Voltage. |
| 8 | RF4 | RF Throw Port 4. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic. |
| 11 | RF3 | RF Throw Port 3. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic. |
| 15 | RF2 | RF Throw Port 2. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic. |
| 18 | RF1 | RF Throw Port 1. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 5 for the interface schematic. |
| 20 | V2 | Control Input 2. See Table 5 for the control voltage truth table, and see Figure 6 for the interface schematic. |
| | EPAD | Exposed Pad. The exposed pad must be connected to the RF and dc ground of the PCB. |

INTERFACE SCHEMATICS

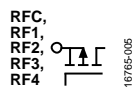


Figure 5. RF Pins (RFC and RF1 to RF4) Interface Schematic

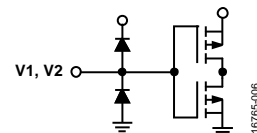


Figure 6. Control Pins (V1 and V2) Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, $V_{CTL} = 0\text{ V}$ or 3.3 V , and $T_{CASE} = 25^\circ\text{C}$ on a $50\ \Omega$ system, unless otherwise noted. Measured on the probe matrix board.

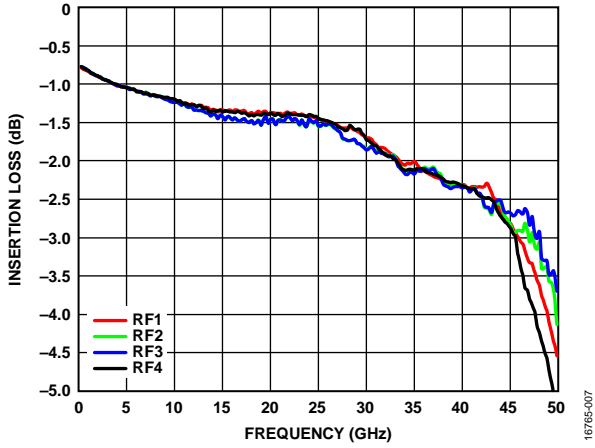


Figure 7. Insertion Loss vs. Frequency for RF1, RF2, RF3, and RF4

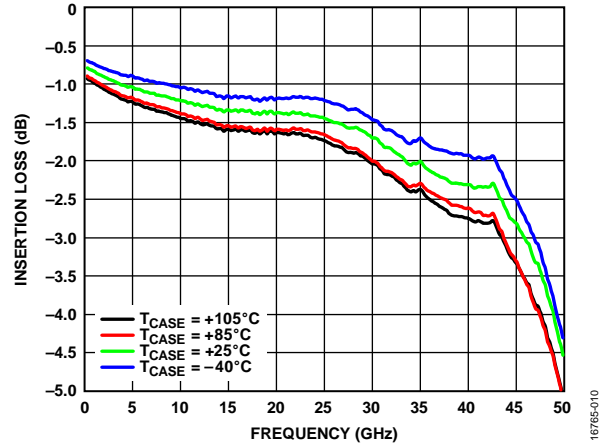


Figure 10. Insertion Loss vs. Frequency over Temperature, RFC and RF1 On

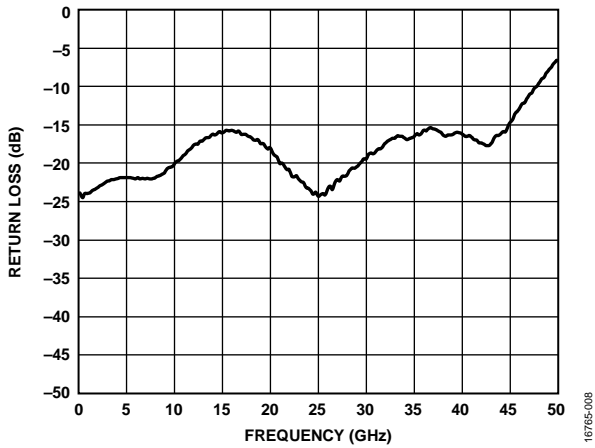


Figure 8. RFC Return Loss vs. Frequency, RFC to RF1 On

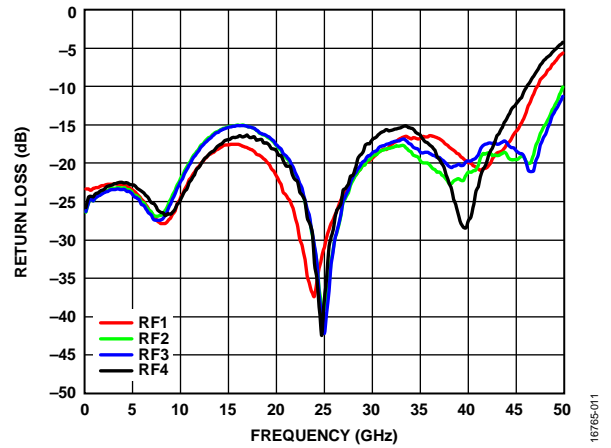


Figure 11. Return Loss vs. Frequency, RF1, RF2, RF3, RF4 On

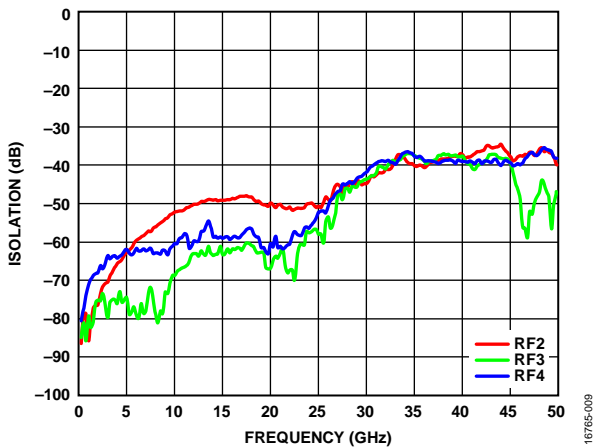


Figure 9. Isolation vs. Frequency, RFC to RF1 On

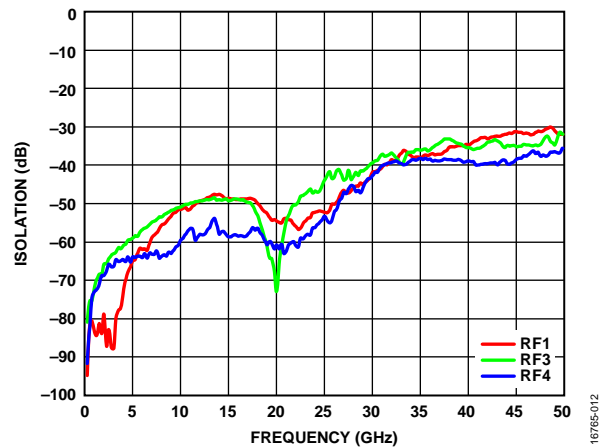


Figure 12. Isolation vs. Frequency, RFC to RF2 On

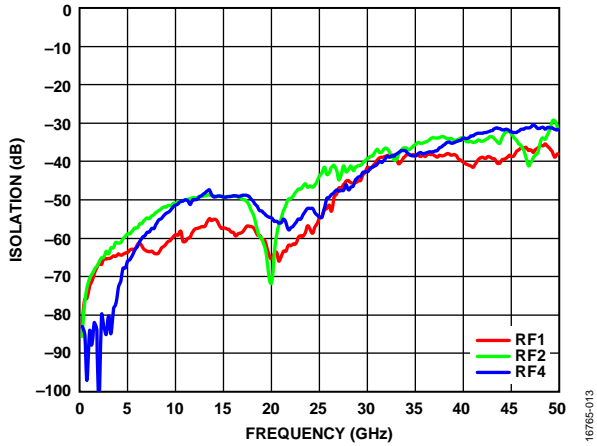


Figure 13. Isolation vs. Frequency, RFC to RF3 On

16765-013

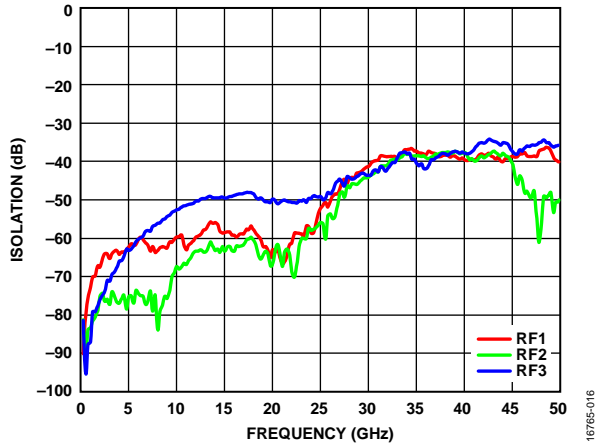


Figure 16. Isolation vs. Frequency, RFC to RF4 On

16765-016

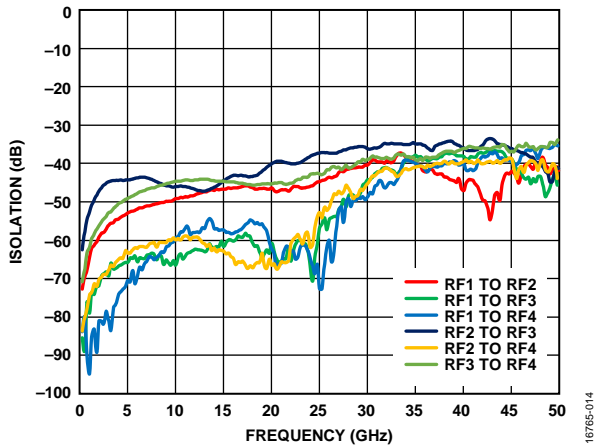


Figure 14. Channel to Channel Isolation vs. Frequency, RFC to RF1 On

16765-014

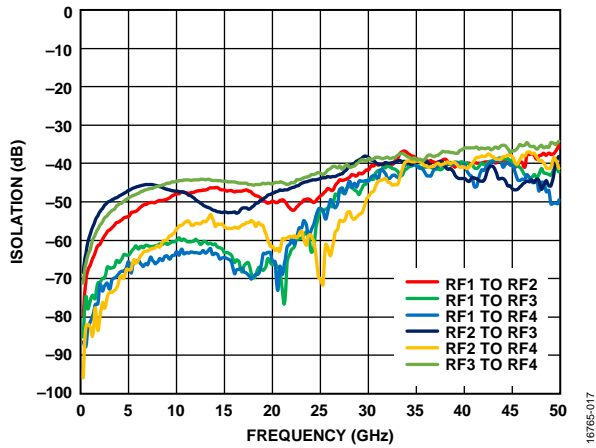


Figure 17. Channel to Channel Isolation vs. Frequency, RFC to RF2 On

16765-017

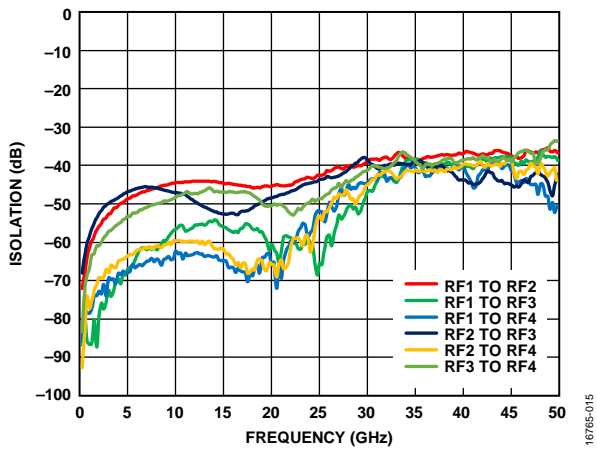


Figure 15. Channel to Channel Isolation vs. Frequency, RFC to RF3 On

16765-015

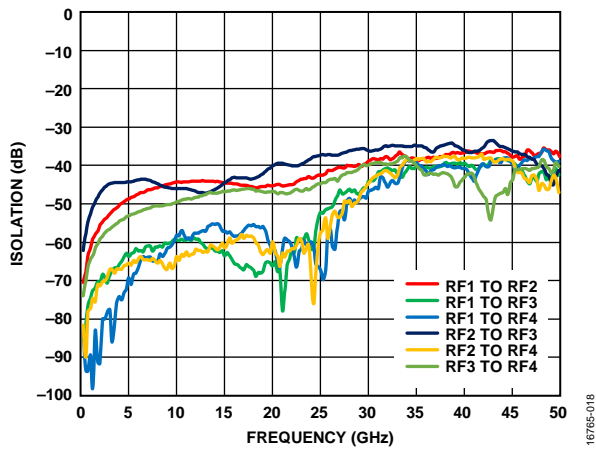


Figure 18. Channel to Channel Isolation vs. Frequency, RFC to RF4 On

16765-018

INPUT 0.1 dB POWER COMPRESSION AND THIRD-ORDER INTERCEPT

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, $V_{CTL} = 0\text{ V}$ or 3.3 V , and $T_{CASE} = 25^\circ\text{C}$ on a $50\ \Omega$ system, unless otherwise noted. Measured on the evaluation board.

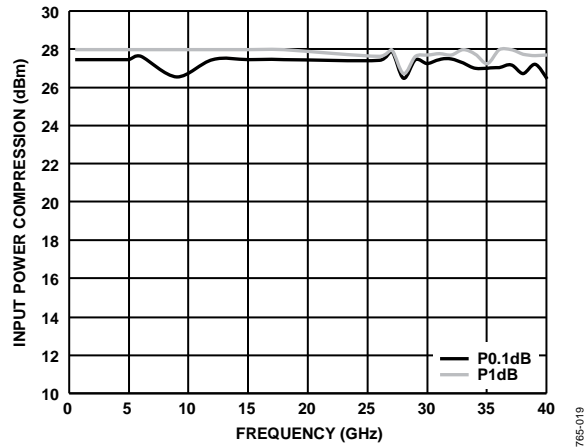


Figure 19. Input Power Compression vs. Frequency

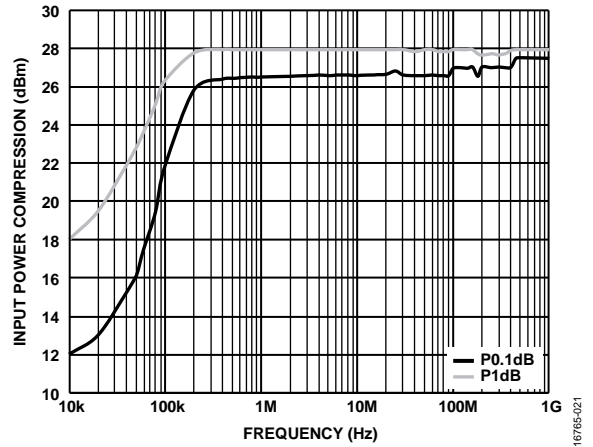


Figure 21. Input Power Compression vs. Frequency (Low Frequency Detail)

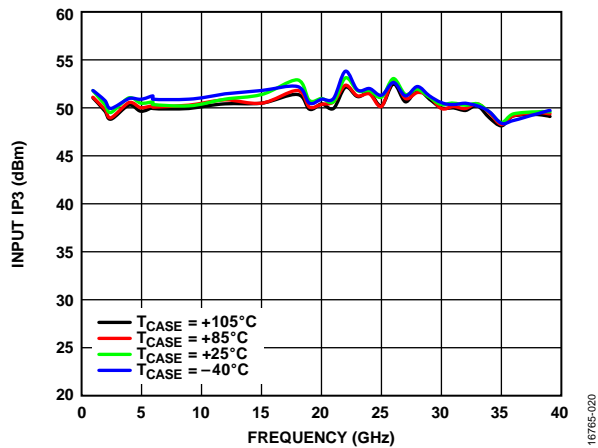


Figure 20. Input IP3 vs. Frequency over Various Temperatures

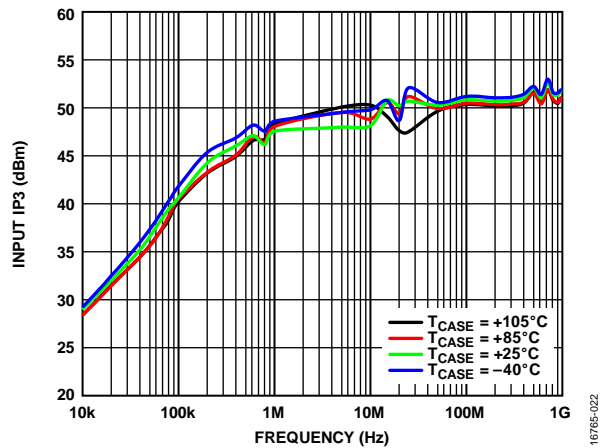


Figure 22. Input IP3 vs. Frequency over Various Temperatures (Low Frequency Detail)

THEORY OF OPERATION

The ADRF5047 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

All of the RF ports (RFC, RF1 to RF4) are dc-coupled to 0 V, and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V. The RF ports are internally matched to 50 Ω . Therefore, external matching networks are not required.

The ADRF5047 integrates a driver to perform logic functions internally and to provide the user with the advantage of a simplified CMOS/LVTTL-compatible control interface. The driver features two digital control input pins (V1 and V2) that control the state of the RF paths. The logic level applied to the V1 and V2 pins determines which RF port is in the insertion loss state, while the other three paths are in the isolation state (see Table 5).

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The switch design is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port. The isolation paths provide high loss between the insertion loss path and the unselected RF throw ports that are reflective.

Table 5. Control Voltage Truth Table

| Digital Control Inputs | | RF Paths | | | |
|------------------------|------|---------------------|---------------------|---------------------|---------------------|
| V1 | V2 | RF1 to RFC | RF2 to RFC | RF3 to RFC | RF4 to RFC |
| Low | Low | Insertion loss (on) | Isolation (off) | Isolation (off) | Isolation (off) |
| High | Low | Isolation (off) | Insertion loss (on) | Isolation (off) | Isolation (off) |
| Low | High | Isolation (off) | Isolation (off) | Insertion loss (on) | Isolation (off) |
| High | High | Isolation (off) | Isolation (off) | Isolation (off) | Insertion loss (on) |

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Apply digital control inputs, V1 and V2. Applying these digital control inputs before applying the VDD supply inadvertently forwards bias and damages the internal ESD protection structures. To avoid this damage, use a series 1 k Ω resistor to limit the current flowing into the control pin. Use pull-up or pull-down resistors if the controller output is in a high impedance state after VDD is powered up and the control pins are not driven to a valid logic state.
4. Apply an RF input signal to either the RFC port or the RF throw port.

The ideal power-down sequence is the reverse order of the power-up sequence.

APPLICATIONS INFORMATION

EVALUATION BOARD

The ADRF5047-EVALZ is a 4-layer evaluation board. The outer copper (Cu) layers are 0.5 oz (0.7 mil) plated to 1.5 oz (2.2 mil) and are separated by dielectric materials. Figure 23 shows the evaluation board cross sectional view.

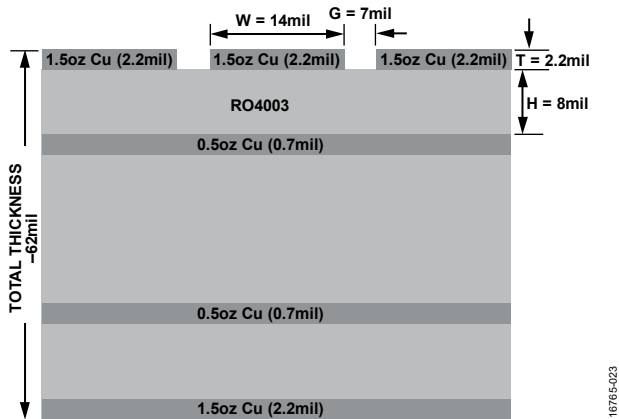


Figure 23. Evaluation Board Cross Sectional View

All RF and dc traces are routed on the top copper layer, whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The top dielectric material is 8 mil Rogers RO4003, offering optimal high frequency performance. The middle and bottom dielectric materials provide mechanical strength. The overall board thickness is 62 mil, which allows 2.4 mm RF launchers to be connected at the board edges. Figure 24 shows the top view of the evaluation board.

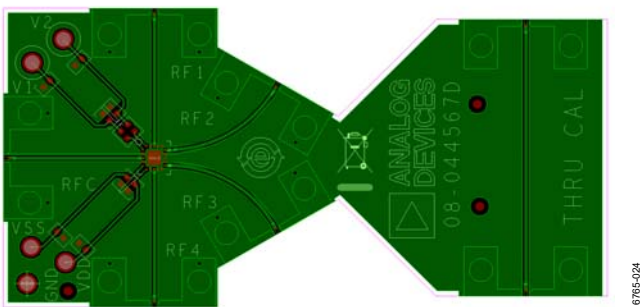


Figure 24. Evaluation Board Layout, Top View

The RF transmission lines were designed using a coplanar waveguide (CPWG) model, with a trace width of 14 mil and ground clearance of 7 mil to have a characteristic impedance of 50 Ω. The RF transmission lines are extended by 8 mil from package edge to the tapered line used for RF pin transition as shown in Figure 25. For optimal RF and thermal grounding, as many plated through vias as possible are arranged around transmission lines and under the exposed pad of the package.

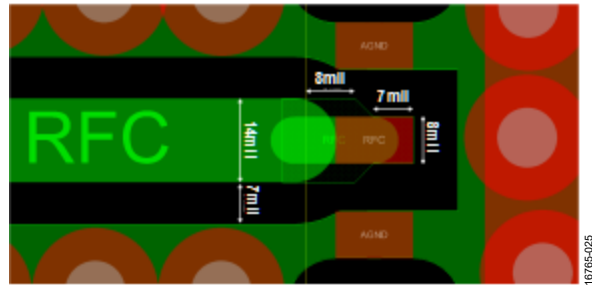


Figure 25. RF Transmission Lines

Two power supply ports are connected to the VDD and VSS test points, control voltages are connected to the V1 and V2 test points, and the ground reference is connected to the GND test point.

On the supply traces, a 100 pF bypass capacitor is used to filter the high frequency noise. Additionally, unpopulated components positions are available for applying extra bypass capacitors.

On the control traces, there are provisions for the resistor capacitor (RC) filter to eliminate dc-coupled noise, if needed, by the application. The resistor can also improve the isolation between the RF and the control signal.

The RF input and output ports (RFC, RF1 to RF4) are connected through 50 Ω transmission lines to the 2.4 mm RF launchers. These high frequency RF launchers are by contact and not soldered onto the board.

A thru calibration line (THRU CAL) connects the unpopulated RF launchers. This transmission line is used to calibrate out the board loss effects from the ADRF5047-EVALZ evaluation board measurements to determine the device performance at the pins of the IC. Figure 26 shows the typical board loss at room temperature, the embedded insertion loss, and the de-embedded insertion loss for the ADRF5047.

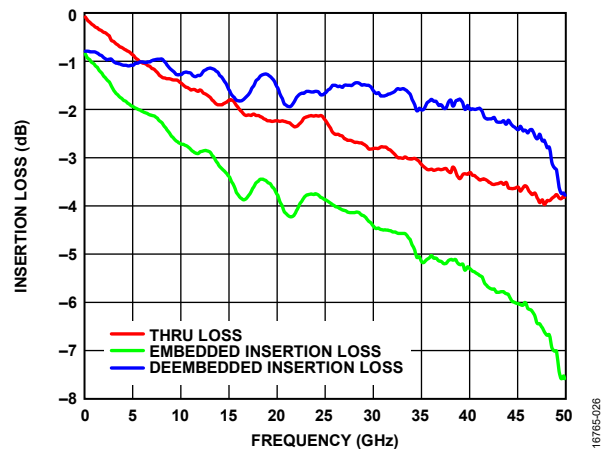
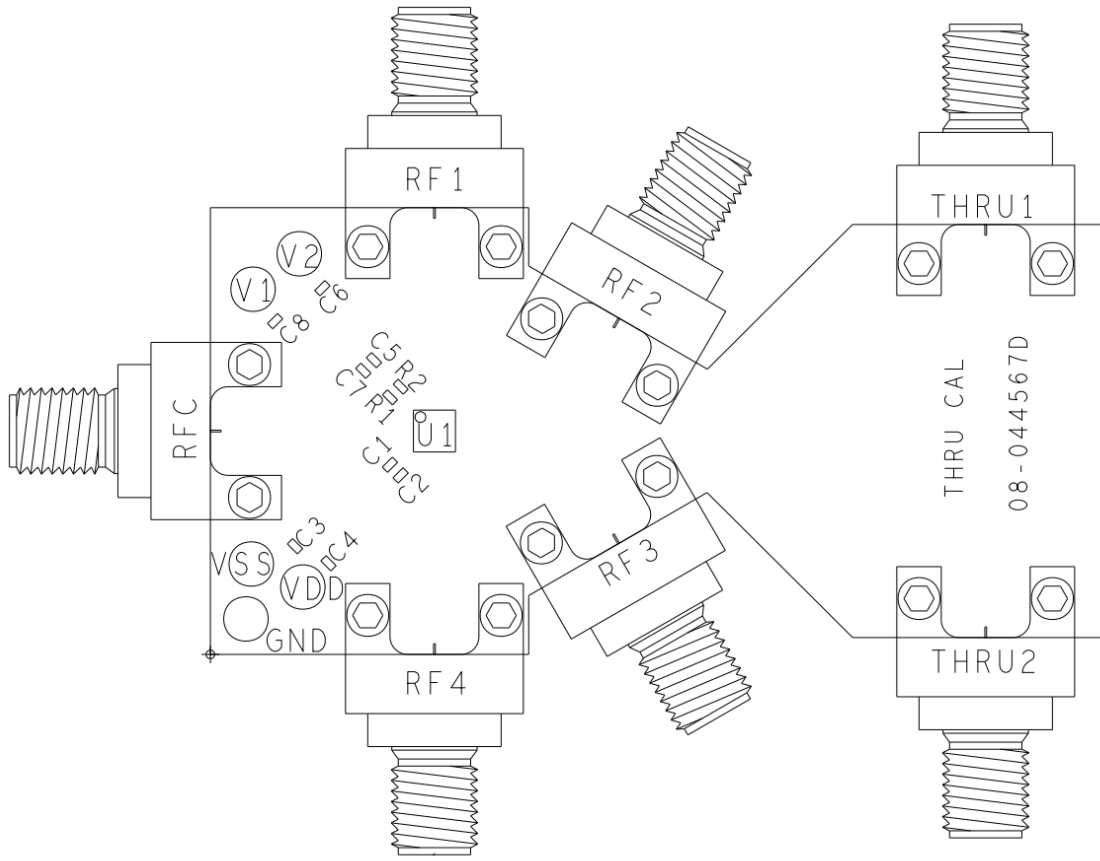


Figure 26. Insertion Loss vs. Frequency

Figure 27 and Figure 28 shows the ADRF5047-EVALZ assembly drawing with component placement and the schematic, respectively.



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Figure 27. Evaluation Board Assembly Drawing

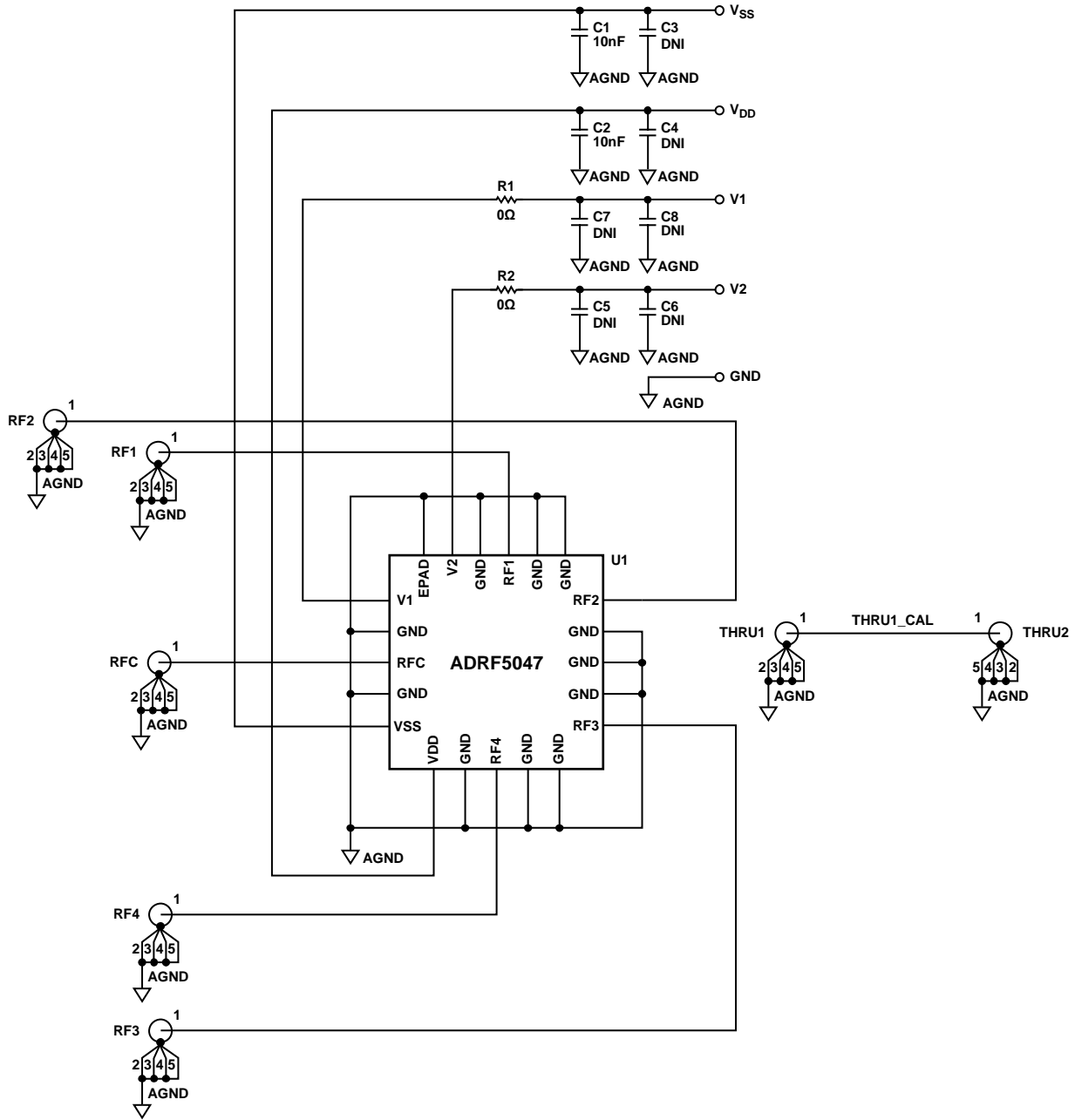


Figure 28. Evaluation Board Schematic

16765-028

Table 6. Evaluation Board Components

| Component | Default Value | Description |
|-----------------------|----------------|---|
| C1, C2 | 10 nF | Capacitors, C0402 package |
| C3, C4, C5, C7 | Not applicable | Capacitors, C0402 package, do not install (DNI) |
| C6, C8 | Not applicable | Capacitors, C0402 package, DNI |
| RFC, RF1 to RF4 | Not applicable | 2.4 mm end launch connectors (Southwest Microwave 1492-04A-5) |
| THRU1, THRU2 | Not applicable | 2.4 mm end launch connectors, DNI |
| R1, R2 | 0 Ω | Resistors, 0402 package |
| VDD, VSS, V1, V2, GND | Not applicable | Through-hole mount test points |
| U1 | ADRF5047 | SP4T switch, Analog Devices, Inc. |
| PCB | 08-044567D | Evaluation PCB, Analog Devices |

PROBE MATRIX BOARD

The probe matrix board uses same stackup as the evaluation board but a different layout designed to take measurements using ground, signal, ground (GSG) probes at close proximity to the RFx pins. Probing eliminates the mismatch reflections caused by connectors, cables, and board layout. Therefore, the probe matrix board provides more accurate measurement of the device performance than the evaluation board. Figure 29 shows the top view of the probe matrix board layout.

The probe matrix board includes a through reflect line (TRL) calibration kit allowing board loss de-embedding. The actual board duplicates the same layout in matrix form to assemble multiple devices at one time. All s parameters were measured on this board.

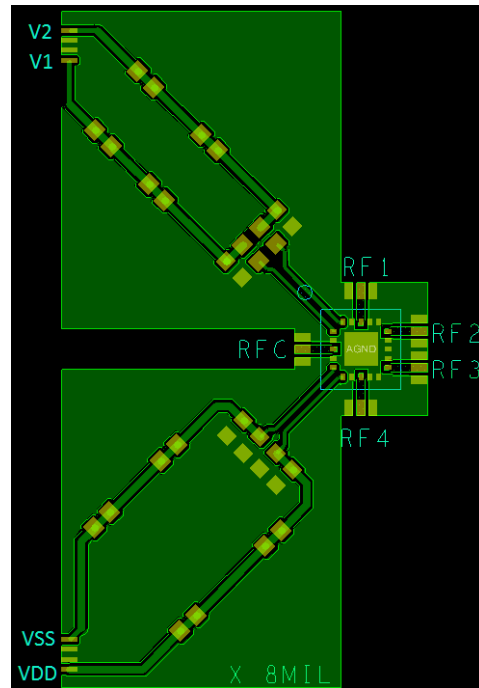


Figure 29. Probe Matrix Board Layout (Top View)

OUTLINE DIMENSIONS

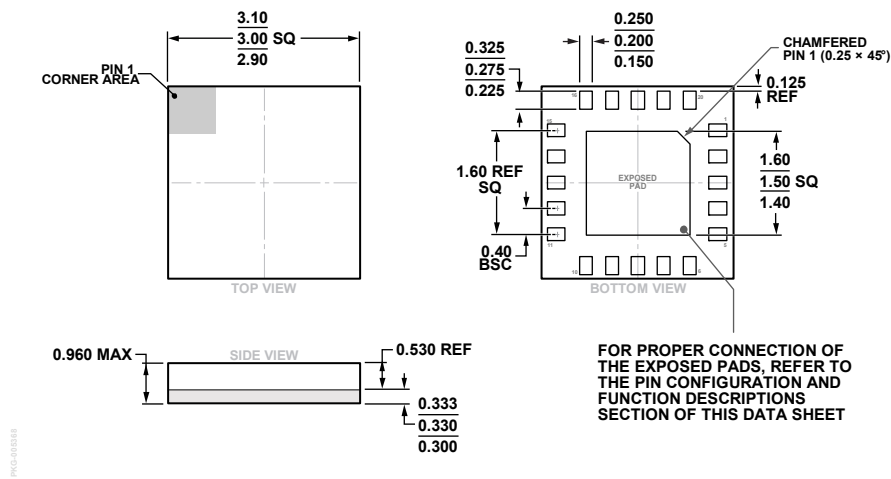


Figure 30. 20-Terminal Land Grid Array [LGA]
(CC-20-6)
Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option | Marking Code |
|--------------------|-------------------|-----------------------------------|----------------|--------------|
| ADRF5047BCCZN | -40°C to +105°C | 20-Terminal Land Grid Array [LGA] | CC-20-6 | 047 |
| ADRF5047BCCZN-R7 | -40°C to +105°C | 20-Terminal Land Grid Array [LGA] | CC-20-6 | 047 |
| ADRF5047-EVALZ | | Evaluation Board | | |

¹ Z = RoHS Compliant Part.

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