Low Voltage Single Supply SPDT Analog Switch

The NLAS4599 is an advanced high speed CMOS single pole – double throw analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining low power dissipation. This switch controls analog and digital voltages that may vary across the full power–supply range (from $V_{\rm CC}$ to GND).

The device has been designed so the ON resistance (R_{ON}) is much lower and more linear over input voltage than R_{ON} of typical CMOS analog switches.

The channel select input is compatible with standard CMOS outputs.

The channel select input structure provides protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. This input structure helps prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- Channel Select Input Over-Voltage Tolerant to 5.5 V
- Fast Switching and Propagation Speeds
- Break-Before-Make Circuitry
- Low Power Dissipation: $I_{CC} = 2 \mu A \text{ (Max)}$ at $T_A = 25^{\circ}\text{C}$
- Diode Protection Provided on Channel Select Input
- Improved Linearity and Lower ON Resistance over Input Voltage
- Latch-up Performance Exceeds 300 mA
- ESD Performance: Human Body Model > 2000 V; Machine Model > 200 V
- Chip Complexity: 38 FETs
- Pb-Free Packages are Available

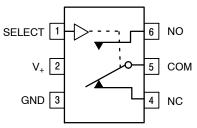


Figure 1. Pin Assignment

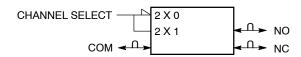


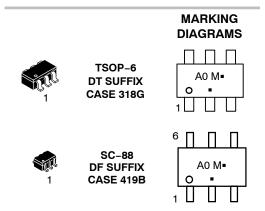
Figure 2. Logic Symbol

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

http://onsemi.com



A0 = Specific Device Code

M = Date Code

= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

FUNCTION TABLE

Select	ON Channel
L	NC
H	NO

ABSOLUTE MAXIMUM RATINGS

Symbol		Parameter	Value	Unit
V _{CC}	Positive DC Supply Voltage		-0.5 to +7.0	V
V _{IS}	Analog Input Voltage (V _{NO} or	· V _{COM})	$-0.5 \le V_{IS} \le V_{CC} + 0.5$	V
V _{IN}	Digital Select Input Voltage		$-0.5 \le V_1 \le +7.0$	V
I _{IK}	DC Current, Into or Out of Ar	ny Pin	±50	mA
P _D	Power Dissipation in Still Air	200 200	mW	
T _{STG}	Storage Temperature Range		-65 to +150	°C
TL	Lead Temperature, 1mm from	n Case for 10 seconds	260	°C
TJ	Junction Temperature Under	Bias	150	°C
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	2000 200 N/A	V
I _{LATCH-UP}	Latch-Up Performance	Above V _{CC} and Below GND at 125°C (Note 4)	±300	mA
θЈΑ	Thermal Resistance	SC-88 TSOP-6	333 333	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Tested to EIA/JESD22-A114-A
- 2. Tested to EIA/JESD22-A115-A
- 3. Tested to JESD22-C101-A
- 4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Characteristics			
V _{CC}	DC Supply Voltage	2.0	5.5	V	
V _{IN}	Digital Select Input Voltage	GND	5.5	V	
V _{IS}	Analog Input Voltage (NC, NO, COM)		GND	V _{CC}	V
T _A	Operating Temperature Range		-55	+125	°C
t _r , t _f	Input Rise or Fall Time, SELECT	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0	100 20	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

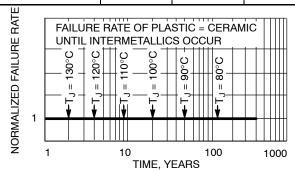


Figure 3. Failure Rate vs. Time Junction Temperature

DC CHARACTERISTICS - Digital Section (Voltages Referenced to GND)

				Gua	aranteed Lim	nit	
Symbol	Parameter	Condition	V _{cc}	-55 to 25°C	<85°C	<125°C	Unit
V _{IH}	Minimum High-Level		2.0	1.5	1.5	1.5	V
	Input Voltage, Select		2.5	1.9	1.9	1.9	
	Input		3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			5.5	3.85	3.85	3.85	
V _{IL}	Maximum Low-Level		2.0	0.5	0.5	0.5	V
	Input Voltage, Select		2.5	0.6	0.6	0.6	
	Input		3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			5.5	1.65	1.65	1.65	
I _{IN}	Maximum Input Leakage Current, Select Input	V _{IN} = 5.5 V or GND	5.5	<u>+</u> 0.1	<u>+</u> 1.0	<u>+</u> 1.0	μΑ
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5 V or GND	0	±10	±10	± 10	μΑ
Icc	Maximum Quiescent Supply Current	Select and V _{IS} = V _{CC} or GND	5.5	1.0	1.0	2.0	μΑ

DC ELECTRICAL CHARACTERISTICS - Analog Section

				Gua	ranteed Lin	nit	
Symbol	Parameter	Condition	V _{CC}	-55 to 25°C	<85°C	<125°C	Unit
R _{ON}	Maximum "ON"	V _{IN} = V _{IL} or V _{IH}	2.5	85	95	105	Ω
	Resistance	V _{IS} = GND to V _{CC}	3.0	45	50	55	
	(Figures 17 – 23)	I _{IN} I ≤ 10.0 mA	4.5	30	35	40	
			5.5	25	30	35	
R _{FLAT} (ON)	ON Resistance Flatness (Figures 17 – 23)	$\begin{split} &V_{IN} = V_{IL} \text{ or } V_{IH} \\ &I_{IN}I \leq 10.0 \text{ mA} \\ &V_{IS} = 1V, 2V, 3.5V \end{split}$	4.5	4	4	5	Ω
ΔR_{ON} (ON)	ON Resistance Match Between Channels	$\begin{split} &V_{IN} = V_{IL} \text{ or } V_{IH} \\ &I_{IN}I \leq 10.0 \text{ mA} \\ &V_{NO} \text{ or } V_{NC} = 3.5 \text{ V} \end{split}$	4.5	2	2	3	Ω
I _{NC(OFF)}	NO or NC Off Leakage Current (Figure 9)	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{NO} \text{ or } V_{NC} = 1.0 V_{COM} 4.5 V$	5.5	1	10	100	nA
I _{COM} (ON	COM ON Leakage Current (Figure 9)	$V_{IN} = V_{IL}$ or V_{IH} V_{NO} 1.0 V or 4.5 V with V_{NC} floating or V_{NO} 1.0 V or 4.5 V with V_{NO} floating $V_{COM} = 1.0$ V or 4.5 V	5.5	1	10	100	nA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ ns}$)

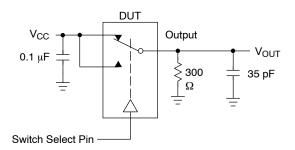
					(Guaran	teed Ma	x Limit	i i			
			v_{cc}	V _{IS}	-5	5 to 25	°C	<85	5°C	<12	5°C	
Symbol	Parameter	Test Conditions	(V)	(V)	Min	Тур*	Max	Min	Max	Min	Max	Unit
t _{ON}	Turn-On Time (Figures 12 and 13)	$R_L = 300 \ \Omega, C_L = 35 \ pF$ (Figures 5 and 6)	2.5 3.0 4.5 5.5	2.0 2.0 3.0 3.0	5 5 2 2	23 16 11 9	28 21 16 14	5 5 2 2	30 25 20 20	5 5 2 2	30 25 20 20	ns
t _{OFF}	Turn-Off Time (Figures 12 and 13)	$R_L = 300 \ \Omega, C_L = 35 \ pF$ (Figures 5 and 6)	2.5 3.0 4.5 5.5	2.0 2.0 3.0 3.0	1 1 1	7 5 4 3	12 10 9 8	1 1 1	15 15 12 12	1 1 1	15 15 12 12	ns
t _{BBM}	Minimum Break-Before-Make Time	V_{IS} = 3.0 V (Figure 4) R_L = 300 Ω , C_L = 35 pF	2.5 3.0 4.5 5.5	2.0 2.0 3.0 3.0	1 1 1	12 11 6 5		1 1 1		1 1 1		ns

^{*}Typical Characteristics are at 25°C.

		Typical @ 25, VCC = 5.0 V	
C _{IN}	Maximum Input Capacitance, Select Input	8	pF
C _{NO} or C _{NC}	Analog I/O (switch off)	10	
C _{COM}	Common I/O (switch off)	10	
C _(ON)	Feedthrough (switch on)	20	

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

			V _{CC}	Typical	
Symbol	Parameter	Condition	(V)	25°C	Unit
BW	Maximum On-Channel -3dB Bandwidth or Minimum Frequency Response (Figure 10)	V _{IN} = 0 dBm V _{IN} centered between V _{CC} and GND (Figure 7)	3.0 4.5 5.5	170 200 200	MHz
V _{ONL}	Maximum Feedthrough On Loss	V _{IN} = 0 dBm @ 100 kHz to 50 MHz V _{IN} centered between V _{CC} and GND (Figure 7)	3.0 4.5 5.5	-3 -3 -3	dB
V _{ISO}	Off-Channel Isolation (Figure 10)	f = 100 kHz; V _{IS} = 1 V RMS V _{IN} centered between V _{CC} and GND (Figure 7)	3.0 4.5 5.5	-93 -93 -93	dB
Q	Charge Injection Select Input to Common I/O (Figure 15)	$\begin{array}{l} V_{IN} = V_{CC~to}~GND,~F_{IS} = 20~kHz\\ t_r = t_f = 3~ns\\ R_{IS} = 0~\Omega,~C_L = 1000~pF\\ Q = C_L \star \Delta V_{OUT}\\ (\text{Figure 8}) \end{array}$	3.0 5.5	1.5 3.0	рС
THD	Total Harmonic Distortion THD + Noise (Figure 14)	F_{IS} = 20 Hz to 100 kHz, R_L = Rgen = 600 Ω, C_L = 50 pF V_{IS} = 5.0 V_{PP} sine wave	5.5	0.1	%



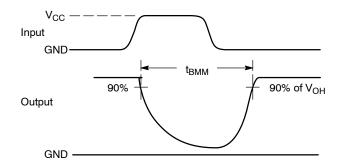
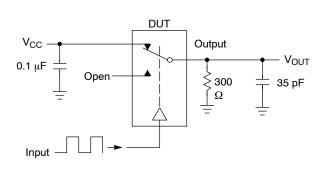


Figure 4. t_{BBM} (Time Break-Before-Make)



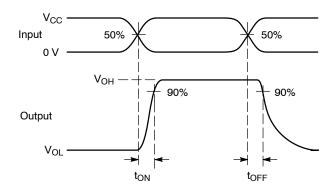
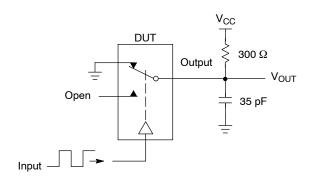


Figure 5. t_{ON}/t_{OFF}



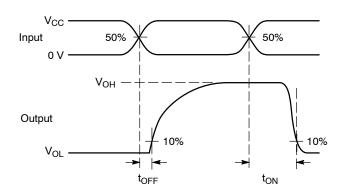
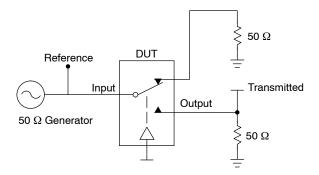


Figure 6. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. $V_{\rm ISO}$, Bandwidth and $V_{\rm ONL}$ are independent of the input signal direction.

$$\begin{split} &V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log } \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz} \\ &V_{ONL} = \text{On Channel Loss} = 20 \text{ Log } \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz} \end{split}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V_{ONL}

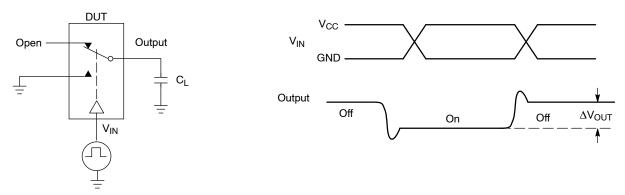


Figure 8. Charge Injection: (Q)

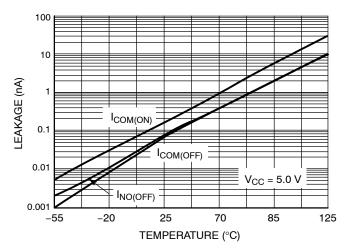


Figure 9. Switch Leakage vs. Temperature

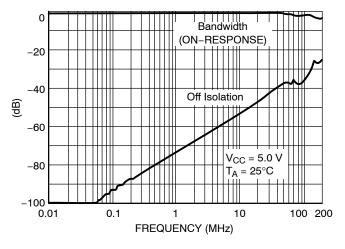


Figure 10. Bandwidth and Off-Channel Isolation

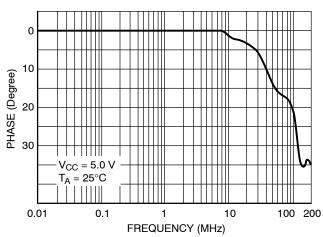


Figure 11. Phase vs. Frequency

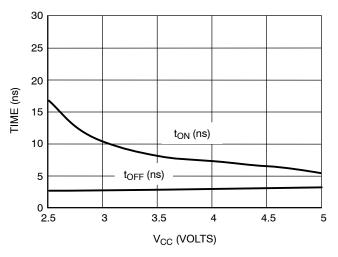


Figure 12. t_{ON} and t_{OFF} vs. V_{CC} at 25°C

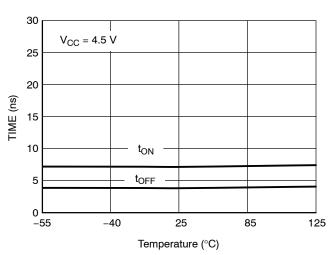


Figure 13. t_{ON} and t_{OFF} vs. Temp

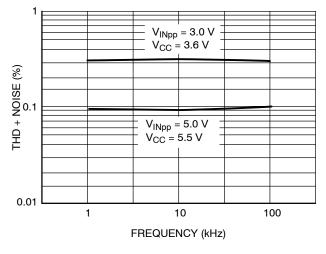


Figure 14. Total Harmonic Distortion Plus Noise vs. Frequency

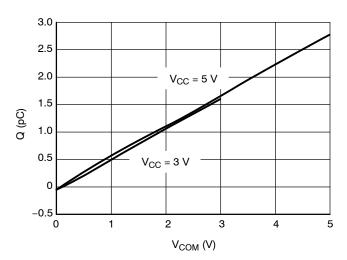
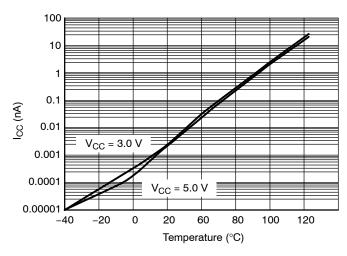


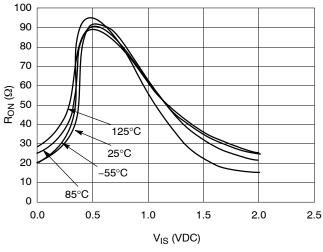
Figure 15. Charge Injection vs. COM Voltage



100 $V_{CC} = 2.0 \text{ V}$ 80 60 R_{ON} (Ω) V_{CC} = 2.5 V40 $V_{CC} = 3.0 \text{ V}$ $V_{CC} = 4.0 \text{ V}$ 20 $V_{CC} = 5.5 V$ 0 0.0 1.0 2.0 3.0 4.0 5.0 6.0 V_{IS} (VDC)

Figure 16. I_{CC} vs. Temp, V_{CC} = 3 V & 5 V

Figure 17. R_{ON} vs. V_{CC,} Temp = 25°C



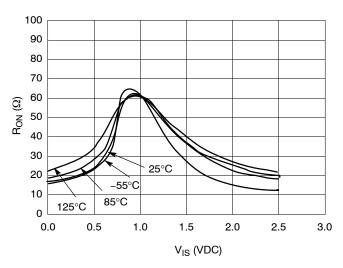
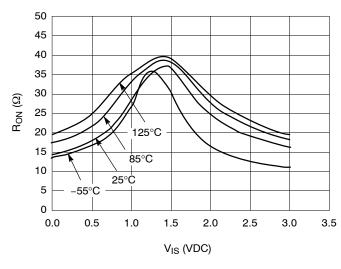


Figure 18. R_{ON} vs Temp, V_{CC} = 2.0 V

Figure 19. R_{ON} vs. Temp, V_{CC} = 2.5 V



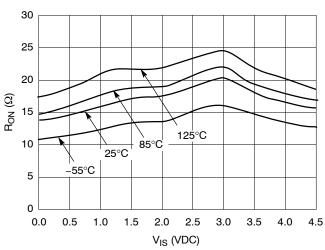
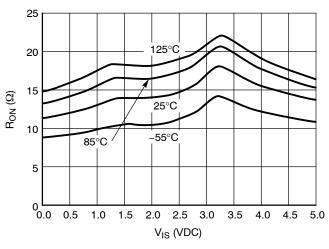


Figure 20. R_{ON} vs. Temp, V_{CC} = 3.0 V

Figure 21. R_{ON} vs. Temp, V_{CC} = 4.5 V



25 20 125°C 10 85°C -55°C 5 0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5 V_{IS} (VDC)

Figure 22. R_{ON} vs. Temp, V_{CC} = 5.0 V

Figure 23. R_{ON} vs. Temp, V_{CC} = 5.5 V

ORDERING INFORMATION

		Device Nom	nenclature			
Device	Circuit Indicator	Technology	Device Function	Suffix	Package	Shipping [†]
NLAS4599DFT2	NL	AS	DF	T2	SC-88	3000 / Tape & Reel
NLAS4599DFT2G	NL	AS	DF	T2G	SC-88 (Pb-Free)	3000 / Tape & Reel
NLAS4599DTT1	NL	AS	DT	T1	TSOP-6	3000 / Tape & Reel
NLAS4599DTT1G	NL	AS	DT	T1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel
NLVAS4599DFT2	NL	AS	DF	T2	SC-88	3000 / Tape & Reel
NLVAS4599DFT2G	NL	AS	DF	T2G	SC-88 (Pb-Free)	3000 / Tape & Reel
NLVAS4599DTT1G	NL	AS	DT	T1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



TSOP-6 CASE 318G-02 **ISSUE V**

12

C SEATING PLANE

DATE 12 JUN 2012

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM
- LEAD THIORNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D
- AND E1 ARE DETERMINED AT DATUM H.
 PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS					
DIM	MIN	NOM	MAX			
Α	0.90	1.00	1.10			
A1	0.01	0.06	0.10			
b	0.25	0.38	0.50			
С	0.10	0.18	0.26			
D	2.90	3.00	3.10			
Е	2.50	2.75	3.00			
E1	1.30	1.50	1.70			
е	0.85	0.95	1.05			
Ĺ	0.20 0.40 0.60					
L2	0.25 BSC					
М	00 100					

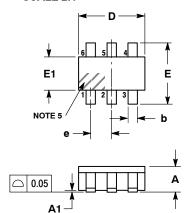
STYLE 5: PIN 1. EMITTER 2 2. BASE 2

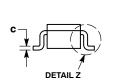
BASE 1

COLLECTOR 1 EMITTER 1

COLLECTOR 2

3.





DETAIL Z

Н

TYLE 1:	STYLE 2:
PIN 1. DRAIN	PIN 1. EMITTER 2
2. DRAIN	2. BASE 1
3. GATE	3. COLLECTOR 1
4. SOURCE	4. EMITTER 1
5. DRAIN	5. BASE 2
6. DRAIN	6. COLLECTOR 2
TYLE 7: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. N/C	

COLLECTOR

6. EMITTER

2. SOURCE 2

DRAIN 2

DRAIN 1

3. GATE 2

STYLE 13: PIN 1. GATE 1

5. SOURCE 1

S

S

3. D(in)+ 4. D(out)+ 5. D(out) 6. GND



STYLE 15: PIN 1. ANODE SOURCE 3. GATE DRAIN

STYLE 3: PIN 1. ENABLE 2. N/C

6. V out

5. V in

3. R BOOST 4. Vz

5. N/C 6. CATHODE



STYLE 16: PIN 1. ANODE/CATHODE

COLLECTOR

CATHODE

3 FMITTER

2. BASE

5. ANODE

6. LOAD	6
STYLE 10: PIN 1. D(OUT)+ 2. GND 3. D(OUT)- 4. D(IN)- 5. VBUS 6. D(IN)+	STYLE PIN 1 2 3 4 5 6

SOURCE 1 DRAIN 2 SOURCE 2 5. GATE 1 6. DRAIN 1/GATE 2

STYLE 17: PIN 1. EMITTER

2. BASE

STYLE 12: 2. GROUND 3. I/O 4. I/O 6. I/O

STYLE 6: PIN 1. COLLECTOR 2. COLLECTOR

3. BASE 4. EMITTER

5. COLLECTOR 6. COLLECTOR

CATHODE/DRAIN **RECOMMENDED SOLDERING FOOTPRINT***

CATHODE/DRAIN

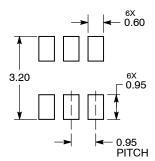
CATHODE/DRAIN

STYLE 14: PIN 1. ANODE

5.

3 GATE

SOURCE



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*

M

for actual part marking. Pb-Free indicator, "G" or microdot '

3 ANODE/CATHODE

CATHODE

COLLECTOR





XXX = Specific Device Code

= Pb-Free Package

= Date Code

XXX = Specific Device Code Α =Assembly Location

", may or may not be present.

Υ = Year

W = Work Week = Pb-Free Package

*This information is generic. Please refer to device data sheet

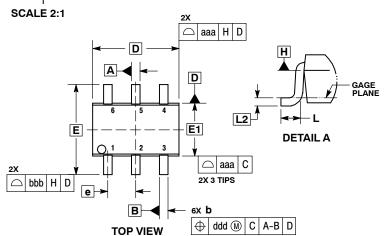
DOCUMENT NUMBER:	98ASB14888C	Electronic versions are uncontrolled except when accessed directly from the Document Repository Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.		
DESCRIPTION:	TSOP-6		PAGE 1 OF 1	

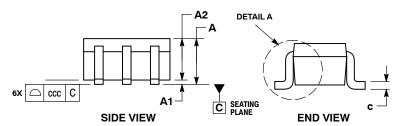
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^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SC-88/SC70-6/SOT-363 CASE 419B-02 **ISSUE Y**

DATE 11 DEC 2012





NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS
- CONTROLLING DIMENSION: MILLIMETERS.
 DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH,
- DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H. DATUMS A AND B ARE DETERMINED AT DATUM H. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.

- DIMENSION & DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION 6 AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

				_		
	MIL	LIMETE	ERS	INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α			1.10			0.043
A1	0.00		0.10	0.000		0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
С	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
е	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

MARKING DIAGRAM*



GENERIC

XXX = Specific Device Code

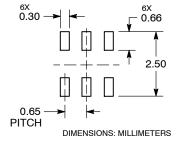
= Date Code*

= Pb-Free Package

(Note: Microdot may be in either location)

- *Date Code orientation and/or position may vary depending upon manufacturing location.
- *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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DATE 11 DEC 2012

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. I OUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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