## NLAS4599

## Low Voltage Single Supply SPDT Analog Switch

The NLAS4599 is an advanced high speed CMOS single pole double throw analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining low power dissipation. This switch controls analog and digital voltages that may vary across the full power-supply range (from $\mathrm{V}_{\mathrm{CC}}$ to GND).

The device has been designed so the ON resistance $\left(\mathrm{R}_{\mathrm{ON}}\right)$ is much lower and more linear over input voltage than $\mathrm{R}_{\mathrm{ON}}$ of typical CMOS analog switches.

The channel select input is compatible with standard CMOS outputs.
The channel select input structure provides protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. This input structure helps prevent device destruction caused by supply voltage - input/output voltage mismatch, battery backup, hot insertion, etc.

- Channel Select Input Over-Voltage Tolerant to 5.5 V
- Fast Switching and Propagation Speeds
- Break-Before-Make Circuitry
- Low Power Dissipation: $\mathrm{I}_{\mathrm{CC}}=2 \mu \mathrm{~A}$ (Max) at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$
- Diode Protection Provided on Channel Select Input
- Improved Linearity and Lower ON Resistance over Input Voltage
- Latch-up Performance Exceeds 300 mA
- ESD Performance: Human Body Model > 2000 V;

Machine Model > 200 V

- Chip Complexity: 38 FETs
- $\mathrm{Pb}-$ Free Packages are Available


FUNCTION TABLE

| Select | ON Channel |
| :---: | :---: |
| L | NC |
| H | NO |

Figure 1. Pin Assignment


Figure 2. Logic Symbol

[^0]ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
| :---: | :---: | :---: | :---: |
| $V_{\text {CC }}$ | Positive DC Supply Voltage | -0.5 to +7.0 | V |
| $\mathrm{V}_{\text {IS }}$ | Analog Input Voltage ( $\mathrm{V}_{\mathrm{NO}}$ or $\mathrm{V}_{\text {com }}$ ) | $-0.5 \leq \mathrm{V}_{\text {IS }} \leq \mathrm{V}_{\text {CC }}+0.5$ | V |
| $\mathrm{V}_{\mathrm{IN}}$ | Digital Select Input Voltage | $-0.5 \leq \mathrm{V}_{1} \leq+7.0$ | V |
| $\mathrm{I}_{\mathrm{K}}$ | DC Current, Into or Out of Any Pin | $\pm 50$ | mA |
| $\mathrm{P}_{\mathrm{D}}$ | Power Dissipation in Still Air $\begin{array}{r}\text { SC-88 } \\ \text { TSOP-6 }\end{array}$ | $\begin{aligned} & 200 \\ & 200 \end{aligned}$ | mW |
| TSTG | Storage Temperature Range | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathrm{L}}$ | Lead Temperature, 1 mm from Case for 10 seconds | 260 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathrm{J}}$ | Junction Temperature Under Bias | 150 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{V}_{\text {ESD }}$ | ESD Withstand Voltage Human Body Model (Note 1) <br> Machine Model (Note 2) <br> Charged Device Model (Note 3) | $\begin{gathered} 2000 \\ 200 \\ \text { N/A } \end{gathered}$ | V |
| ILATCH-UP | Latch-Up Performance $\quad$ Above V ${ }_{\text {CC }}$ and Below GND at 125 ${ }^{\circ} \mathrm{C}$ (Note 4) | $\pm 300$ | mA |
| $\theta_{\text {JA }}$ | Thermal Resistance $\begin{array}{r}\text { SC-88 } \\ \text { TSOP-6 }\end{array}$ | $\begin{aligned} & 333 \\ & 333 \end{aligned}$ | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22-A114-A
2. Tested to EIA/JESD22-A115-A
3. Tested to JESD22-C101-A
4. Tested to EIA/JESD78

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Characteristics |  | Min | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | DC Supply Voltage |  | 2.0 | 5.5 | V |
| $\mathrm{V}_{\text {IN }}$ | Digital Select Input Voltage |  | GND | 5.5 | V |
| $\mathrm{V}_{\text {IS }}$ | Analog Input Voltage (NC, NO, COM) |  | GND | $\mathrm{V}_{\mathrm{CC}}$ | V |
| $\mathrm{T}_{\mathrm{A}}$ | Operating Temperature Range |  | -55 | +125 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{t}_{\mathrm{r}}, \mathrm{t}_{\mathrm{f}}$ | Input Rise or Fall Time, SELECT | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=3.3 \mathrm{~V} \pm 0.3 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V} \pm 0.5 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 100 \\ & 20 \end{aligned}$ | ns/V |

## DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1\% BOND FAILURES

| Junction <br> Temperature ${ }^{\circ} \mathbf{C}$ | Time, Hours | Time, Years |
| :---: | :---: | :---: |
| 80 | $1,032,200$ | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |



Figure 3. Failure Rate vs. Time Junction Temperature

DC CHARACTERISTICS - Digital Section (Voltages Referenced to GND)

| Symbol | Parameter | Condition | $\mathrm{V}_{\mathrm{cc}}$ | Guaranteed Limit |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | -55 to $25^{\circ} \mathrm{C}$ | $<85{ }^{\circ} \mathrm{C}$ | $<125^{\circ} \mathrm{C}$ |  |
| $\mathrm{V}_{\mathrm{IH}}$ | Minimum High-Level Input Voltage, Select Input |  | $\begin{aligned} & 2.0 \\ & 2.5 \\ & 3.0 \\ & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{gathered} \hline 1.5 \\ 1.9 \\ 2.1 \\ 3.15 \\ 3.85 \end{gathered}$ | $\begin{gathered} 1.5 \\ 1.9 \\ 2.1 \\ 3.15 \\ 3.85 \end{gathered}$ | $\begin{gathered} \hline 1.5 \\ 1.9 \\ 2.1 \\ 3.15 \\ 3.85 \end{gathered}$ | V |
| VIL | Maximum Low-Level Input Voltage, Select Input |  | $\begin{aligned} & 2.0 \\ & 2.5 \\ & 3.0 \\ & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{gathered} \hline 0.5 \\ 0.6 \\ 0.9 \\ 1.35 \\ 1.65 \end{gathered}$ | $\begin{gathered} \hline 0.5 \\ 0.6 \\ 0.9 \\ 1.35 \\ 1.65 \end{gathered}$ | $\begin{gathered} \hline 0.5 \\ 0.6 \\ 0.9 \\ 1.35 \\ 1.65 \end{gathered}$ | V |
| $\mathrm{I}_{\mathrm{N}}$ | Maximum Input Leakage Current, Select Input | $\mathrm{V}_{\mathrm{IN}}=5.5 \mathrm{~V}$ or GND | 5.5 | $\pm 0.1$ | $\pm 1.0$ | $\pm 1.0$ | $\mu \mathrm{A}$ |
| IOFF | Power Off Leakage Current | $\mathrm{V}_{\mathrm{IN}}=5.5 \mathrm{~V}$ or GND | 0 | $\pm 10$ | $\pm 10$ | $\pm 10$ | $\mu \mathrm{A}$ |
| $\mathrm{I} C \mathrm{C}$ | Maximum Quiescent Supply Current | Select and $\mathrm{V}_{\text {IS }}=\mathrm{V}_{\text {CC }}$ or GND | 5.5 | 1.0 | 1.0 | 2.0 | $\mu \mathrm{A}$ |

## DC ELECTRICAL CHARACTERISTICS - Analog Section

| Symbol | Parameter | Condition | $\mathrm{V}_{\mathrm{cc}}$ | Guaranteed Limit |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | -55 to $25^{\circ} \mathrm{C}$ | $<85^{\circ} \mathrm{C}$ | $<125^{\circ} \mathrm{C}$ |  |
| $\mathrm{R}_{\text {ON }}$ | Maximum "ON" <br> Resistance <br> (Figures 17-23) | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{IS}}=\mathrm{GND} \text { to } \mathrm{V}_{\mathrm{CC}} \\ & \mathrm{I}_{\mathrm{IN}} \leq 10.0 \mathrm{~mA} \end{aligned}$ | $\begin{aligned} & 2.5 \\ & 3.0 \\ & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & 85 \\ & 45 \\ & 30 \\ & 25 \end{aligned}$ | $\begin{aligned} & 95 \\ & 50 \\ & 35 \\ & 30 \end{aligned}$ | $\begin{aligned} & 105 \\ & 55 \\ & 40 \\ & 35 \end{aligned}$ | $\Omega$ |
| $\mathrm{R}_{\text {FLAT }}$ (ON) | ON Resistance Flatness <br> (Figures 17 - 23) | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{IIN}^{\mathrm{IN}} \leq 10.0 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{IS}}=1 \mathrm{~V}, 2 \mathrm{~V}, 3.5 \mathrm{~V} \end{aligned}$ | 4.5 | 4 | 4 | 5 | $\Omega$ |
| $\Delta R_{\text {ON }}$ <br> (ON) | ON Resistance Match Between Channels | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{I}_{\mathrm{IN}} \leq 10.0 \mathrm{~mA} \\ & \mathrm{~V}_{\mathrm{NO}} \text { or } \mathrm{V}_{\mathrm{NC}}=3.5 \mathrm{~V} \end{aligned}$ | 4.5 | 2 | 2 | 3 | $\Omega$ |
| $\mathrm{I}_{\mathrm{NC}(\mathrm{OFF})}$ $\mathrm{I}_{\mathrm{NO}(\mathrm{OFF})}$ | NO or NC Off Leakage Current (Figure 9) | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{NO}} \text { or } \mathrm{V}_{\mathrm{NC}}=1.0 \mathrm{~V}_{\mathrm{COM}} 4.5 \mathrm{~V} \end{aligned}$ | 5.5 | 1 | 10 | 100 | nA |
| $\mathrm{I}_{\mathrm{COM}(\mathrm{ON}}$ <br> ) | COM ON Leakage Current (Figure 9) | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{NO}} 1.0 \mathrm{~V} \text { or } 4.5 \mathrm{~V} \text { with } \mathrm{V}_{\mathrm{NC}} \\ & \text { floating or } \\ & \mathrm{V}_{\mathrm{NO}} 1.0 \mathrm{~V} \text { or } 4.5 \mathrm{~V} \text { with } \mathrm{V}_{\mathrm{NO}} \\ & \text { floating } \\ & \mathrm{V}_{\mathrm{COM}}=1.0 \mathrm{~V} \text { or } 4.5 \mathrm{~V} \end{aligned}$ | 5.5 | 1 | 10 | 100 | nA |

AC ELECTRICAL CHARACTERISTICS (Input $\mathrm{t}_{\mathrm{r}}=\mathrm{t}_{\mathrm{f}}=3.0 \mathrm{~ns}$ )

| Symbol | Parameter | Test Conditions | $\mathrm{V}_{\mathrm{cc}}$ <br> (V) | $\mathrm{V}_{\text {IS }}$ <br> (V) | Guaranteed Max Limit |  |  |  |  | $<125^{\circ} \mathrm{C}$ |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | -55 to $25^{\circ} \mathrm{C}$ |  |  | $<85^{\circ} \mathrm{C}$ |  |  |  |  |
|  |  |  |  |  | Min | Typ* | Max | Min | Max | Min | Max |  |
| ton | Turn-On Time <br> (Figures 12 and 13) | $\mathrm{R}_{\mathrm{L}}=300 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF}$ <br> (Figures 5 and 6) | $\begin{aligned} & \hline 2.5 \\ & 3.0 \\ & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 2.0 \\ & 3.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 5 \\ & 5 \\ & 2 \\ & 2 \end{aligned}$ | $\begin{gathered} \hline 23 \\ 16 \\ 11 \\ 9 \end{gathered}$ | $\begin{aligned} & 28 \\ & 21 \\ & 16 \\ & 14 \end{aligned}$ | $\begin{aligned} & 5 \\ & 5 \\ & 2 \\ & 2 \end{aligned}$ | $\begin{aligned} & 30 \\ & 25 \\ & 20 \\ & 20 \end{aligned}$ | $\begin{aligned} & 5 \\ & 5 \\ & 2 \\ & 2 \end{aligned}$ | $\begin{aligned} & 30 \\ & 25 \\ & 20 \\ & 20 \end{aligned}$ | ns |
| tofF | Turn-Off Time (Figures 12 and 13) | $\mathrm{R}_{\mathrm{L}}=300 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF}$ <br> (Figures 5 and 6) | $\begin{aligned} & \hline 2.5 \\ & 3.0 \\ & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & \hline 2.0 \\ & 2.0 \\ & 3.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & \hline 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & \hline 7 \\ & 5 \\ & 4 \\ & 3 \end{aligned}$ | $\begin{gathered} \hline 12 \\ 10 \\ 9 \\ 8 \end{gathered}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 15 \\ & 15 \\ & 12 \\ & 12 \end{aligned}$ | $\begin{aligned} & \hline 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 15 \\ & 15 \\ & 12 \\ & 12 \end{aligned}$ | ns |
| $\mathrm{t}_{\text {BBM }}$ | Minimum <br> Break-Before-Make Time | $\begin{aligned} & \mathrm{V}_{\mathrm{IS}}=3.0 \mathrm{~V} \text { (Figure 4) } \\ & \mathrm{R}_{\mathrm{L}}=300 \Omega, \mathrm{C}_{\mathrm{L}}=35 \mathrm{pF} \end{aligned}$ | $\begin{aligned} & \hline 2.5 \\ & 3.0 \\ & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & \hline 2.0 \\ & 2.0 \\ & 3.0 \\ & 3.0 \end{aligned}$ | 1 1 1 1 | $\begin{gathered} \hline 12 \\ 11 \\ 6 \\ 5 \end{gathered}$ |  | 1 1 1 1 |  | 1 1 1 1 |  | ns |

*Typical Characteristics are at $25^{\circ} \mathrm{C}$.

|  |  | Typical @ 25, VCC = 5.0 V |  |
| :--- | :--- | :---: | :---: |
| $\mathrm{C}_{\mathrm{IN}}$ | Maximum Input Capacitance, Select Input | 8 | pF |
| $\mathrm{C}_{\mathrm{NO}}$ or $\mathrm{C}_{\mathrm{NC}}$ | Analog I/O (switch off) | 10 |  |
| $\mathrm{C}_{\mathrm{COM}}$ | Common I/O (switch off) | 10 |  |
| $\mathrm{C}_{(\mathrm{ON})}$ | Feedthrough (switch on) | 20 |  |

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

| Symbol | Parameter | Condition | $\mathrm{V}_{\mathrm{cc}}$ <br> (V) | Typical | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | $25^{\circ} \mathrm{C}$ |  |
| BW | Maximum On-Channel -3dB Bandwidth or Minimum Frequency Response (Figure 10) | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{dBm}$ <br> $\mathrm{V}_{\text {IN }}$ centered between $\mathrm{V}_{\mathrm{CC}}$ and GND <br> (Figure 7) | $\begin{aligned} & 3.0 \\ & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & \hline 170 \\ & 200 \\ & 200 \end{aligned}$ | MHz |
| V ${ }_{\text {ONL }}$ | Maximum Feedthrough On Loss | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{dBm}$ @ 100 kHz to 50 MHz <br> $\mathrm{V}_{\mathrm{IN}}$ centered between $\mathrm{V}_{\mathrm{CC}}$ and GND <br> (Figure 7) | $\begin{aligned} & 3.0 \\ & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & \hline-3 \\ & -3 \\ & -3 \end{aligned}$ | dB |
| VISO | Off-Channel Isolation (Figure 10) | $\mathrm{f}=100 \mathrm{kHz} ; \mathrm{V}_{\mathrm{IS}}=1 \mathrm{VRMS}$ <br> $\mathrm{V}_{\text {IN }}$ centered between $\mathrm{V}_{\mathrm{CC}}$ and GND <br> (Figure 7) | $\begin{aligned} & 3.0 \\ & 4.5 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & \hline-93 \\ & -93 \\ & -93 \end{aligned}$ | dB |
| Q | Charge Injection Select Input to Common I/O <br> (Figure 15) | $\begin{aligned} & \hline \mathrm{V}_{I N}=\mathrm{V}_{\mathrm{CC}} \text { to } \mathrm{GND}, \mathrm{~F}_{I S}=20 \mathrm{kHz} \\ & \mathrm{t}_{\mathrm{r}}==_{\mathrm{f}}=3 \mathrm{nS} \\ & \mathrm{R}_{I S}=0 \Omega, \mathrm{C}_{\mathrm{L}}=1000 \mathrm{pF} \\ & \mathrm{Q}=\mathrm{C}_{\mathrm{L}}{ }^{*} \Delta \mathrm{~V}_{\text {OUT }} \\ & \text { (Figure 8) } \end{aligned}$ | $\begin{aligned} & 3.0 \\ & 5.5 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 3.0 \end{aligned}$ | pC |
| THD | Total Harmonic Distortion THD + Noise (Figure 14) | $\begin{aligned} & \mathrm{F}_{\text {IS }}=20 \mathrm{~Hz} \text { to } 100 \mathrm{kHz}, \mathrm{R}_{\mathrm{L}}=\mathrm{Rgen}=600 \Omega, \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \\ & \mathrm{~V}_{\mathrm{IS}}=5.0 \mathrm{~V}_{\mathrm{PP}} \text { sine wave } \end{aligned}$ | 5.5 | 0.1 | \% |



Figure 4. $\mathrm{t}_{\mathrm{BBM}}$ (Time Break-Before-Make)


Figure 5. $\mathrm{t}_{\mathrm{ON}} / \mathrm{t}_{\mathrm{OFF}}$


Figure 6. $\mathrm{t}_{\mathrm{ON}} / \mathrm{t}_{\mathrm{OFF}}$


Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. $\mathrm{V}_{\text {ISO }}$, Bandwidth and $\mathrm{V}_{\text {ONL }}$ are independent of the input signal direction.
$\mathrm{V}_{\text {ISO }}=$ Off Channel Isolation $=20 \log \left(\frac{\mathrm{VOUT}}{\mathrm{V}_{\text {IN }}}\right)$ for $\mathrm{V}_{\text {IN }}$ at 100 kHz
$\mathrm{V}_{\text {ONL }}=$ On Channel Loss $=20$ Log $\left(\frac{\mathrm{V}_{\text {OUT }}}{\mathrm{V}_{\text {IN }}}\right)$ for $\mathrm{V}_{\text {IN }}$ at 100 kHz to 50 MHz
Bandwidth $(B W)=$ the frequency 3 dB below $\mathrm{V}_{\mathrm{ONL}}$
Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/V ${ }_{\text {ONL }}$


Figure 8. Charge Injection: (Q)


Figure 9. Switch Leakage vs. Temperature


Figure 10. Bandwidth and Off-Channel Isolation


Figure 12. $\mathrm{t}_{\mathrm{ON}}$ and $\mathrm{t}_{\mathrm{OFF}}$ vs. $\mathrm{V}_{\mathrm{CC}}$ at $25^{\circ} \mathrm{C}$


Figure 14. Total Harmonic Distortion Plus Noise vs. Frequency


Figure 11. Phase vs. Frequency


Figure 13. $\mathrm{t}_{\mathrm{ON}}$ and $\mathrm{t}_{\mathrm{OFF}}$ vs. Temp


Figure 15. Charge Injection vs. COM Voltage


Figure 16. $\mathrm{I}_{\mathrm{Cc}}$ vs. Temp, $\mathrm{V}_{\mathrm{cc}}=3 \mathrm{~V}$ \& 5 V


Figure 18. $\mathrm{R}_{\mathrm{ON}} \mathrm{vs}$ Temp, $\mathrm{V}_{\mathrm{Cc}}=2.0 \mathrm{~V}$


Figure 20. R $_{\mathrm{ON}}$ vs. Temp, $\mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}$


Figure 17. $\mathrm{R}_{\mathrm{ON}}$ vs. $\mathrm{V}_{\mathrm{CC}}$, $\mathrm{Temp}=\mathbf{2 5}^{\circ} \mathrm{C}$


Figure 19. $\mathrm{R}_{\mathrm{ON}}$ vs. $\mathrm{Temp}^{\mathrm{V}} \mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}$


Figure 21. $\mathrm{R}_{\mathrm{ON}} \mathrm{vs}$. Temp, $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$

NLAS4599


Figure 22. Ron vs. Temp, $\mathrm{V}_{\mathrm{Cc}}=5.0 \mathrm{~V}$


Figure 23. Ron vs. Temp, $\mathrm{V}_{\mathrm{Cc}}=5.5 \mathrm{~V}$

ORDERING INFORMATION

| Device | Device Nomenclature |  |  |  | Package | Shipping ${ }^{\dagger}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Circuit Indicator | Technology | Device Function | Suffix |  |  |
| NLAS4599DFT2 | NL | AS | DF | T2 | SC-88 | 3000 / Tape \& Reel |
| NLAS4599DFT2G | NL | AS | DF | T2G | $\begin{gathered} \text { SC-88 } \\ \text { (Pb-Free) } \end{gathered}$ | 3000 / Tape \& Reel |
| NLAS4599DTT1 | NL | AS | DT | T1 | TSOP-6 | 3000 / Tape \& Reel |
| NLAS4599DTT1G | NL | AS | DT | T1G | TSOP-6 ( $\mathrm{Pb}-\mathrm{Free}$ ) | 3000 / Tape \& Reel |
| NLVAS4599DFT2 | NL | AS | DF | T2 | SC-88 | 3000 / Tape \& Reel |
| NLVAS4599DFT2G | NL | AS | DF | T2G | $\begin{gathered} \text { SC-88 } \\ \text { (Pb-Free) } \end{gathered}$ | 3000 / Tape \& Reel |
| NLVAS4599DTT1G | NL | AS | DT | T1G | TSOP-6 <br> ( $\mathrm{Pb}-\mathrm{Free}$ ) | 3000 / Tape \& Reel |

$\dagger$ For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. 2. CONTROLLING DIMENSION: MILLIMETERS.
2. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H
4. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

| DIM | MILLIMETERS |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | NOM | MAX |  |  |
| A | 0.90 | 1.00 | 1.10 |  |  |
| A1 | 0.01 | 0.06 | 0.10 |  |  |
| b | 0.25 | 0.38 | 0.50 |  |  |
| c | 0.10 | 0.18 | 0.26 |  |  |
| D | 2.90 | 3.00 | 3.10 |  |  |
| E | 2.50 | 2.75 | 3.00 |  |  |
| E1 | 1.30 | 1.50 | 1.70 |  |  |
| e | 0.85 | 0.95 | 1.05 |  |  |
| L | 0.20 | 0.40 |  |  | 0.60 |
| L2 | 0.25 BSC |  |  |  |  |
| M | $0^{\circ}$ | - |  |  |  |

STYLE 1
STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR
3. COLLECTOR
4. EMITTER
5. BASE 2
6. COLLECTOR 2

## STYLE 7:

PIN 1. COLLECTOR
STYLE 8:
2. COLLECTOR
3. BASE
4. N/C
. COLLECTOR
N 1. Vbus
2. $D(i n)$
3. $D(i n)+$
4. D(out)+
5. D(out)
6. GND

## STYLE 13:

PIN 1. GATE 1
2. SOURCE
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14 :
PIN 1. ANODE
2. SOURCE 3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN 6. CATHODE/DRAIN


STYLE 3:
PIN 1. ENABLE
2. $N / C$
3. R BOOST
4. Vz
5. $V$ in
6. Vout

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 4: PIN 1. N/C

> 1. $\mathrm{V} / \mathrm{C}$ 3. NOT USED 4. GROUND
. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 4. EMITTER 5. BASE 1 6. COLLECTOR 2

## STYLE 10

PIN 1. D(OUT)+
STYLE 11
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

6. $\mathrm{D}(\mathrm{IN})+$

STYLE 6:
PIN 1. COLLECTOR 2. COLLECTOR 2. COLLE 3. BASE 4. EMITTER 5. COLLECTOR
6. COLLECTOR

STYLE 12:
PIN 1. I/O
2. GROUND
3. $1 / \mathrm{O}$ 4. I/O 5. VCC 6. I/O

STYLE 15: STYLE 16:
STYLE 17:
PIN 1. ANODE
2. SOURCE 3. GATE PIN 1. ANODE/CATHODE

PIN 1. EMITTER 2. BASE
2. BASE
4. DRAIN 4 4. COLLECTOR
4. COLLECTOR 4. ANODE
5. N/C 5. ANODE
$\begin{array}{lll}\text { 6. CATHODE } & \text { 5. ANODE } & \text { 6. CATHODE }\end{array}$
5. CATHODE

## RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS
*For additional information on our $\mathrm{Pb}-$ Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*


IC
XXX = Specific Device Code
A =Assembly Location
Y = Year
W = Work Week

- = Pb-Free Package
*This information is generic. Please refer to device data sheet for actual part marking. $\mathrm{Pb}-F r e e$ indicator, " G " or microdot " -", may or may not be present.

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RECOMMENDED SOLDERING FOOTPRINT*

*For additional information on our Pb -Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. 2. CONTROLLING DIMENSION: MILLIMETERS.
2. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
3. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF DIMENSIONS D AND E1 AT THE OUT
THE PLASTIC BODY AND DATUM H.
THE PLASTIC BODY AND DATUMIN.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE DIMENSIONS b AND c APPLY TO THE FLAT SEC
LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

| DIM | MILLIMETERS |  |  | INCHES |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | --- | 1.10 | --- | --- | 0.043 |
| A1 | 0.00 | -- | 0.10 | 0.000 | -- | 0.004 |
| A2 | 0.70 | 0.90 | 1.00 | 0.027 | 0.035 | 0.039 |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| C | 0.08 | 0.15 | 0.22 | 0.003 | 0.006 | 0.009 |
| D | 1.80 | 2.00 | 2.20 | 0.070 | 0.078 | 0.086 |
| E | 2.00 | 2.10 | 2.20 | 0.078 | 0.082 | 0.086 |
| E1 | 1.15 | 1.25 | 1.35 | 0.045 | 0.049 | 0.053 |
| e | 0.65 BSC |  |  | 0.026 BSC |  |  |
| L | 0.26 | 0.36 | 0.46 | 0.010 | 0.014 | 0.018 |
| L2 | 0.15 BSC |  |  | 0.006 BSC |  |  |
| aaa | 0.15 |  |  | 0.006 |  |  |
| bbb | 0.30 |  |  | 0.012 |  |  |
| ccc | 0.10 |  |  | 0.004 |  |  |
| ddd | 0.10 |  |  | 0.004 |  |  |
|  | GENERIC |  |  |  |  |  |
|  | MARKING DIAGRAM* |  |  |  |  |  |



XXX = Specific Device Code
M = Date Code*

- = Pb-Free Package
(Note: Microdot may be in either location)
*Date Code orientation and/or position may vary depending upon manufacturing location.
*This information is generic. Please refer to device data sheet for actual part marking. $\mathrm{Pb}-F r e e$ indicator, " G " or microdot " r ", may or may not be present. Some products may not follow the Generic Marking.


## STYLES ON PAGE 2

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| DESCRIPTION: | SC-88/SC70-6/SOT-363 | PAGE 1 OF 2 |

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## SC-88/SC70-6/SOT-363

CASE 419B-02
ISSUE Y
STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 19:
PIN 1. IOUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF
STYLE $25:$
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1
STYLE 2:
CANCELLED

STYLE 8:
CANCELLED

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR
STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

| STYLE $3:$ <br> CANCELLED | STYLE 4: <br> PIN 1. CATHODE <br> 2. CATHODE <br> 3. COLLECTOR <br> 4. EMITTER <br> 5. BASE <br> 6. ANODE | STYLE 5: <br> PIN 1. ANODE <br> 2. ANODE <br> 3. COLLECTOR <br> 4. EMITTER <br> 5. BASE <br> 6. CATHODE | STYLE 6: <br> PIN 1. ANODE 2 <br> 2. $\mathrm{N} / \mathrm{C}$ <br> 3. CATHODE 1 <br> 4. ANODE 1 <br> 5. N/C <br> 6. CATHODE 2 |
| :---: | :---: | :---: | :---: |
| STYLE 9: | STYLE 10: | STYLE 11: | STYLE 12: |
| PIN 1. EMITTER 2 | PIN 1. SOURCE 2 | PIN 1. CATHODE 2 | PIN 1. ANODE 2 |
| 2. EMITTER 1 | 2. SOURCE 1 | 2. CATHODE 2 | 2. ANODE 2 |
| 3. COLLECTOR 1 | 3. GATE 1 | 3. ANODE 1 | 3. CATHODE 1 |
| 4. BASE 1 | 4. DRAIN 1 | 4. CATHODE 1 | 4. ANODE 1 |
| 5. BASE 2 | 5. DRAIN 2 | 5. CATHODE 1 | 5. ANODE 1 |
| 6. COLLECTOR 2 | 6. GATE 2 | 6. ANODE 2 | 6. CATHODE 2 |
| STYLE 15: | STYLE 16: | STYLE 17: | STYLE 18: |
| PIN 1. ANODE 1 | PIN 1. BASE 1 | PIN 1. BASE 1 | PIN 1. VIN1 |
| 2. ANODE 2 | 2. EMITTER 2 | 2. EMITTER 1 | 2. VCC |
| 3. ANODE 3 | 3. COLLECTOR 2 | 3. COLLECTOR 2 | 3. VOUT2 |
| 4. CATHODE 3 | 4. BASE 2 | 4. BASE 2 | 4. VIN2 |
| 5. CATHODE 2 | 5. EMITTER 1 | 5. EMITTER 2 | 5. GND |
| 6. CATHODE 1 | 6. COLLECTOR 1 | 6. COLLECTOR 1 | 6. VOUT1 |
| STYLE 21: | STYLE 22: | STYLE 23: | STYLE 24: |
| PIN 1. ANODE 1 | PIN 1. D1 (i) | PIN 1. Vn | PIN 1. CATHODE |
| 2. N/C | 2. GND | 2. CH 1 | 2. ANODE |
| 3. ANODE 2 | 3. D2 (i) | 3. Vp | 3. CATHODE |
| 4. CATHODE 2 | 4. D2 (c) | 4. N/C | 4. CATHODE |
| 5. N/C | 5. VBUS | 5. CH 2 | 5. CATHODE |
| 6. CATHODE 1 | 6. D1 (c) | 6. N/C | 6. CATHODE |
| STYLE 27: | STYLE 28: | STYLE 29: | STYLE 30: |
| PIN 1. BASE 2 | PIN 1. DRAIN | PIN 1. ANODE | PIN 1. SOURCE 1 |
| 2. BASE 1 | 2. DRAIN | 2. ANODE | 2. DRAIN 2 |
| 3. COLLECTOR 1 | 3. GATE | 3. COLLECTOR | 3. DRAIN 2 |
| 4. EMITTER 1 | 4. SOURCE | 4. EMITTER | 4. SOURCE 2 |
| 5. EMITTER 2 | 5. DRAIN | 5. BASE/ANODE | 5. GATE 1 |
| 6. COLLECTOR 2 | 6. DRAIN | 6. CATHODE | 6. DRAIN 1 |

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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