Title	***Reference Design Report for a 0.48 W Non-Isolated Power Supply With Lossless AC Zero-Crossing Detection Using LinkSwitch™-TNZ LNK3302D***
Specification	90 VAC – 305 VAC Input, 6 V, 80 mA Output
Application	Home and Building Automation
Author	Applications Engineering Department
Document Number	RDR-874
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Revision	1.1

Summary and Features

- Highly integrated solution with LNK3302D
- Low-component count with integrated 725 V power MOSFET, current sensing and protection
- Wide-range AC input
- <200 μA standby input current across AC line
- Zero-crossing signal output synchronized to AC line
- Meets EN550022 and CISPR-22 Class B conducted EMI
- Compact solution 1" x 1", 10 mm maximum height
- <20 mW no-load input power
- Load short-circuit protection

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a high-side buck converter designed to provide a nominal output voltage of 6 V at 80 mA load from a wide input voltage range of 90 VAC to 305 VAC, as well as a zero-crossing detection (ZCD) signal. This power supply utilizes the LNK3302D from the LinkSwitch-TNZ family of ICs.

This document contains the complete power supply specifications, bill of materials, transformer construction, circuit schematic and printed circuit board layout, along with performance data and electrical waveforms.

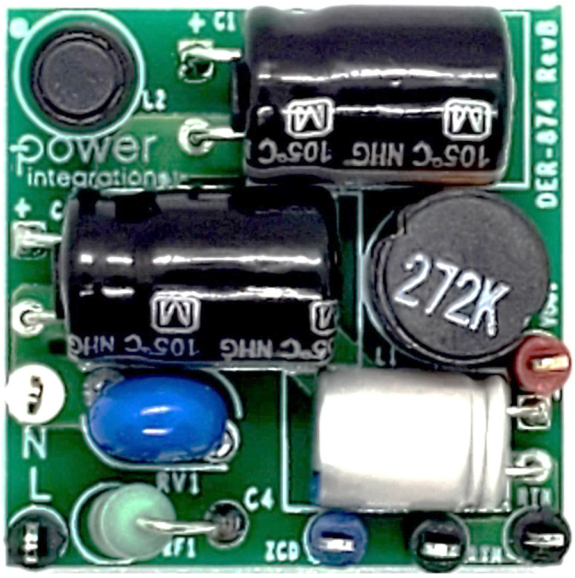

Figure 1 – Populated Circuit Board, Top View.

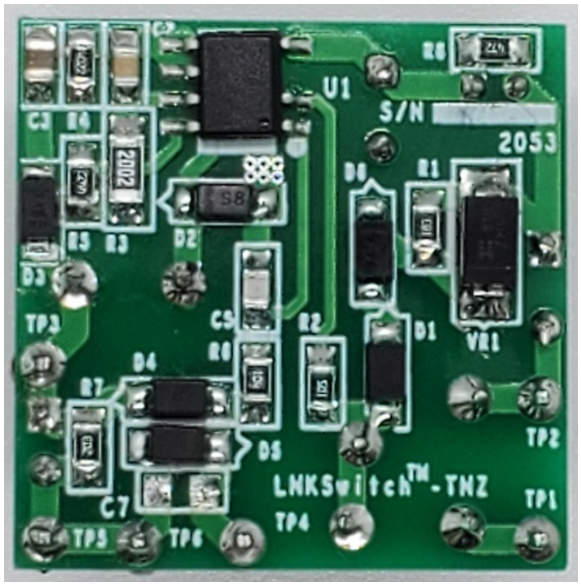

Figure 2 – Populated Circuit Board, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		305	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Current			150		μA	120 VAC.
			120		μA	230 VAC.
Output						
Output Voltage	V_{OUT}		6		V	± 5%.
Output Current	I_{OUT}		0.08		A	
Total Output Power						
Continuous Output Power	P_{OUT}		0.48		W	
Efficiency						
Full Load	η	60			%	Measured at P_{OUT} 25 °C.
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC 60950-1				
Surge			1		kV	1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Surge: 2 Ω
Ring Wave			2.5		kV	Ring Wave: 12 Ω

3 Schematic

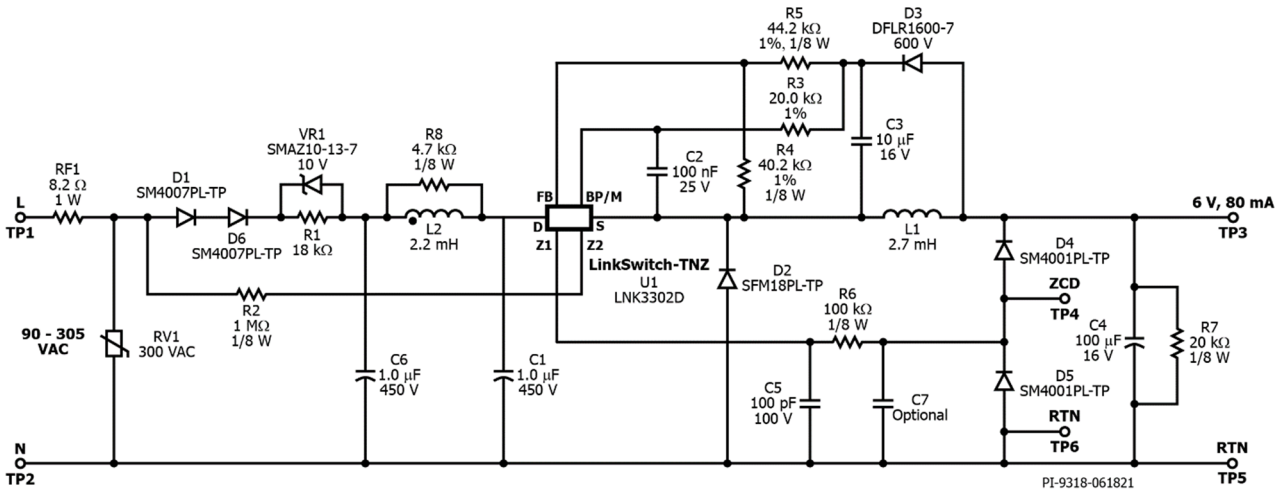

Figure 3 – Schematic.

4 Circuit Description

This circuit is configured as a high-side buck topology power supply utilizing the LNK3302D.

4.1 *Input Rectifier and Filter*

The AC input voltage is half-wave rectified by series-connected diodes D1 and D6. The added diode is needed to pass 2.5 kV ring-wave. The series connection is preferred instead of placing the other diode on the Neutral line to measure the zero-crossing signal properly.

The rectified DC is then filtered by the bulk storage capacitors C1 and C6. Inductor L2, C1 and C6 form an input pi filter, which attenuates differential mode conducted EMI. The damping resistor R8 reduces the Q factor of the inductor L2 to allow noise filtering more effective at wider bandwidth.

4.2 *Input Protection*

The fusible resistor RF1 provides safety protection against catastrophic circuit failures. It also reduces inrush current at startup. Varistor RV1 protects against surge events.

4.3 *Power Factor Circuit*

Power Integrations' RZ circuit, that is resistor R1 and Zener diode VR1, minimizes the no-load input current that is important in many 2-wire switch or dimmer applications. VR1 is rated 1W with a 10V clamping voltage. Higher Zener voltage may reduce no-load input current further, but it might cause higher power dissipation during surge. Resistor R1 is tuned either at no-load or at standby, whichever is applicable. The resistance is set such as its peak voltage is just below the Zener voltage. This yields the lowest input current.

4.4 *LNK3302 Power Supply Operation*

LinkSwitch-TNZ combines a high-voltage power MOSFET switch, a power supply controller, and a Zero Crossing Detector in a single device. Unlike conventional PWM (pulse width modulator) controllers, LinkSwitch-TNZ uses a simple ON/OFF control to regulate the output voltage. The LinkSwitch-TNZ controller consists of an oscillator, feedback (sense and logic) circuit, 5 V regulator, BYPASS pin undervoltage circuit, over-temperature protection, line and output overvoltage protection, frequency jittering, current limit circuit, leading edge blanking and a 725 V power MOSFET.

This design is configured as a high-side buck converter using U1 LNK3302. At AC start-up, the device starts switching once the BYPASS (BP/M) pin voltage charges to V_{BP}. A 100 nF capacitor C2 connected to BP sets the current limit to standard. Resistor R5 provides external bias to the BP/M pin and reduces the no-load input power by setting R5 to provide about 75 μA (I_{S1}) to the BYPASS pin.

When the MOSFET turns ON, current flows to the load via inductor L1. Energy is stored in the inductor, and the output capacitor C4 gets charged. When the MOSFET turns OFF, the stored energy from L1 is released to the load via free-wheeling diode D2. The charge

stored in C4 supplies the current until the next switching event occurs. Diode D2 must be an ultrafast diode with a reverse recovery time (trr) of 35 ns or less. This is because the converter operates in Continuous Conduction Mode (CCM).

4.5 *Feedback and Output Voltage Regulation*

In this high-side buck, direct feedback configuration, the rectified voltage across L1 via D3 and C3 tracks the output voltage. Resistors R3 and R4 divides the voltage such that the FB pin is set to 2 V. When the current delivered into this pin exceeds IFB (49 µA), a low logic level (disable) is generated at the output of the feedback circuit. This output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled), otherwise the power MOSFET remains off (disabled). The current limit circuit senses the current in the power MOSFET.
When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle.

Regulation is maintained by skipping switching cycles. As the output voltage rises, the current into the FEEDBACK pin will rise. If this exceeds I_{FB} then subsequent cycles will be skipped until the current reduces below I_{FB}. Thus, as the output load is reduced, more cycles will be skipped and if the load increases, fewer cycles are skipped.

A small pre-load R7 is required to limit the output voltage to about 110% of the rated voltage during light load or no-load condition.

4.6 *Zero-Crossing Detection*

Z1 and Z2 pins are configured to provide a loss-less (<5 mW) zero-crossing detection (ZCD) circuit. Z2 is connected to one of the input AC lines through resistor R2 while Z1 forms the ZCD signal output.

When the AC voltage is more positive with respect to Neutral, D4 is forward-biased and clamps ZCD output to V_{OUT} + 0.7 V. At the negative-going phase of the AC input, D5 is forward-biased and clamps ZCD output to -0.7 V.

The passive components comprised of R2, C5, R6, and optional C7 provide noise filtering to ensure clean ZCD signal. The values are chosen such that the overall ZCD delay is kept below 200 µs. C7 is a placeholder for the additional filter if needed. Diode D5 has capacitance that helps avoid adding the extra capacitor. However, too much capacitance will cause more delay.

5 PCB Layout

Number of layers:	2
PCB Board thickness:	1.59 mm / 0.062 inches
Material:	FR4
Copper thickness:	2 oz

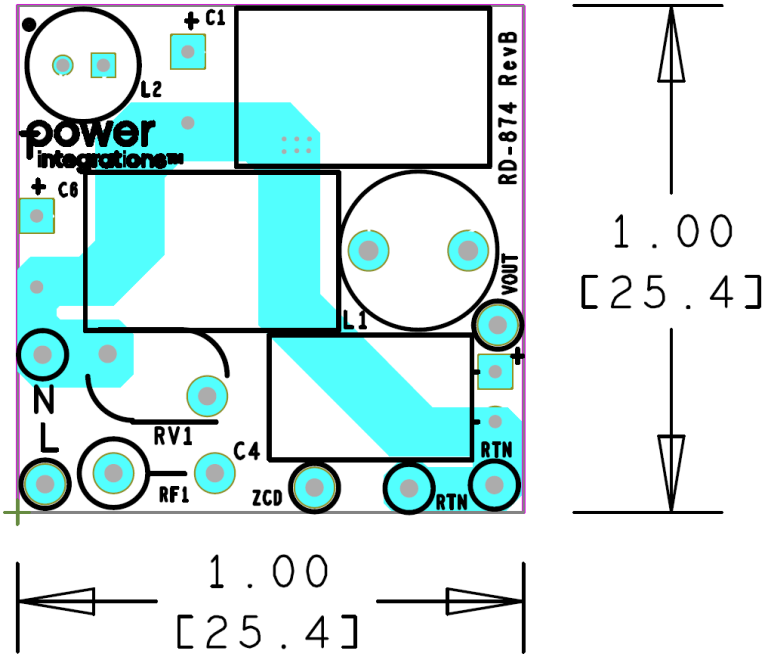

Figure 4 – Populated Circuit Board, Top View.

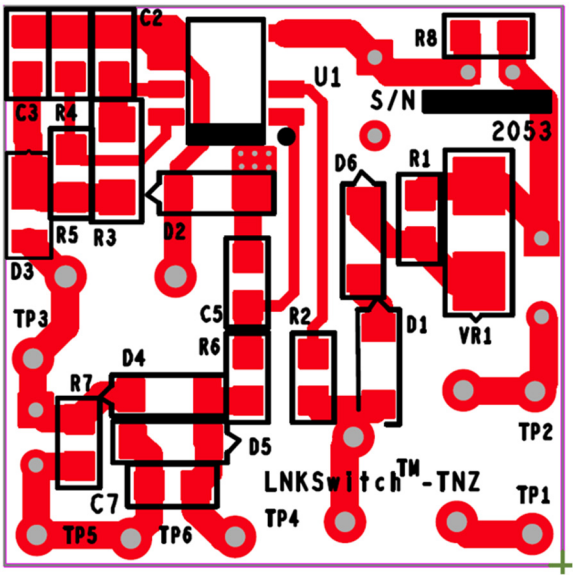

Figure 5 – Populated Circuit Board, Bottom View.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C1	1.0 μF, 450 V, Electrolytic, NHG, (8 x 11.5)	ECA-2WHG010	Panasonic
2	1	C2	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX
3	1	C3	10 μF, ±10%, 16 V, X7R, Ceramic, SMT, MLCC 0805	CL21B106KOQNNNE	Samsung
4	1	C4	100 μF, ±20%, 16 V, Electrolytic, Gen. Purpose, 2000 Hrs @ 105°C, (6.3 x 9)	A750EK107M1CAAE018	Nichicon
5	1	C5	100 pF, 100 V, Ceramic, COG, 0805	C0805C101J1GACTU	Kemet
6	1	C6	1.0 μF, 450 V, Electrolytic, NHG, (8 x 11.5)	ECA-2WHG010	Panasonic
7	1	D1	1000V, 1 A, Standard Recovery, SOD-123FL	SM4007PL-TP	Micro Commercial
8	1	D2	Diode, GEN PURP, 600 V, 1 A, SOD123FL, SOD-123F	SFM18PL-TP	Micro Commercial
9	1	D3	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
10	1	D4	Diode, GEN PURP, 50 V, 1 A, SOD-123F, SOD123FL	SM4001PL-TP	Micro Commercial
11	1	D5	Diode, GEN PURP, 50 V, 1 A, SOD-123F, SOD123FL	SM4001PL-TP	Micro Commercial
12	1	D6	1000 V, 1 A, Standard Recovery, SOD-123FL	SM4007PL-TP	Micro Commercial
13	1	L1	FIXED IND, 2.7 mH, 10%, Imax = 160 mA, 8Ω max, TH, UNSHIELDED	AIUR-10-272K	Abracon
14	1	L2	2.2 mH, 0.046 A, 20%	RL-5480-1-2200	Renco
15	1	R1	RES, 18 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ183V	Panasonic
16	1	R2	RES, 1.0 MΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ105V	Panasonic
17	1	R3	RES, 20.0 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2002V	Panasonic
18	1	R4	RES, 40.2 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4022V	Panasonic
19	1	R5	RES, 44.2 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4422V	Panasonic
20	1	R6	RES, 100 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
21	1	R7	RES, 20 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ203V	Panasonic
22	1	R8	RES, 4.7 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ472V	Panasonic
23	1	RF1	RES, 8.2 Ω, 1 W, 5%, Fusible/Flame Proof Wire Wound	FKN1WSJR-52-8R2	Yageo
24	1	RV1	300 Vac, 15 J, 5 mm, RADIAL	S05K300E2	Epcos
25	1	U1	LinkSwitch-TNZ, SO8	LNK3302D	Power Integrations
26	1	VR1	Diode, ZENER, 10 V, ±5%, 1 W, DO-214AC, SMA	SMAZ10-13-F	Diodes, Inc.

Mechanical Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	TP1	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
2	1	TP2	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
3	1	TP3	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
4	1	TP4	Test Point, BLUE, Miniature THRU-HOLE MOUNT	5117	Keystone
5	1	TP5	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
6	1	TP6	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone

7 Design Spreadsheet

1	ACDC_LinkSwitchTNZ_Buck_081420; Rev.0.1; Copyright Power Integrations 2020	INPUT	INFO	OUTPUT	UNIT	ACDC LinkSwitch-TNZ Buck
2	**ENTER APPLICATION VARIABLES**					
3	LINE VOLTAGE RANGE			Custom		AC line voltage range
4	VACMIN	90.00		90.00	V	Minimum AC line voltage
5	VACMAX	300.00	Info	300.00	V	The maximum AC line voltage is too high
6	fL			60.00	Hz	AC mains frequency
7	LINE RECTIFICATION TYPE	H		H		Line rectification type: select "F" if full wave rectification or "H" if half wave rectification
8	VOUT	6.00		6.00	V	Output voltage
9	IOUT	0.080		0.080	A	Average output current
10	EFFICIENCY_ESTIMATED	0.65		0.65		Efficiency estimate at output terminals
11	EFFICIENCY_CALCULATED			0.72		Calculated efficiency based on real components and operating point
12	POUT			0.48	W	Continuous output power
13	CIN	2.00		2.00	uF	Input capacitor
14	VMIN			76.1	V	Valley voltage of the rectified minimum AC line voltage
15	VMAX			424.3	V	Peak voltage of the maximum AC line voltage
16	INPUT STAGE RESISTANCE			10	Ohms	Input stage resistance in ohms (includes thermistor, filtering components, etc)
17	PLOSS_INPUTSTAGE			0.001	W	Maximum input stage loss
21	**ENTER LINKSWITCH-TNZ VARIABLES**					
22	OPERATION MODE			MCM		Mostly continuous mode of operation
23	CURRENT LIMIT MODE	STD		STD		Choose 'RED' for reduced current limit or 'STD' for standard current limit
24	PACKAGE			SO-8C		Select the device package
25	DEVICE SERIES	AUTO		LNK3302		Generic LinkSwitch-TNZ device
26	DEVICE CODE			LNK3302D		Required LinkSwitch-TNZ device
27	ILIMITMIN			0.126	A	Minimum current limit of the device
28	ILIMITTYP			0.136	A	Typical current limit of the device
29	ILIMITMAX			0.146	A	Maximum current limit of the device
30	RDSON			88.40	ohms	Primary switch on-time drain to source resistance at 100degC
31	FSMIN			62000	Hz	Minimum switching frequency
32	FSTYP			66000	Hz	Typical switching frequency
33	FSMAX			70000	Hz	Maximum switching frequency
34	BVDSS			725	V	Device breakdown voltage
38	**SWITCH PARAMETERS**					
39	VDSON			2.00	V	Switch on-time drain to source voltage estimate
40	VDSOFF			445.5	V	Switch off-time drain-to-source voltage stress
41	DUTY			0.092		Maximum duty cycle
42	TIME_ON_MIN			0.697	us	Switch minimum on-time
43	IPED_SWITCH			0.038	A	Maximum switch pedestal current
44	IRMS_SWITCH			0.026	A	Maximum switch RMS current
45	PLOSS_SWITCH			0.076	W	Maximum switch loss
46	THERMAL RESISTANCE OF SWITCH			100	degC/W	Net thermal resistance of the switch
47	T_RISE_SWITCH			7.6	degC	Maximum temperature rise of the switch in degrees Celsius
51	**BUCK INDUCTOR PARAMETERS**					
52	INDUCTANCE_MIN			2430	uH	Minimum design inductance required for current delivery
53	INDUCTANCE_TYP	2700		2700	uH	Typical design inductance required for current delivery

54	INDUCTANCE_MAX			2970	uH	Maximum design inductance required for current delivery
55	TOLERANCE_INDUCTANCE			10	%	Tolerance of the design inductance
56	DC RESISTANCE OF INDUCTOR			2.0	ohms	DC resistance of the buck inductor
57	FACTOR_KLOSS			0.50		Factor that accounts for "off-state" power loss to be supplied by inductor (usually between 50% to 66%)
58	IRMS_INDUCTOR			0.096	A	Maximum inductor RMS current
59	PLOSS_INDUCTOR			0.018	W	Maximum inductor losses
63	**FREEWHEELING DIODE PARAMETERS**					
64	VF_FREEWHEELING	0.90		0.90	V	Forward voltage drop across the freewheeling diode
65	PIV_RATING			600.0	V	Peak inverse voltage rating of the freewheeling diode
66	TRR			30	ns	Reverse recovery time of the freewheeling diode
67	PIV_CALCULATED			530.3	V	Computed peak inverse voltage across the freewheeling diode
68	IRMS_DIODE			0.095	A	Maximum diode RMS current
69	PLOSS_DIODE			0.096	W	Maximum freewheeling diode loss
70	RECOMMENDED DIODE			BYV26C		Recommended freewheeling diode
74	**BIAS/FEEDBACK PARAMETERS**					
75	VF_BIAS	0.50		0.50	V	Forward voltage drop of the bias diode
76	RBIAS	40200		40200	Ohms	Bias resistor (connected across FB and S pin). Results into IFB_BIAS value of 49.751 uA
77	RBP			18700	Ohms	BP pin resistor
78	CBP			0.1	uF	BP pin capacitor
79	RFB			44200	Ohms	Feedback resistor
80	CFB			10	uF	Feedback capacitor
81	C_SOFTSTART			N/A	uF	No soft-start capacitor required
82	PLOSS_FEEDBACK			0.000	W	Maximum feedback component losses
86	**X-CAPACITOR DISCHARGE COMPONENTS**					
87	XCAP REQUIRED	NO		NO		Select whether an X-capacitor is required or not
88	XCAP			N/A	nF	X-capacitor in the input
89	TOLERANCE_RZ	0.05		N/A		Tolerance of the X-capacitor discharge resistors
90	RZ1			N/A	MOhms	X-capacitor discharge resistor connected from the input line to Z1 pin of LinkSwitch-TNZ device
91	RZ2			N/A	MOhms	X-capacitor discharge resistor connected from the input neutral to Z2 pin of LinkSwitch-TNZ device
92	t_XCAP_DISCHARGE			N/A	sec	Actual time (worst-case) to discharge the X-capacitor to 60 V after AC input disconnection
96	**OUTPUT CAPACITOR**					
97	OUTPUT VOLTAGE RIPPLE			120	mV	Desired output voltage ripple
98	IRMS_COUT			0.053	A	Maximum output capacitor RMS current
99	PLOSS_COUT			0.004	W	Maximum output capacitor power loss
100	ESR_COUT			1421	mOhms	ESR of the output capacitor

8 Performance Data

8.1 *Efficiency*

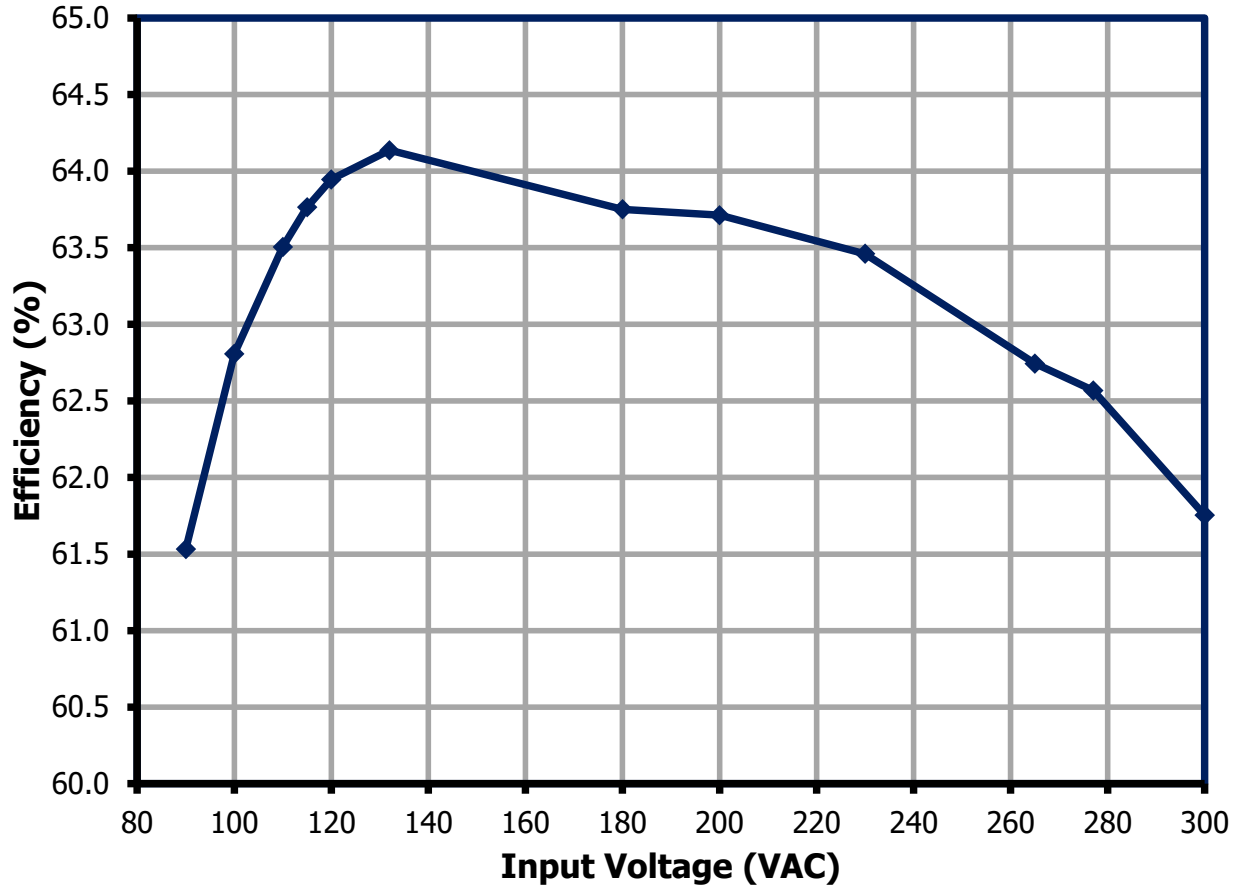

Figure 6 – Full Load Efficiency vs. Line.

8.2 *No-Load Input Current*

Test Condition: Soak for 5 minutes each line and 1 minute integration time.

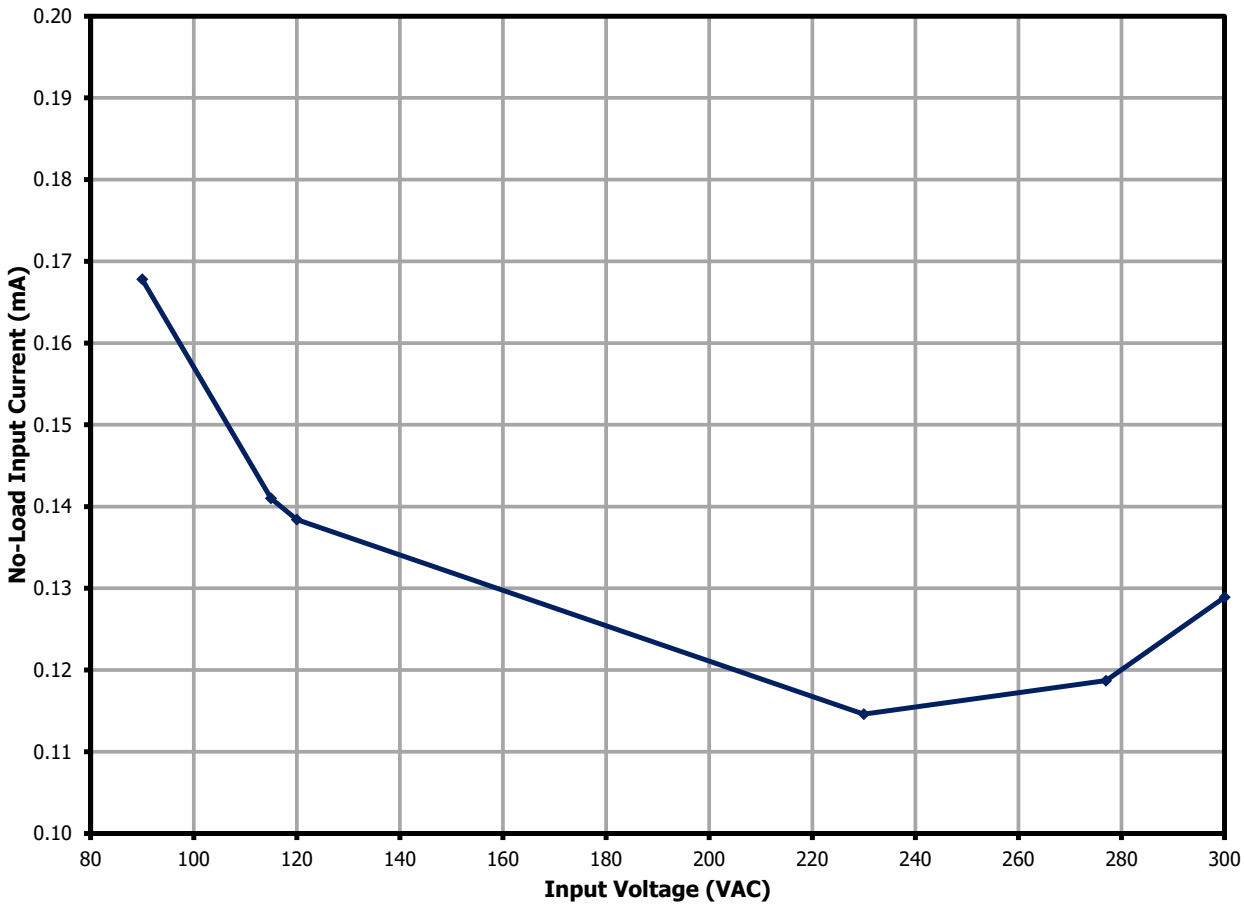

Figure 7 – No-Load Input Current vs. Line.

8.3 *Line Regulation*

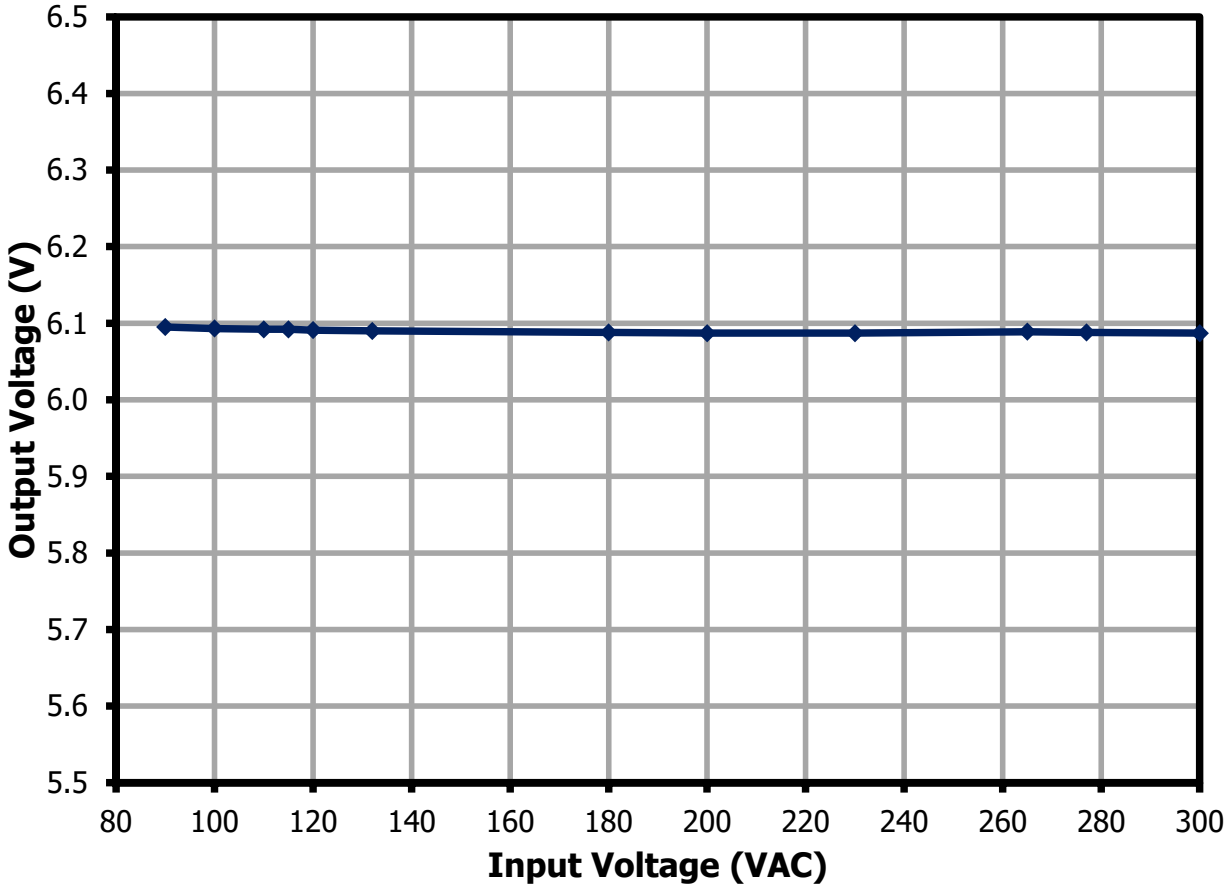

Figure 8 – Output Voltage vs. Line Voltage.

8.4 *Load Regulation*

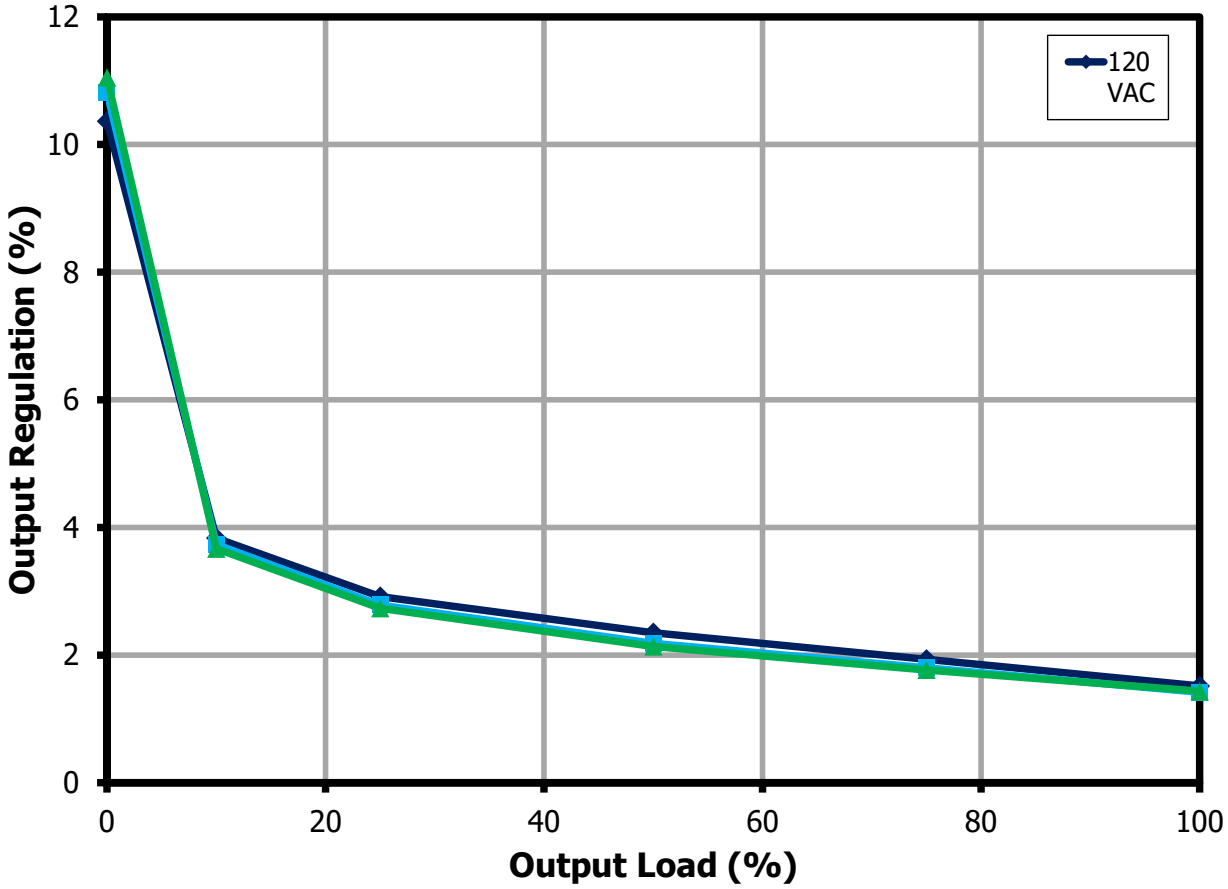

Figure 9 – Output Voltage vs. Percent Load.

9 Waveforms

9.1 *Zero-Crossing Detection*

9.1.1 Zero-Crossing Detection at Normal Operation

9.1.1.1 100% Load

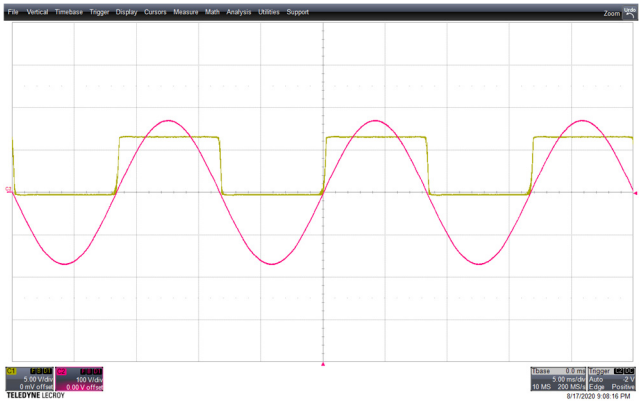

Figure 10 – 120 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.

Figure 11 – 230 VAC 50 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.

9.1.1.2 0% Load

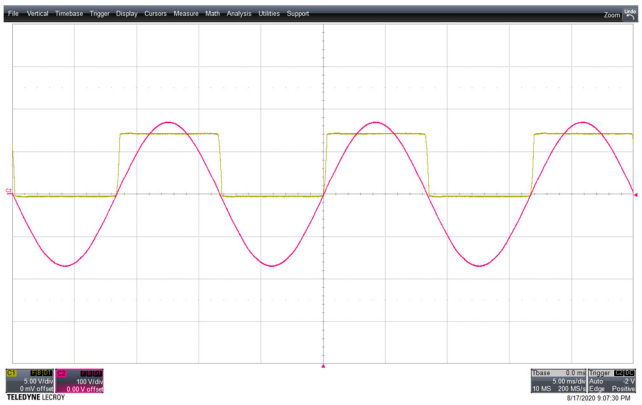

Figure 12 – 120 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.

Figure 13 – 230 VAC 50 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.

9.1.2 Zero-Crossing Detection at Start-up

9.1.2.1 0° Start-up Phase

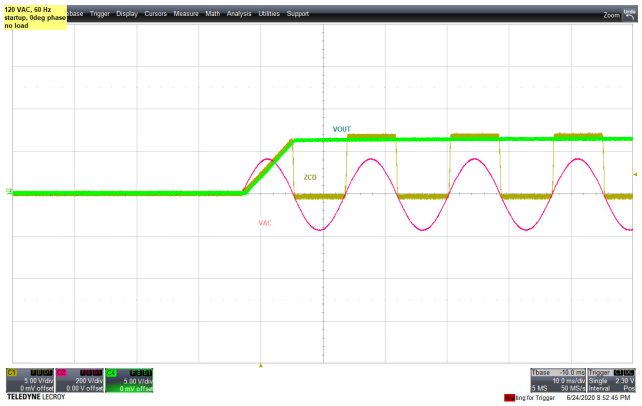

Figure 14 – 120 VAC 60 Hz, No-Load.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.
CH4: V_{OUT}, 5 V / div., 5 ms / div.

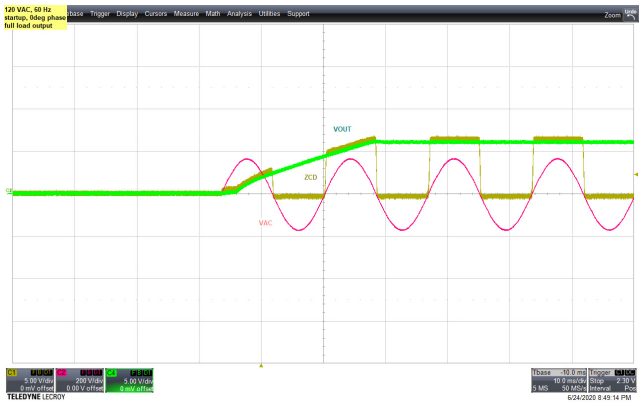

Figure 15 – 120 VAC 60 Hz, Full Load.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.
CH4: V_{OUT}, 5 V / div., 5 ms / div.

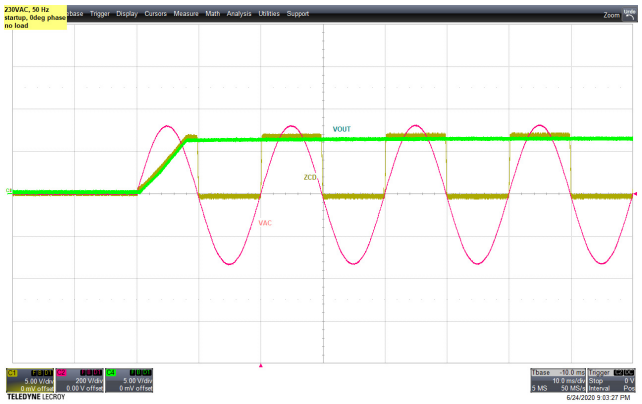

Figure 16 – 230 VAC 50 Hz, No-Load.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.
CH4: V_{OUT}, 5 V / div., 5 ms / div.

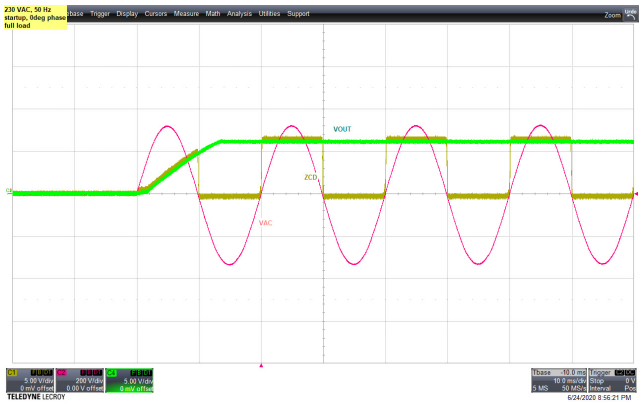

Figure 17 – 230 VAC 50 Hz, Full Load.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.
CH4: V_{OUT}, 5 V / div., 5 ms / div.

9.1.2.2 90° Start-up Phase

Figure 18 – 120 VAC 60 Hz, No-Load.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.
CH4: V_{OUT}, 5 V / div., 5 ms / div.

Figure 19 – 120 VAC 60 Hz, Full Load.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.
CH4: V_{OUT}, 5 V / div., 5 ms / div.

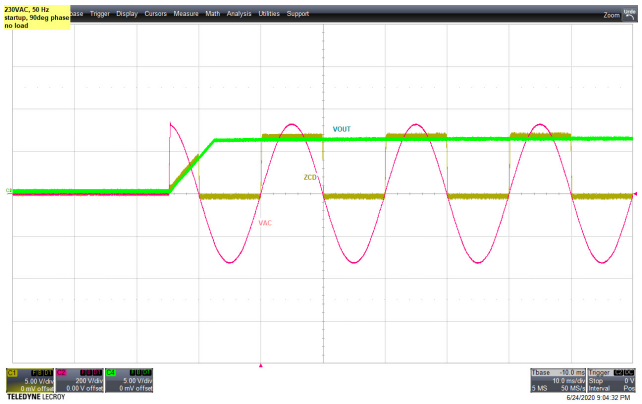

Figure 20 – 230 VAC 50 Hz, No-Load.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.
CH4: V_{OUT}, 5 V / div., 5 ms / div.

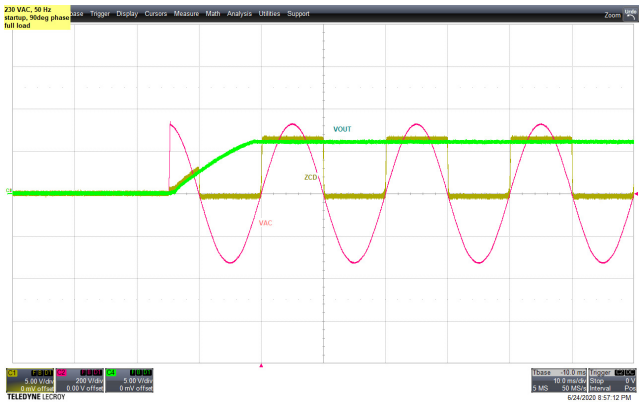

Figure 21 – 230 VAC 50 Hz, Full Load.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.
CH4: V_{OUT}, 5 V / div., 5 ms / div.

9.1.3 Zero Crossing Detection Delay

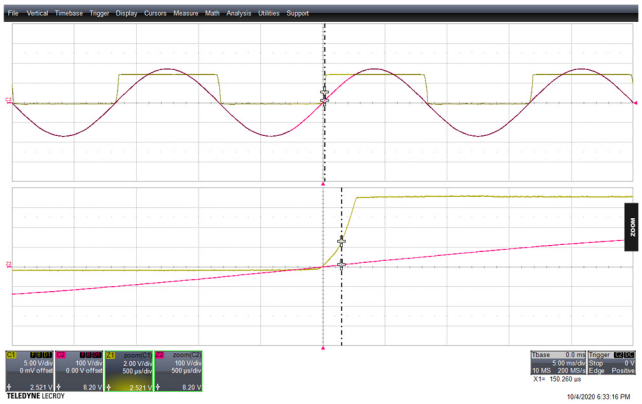

Figure 22 – 115 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.
Rising Edge Delay = 150 μs.

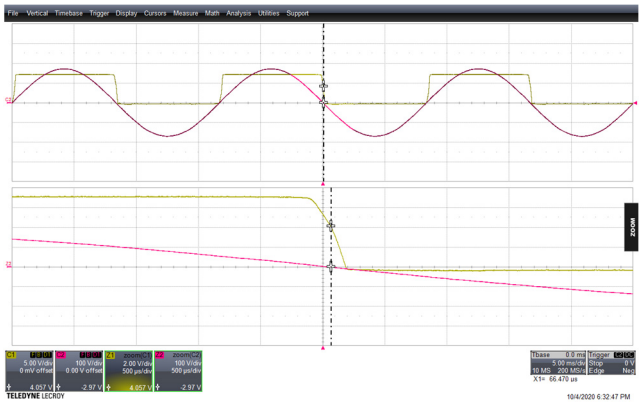

Figure 23 – 115 VAC 60 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.
Rising Edge Delay = 66 μs.

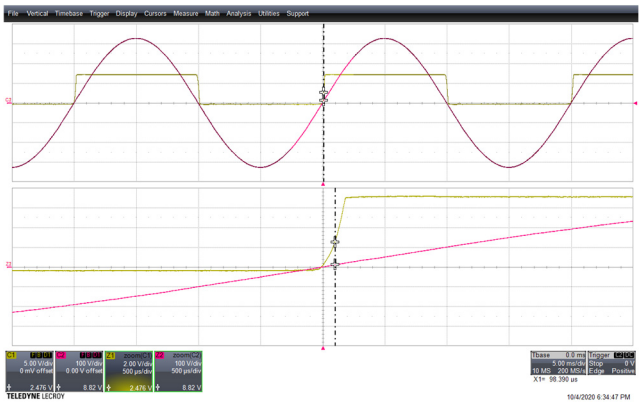

Figure 24 – 230 VAC 50 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.
Rising Edge Delay = 98 μs.

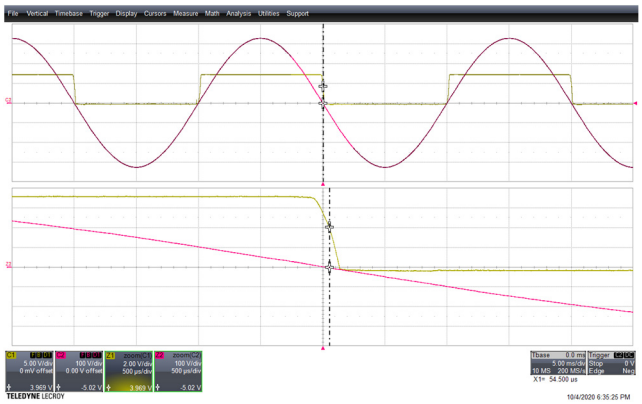

Figure 25 – 230 VAC 50 Hz.
CH1: ZCD, 5 V / div., 5 ms / div.
CH2: V_{IN}, 100 V / div., 5 ms / div.
Rising Edge Delay = 55 μs.

9.2 *Output Voltage at Start-up*

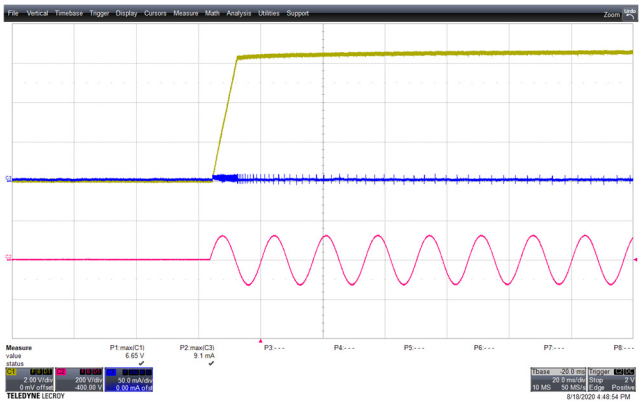

Figure 26 – 90 VAC 60 Hz, No-load.
CH1: V_{OUT}, 5 V / div., 20 ms / div.
CH2: V_{IN}, 200 V / div., 20 ms / div.
CH3: I_{OUT}, 50 mA / div., 20 ms / div.

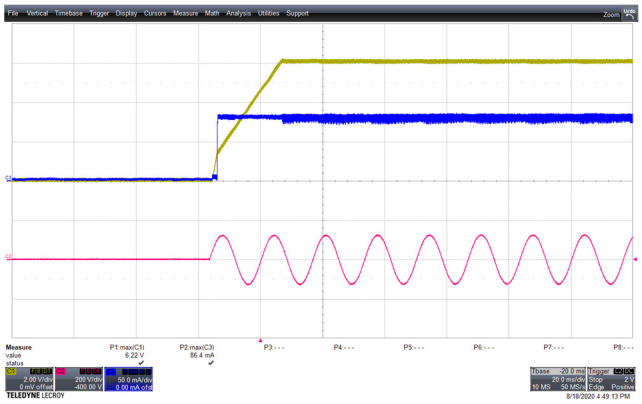

Figure 27 – 90 VAC 60 Hz, Full load.
CH1: V_{OUT}, 5 V / div., 20 ms / div.
CH2: V_{IN}, 200 V / div., 20 ms / div.
CH3: I_{OUT}, 50 mA / div., 20 ms / div.

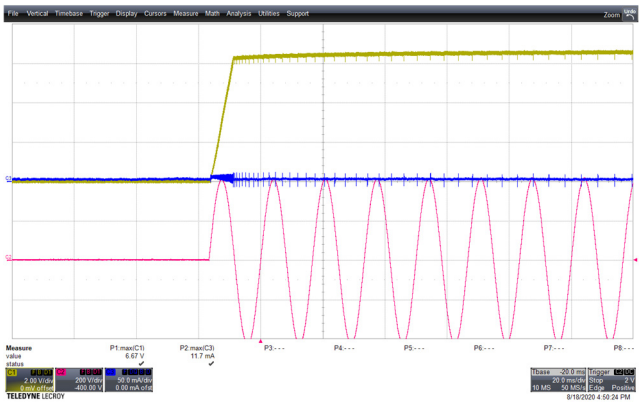

Figure 28 – 300 VAC 50 Hz, No-load.
CH1: V_{OUT}, 5 V / div., 20 ms / div.
CH2: V_{IN}, 200 V / div., 20 ms / div.
CH3: I_{OUT}, 50 mA / div., 20 ms / div.

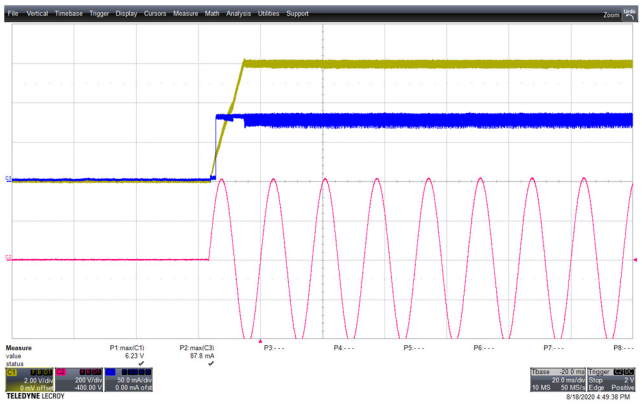

Figure 29 – 300 VAC 50 Hz, Full load.
CH1: V_{OUT}, 5 V / div., 20 ms / div.
CH2: V_{IN}, 200 V / div., 20 ms / div.
CH3: I_{OUT}, 50 mA / div., 20 ms / div.

9.3 *Switching Waveforms*

9.3.1 Primary MOSFET Drain-Source Voltage and Current at Normal Operation

9.3.1.1 100% Load

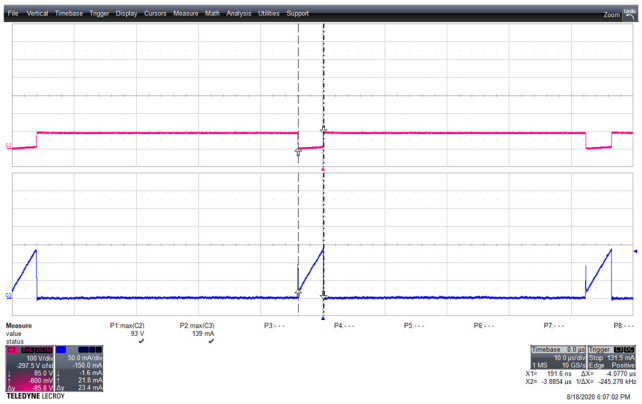

Figure 30 – 90 VAC 60 Hz.
CH2: V_{DS}, 100 V / div., 10 µs / div.
CH3: I_{DS}, 50 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 93 V.
$I_{DS(MAX)}$ = 139 mA.

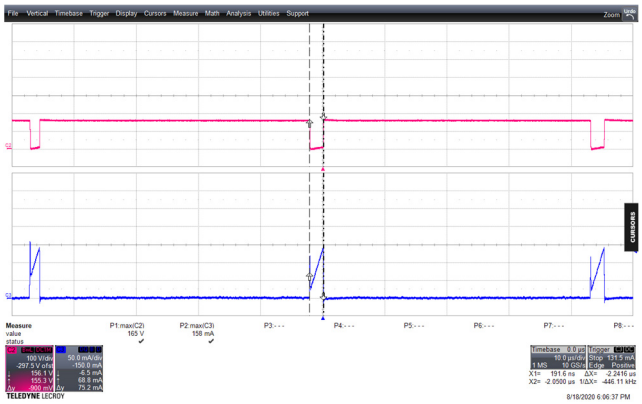

Figure 31 – 120 VAC 60 Hz.
CH2: V_{DS}, 100 V / div., 10 µs / div.
CH3: I_{DS}, 50 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 165 V.
$I_{DS(MAX)}$ = 158 mA.

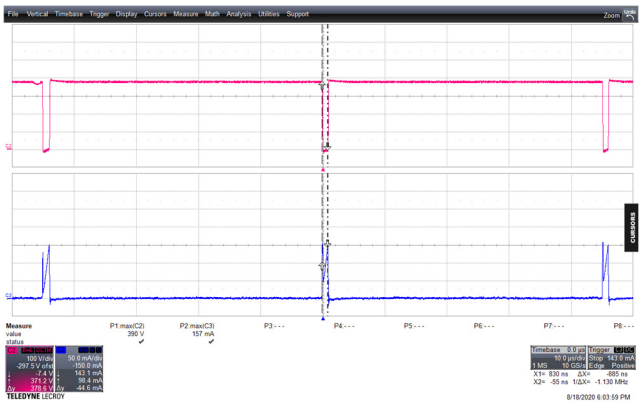

Figure 32 – 277 VAC 60 Hz.
CH2: V_{DS}, 100 V / div., 10 µs / div.
CH3: I_{DS}, 50 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 390 V.
$I_{DS(MAX)}$ = 157 mA.

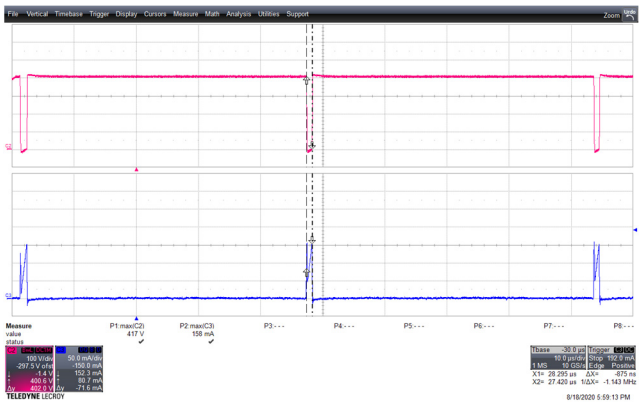

Figure 33 – 300 VAC 60 Hz.
CH2: V_{DS}, 100 V / div., 10 µs / div.
CH3: I_{DS}, 50 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 417 V.
$I_{DS(MAX)}$ = 158 mA.

9.3.1.2 0% Load

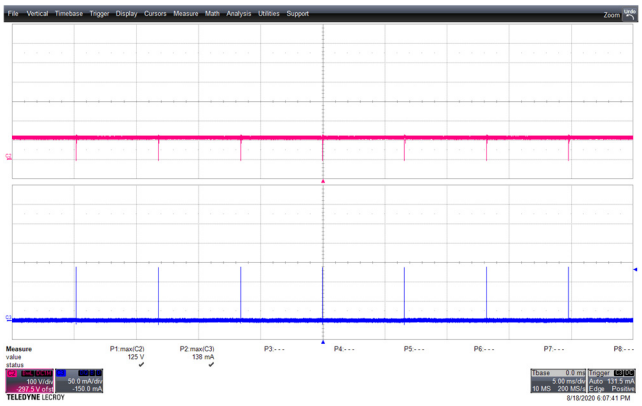

Figure 34 – 90 VAC 60 Hz.
CH2: V_{DS}, 100 V / div., 10 µs / div.
CH3: I_{DS}, 50 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 125 V.
$I_{DS(MAX)}$ = 138 mA.

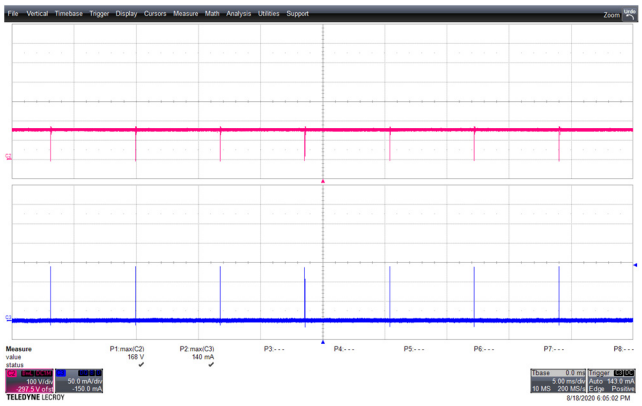

Figure 35 – 120 VAC 60 Hz.
CH2: V_{DS}, 100 V / div., 10 µs / div.
CH3: I_{DS}, 50 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 168 V.
$I_{DS(MAX)}$ = 140 mA.

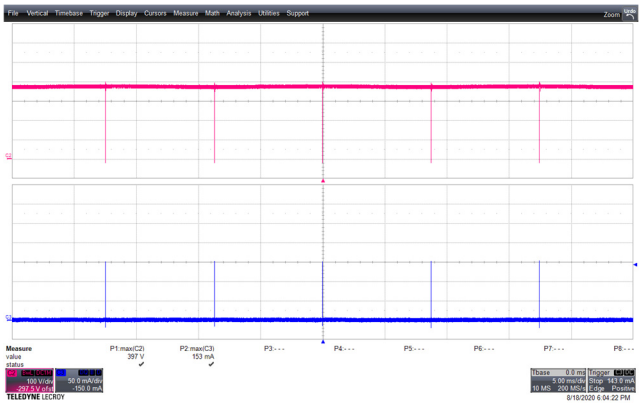

Figure 36 – 277 VAC 60 Hz.
CH2: V_{DS}, 100 V / div., 10 µs / div.
CH3: I_{DS}, 50 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 397 V.
$I_{DS(MAX)}$ = 153 mA.

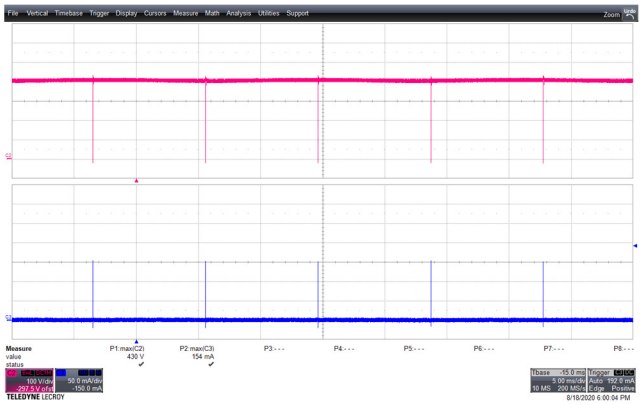

Figure 37 – 300 VAC 60 Hz.
CH2: V_{DS}, 100 V / div., 10 µs / div.
CH3: I_{DS}, 50 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 430 V.
$I_{DS(MAX)}$ = 154 mA.

9.3.2 Primary MOSFET Drain-Source Voltage and Current at Start-up Operation

9.3.2.1 100% Load

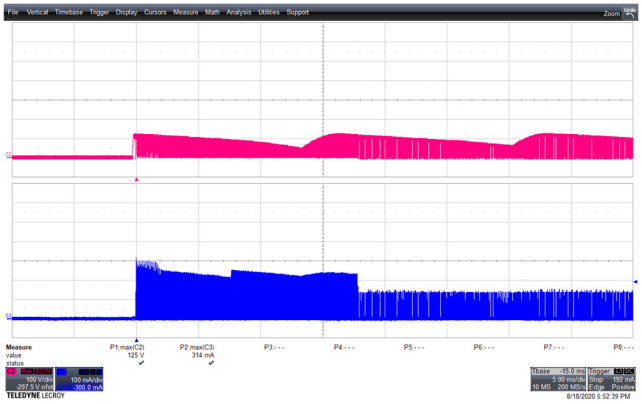

Figure 38 – 90 VAC 60 Hz.
CH2: V_{DS}, 100 V / div., 5 ms / div.
CH3: I_{DS}, 100 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 125 V.
$I_{DS(MAX)}$ = 314 mA.

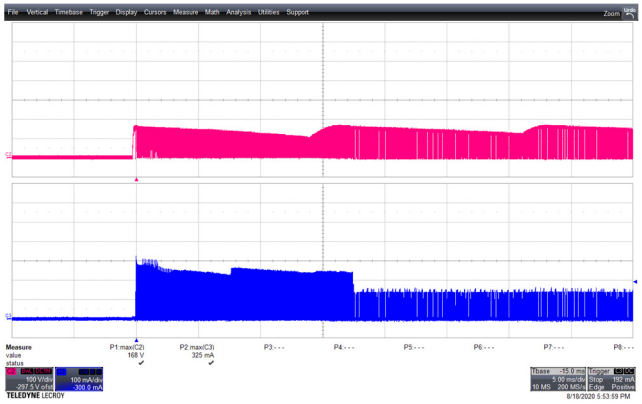

Figure 39 – 120 VAC 60 Hz.
CH2: V_{DS}, 100 V / div., 5 ms / div.
CH3: I_{DS}, 100 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 168 V.
$I_{DS(MAX)}$ = 325 mA.

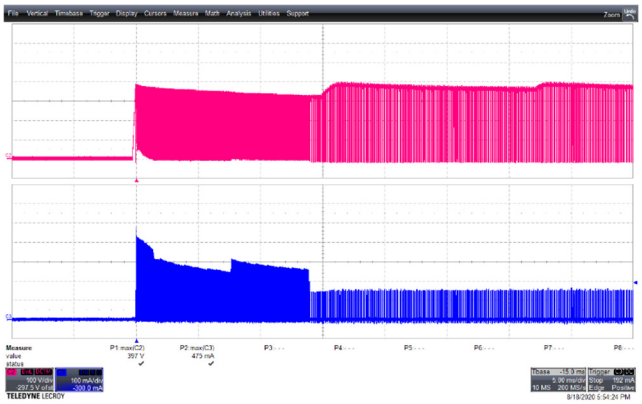

Figure 40 – 277 VAC 60 Hz.
CH2: V_{DS}, 100 V / div., 5 ms / div.
CH3: I_{DS}, 100 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 397 V.
$I_{DS(MAX)}$ = 475 mA.

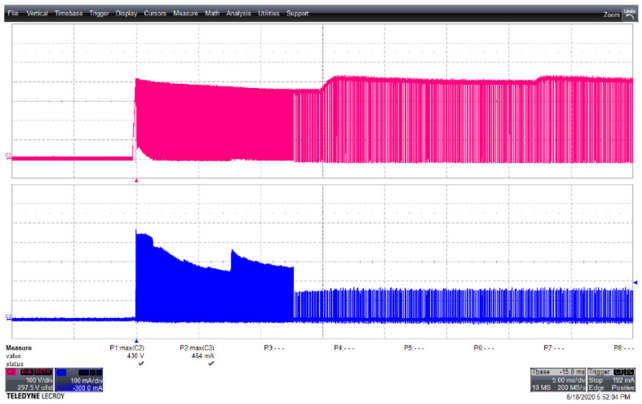

Figure 41 – 300 VAC 60 Hz.
CH2: V_{DS}, 100 V / div., 5 ms / div.
CH3: I_{DS}, 100 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 430 V.
$I_{DS(MAX)}$ = 454 mA.

9.3.2.2 0% Load

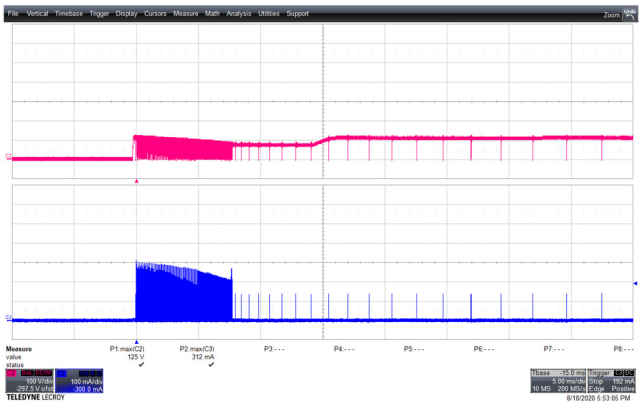

Figure 42 – 90 VAC 60 Hz.
CH2: V_{DS}, 100 V / div., 5 ms / div.
CH3: I_{DS}, 100 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 125 V.
$I_{DS(MAX)}$ = 312 mA.

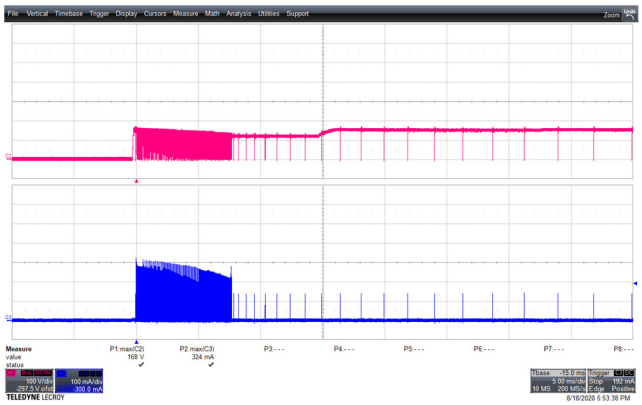

Figure 43 – 115 VAC 60 Hz.
CH2: V_{DS}, 100 V / div., 5 ms / div.
CH3: I_{DS}, 100 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 168 V.
$I_{DS(MAX)}$ = 324 mA.

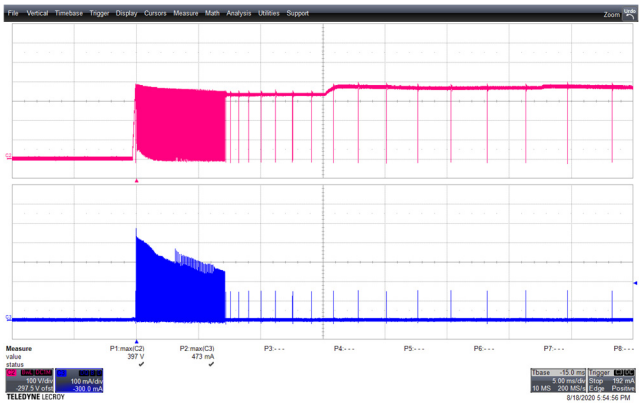

Figure 44 – 277 VAC 50 Hz.
CH2: V_{DS}, 100 V / div., 5 ms / div.
CH3: I_{DS}, 100 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 397 V.
$I_{DS(MAX)}$ = 473 mA.

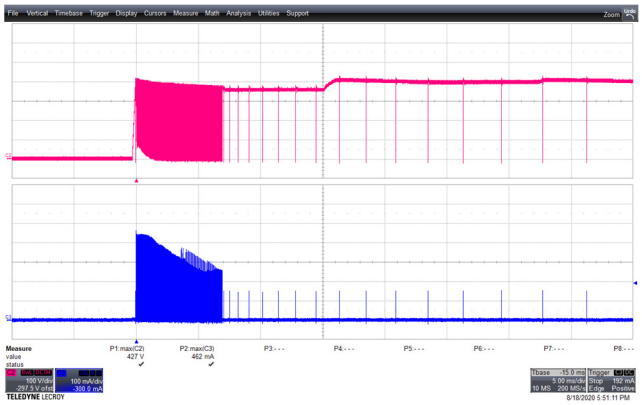

Figure 45 – 300 VAC 50 Hz.
CH2: V_{DS}, 100 V / div., 5 ms / div.
CH3: I_{DS}, 100 mA / div., 5 ms / div.
$V_{DS(MAX)}$ = 427 V.
$I_{DS(MAX)}$ = 462 mA.

10 Thermal Performance

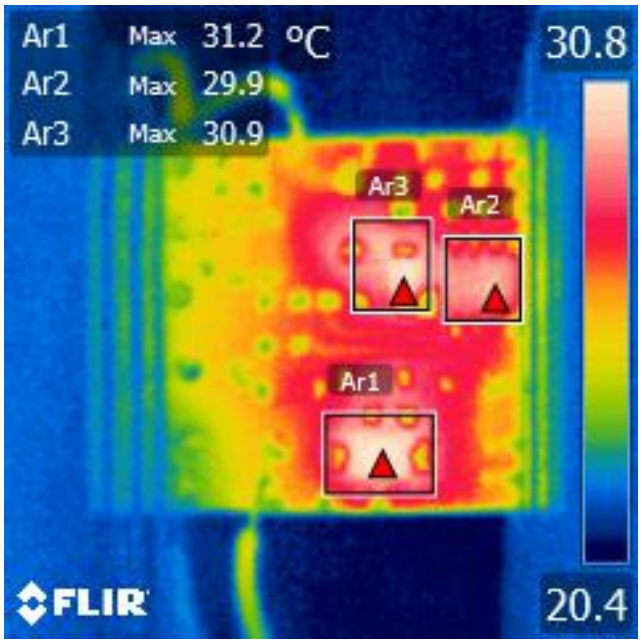

Figure 46 – 90 VAC 60 Hz, Bottom.
Ar1: VR1, 31.2 °C.
Ar2: LinkSwitch-TNZ, 29.9 °C.
Ar3: Freewheeling Diode, 30.9 °C.

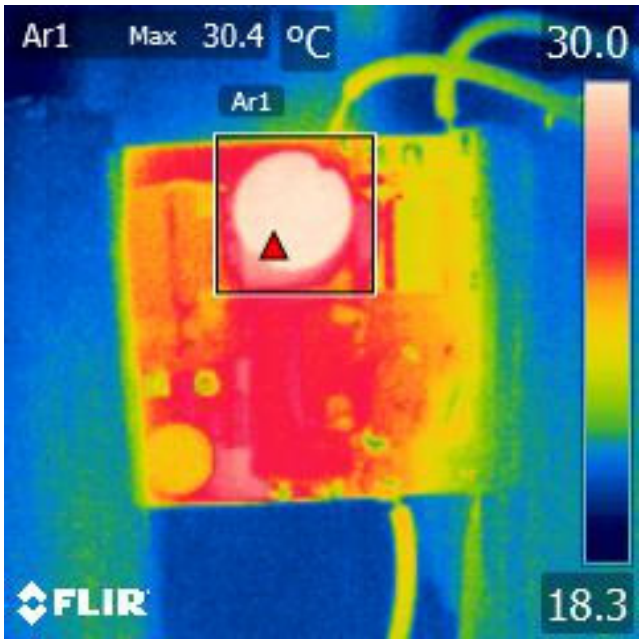

Figure 47 – 90 VAC 60 Hz, Top.
Ar1: Output Inductor, 30.4 °C.

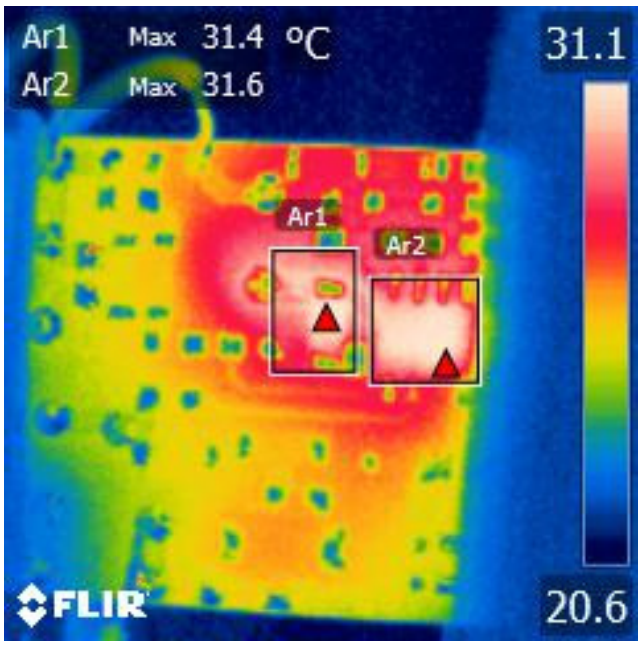

Figure 48 – 300 VAC 60 Hz, Bottom.
Ar1: Freewheeling Diode, 31.4 °C.
Ar2: LinkSwitch-TNZ, 31.6 °C.

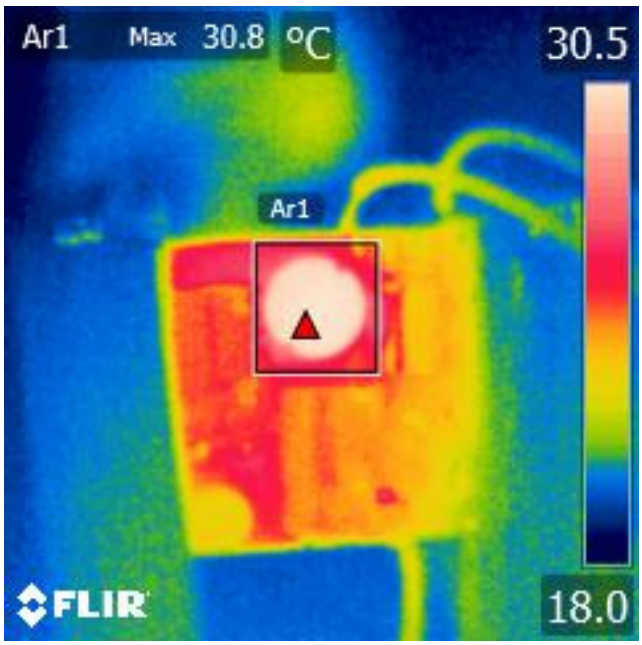

Figure 49 – 300 VAC 60 Hz, Top.
Ar1: Output Inductor, 30.8 °C.

11 Conducted EMI

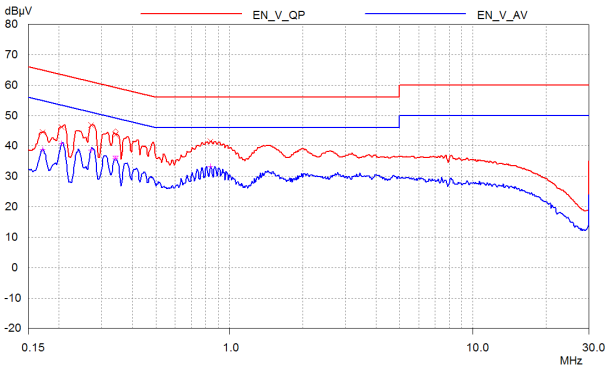

Figure 50 – 115 VAC 60 Hz.

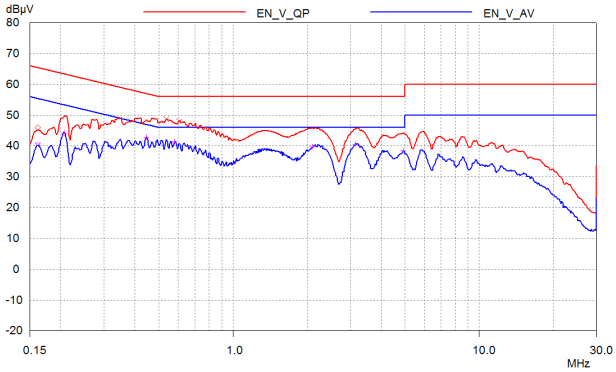

Figure 51 – 230 VAC 60 Hz.

12 Line Surge

Differential and common mode input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

12.1 *Surge*

DM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (º)	Test Result (Pass/Fail)
+1000	230	L to N	0	Pass
-1000	230	L to N	0	Pass
+1000	230	L to N	90	Pass
-1000	230	L to N	90	Pass
+1000	230	L to N	180	Pass
-1000	230	L to N	180	Pass
+1000	230	L to N	270	Pass
-1000	230	L to N	270	Pass

Note: In all PASS results, no damage and no auto-restart was observed.

12.2 *Ring Wave*

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (º)	Test Result (Pass/Fail)
+2500	230	L to N	0	Pass
-2500	230	L to N	0	Pass
+2500	230	L to N	90	Pass
-2500	230	L to N	90	Pass
+2500	230	L to N	180	Pass
-2500	230	L to N	180	Pass
+2500	230	L to N	270	Pass
-2500	230	L to N	270	Pass

Note: In all PASS results, no damage and no auto-restart was observed.

13 Revision History

Date	Author	Revision	Description and Changes	Reviewed
23-Feb-21	DS	1.0	Initial Release.	Apps & Mktg
08-Jun-21	KM	1.1	Updated C2 in Schematic.	Apps & Mktg

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