Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020M-6 (SOT1220-2) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- · Low threshold voltage
- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- · Exposed drain pad for excellent thermal conduction

3. Applications

- Charging switch for portable devices
- DC-to-DC converters
- · Power management in battery-driven portables
- · Hard disk and computing power management

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j = 25 °C		-	-	30	V
V_{GS}	gate-source voltage			-12	-	12	V
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-	10	Α
Static characte	eristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 7.3 \text{ A}; T_j = 25 ^{\circ}\text{C}$		-	14.8	18.4	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain		
2	D	drain		
3	G	gate		D —
4	S	source	2 5	
5	D	drain	3 8 4	G—UFIA)
6	D	drain	Transparent top view	mbb076 S
7	D	drain	DFN2020M-6 (SOT1220-2)	
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PMPB14R8XN		plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1220-2		

7. Marking

Table 4. Marking codes

Type number	Marking code
PMPB14R8XN	ZY

30 V, N-channel Trench MOSFET

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j = 25 °C		-	30	V
V_{GS}	gate-source voltage			-12	12	V
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	10	А
		V _{GS} = 4.5 V; T _{amb} = 25 °C	[1]	-	7.3	А
		V _{GS} = 4.5 V; T _{amb} = 100 °C	[1]	-	4.6	А
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \mu s$		-	100	А
P _{tot}	total power dissipation	T _{amb} = 25 °C; t ≤ 5 s	[1]	-	1	W
		T _{amb} = 25 °C	[1]	-	1.5	W
		T _{sp} = 25 °C		-	18	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain	n diode					
Is	source current	T _{amb} = 25 °C	[1]	-	1.5	А

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

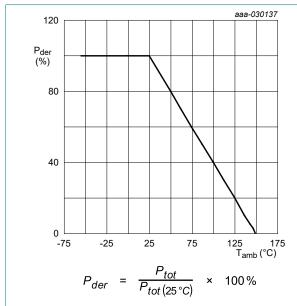


Fig. 1. Normalized total power dissipation as a function of ambient temperature

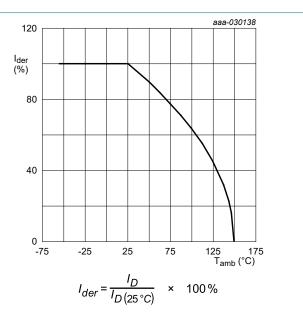


Fig. 2. Normalized continuous drain current as a function of ambient temperature

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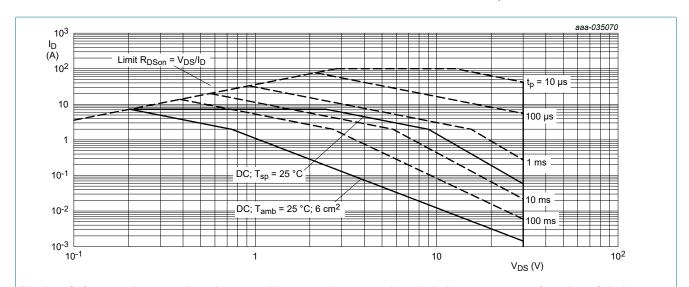


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

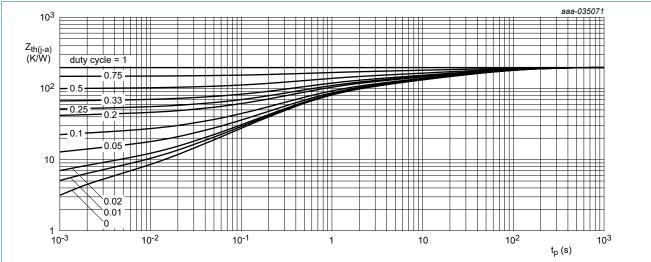
30 V, N-channel Trench MOSFET

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
uiy-a)	thermal resistance from	<u>-</u>	[1]	-	200	250	K/W
	junction to ambient		[2]	-	65	85	K/W
		in free air; t ≤ 5 s	[2]	-	33	42	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	5.6	7	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

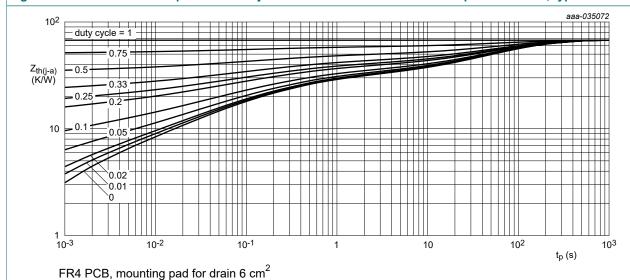


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

30 V, N-channel Trench MOSFET

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	cteristics					
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	0.4	0.65	0.9	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μΑ
I _{GSS}	gate leakage current	V _{GS} = 12 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
		$V_{GS} = -12 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	-100	nA
R _{DSon}	drain-source on-state	$V_{GS} = 4.5 \text{ V}; I_D = 7.3 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	14.8	18.4	mΩ
resistance	resistance	$V_{GS} = 4.5 \text{ V}; I_D = 7.3 \text{ A}; T_j = 150 \text{ °C}$	-	23	28	mΩ
		$V_{GS} = 2.5 \text{ V}; I_D = 6.3 \text{ A}; T_j = 25 \text{ °C}$	-	18.4	24.2	mΩ
	V _{GS} = 1.8 V; I _D = 5.2 A; T _j = 25 °C	-	24.6	34.8	mΩ	
9 _{fs}	forward transconductance	$V_{DS} = 5 \text{ V}; I_D = 7.3 \text{ A}; T_j = 25 \text{ °C}$	-	17.9	-	S
R _G	gate resistance	f = 1 MHz	-	2.1	-	Ω
Dynamic ch	aracteristics		·	·		
Q _{G(tot)}	total gate charge	$V_{DS} = 15 \text{ V}; I_D = 7.3 \text{ A}; V_{GS} = 4.5 \text{ V};$	-	4.3	6.5	nC
Q_{GS}	gate-source charge	T _j = 25 °C	-	0.7	-	nC
Q_{GD}	gate-drain charge		-	0.9	-	nC
C _{iss}	input capacitance	$V_{DS} = 15 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V};$	-	500	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	88	-	pF
C _{rss}	reverse transfer capacitance		-	30	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = 15 V; I_{D} = 7.3 A; V_{GS} = 4.5 V;	-	3	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	5	-	ns
t _{d(off)}	turn-off delay time		-	10	-	ns
t _f	fall time		-	5	-	ns
Source-drai	n diode					
V _{SD}	source-drain voltage	$I_S = 1.5 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	0.7	1.2	V

30 V, N-channel Trench MOSFET

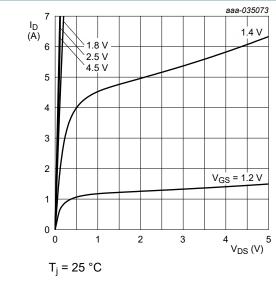


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

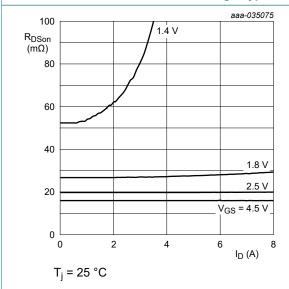
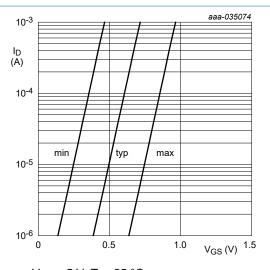


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values



 $V_{DS} = 5 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$

Fig. 7. Sub-threshold drain current as a function of gate-source voltage

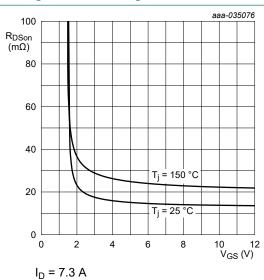


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

30 V, N-channel Trench MOSFET

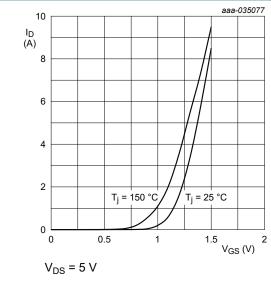


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

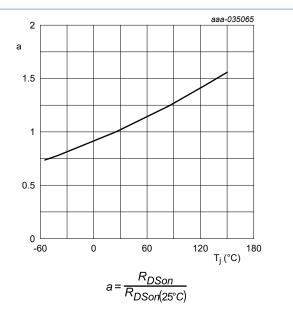


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

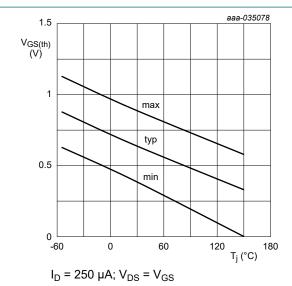
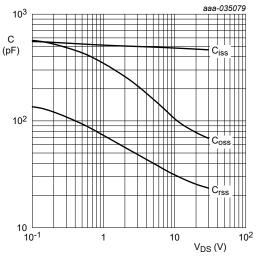


Fig. 12. Gate-source threshold voltage as a function of junction temperature



 $f = 1 MHz; V_{GS} = 0 V$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

30 V, N-channel Trench MOSFET

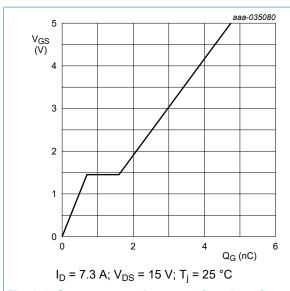


Fig. 14. Gate-source voltage as a function of gate charge; typical values

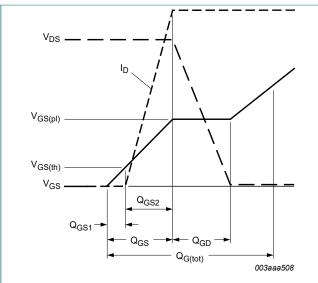


Fig. 15. Gate charge waveform definitions

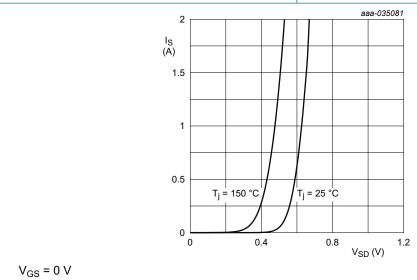
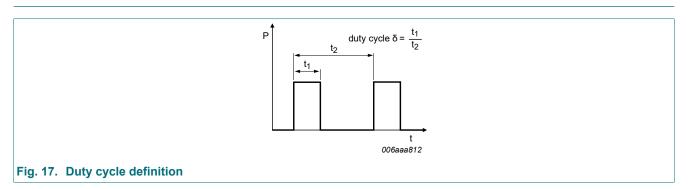


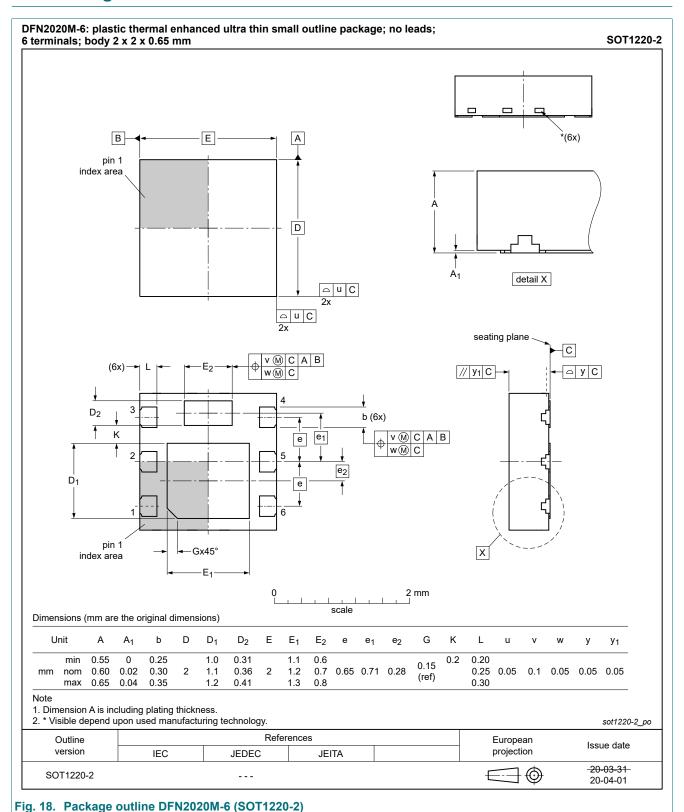
Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information



30 V, N-channel Trench MOSFET

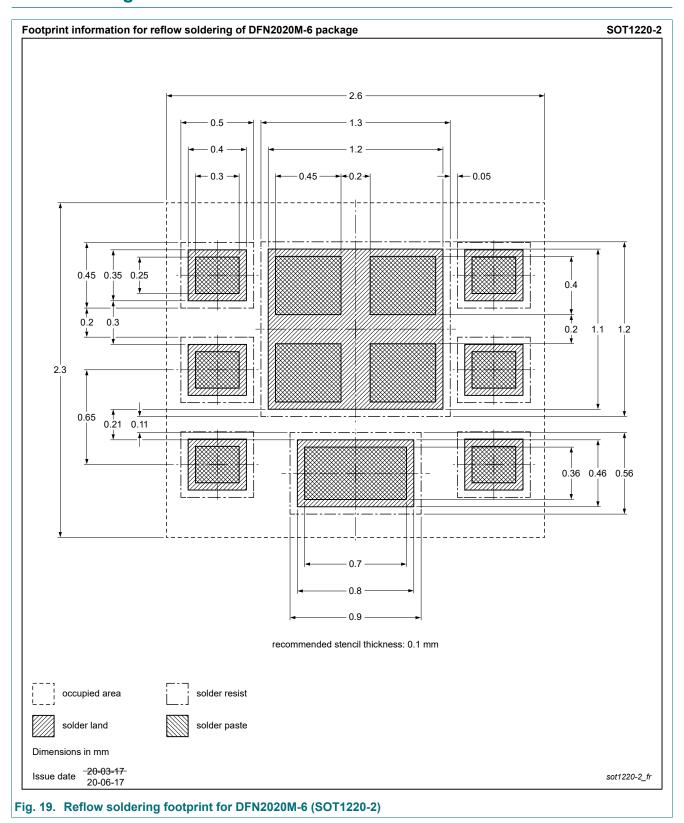
12. Package outline



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30 V, N-channel Trench MOSFET

13. Soldering



30 V, N-channel Trench MOSFET

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB14R8XN v.1	20221024	Product data sheet	-	-

30 V, N-channel Trench MOSFET

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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30 V, N-channel Trench MOSFET

Contents

1.	General description	1
2.	Features and benefits	1
3.	Applications	1
4.	Quick reference data	1
5.	Pinning information	2
6.	Ordering information	2
7.	Marking	2
8.	Limiting values	3
9.	Thermal characteristics	5
10.	Characteristics	6
11.	Test information	9
12.	Package outline	10
13.	Soldering	11
14.	Revision history	12
	Legal information	

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